Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

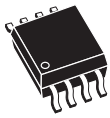
Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

M41T82, M41T83

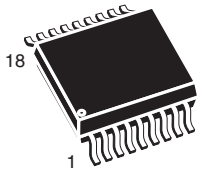
Serial I²C bus real-time clock (RTC) with battery switchover

Datasheet - production data

QFN16 (4 mm x 4 mm)



SO8 (4.90 mm x 3.90 mm)



SOX18, embedded crystal
(11.61 mm x 7.62 mm)

Features

- Ultra-low battery supply current of 365 nA
- Factory-calibrated accuracy of ±5 ppm typical after 2 reflows (SOX18)
  - Much better accuracies achievable using built-in programmable analog and digital calibration circuits
- 2.0 V to 5.5 V clock operating voltage
- Counters for tenths/hundredths of seconds, seconds, minutes, hours, day, date, month, year, and century
- Automatic switchover and reset output circuitry (fixed reference)
  - M41T83S: V_{CC} = 3.00 V to 5.50 V
  - M41T83R: V_{CC} = 2.70 V to 5.50 V
  - M41T83Z: V_{CC} = 2.38 V to 5.50 V
- Serial interface supports I²C bus (400 kHz protocol)
- Programmable alarm with interrupt function (valid even during battery backup mode)
- Optional 2nd programmable alarm available
- Square wave output defaults to 32 KHz on power-up (M41T83 only)
- RESET ($\overline{RST}$) output
- Watchdog timer
- Programmable 8-bit counter/timer
- 7 bytes of battery-backed user SRAM
- Battery low flag
- Low operating current of 80 µA
- Oscillator stop detection
- Battery or SuperCap™ backup
- Operating temperature of –40 °C to 85 °C
- Package options
  - a 16-lead QFN (M41T83)
  - an 8-lead SOIC (M41T82) or
  - an 18-lead embedded crystal SOIC (M41T83)
- RoHS compliance: lead-free components are compliant with the RoHS directive

Contents

List of tables

List of figures

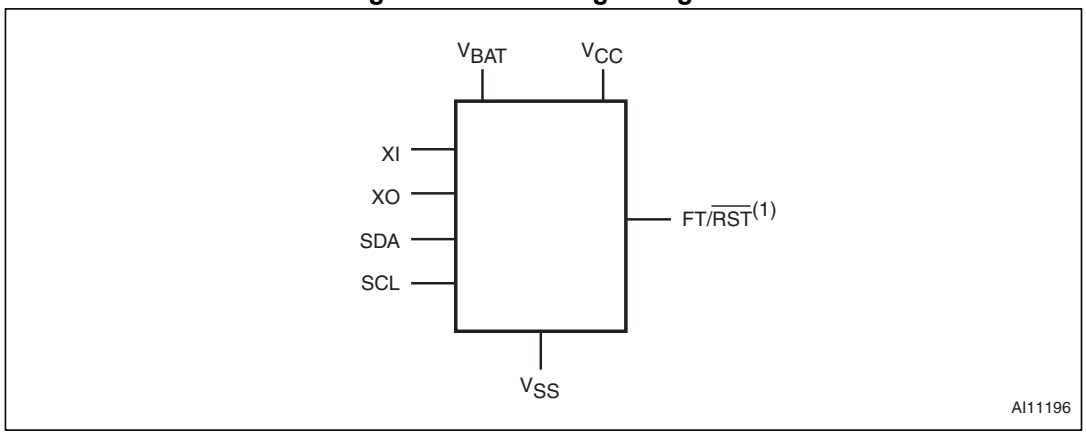
1 Description

The M41T8x are low-power serial I^2C real-time clocks (RTCs) with a built-in 32.768 kHz oscillator (external crystal-controlled for the QFN16 and SO8 packages, embedded crystal for the SOX18 package). Eight bytes of the register map (see *Table 2 on page 23*) are used for the clock/calendar function and are configured in binary-coded decimal (BCD) format. An additional 17 bytes of the register map provide status/control of the two alarms, watchdog, 8-bit counter, and square wave functions. An additional seven bytes are made available as user SRAM.

Addresses and data are transferred serially via a two-line, bidirectional I^2C interface. The built-in address register is incremented automatically after each WRITE or READ data byte. The M41T8x has a built-in power sense circuit which detects power failures and automatically switches to the battery supply when a power failure occurs. The energy needed to sustain the clock operations can be supplied by a small lithium button battery when a power failure occurs.

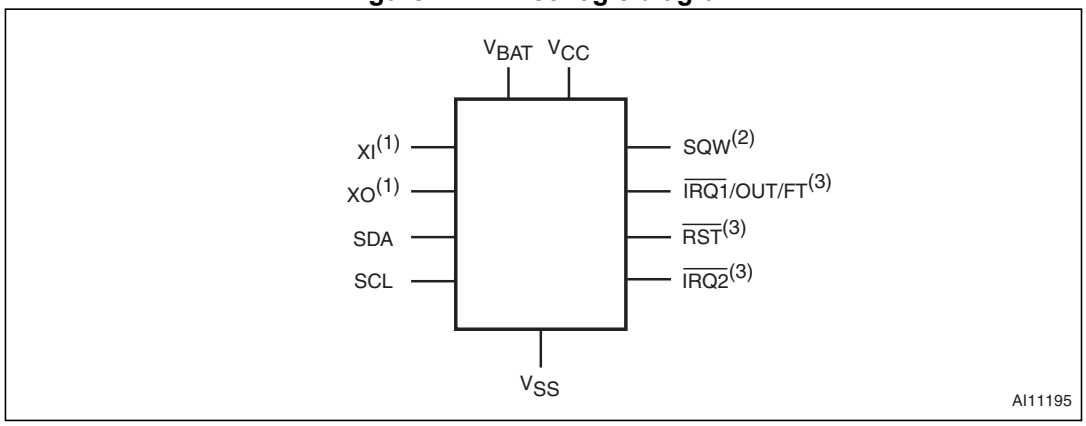
Functions available to the user include a non-volatile, time-of-day clock/calendar, two alarm interrupts, watchdog timer, programmable 8-bit counter, and square wave outputs. The eight clock address locations contain the century, year, month, date, day, hour, minute, second, and tenths/hundredths of a second in 24-hour BCD format. Corrections for 28, 29 (leap year), 30, and 31 day months are made automatically. The M41T83 is supplied in either a QFN16 or an SOX18, 300 mil SOIC which includes an embedded 32 KHz crystal. The SOX18 package requires only a user-supplied battery to provide non-volatile operation. The M41T82 is available only in an SO8 package.

Figure 1. M41T82 logic diagram



1. Open drain

Figure 2. M41T83 logic diagram



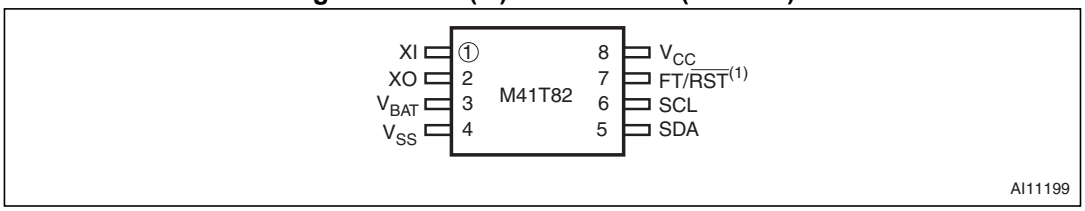
1. For QFN16 package only
2. Defaults to 32 KHz on power-up
3. Open drain

Table 1. Signal names

Symbol	Description
XI(1)	32 KHz oscillator input
XO(1)	32 KHz oscillator output
$\overline{IRQ1}$/OUT/FT(2)	Interrupt 1/output driver/frequency test output (open drain)
SQW(3)	32 KHz programmable square wave output
$\overline{RST}$	Power-on reset output (open drain)
FT/$\overline{RST}$	Frequency test output/power-on reset (open drain - M41T82 only)
$\overline{IRQ2}$(2)	Interrupt for alarm 2 (open drain)
SDA	Serial data address input/output
SCL	Serial clock input
V_{BAT}	Battery supply voltage (tie V_{BAT} to V_{SS} if no battery is connected.)
DU(4)	Do not use
V_{CC}	Supply voltage
V_{SS}	Ground

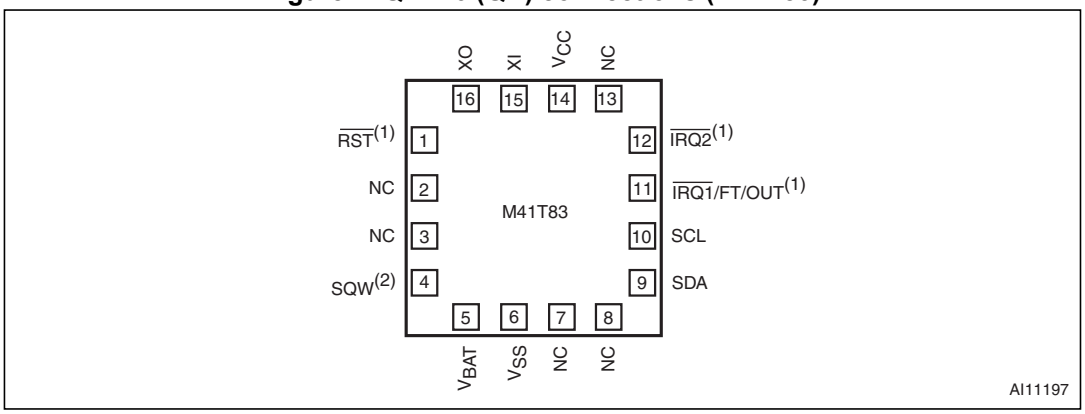
1. For SO8 and QFN16 packages only.
2. For SOX18 and QFN16 packages only.
3. Defaults to 32 KHz on power-up.
4. DU pin must be tied to V_{CC}.

Figure 3. SO8 (M) connections (M41T82)



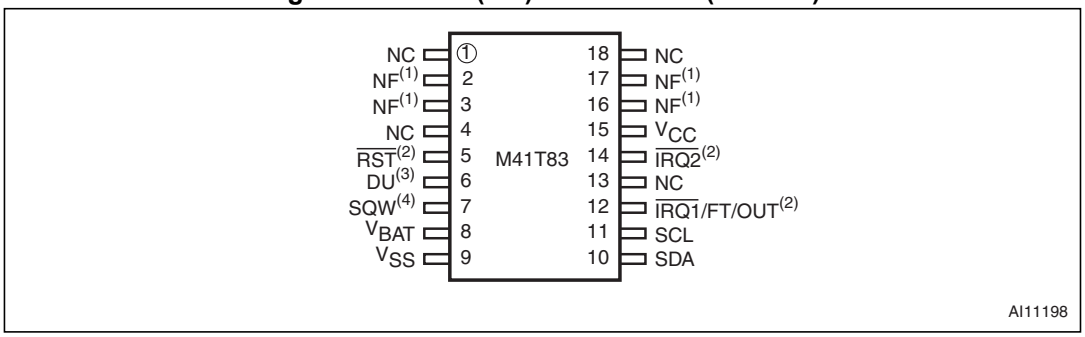
1. Open drain output

Figure 4. QFN16 (QA) connections (M41T83)



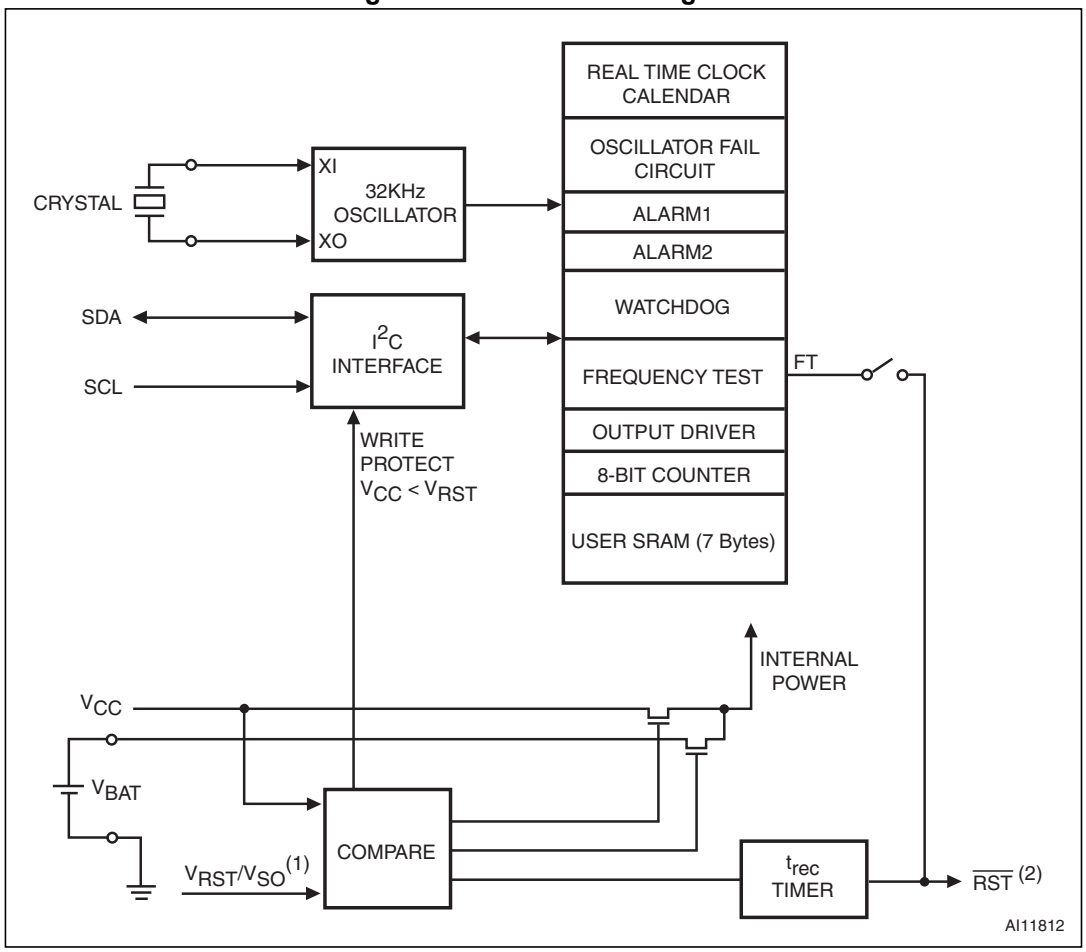
1. Open drain output.
2. Defaults to 32 KHz on power-up.

Figure 5. SOX18 (MY) connections (M41T83)



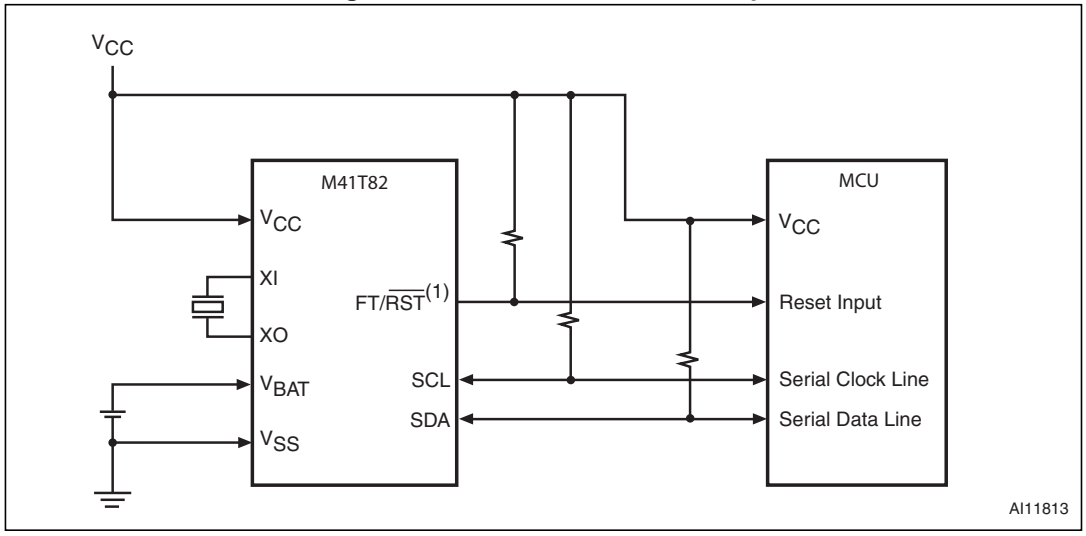
1. NF pins must be tied to V_{SS}. Pins 2 and 3, and 16 and 17 are internally shorted together.
2. Open drain output.
3. Do not use (must be tied to V_{CC}).
4. Defaults to 32 KHz on power-up.

Figure 6. M41T82 block diagram



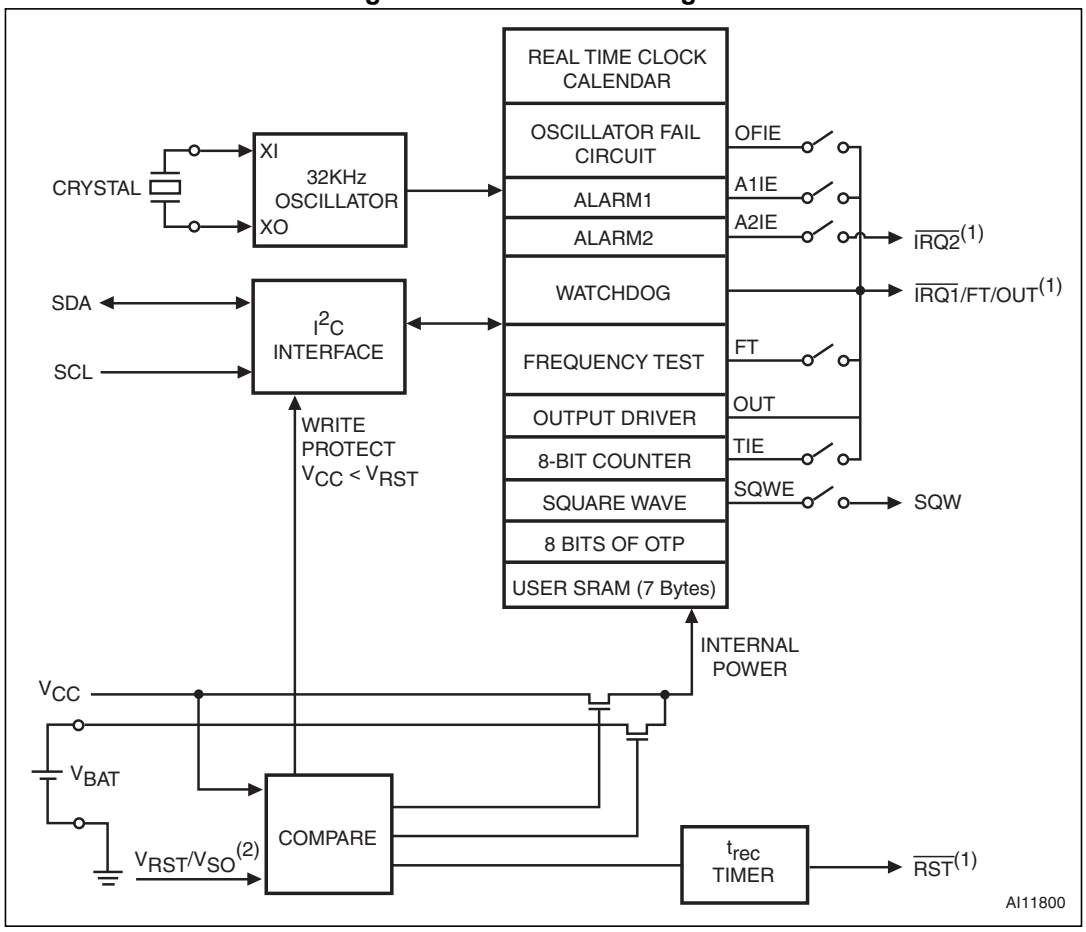
1. $V_{RST} = V_{SO}$ = 2.93 V (S), 2.63 V (R), and 2.32 V (Z).
2. Open drain output.

Figure 7. M41T82 hardware hookup



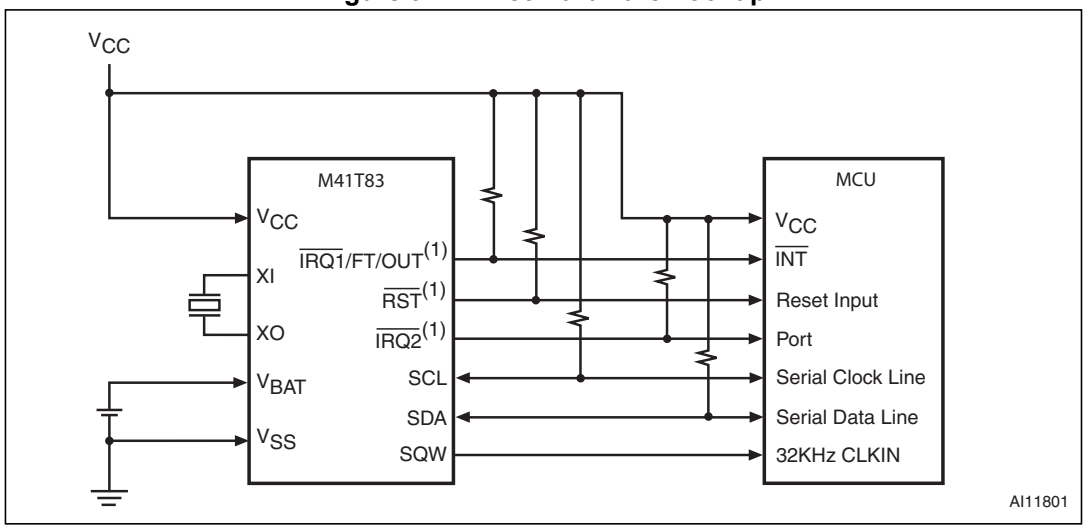
1. Open drain output.

Figure 8. M41T83 block diagram



1. Open drain output.
2. $V_{RST} = V_{SO}$ = 2.93 V (S), 2.63 V (R), and 2.32 V (Z).

Figure 9. M41T83 hardware hookup



1. Open drain output.

2 Operation

The M41T8x clock operates as a slave device on the serial bus. Access is obtained by implementing a start condition followed by the correct slave address (D0h). The 32 bytes contained in the device can then be accessed sequentially in the following order:

- 1st byte: tenths/hundredths of a second register
- 2nd byte: seconds register
- 3rd byte: minutes register
- 4th byte: century/hours register
- 5th byte: day register
- 6th byte: date register
- 7th byte: month register
- 8th byte: year register
- 9th byte: digital calibration register
- 10th byte: watchdog register
- 11th - 15th bytes: alarm 1 registers
- 16th byte: flags register
- 17th byte: timer value register
- 18th byte: timer control register
- 19th byte: analog calibration register
- 20th byte: square wave register
- 21st - 25th bytes: alarm 2 registers
- 26th - 32nd bytes: user RAM

The M41T8x clock continually monitors V_{CC} for an out-of-tolerance condition. Should V_{CC} fall below V_{RST}, the device terminates an access in progress and resets the device address counter. Inputs to the device will not be recognized at this time to prevent erroneous data from being written to the device from an out-of-tolerance system. The power input will also be switched from the V_{CC} pin to the battery when V_{CC} falls below the battery back-up switchover voltage ($V_{SO} = V_{RST}$). At this time the clock registers will be maintained by the attached battery supply. As system power returns and V_{CC} rises above V_{SO}, the battery is disconnected, and the power supply is switched to external V_{CC}.

2.1 2-wire bus characteristics

The bus is intended for communication between different ICs. It consists of two lines: a bi-directional data signal (SDA) and a clock signal (SCL). Both the SDA and SCL lines must be connected to a positive supply voltage via a pull-up resistor.

The following protocol has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is high.
- Changes in the data line, while the clock line is high, will be interpreted as control signals.

Accordingly, the following bus conditions have been defined:

2.1.1 Bus not busy

Both data and clock lines remain high.

2.1.2 Start data transfer

A change in the state of the data line, from high to low, while the clock is high, defines the START condition.

2.1.3 Stop data transfer

A change in the state of the data line, from low to high, while the clock is high, defines the STOP condition.

2.1.4 Data valid

The state of the data line represents valid data when after a start condition, the data line is stable for the duration of the high period of the clock signal. The data on the line may be changed during the low period of the clock signal. There is one clock pulse per bit of data. Each data transfer is initiated with a start condition and terminated with a stop condition. The number of data bytes transferred between the start and stop conditions is not limited. The information is transmitted byte-wide and each receiver acknowledges with a ninth bit.

By definition a device that gives out a message is called “transmitter,” the receiving device that gets the message is called “receiver.” The device that controls the message is called “master.” The devices that are controlled by the master are called “slaves.”

2.1.5 Acknowledge

Each byte of eight bits is followed by one acknowledge bit. This acknowledge bit is a low level put on the bus by the receiver whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed is obliged to generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

The device that acknowledges has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is a stable low during the high period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master receiver must signal an end of data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this case the transmitter must leave the data line high to enable the master to generate the STOP condition.

Figure 10. Serial bus data transfer sequence

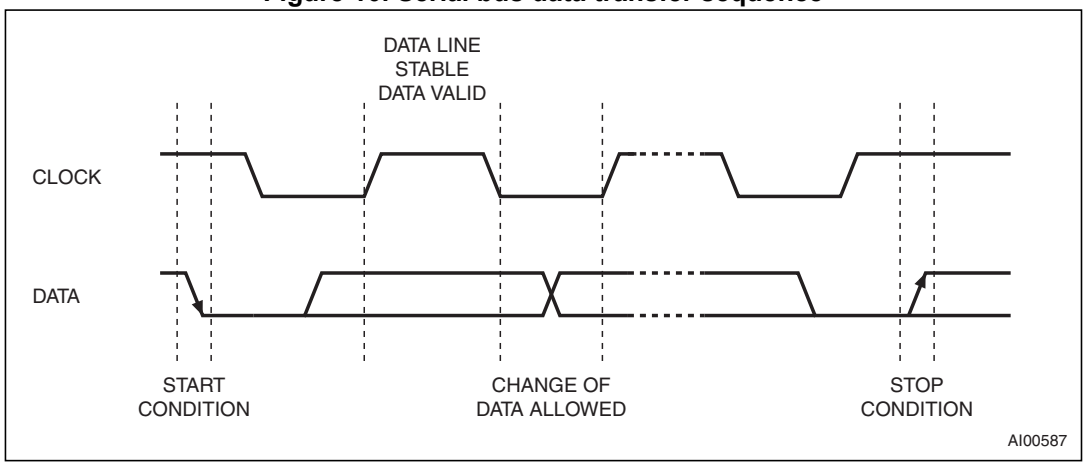
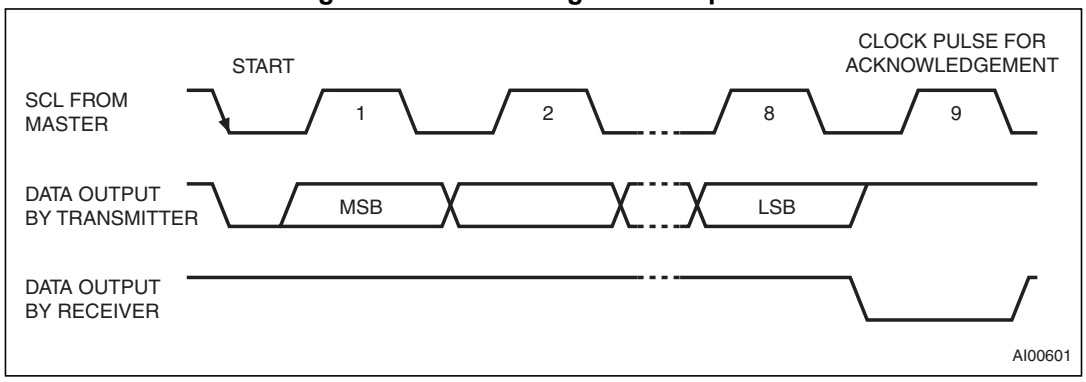


Figure 11. Acknowledgement sequence



2.2 Read mode

In this mode the master reads the M41T8x slave after setting the slave address (see *Figure 13 on page 16*). Following the WRITE mode control bit (R/W = 0) and the acknowledge bit, the word address 'An' is written to the on-chip address pointer. Next the START condition and slave address are repeated followed by the READ mode control bit (R/W = 1). At this point the master transmitter becomes the master receiver. The data byte which was addressed will be transmitted and the master receiver will send an acknowledge bit to the slave transmitter. The address pointer is only incremented on reception of an acknowledge clock. The M41T8x slave transmitter will now place the data byte at address An+1 on the bus, the master receiver reads and acknowledges the new byte and the address pointer is incremented to An+2.

This cycle of reading consecutive addresses will continue until the master receiver sends a STOP condition to the slave transmitter. Most of the registers and memory locations are accessed directly, but the RTC counters are accessed via a set of buffer/transfer registers at addresses 00h to 07h. The counters are not directly read nor written. Instead, at the start of a read or write cycle, the counters are copied into the eight buffer/transfer registers so that the user can read them out sequentially, receiving a coherent set of data, copied from the same instant in time.

An alternate READ mode may also be implemented whereby the master reads the M41T8x slave without first writing to the (volatile) address pointer. The first address that is read is the last one stored in the pointer (see *Figure 14 on page 16*).

Figure 12. Slave address location

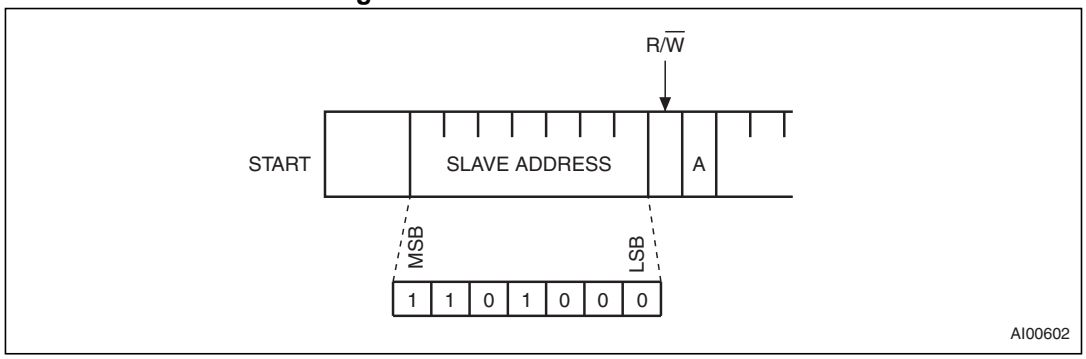


Figure 13. Read mode sequence

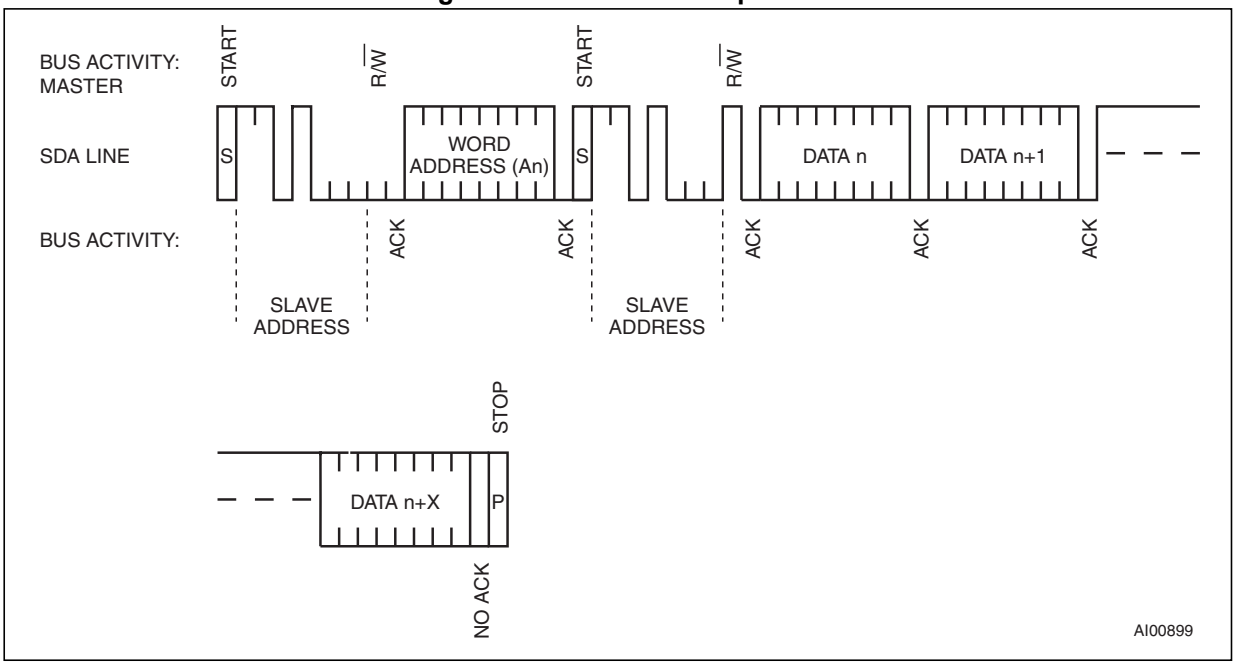
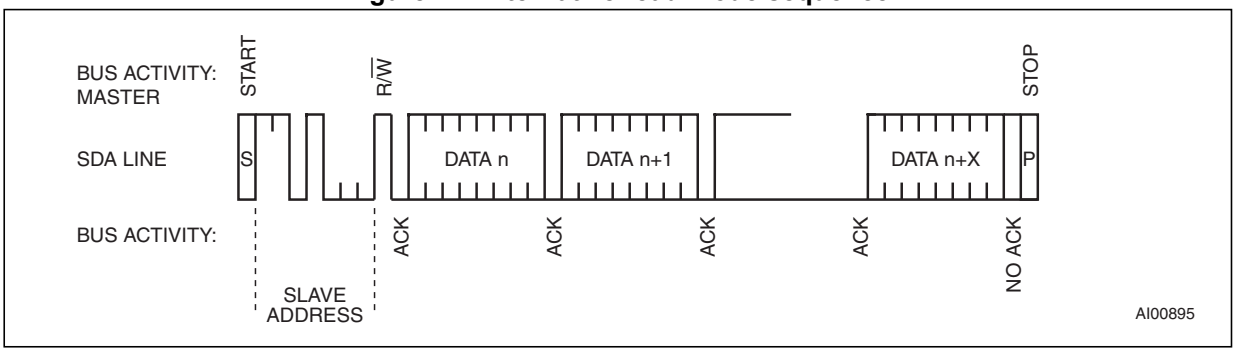


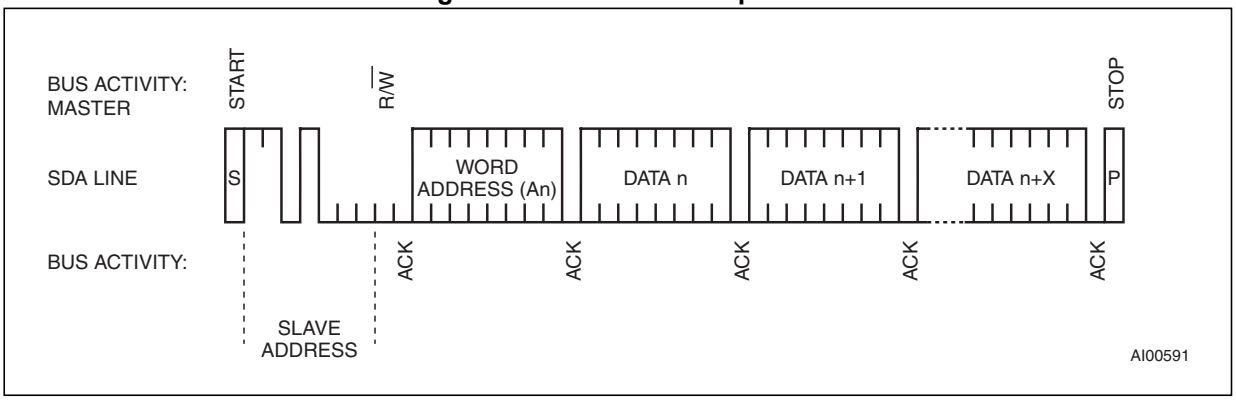
Figure 14. Alternative read mode sequence



2.3 Write mode

In this mode the master transmitter transmits to the M41T8x slave receiver. Bus protocol is shown in *Figure 15*. Following the START condition and slave address, a logic 0 (R/W = 0) is placed on the bus and indicates to the addressed device that word address “An” will follow and is to be written to the on-chip address pointer. The data word to be written to the memory is strobed in next and the internal address pointer is incremented to the next address location on the reception of an acknowledge clock. The M41T8x slave receiver will send an acknowledge clock to the master transmitter after it has received the slave address (see *Figure 12 on page 15*) and again after it has received the word address and each data byte.

Figure 15. Write mode sequence



As in the case of reading, some registers and memory locations are written directly, but the RTC counters are written via a set of eight buffer/transfer registers at addresses 00h to 07h. The user will write the date and time information sequentially, and then, at the end of the I^2C write cycle or when the address pointer increments beyond 07h, the buffer/transfer registers will be copied into the RTC counters. All the time parameters - fractions, seconds, minutes, hours, day, date, month, year, and century bits - are copied simultaneously.

Whatever value is in the buffer/transfer registers will be copied to the counters, so if the user only changes one of the eight bytes, the remaining seven bytes will receive the unchanged contents of the buffer/transfer registers, which will contain whatever was in the counters at the start of the write access.

For example, if the user starts a write cycle on Monday, November 16, 2009, at 17:52:27.03, and writes a 22 to the minutes registers, the value Monday, November 16, 2009, 17:52:22.03 will be written back into the counters. At the start of the write cycle, the eight bytes of counters were copied into the buffer/transfer registers. Then, the seconds register was overwritten. Finally, the eight bytes were copied back into the counters with the result that the seconds value was changed.

2.4 Data retention and battery switchover (V_{SO} = V_{RST})

Once V_{CC} falls below the switchover voltage (V_{SO} = V_{RST}), the device automatically switches over to the battery and powers down into an ultra low current mode of operation to preserve battery life. If V_{BAT} is less than, or greater than V_{RST}, the device power is switched from V_{CC} to V_{BAT} when V_{CC} drops below V_{RST} (see *Figure 28 on page 54*). At this time the clock registers and user RAM will be maintained by the attached battery supply.

When it is powered back up, the device switches back from battery to V_{CC} at V_{SO} + hysteresis. When V_{CC} rises above V_{RST}, it will recognize the inputs. For more information on battery storage life refer to Application Note AN1012.

2.5 Power-on reset (t_{rec})

The M41T8x continuously monitors V_{CC}. When V_{CC} falls to the power fail detect trip point, the $\overline{RST}$ output pulls low (open drain) and remains low after power-up for t_{rec} (210 ms typical) after V_{CC} rises above V_{RST} (max).

Note: The t_{rec} period does not affect the RTC operation. Write protect only occurs when V_{CC} is below V_{RST}. When V_{CC} rises above V_{RST}, the RTC will be selectable immediately. Only the $\overline{RST}$ output is affected by the t_{rec} period.

The $\overline{RST}$ pin is an open drain output and an appropriate pull-up resistor to V_{CC} should be chosen to control the rise time.

3 Clock operation

The M41T8x is driven by a quartz-controlled oscillator with a nominal frequency of 32.768 kHz. The accuracy of the real-time clock depends on the frequency of the quartz crystal that is used as the time-base for the RTC.

The 8-byte clock register (see *Table 2 on page 23* and *Table 4 on page 25*) is used to both set the clock and to read the date and time from the clock, in binary coded decimal format. Tenths/hundredths of seconds, seconds, minutes, and hours are contained within the first four registers.

Bit D7 of register 01h contains the STOP bit (ST). Setting this bit to a '1' will cause the oscillator to stop. When reset to a 0 the oscillator restarts within one second (typical).

Note: Upon initial power-up, the user should set the ST bit to a '1,' then immediately reset the ST bit to 0. This provides an additional "kick-start" to the oscillator circuit.

Bits D6 and D7 of clock register 03h (century/ hours register) contain the CENTURY bit 0 (CB0) and CENTURY bit 1 (CB1). Bits D0 through D2 of register 04h contain the day (day of week). Registers 05h, 06h, and 07h contain the date (day of month), month, and years. The ninth clock register is the digital calibration register, while the analog calibration register is found at address 12h (these are both described in *Section 3.4: Clock calibration*). The RTC includes an oscillator fail detect circuit which sets the OF bit in the flags register (bit 2, register 0fh). For the M41T83, bit D7 of register 09h (watchdog register) contains the oscillator fail interrupt enable bit (OFIE) which can be used to enable an interrupt when the OF bit is set (see *Section 3.12: Oscillator fail detection on page 44*) will also generate an interrupt output.

Note: A WRITE to ANY location within the first eight bytes of the clock register (00h-07h), including the ST bit and CB0-CB1 bits will result in an update of the RTC counters and a reset of the divider chain. This could result in an inadvertent change of the current time. For example, the ST bit is in the seconds register (address 01h) and the century bits (CB0-CB1) are in the hours register (address 03h), so the user should take care to not alter these other parameters when changing the ST bit or the century bits.

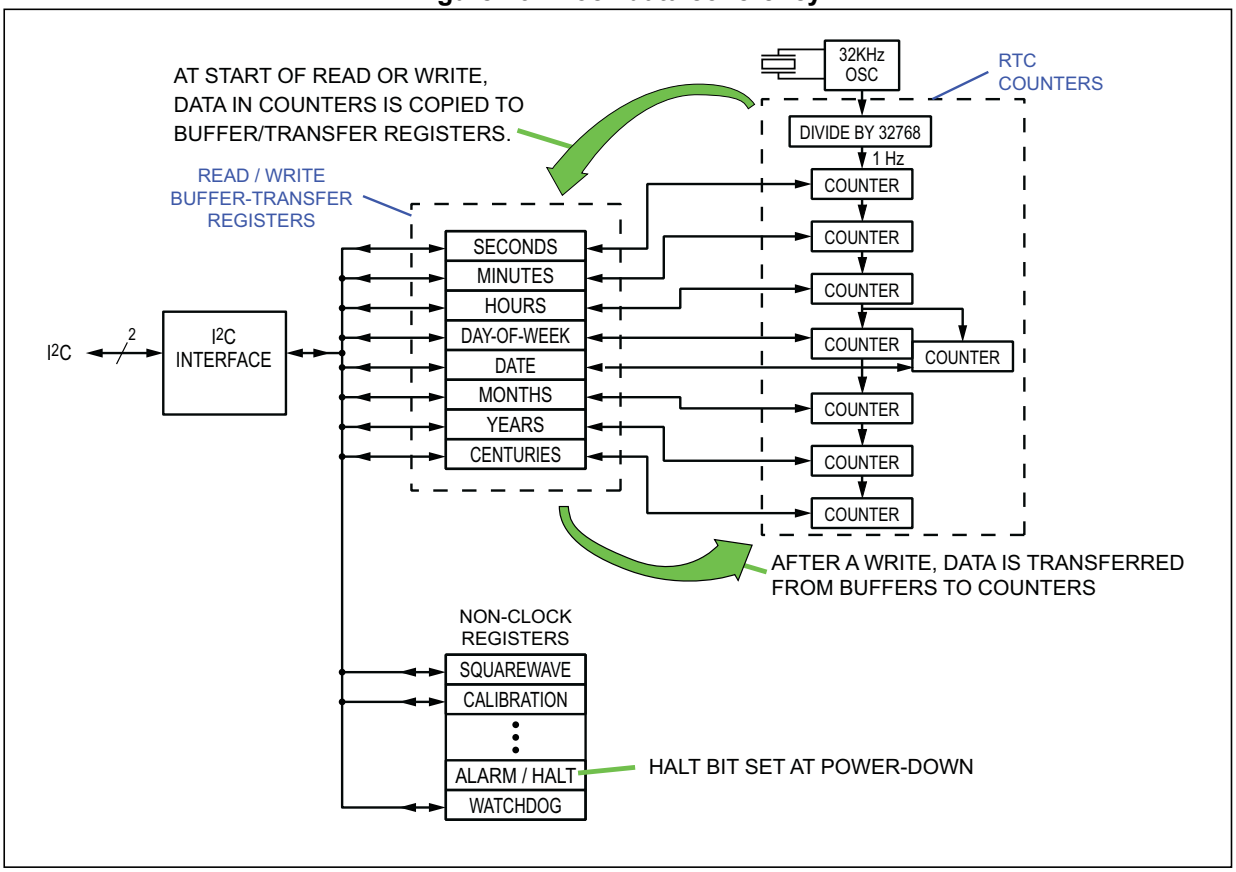
The eight clock registers may be read one byte at a time or in a sequential block. At the start of a read cycle, a copy of the time/date counters is placed in the buffer/transfer registers and can then be transferred out sequentially without concern that the time/date increments during the transfer and thus yields a corrupt value. For example, if the user were to read the seconds register, then start another bus cycle to read the minutes register, the minutes counter could have incremented during the time between the two read cycles. The seconds and minutes values would not be from the same instant in time; they would not be coherent. By using the sequential read feature, the values shifted out are from the same instant in time and are thus coherent.

Similarly, when writing to the RTC registers, during one write cycle, the user can sequentially transfer all eight bytes of time/date into the buffer/transfer registers whereupon they will be loaded simultaneously into the RTC counters thus ensuring a coherent update of the time/date.

3.1 Clock data coherency

In order to synchronize the data during reads and writes of the real-time clock device, a set of buffer transfer registers resides between the I^2C serial interface on the user side, and the clock/calendar counters in the part. While the read/write data is transferred in and out of the device one bit at a time to the user, the transfers between the buffer registers and counters occur such that all the bits are copied simultaneously. This keeps the data coherent and ensures that none of the counters are incremented while the data is being transferred.

Figure 16. Clock data coherency



3.1.1 Example of incoherency

Without having the intervening buffer/transfer registers, if the user began directly reading the counters at 23:59:59, a read of the seconds register would return 59 seconds. After the address pointer incremented, the next read would return 59 minutes. Then the next read should return 23 hours, but if the clock happened to increment between the reads, the user would see 00 hours. When the time was re-assembled, it would appear as 00:59:59, and thus be incorrect by one hour.

By using the buffer/transfer registers to hold a copy of the time, the user is able to read the entire set of registers without any values changing during the read.

Similarly, when the application needs to change the time in the counters, it is necessary that all the counters be loaded simultaneously. Thus, the user writes sequentially to the various buffer/transfer registers, then they are copied to the counters in a single transfer thereby coherently loading the counters.

3.1.2 Accessing the device

The M41T82/83 is comprised of 32 addresses which provide access to registers for time and date, digital and analog calibration, two alarms, watchdog, flags, timer, squarewave (M41T83 only) and NVRAM. The clock and alarm parameters are in binary coded decimal (BCD) format. The calibration, timer, watchdog, and squarewave parameters are in a binary format.

In the case of the M41T82 and M41T83, at the start of each read or write serial transfer, the counters are automatically copied to the buffer registers. In the event of a write to any register in the range 0-7, at the end of the serial transfer, the buffer registers are copied back into the counters thus revising the date/time. Any of the eight clock registers (addresses 0-7) not updated during the transfer will have its old value written back into the counters. For example, if only the seconds value is revised, the other seven counters will end up with the same values they had at the start of the serial transfer.

However, writes which do not affect the clock registers - that is, a write only to the non-clock registers (addresses 0x08 to 0x1F) - will not cause the buffer registers to be copied back to the counters. The counters are only updated if a register in the range 0-7 was written.

Whenever the RTC registers (addresses 0-7) are written, the divider chain from the oscillator is reset.

3.2 Halt bit (HT) operation

When the part is powered down into battery backup mode, a control bit, called the Halt or HT bit, is set automatically. This inhibits any subsequent transfers from the counters to the buffer registers thereby freezing in the buffer registers the time/date of the last access of the part.

Repeated reads of the clock registers will return the same value. After the HT bit is cleared, by writing bit 6 of address 0x0C to 0, the next read of the RTC will return the present time.

Note: Writes to the RTC registers (addresses 0-7) with the HT bit set can cause time corruption. Since the buffer registers contain the time of the last access prior to the HT bit being set, any write in the address range 0-7 will result in the time of the last access being copied back into the counters.

Example: The last access was November 17, 2009, at 16:15:07.77. The system later powered down thus setting the HT bit and freezing that value in the buffers. Later, on December 18, 2009, at 03:22:43.35, the system is powered up and the user writes the seconds to 46 without first clearing the HT bit. At the end of the serial transfer, the old time/date, with the seconds modified to 46, will be written back into the clock registers thereby corrupting them. The new, wrong time will be November 17, 2009, at 16:15:46.77. This makes it appear the RTC lost time during the power outage.

Thus, at power-up, the user should always clear the HT bit (write bit 6 to 0 at address 0x0C) before writing to any address in the range 0-7.

A typical power-up flow is to read the time of last access, then clear the HT bit, then read the current time.

3.2.1 Power-down time-stamp

Some applications may need to determine the amount of time spent in backup mode. That can be calculated if the time of power-down and the time of power-up are known. The latter is straightforward to obtain. But the time of power-down is only available if an access occurred just prior to power-down. That is, if there was an access of the device just prior to power-down, the time of the access would have been frozen in the buffer transfer registers and thus the approximate time of power-down could be obtained.

If an application requires the time of power-down, the best way to implement it is to set up the software to do frequent reads of the clock, such as once every 1 or 5 seconds. That way, at power-up, the buffer-transfer registers will contain a time value within 1 (or 5) seconds of the actual time of power-down. For more information, please refer to AN1572, “Power-down time-stamp function in serial real-time clocks (RTCs)”.

Table 2. M41T82 clock/control register map (32 bytes)(1)

Addr	D7	D6	D5	D4	D3	D2	D1	D0	Function/range BCD format	
00h	0.1 seconds				0.01 seconds				seconds	00-99
01h	ST	10 seconds			seconds				seconds	00-59
02h	0	10 minutes			minutes				minutes	00-59
03h	CB1	CB0	10 hours		Hours (24 hour format)				Century/hours	0-3/00-23
04h	0	0	0	0	0	Day of week			Day	01-7
05h	0	0	10 date		Date: day of month				Date	01-31
06h	0	0	0	10M	Month				Month	01-12
07h	10 years				Year				Year	00-99
08h	0	FT	DCS	DC4	DC3	DC2	DC1	DC0	Digital calibration	
09h	0	BMB4	BMB3	BMB2	BMB1	BMB0	RB1	RB0	Watchdog	
0Ah	0	0	ABE	AI1 10M	Alarm1 month				AI1 month	01-12
0Bh	RPT14	RPT15	AI1 10 date		Alarm1 date				AI1 date	01-31
0Ch	RPT13	HT	AI1 10 hour		Alarm1 hour				AI1 hour	00-23
0Dh	RPT12	Alarm1 10 minutes			Alarm1 minutes				AI1 min	00-59
0Eh	RPT11	Alarm1 10 seconds			Alarm1 seconds				AI1 sec	00-59
0Fh	WDF	AF1	AF2(2)	BL	TF	OF	0	0	Flags	
10h	Timer countdown value								Timer value	
11h	TE	0	0	0	0	0	TD1	TD0	Timer control	
12h	ACS	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Analog calibration	
13h	0	0	0	0	0	0	AL2E	0	SQW	
14h	0(3)	0(3)	0(3)	AI2 10M	Alarm2 month				SRAM/AI2 month	01-12
15h	RPT24	RPT25	AI2 10 date		Alarm2 month				SRAM/AI2 date	01-31
16h	RPT23	0(3)	AI2 10 hour		Alarm2 date				SRAM/AI2 hour	00-23
17h	RPT22	Alarm2 10 minutes			Alarm2 minutes				SRAM/AI2 min	00-59
18h	RPT21	Alarm2 10 seconds			Alarm2 seconds				SRAM/AI2 sec	00-59
19h-1Fh	User SRAM (7 bytes)								SRAM	

1. See *Table 3: Key to Table 2: M41T82 clock/control register map (32 bytes)*
2. AF2 will always read 0, if the AL2E bit is set to 0.
3. As indicated in *Table 3*, the 0 bits should be written to 0. But in the case of these four bits, when AL2E is 0, registers 14-18h are SRAM locations and these bits become SRAM cells which are thus excluded from that restriction.

Table 3. Key to *Table 2: M41T82 clock/control register map (32 bytes)*

Code	Explanation
0	Must be set to zero
ABE	Alarm in battery backup enable bit
AC0-AC6	Analog calibration bits
ACS	Analog calibration sign bit
AF1, AF2	Alarm flag bits
AL2E	Alarm 2 enable bit
BL	Battery low bit
BMB0-BMB4	Watchdog multiplier bits
CB0, CB1	Century bits
DC0-DC4	Digital calibration bits
DCS	Digital calibration sign bit
FT	Frequency test bit
HT	Halt update bit
OF	Oscillator fail bit
RB0-RB2	Watchdog resolution bits
RPT11-RPT15	Alarm 1 repeat mode bits
RPT21-RPT25	Alarm 2 repeat mode bits
ST	Stop bit
TD0, TD1	Timer frequency bits
TE	Timer enable bit
TF	Timer flag
WDF	Watchdog flag

Table 4. M41T83 clock/control register map (32 bytes)(1)

Addr	D7	D6	D5	D4	D3	D2	D1	D0	Function/range BCD format	
00h	0.1 seconds				0.01 seconds				seconds	00-99
01h	ST	10 seconds			seconds				seconds	00-59
02h	0	10 minutes			Minutes				Minutes	00-59
03h	CB1	CB0	10 hours		Hours (24 hour format)				Century/hours	0-3/00-23
04h	0	0	0	0	0	Day of week			Day	01-7
05h	0	0	10 date		Date: day of month				Date	01-31
06h	0	0	0	10M	Month				Month	01-12
07h	10 years				Year				Year	00-99
08h	OUT	FT	DCS	DC4	DC3	DC2	DC1	DC0	Digital calibration	
09h	OFIE	BMB4	BMB3	BMB2	BMB1	BMB0	RB1	RB0	Watchdog	
0Ah	A1IE	SQWE	ABE	AI1 10M	Alarm 1month				AI1 month	01-12
0Bh	RPT14	RPT15	AI1 10 date		Alarm1 date				AI1 date	01-31
0Ch	RPT13	HT	AI1 10 hour		Alarm1 hour				AI1 hour	00-23
0Dh	RPT12	Alarm1 10 minutes			Alarm1 minutes				AI1 min	00-59
0Eh	RPT11	Alarm1 10 seconds			Alarm1 seconds				AI1 sec	00-59
0Fh	WDF	AF1	AF2(2)	BL	TF	OF	0	0	Flags	
10h	Timer countdown value								Timer value	
11h	TE	$\overline{TI}$/TP	TIE	0	0	0	TD1	TD0	Timer control	
12h	ACS	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Analog calibration	
13h	RS3	RS2	RS1	RS0	0	0	AL2E	OTP	SQW	
14h	A2IE	0(3)	0(3)	AI2 10M	Alarm2 month				SRAM/AI2 month	01-12
15h	RPT24	RPT25	AI2 10 date		Alarm2 date				SRAM/AI2 date	01-31
16h	RPT23	0(3)	AI2 10 hour		Alarm2 hour				SRAM/AI2 hour	00-23
17h	RPT22	Alarm2 10 minutes			Alarm2 minutes				SRAM/AI2 min	00-59
18h	RPT21	Alarm2 10 seconds			Alarm2 seconds				SRAM/AI2 sec	00-59
19h-1Fh	User SRAM (7 bytes)								SRAM	

1. See *Table 5: Key to Table 4: M41T83 clock/control register map (32 bytes)*.
2. AF2 will always read 0, if the AL2E bit is set to 0.
3. As indicated in *Table 5*, the 0 bits should be written to 0. But in the case of these three bits, when AL2E is 0, registers 14-18h are SRAM locations and these bits become SRAM cells which are thus excluded from that restriction.