Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

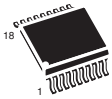
Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

M41T93

Serial SPI bus real-time clock (RTC) with battery switchover

Datasheet - production data

QFN16, 4 mm x 4 mm



SOX18, 11.61 x 7.62 mm
(embedded crystal)

Features

- Ultra-low battery supply current of 365 nA
- Factory calibrated accuracy ±5 ppm typical after 2 reflows (SOX18) (much better accuracies are achievable using built-in programmable analog and digital calibration circuits)
- 2.0 V to 5.5 V clock operating voltage
- Counters for tenths/hundredths of seconds, seconds, minutes, hours, day, date, month, year, and century
- Automatic switchover and reset output circuitry (fixed reference):
  M41T93S: V_{CC} = 3.0 V to 5.5 V;
  M41T93R: V_{CC} = 2.7 V to 5.5 V;
  M41T93Z: V_{CC} = 2.38 V to 5.50 V
- Compatible with SPI bus serial interface (supports SPI mode 0 [CPOL = 0, CPHA = 0])
- Programmable alarm with interrupt function (valid even during battery backup mode)
- Optional 2nd programmable alarm available
- Square wave output (defaults to 32 KHz on power-up)
- RESET ($\overline{RST}$) output
- Watchdog timer
- Programmable 8-bit counter/timer
- 7 bytes of battery-backed user SRAM
- Battery low flag
- Low operating current of 80 µA
- Oscillator stop detection
- Battery or supercapacitor backup
- Operating temperature of –40 °C to +85 °C
- Package options include a 16-lead QFN and an 18-lead embedded crystal SOIC

Contents

List of tables

List of figures

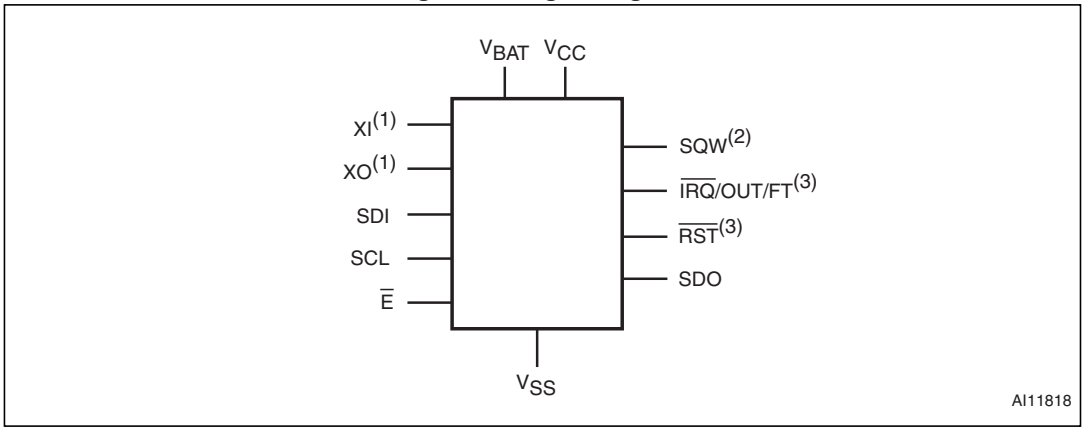
1 Description

The M41T93 is a low-power serial SPI bus real-time clock (RTC) with a built-in 32.768 kHz oscillator (external crystal-controlled for the QFN16 package, and embedded crystal for the SOX18 package). Eight bytes of the register map are used for the clock/calendar function and are configured in binary coded decimal (BCD) format. An additional 17 bytes of the register map provide status/control of the two alarms, watchdog, 8-bit counter, and square wave functions. An additional seven bytes are made available as user SRAM.

Addresses and data are transferred serially via a serial SPI bus-compatible interface. The built-in address register is incremented automatically after each WRITE or READ data byte. The M41T93 has a built-in power sense circuit which detects power failures and automatically switches to the battery supply when a power failure occurs. The energy needed to sustain the clock operations can be supplied by a small lithium button battery when a power failure occurs.

Functions available to the user include a non-volatile, time-of-day clock/calendar, alarm interrupt, watchdog timer, programmable 8-bit counter, and square wave outputs. The eight clock address locations contain the century, year, month, date, day, hour, minute, second, and tenths/hundredths of a second in 24-hour BCD format. Corrections for 28, 29 (leap year), 30, and 31 day months are made automatically. The M41T93 is supplied in either a QFN16 or an SOX18, 300 mil SOIC which includes an embedded 32 KHz crystal. The SOX18 package requires only a user-supplied battery to provide non-volatile operation.

Figure 1. Logic diagram



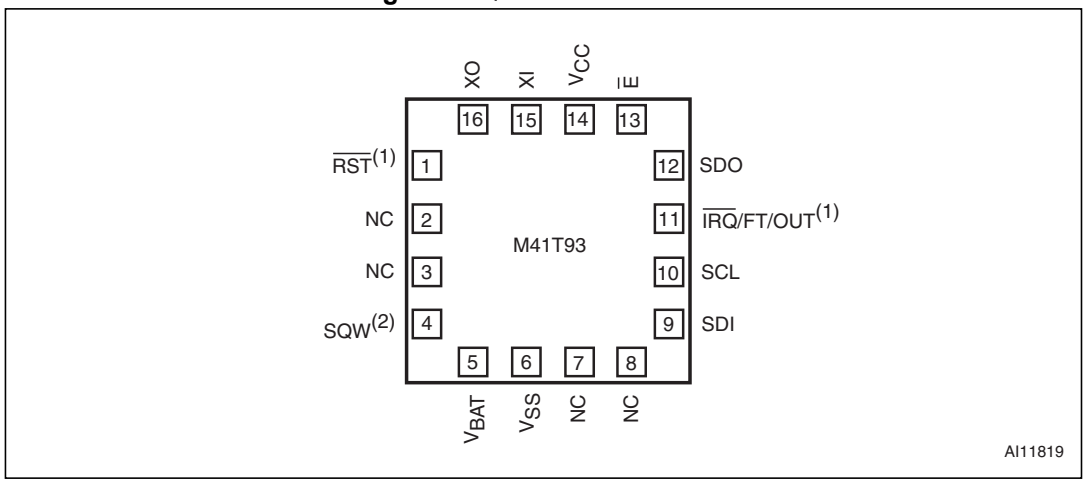
1. For QFN16 package only
2. Defaults to 32 KHz on power-up
3. Open drain

Table 1. Signal names

Symbol	Description
XI(1)	32 KHz oscillator input
XO(1)	32 KHz oscillator output
$\overline{IRQ}$/FT/OUT	Interrupt/frequency test/output driver (open drain)
SQW(2)	32 KHz programmable square wave output
$\overline{RST}$	Power-on reset output (open drain)
$\overline{E}$	Chip enable
SDI	Serial data address input
SDO	Serial data address output
SCL	Serial clock input
V_{BAT}	Battery supply voltage (tie V_{BAT} to V_{SS} if no battery is connected)
DU(3)	Do not use
V_{CC}	Supply voltage
V_{SS}	Ground

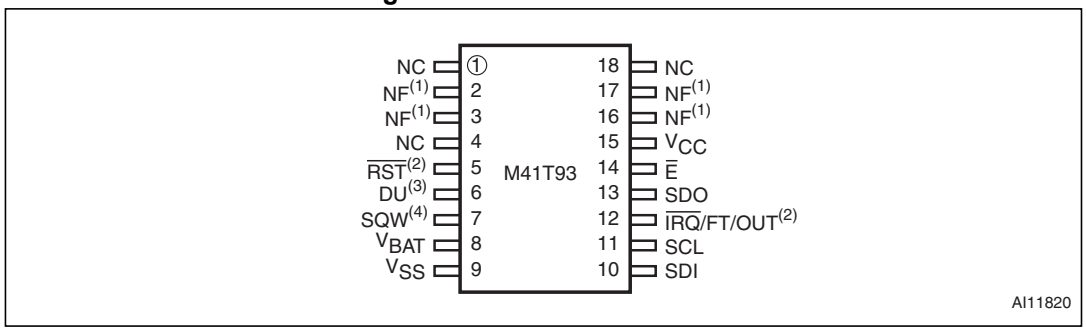
1. For QFN16 package only
2. Defaults to 32 KHz on power-up
3. Do not use (must be tied to V_{CC})

Figure 2. QFN16 connections



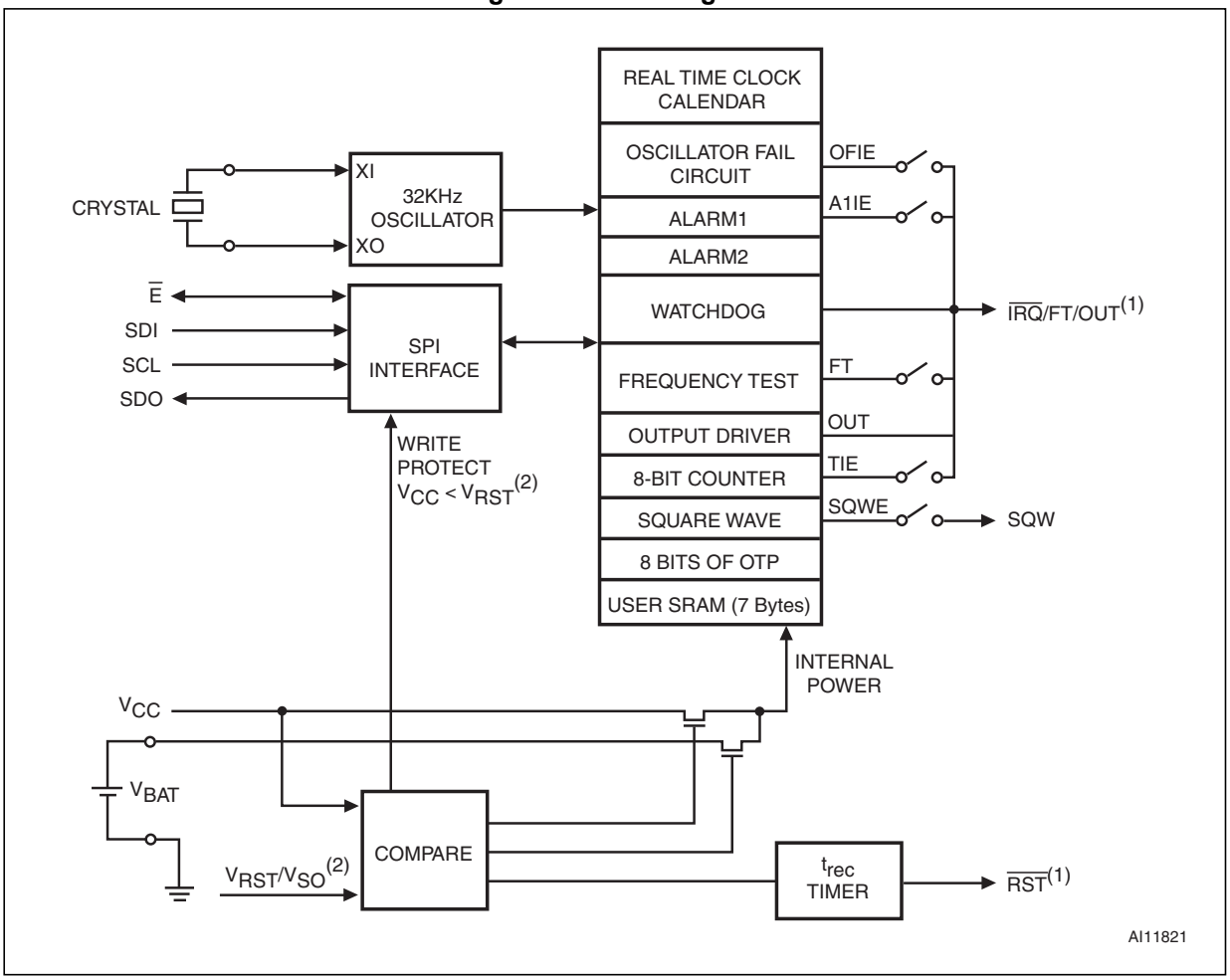
1. Open drain output
2. Defaults to 32 KHz on power-up

Figure 3. SOX18 connections



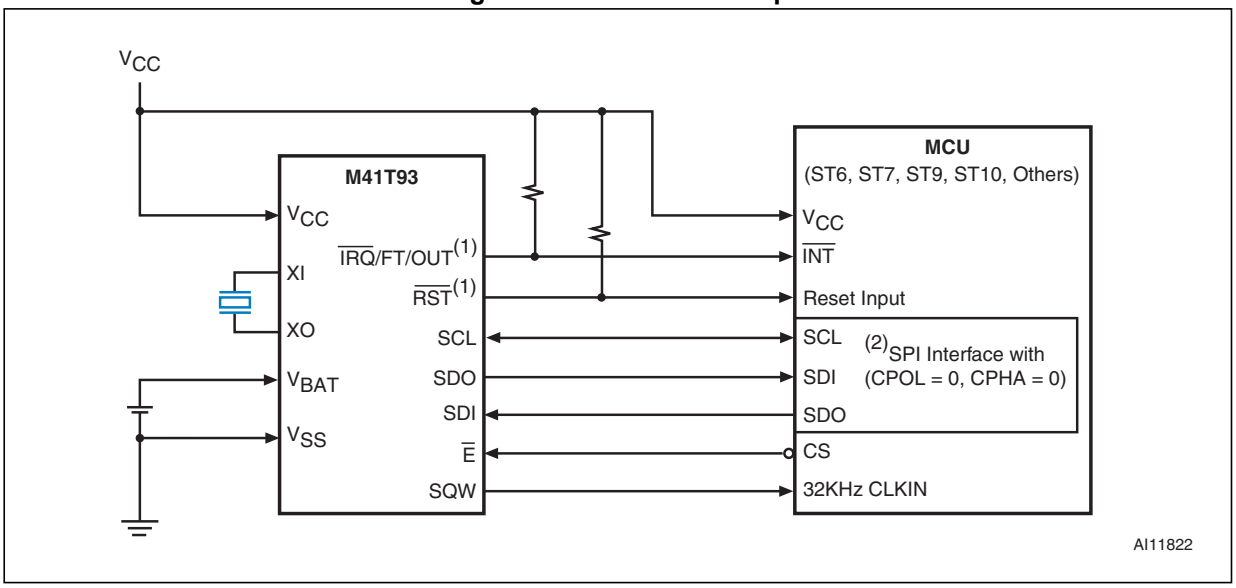
1. NF pins must be tied to V_{SS}. Pins 2 and 3, and 16 and 17 are internally shorted together.
2. Open drain output
3. Do not use (must be tied to V_{CC})
4. Defaults to 32 KHz on power-up

Figure 4. Block diagram



1. Open drain output
2. $V_{RST} = V_{SO}$ = 2.93 V (S), 2.63 V (R), and 2.32 V (Z)

Figure 5. Hardware hookup



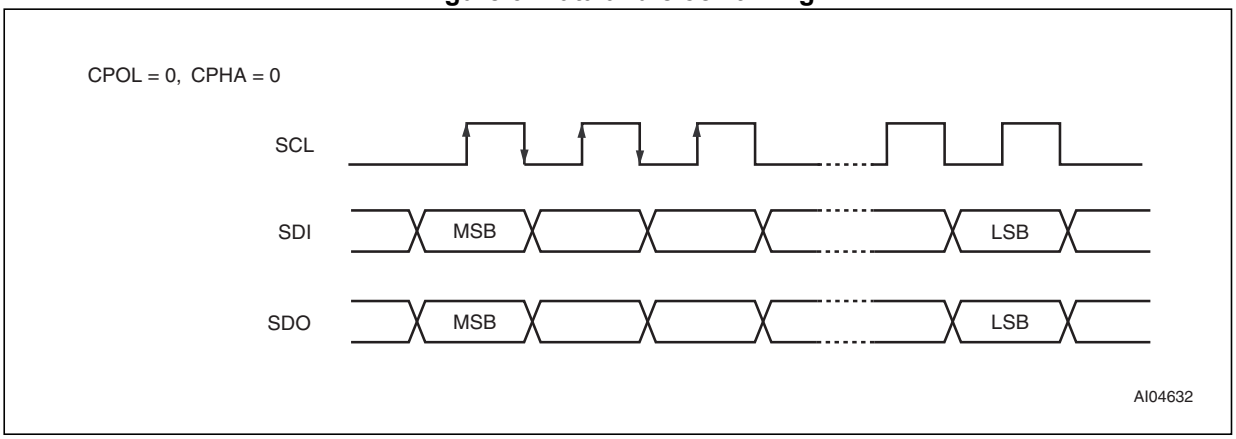
1. Open drain output
2. CPOL (clock polarity) and CPHA (clock phase) are bits that may be set in the SPI control register of the MCU.

Table 2. Function table

Mode	E	SCL	SDI	SDO
Disable reset	H	Input disabled	Input disabled	High Z
WRITE	L		Data bit latch	High Z
READ	L		X	Next data bit shift(1)

1. SDO remains at High Z until eight bits of data are ready to be shifted out during a READ.

Figure 6. Data and clock timing



Note: Supports SPI mode 0 (CPOL = 0, CPHA = 0) only.

1.1 SPI signal description

1.1.1 Serial data output (SDO)

The output pin is used to transfer data serially out of the device. Data is shifted out on the falling edge of the serial clock.

1.1.2 Serial data input (SDI)

The input pin is used to transfer data serially into the device. Instructions, addresses, and the data to be written, are each received this way. Input is latched on the rising edge of the serial clock.

1.1.3 Serial clock (SCL)

The serial clock provides the timing for the serial interface (as shown in *Figure 23 on page 48* and *Figure 24 on page 48*). The W/R bit, addresses, or data are latched, from the input pin, on the rising edge of the clock input. The output data on the SDO pin changes state after the falling edge of the clock input.

The M41T93 can be driven by a microcontroller with its SPI peripheral running in only mode 0: (CPOL, CPHA) = (0,0).

For this mode, input data (SDI) is latched in by the low-to-high transition of clock SCL, and output data (SDO) is shifted out on the high-to-low transition of SCL (see *Table 2 on page 10* and *Figure 6 on page 10*).

1.1.4 Chip enable ($\overline{E}$)

When $\overline{E}$ is high, the memory device is deselected, and the SDO output pin is held in its high impedance state.

After power-on, a high-to-low transition on $\overline{E}$ is required prior to the start of any operation.

2 Operation

The M41T93 clock operates as a slave device on the SPI serial bus. It is accessed by a simple serial interface that is SPI bus-compatible. The bus signals are SCL, SDI, SDO, and $\overline{E}$ (see *Table 1 on page 7* and *Figure 5 on page 10*). The device is selected when the chip enable input ($\overline{E}$) is held low. All instructions, addresses and data are shifted serially in and out of the chip. The most significant bit is presented first, with the data input (SDI) sampled on the first rising edge of the clock (SCL) after the chip enable ($\overline{E}$) goes low. The 32 bytes contained in the device can then be accessed sequentially in the following order:

- 1st byte: tenths/hundredths of a second register
- 2nd byte: seconds register
- 3rd byte: minutes register
- 4th byte: century/hours register
- 5th byte: day register
- 6th byte: date register
- 7th byte: month register
- 8th byte: year register
- 9th byte: digital calibration register
- 10th byte: watchdog register
- 11th - 15th bytes: alarm 1 registers
- 16th byte: flags register
- 17th byte: timer value register
- 18th byte: timer control register
- 19th byte: analog calibration register
- 20th byte: square wave register
- 21st - 25th bytes: alarm 2 registers
- 26th - 32nd bytes: user RAM

The M41T93 clock continually monitors V_{CC} for an out-of tolerance condition. Should V_{CC} fall below V_{RST}, the device terminates any access in progress and resets the device address counter. Inputs to the device will not be recognized at this time to prevent erroneous data from being written to the device from an out-of-tolerance system.

The power input will also be switched from the V_{CC} pin to the external battery when V_{CC} falls below the battery back-up switchover voltage ($V_{SO} = V_{RST}$). At this time the clock registers will be maintained by the battery supply. As system power returns and V_{CC} rises above V_{SO}, the battery is disconnected, and the power supply is switched to external V_{CC}.

The device remains write protected until t_{REC} seconds elapse after V_{CC} rises above V_{PFD} (min). For more information on battery storage life refer to application note AN1012.

2.1 SPI bus characteristics

The serial peripheral interface (SPI) bus is intended for synchronous communication between different ICs. It consists of four signal lines: serial data input (SDI), serial data output (SDO), serial clock (SCL) and a chip enable ($\overline{E}$).

By definition a device that gives out a message is called “transmitter,” the receiving device that gets the message is called “receiver.” The device that controls the message is called “master.” The devices that are controlled by the master are called “slaves.”

The $\overline{E}$ input is used to initiate and terminate a data transfer. The SCL input is used to synchronize data transfer between the master (micro) and the slave (M41T93) device.

The SCL input, which is generated by the microcontroller, is active only during address and data transfer to any device on the SPI bus (see *Figure 5 on page 10*).

The M41T93 can be driven by a microcontroller with its SPI peripheral running in only mode 0: (CPOL, CPHA) = (0,0).

For this mode, input data (SDI) is latched in by the low-to-high transition of clock SCL, and output data (SDO) is shifted out on the high-to-low transition of SCL (see *Table 2* and *Figure 6 on page 10*).

There is one clock for each bit transferred. Address and data bits are transferred in groups of eight bits. Since only 32 addresses are required, address bit 6 is a “don’t care”.

2.2 READ and WRITE cycles

Address and data are shifted MSB first into the serial data input (SDI) and out of the serial data output (SDO). Any data transfer considers the first bit to define whether a READ or WRITE will occur. This is followed by seven bits defining the address to be read or written. Data is transferred out of the SDO for a READ operation and into the SDI for a WRITE operation. The address is always the second through the eighth bit written after the enable ($\overline{E}$) pin goes low. If the first bit is a '1,' one or more WRITE cycles will occur. If the first bit is a '0,' one or more READ cycles will occur (see *Figure 7* and *Figure 8 on page 14*).

Data transfers can occur one byte at a time or in multiple byte burst mode, during which the address pointer will be automatically incremented. For a single byte transfer, one byte is read or written and then $\overline{E}$ is driven high. For a multiple byte transfer all that is required is that $\overline{E}$ continue to remain low. Under this condition, the address pointer will continue to increment as stated previously. Incrementing will continue until the device is deselected by taking $\overline{E}$ high. The address will wrap to 00h after incrementing to 3Fh.

Reads and writes of the internal counters are performed through a set of buffer/transfer registers as shown in *Figure 9 on page 17*. At the start of any read or write cycle, the counters are copied to the buffer/transfer registers. Thus, the time/date is effectively frozen for the user until the access is completed, although the counters are still running and maintaining the correct time.

Note: This is true both in READ and WRITE mode.

Figure 7. READ mode sequence

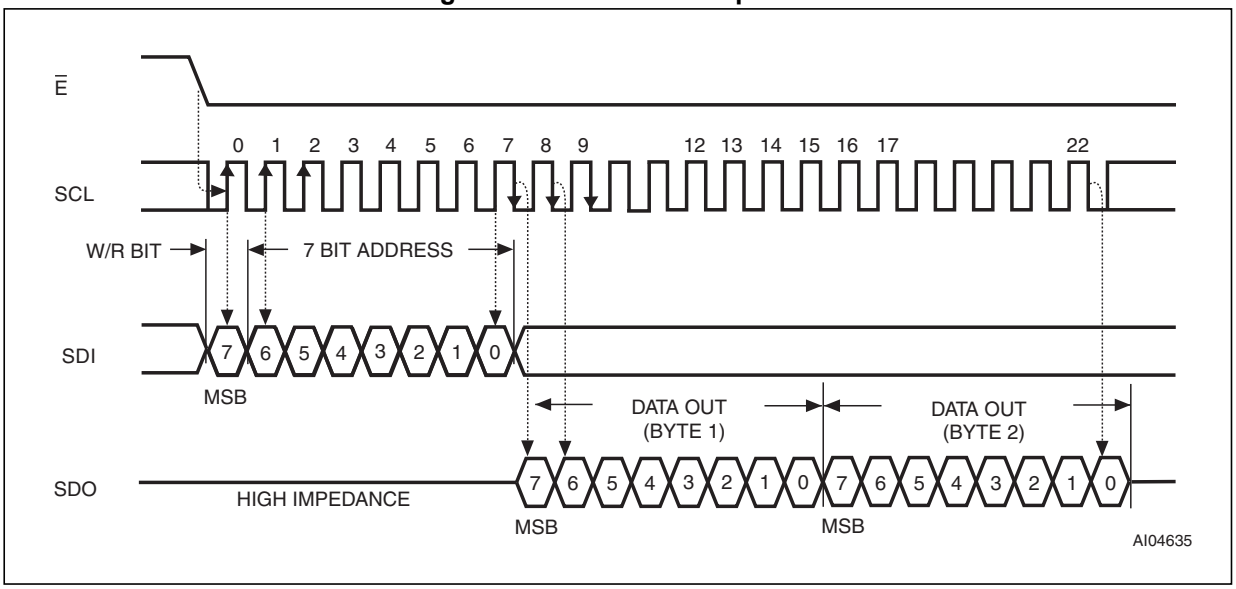
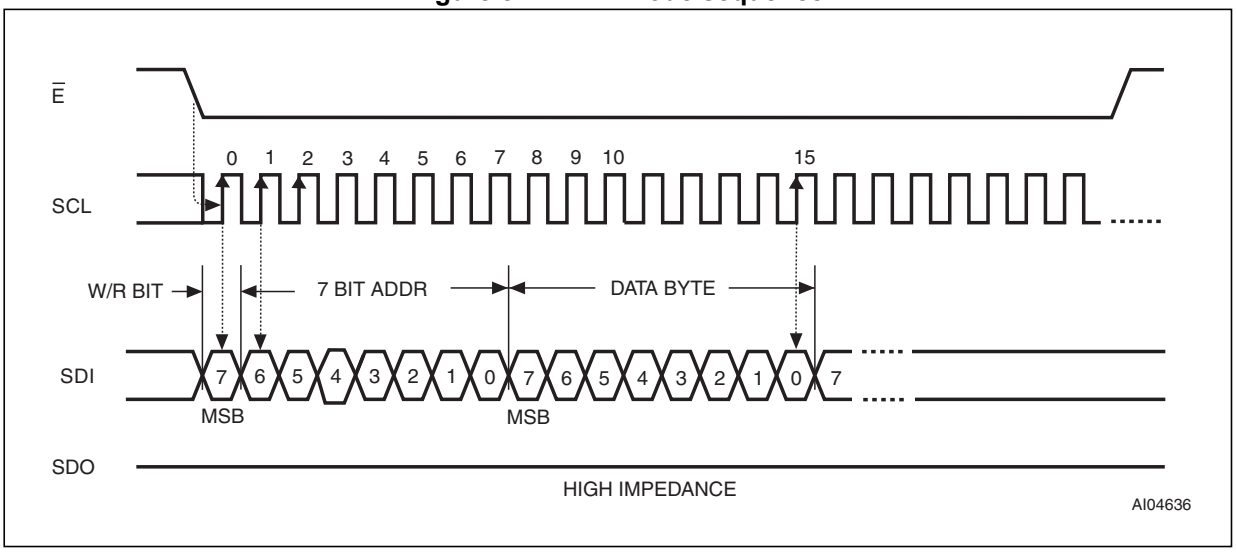


Figure 8. WRITE mode sequence



2.3 Data retention and battery switchover (V_{SO} = V_{RST})

Once V_{CC} falls below the switchover voltage (V_{SO} = V_{RST}), the device automatically switches over to the battery and powers down into an ultra low current mode of operation to preserve battery life (see *Figure 22 on page 47*). At this time the clock registers and user RAM will be maintained by the attached battery supply.

When it is powered back up, the device switches back from battery to V_{CC} at V_{SO} + hysteresis. When V_{CC} rises above V_{RST}, it will recognize the inputs. For more information on battery storage life refer to application note AN1012.

2.4 Power-on reset (t_{rec})

The M41T93 continuously monitors V_{CC}. When V_{CC} falls to the power fail detect trip point, the $\overline{RST}$ output pulls low (open drain) and remains low after power-up for t_{rec} (210 ms typical) after V_{CC} rises above V_{RST} (max).

Note: The t_{rec} period does not affect the RTC operation. Write protect only occurs when V_{CC} is below V_{RST}. When V_{CC} rises above V_{RST}, the RTC will be selectable immediately. Only the $\overline{RST}$ output is affected by the t_{rec} period.

The $\overline{RST}$ pin is an open drain output and an appropriate pull-up resistor to V_{CC} should be chosen to control the rise time.

3 Clock operation

The M41T93 is driven by a quartz-controlled oscillator with a nominal frequency of 32.768 kHz. The accuracy of the real-time clock depends on the frequency of the quartz crystal that is used as the time-base for the RTC.

The 8-byte clock register (see *Table 3 on page 20*) is used to both set the clock and to read the date and time from the clock, in binary coded decimal format. Tenths/hundredths of seconds, seconds, minutes, and hours are contained within the first four registers.

Bit D7 of register 01h contains the STOP bit (ST). Setting this bit to a '1' will cause the oscillator to stop. When reset to a '0' the oscillator restarts within one second (typical).

Note: Upon initial power-up, the user should set the ST bit to a '1,' then immediately reset the ST bit to '0.' This provides an additional "kick-start" to the oscillator circuit.

Bits D6 and D7 of clock register 03h (century/ hours register) contain the CENTURY bit 0 (CB0) and CENTURY bit 1 (CB1). Bits D0 through D2 of register 04h contain the day (day of week). Registers 05h, 06h, and 07h contain the date (day of month), month, and years. The ninth clock register is the digital calibration register, while the analog calibration register is found at address 12h (these are both described in the clock calibration section). Bit D7 of register 09h (watchdog register) contains the oscillator fail interrupt enable bit (OFIE). When the user sets this bit to '1,' any condition which sets the oscillator fail bit (OF) (see *Oscillator fail detection on page 38*) will also generate an interrupt output.

Note: A WRITE to ANY location within the first eight bytes of the clock registers (00h-07h), including the ST bit and CB0-CB1 bits will result in an update of the RTC counters and a reset of the divider chain. This could result in an inadvertent change of the current time. For example, the ST bit is in the seconds register (address 01h) and the century bits (CB0-CB1) are in the hours register (address 03h), so the user should take care to not alter these other parameters when changing the ST bit or the century bits.

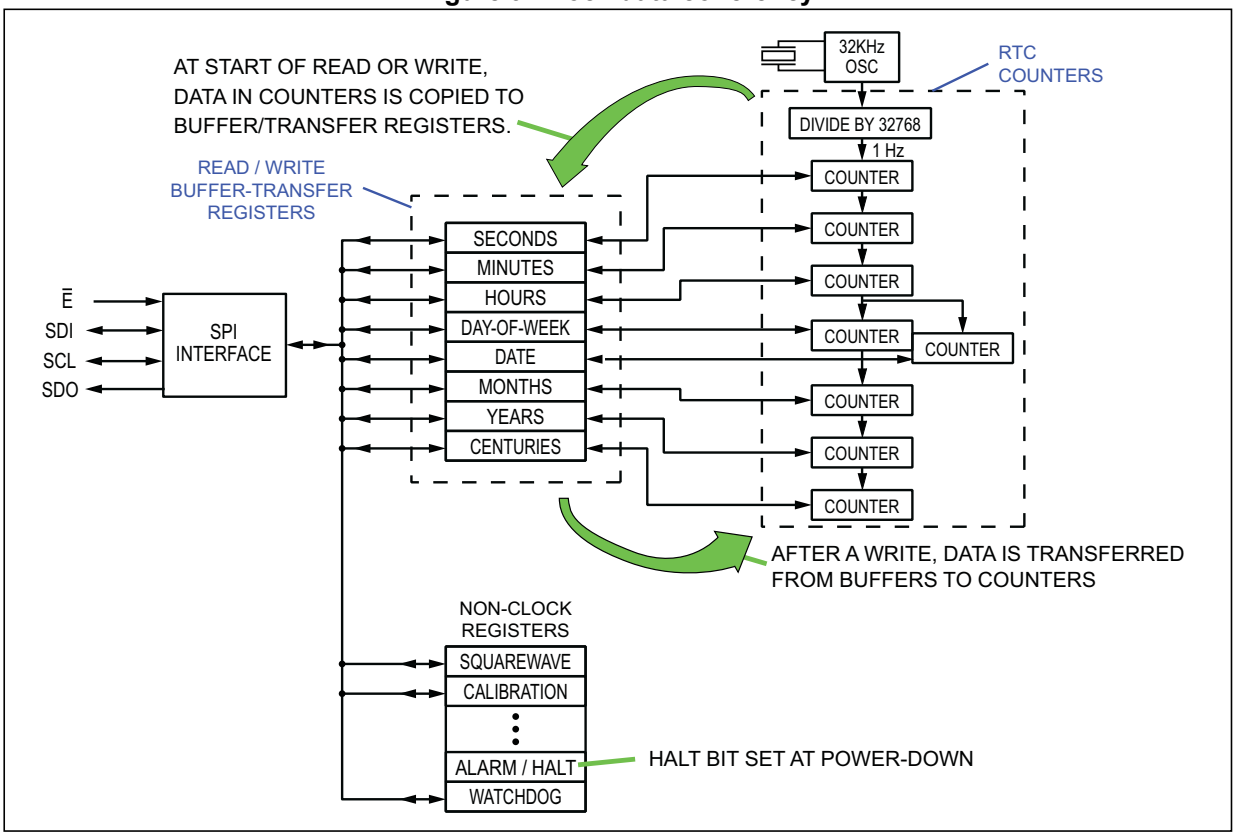
The eight clock registers may be read one byte at a time, or in a sequential block. At the start of a read cycle, a copy of the time/date counters is placed in the buffer/transfer registers and can then be transferred out sequentially without concern that the time/date increments during the transfer and thus yields a corrupt value. For example, if the user were to read the seconds register, then start another bus cycle to read the minutes register, the minutes counter could have incremented during the time between the two read cycles. The seconds and minutes values would not be from the same instant in time; they would not be coherent. By using the sequential read feature, the values shifted out are from the same instant in time and are thus coherent.

Similarly, when writing to the RTC registers, during one write cycle, the user can sequentially transfer all eight bytes of time/date into the buffer/transfer registers whereupon they will be loaded simultaneously into the RTC counters thus ensuring a coherent update of the time/date.

3.1 Clock data coherency

In order to synchronize the data during reads and writes of the real-time clock device, a set of buffer transfer registers resides between the SPI serial interface on the user side, and the clock/calendar counters in the part. While the read/write data is transferred in and out of the device one bit at a time to the user, the transfers between the buffer registers and counters occur such that all the bits are copied simultaneously. This keeps the data coherent and ensures that none of the counters are incremented while the data is being transferred.

Figure 9. Clock data coherency



3.1.1 Example of incoherency

Without having the intervening buffer/transfer registers, if the user began directly reading the counters at 23:59:59, a read of the seconds register would return 59 seconds. After the address pointer incremented, the next read would return 59 minutes. Then the next read should return 23 hours, but if the clock happened to increment between the reads, the user would see 00 hours. When the time was re-assembled, it would appear as 00:59:59, and thus be incorrect by one hour.

By using the buffer/transfer registers to hold a copy of the time, the user is able to read the entire set of registers without any values changing during the read.

Similarly, when the application needs to change the time in the counters, it is necessary that all the counters be loaded simultaneously. Thus, the user writes sequentially to the various buffer/transfer registers, then they are copied to the counters in a single transfer thereby coherently loading the counters.

3.1.2 Accessing the device

The M41T93 is comprised of 32 addresses which provide access to registers for time and date, digital and analog calibration, two alarms, watchdog, flags, timer, squarewave and NVRAM. The clock and alarm parameters are in binary coded decimal (BCD) format. The calibration, timer, watchdog, and squarewave parameters are in a binary format.

In the case of the M41T93, at the start of each read or write serial transfer, the counters are automatically copied to the buffer registers. In the event of a write to any register in the range 0-7, at the end of the serial transfer, the buffer registers are copied back into the counters thus revising the date/time. Any of the eight clock registers (addresses 0-7) not updated during the transfer will have its old value written back into the counters. For example, if only the seconds value is revised, the other seven counters will end up with the same values they had at the start of the serial transfer.

However, writes which do not affect the clock registers - that is, a write only to the non-clock registers (addresses 0x08 to 0x1F) - will not cause the buffer registers to be copied back to the counters. The counters are only updated if a register in the range 0-7 was written.

Whenever the RTC registers (addresses 0-7) are written, the divider chain from the oscillator is reset.

3.2 Halt bit (HT) operation

When the part is powered down into battery backup mode, a control bit, called the Halt or HT bit, is set automatically. This inhibits any subsequent transfers from the counters to the buffer registers thereby freezing in the buffer registers the time/date of the last access of the part.

Repeated reads of the clock registers will return the same value. After the HT bit is cleared, by writing bit 6 of address 0x0C to 0, the next read of the RTC will return the present time.

Note: Writes to the RTC registers (addresses 0-7) with the HT bit set can cause time corruption. Since the buffer registers contain the time of the last access prior to the HT bit being set, any write in the address range 0-7 will result in the time of the last access being copied back into the counters.

Example: The last access was November 17, 2009, at 16:15:07.77. The system later powered down thus setting the HT bit and freezing that value in the buffers. Later, on December 18, 2009, at 03:22:43.35, the system is powered up and the user writes the seconds to 46 without first clearing the HT bit. At the end of the serial transfer, the old time/date, with the seconds modified to 46, will be written back into the clock registers thereby corrupting them. The new, wrong time will be November 17, 2009, at 16:15:46.77. This makes it appear the RTC lost time during the power outage.

Thus, at power-up, the user should always clear the HT bit (write bit 6 to 0 at address 0x0C) before writing to any address in the range 0-7.

A typical power-up flow is to read the time of last access, then clear the HT bit, then read the current time.

3.2.1 Power-down time stamp

Some applications may need to determine the amount of time spent in backup mode. That can be calculated if the time of power-down and the time of power-up are known. The latter is straightforward to obtain. But the time of power-down is only available if an access occurred just prior to power-down. That is, if there was an access of the device just prior to power-down, the time of the access would have been frozen in the buffer transfer registers and thus the approximate time of power-down could be obtained.

If an application requires the time of power-down, the best way to implement it is to set up the software to do frequent reads of the clock, such as once every 1 or 5 seconds. That way, at power-up, the buffer-transfer registers will contain a time value within 1 (or 5) seconds of the actual time of power-down. For more information, please refer to AN1572, “Power-down time-stamp function in serial real-time clocks (RTCs)”.

Table 3. Clock/control register map (32 bytes)

Addr	D7	D6	D5	D4	D3	D2	D1	D0	Function/range BCD format	
00h	0.1 seconds				0.01 seconds				Seconds	00-99
01h	ST	10 seconds			Seconds				Seconds	00-59
02h	0	10 minutes			Minutes				Minutes	00-59
03h	CB1	CB0	10 hours		Hours (24-hour format)				Century/hours	0-3/00-23
04h	0	0	0	0	0	Day of week			Day	01-7
05h	0	0	10 date		Date: day of month				Date	01-31
06h	0	0	0	10M	Month				Month	01-12
07h	10 Years				Year				Year	00-99
08h	OUT	FT	DCS	DC4	DC3	DC2	DC1	DC0	Digital calibration	
09h	OFIE	BMB4	BMB3	BMB2	BMB1	BMB0	RB1	RB0	Watchdog	
0Ah	A1IE	SQWE	ABE	AI1 10M	Alarm1month				AI1 month	01-12
0Bh	RPT14	RPT15	AI1 10 date		Alarm1 date				AI1 date	01-31
0Ch	RPT13	HT	AI1 10 hour		Alarm1 hour				AI1 hour	00-23
0Dh	RPT12	Alarm1 10 minutes			Alarm1 minutes				AI1 min	00-59
0Eh	RPT11	Alarm1 10 seconds			Alarm1 seconds				AI1 sec	00-59
0Fh	WDF	AF1	AF2(1)	BL	TF	OF	0	0	Flags	
10h	Timer countdown value								Timer value	
11h	TE	TI/TP	TIE	0	0	0	TD1	TD0	Timer control	
12h	ACS	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Analog calibration	
13h	RS3	RS2	RS1	RS0	0	0	AL2E	OTP	SQW	
14h	0	0	0	AI2 10M	Alarm2 month				SRAM/AI2 month	01-12
15h	RPT24	RPT25	AI2 10 date		Alarm2 month				SRAM/AI2 date	01-31
16h	RPT23	0	AI2 10 hour		Alarm2 date				SRAM/AI2 hour	00-23
17h	RPT22	Alarm2 10 minutes			Alarm2 minutes				SRAM/AI2 min	00-59
18h	RPT21	Alarm2 10 seconds			Alarm2 seconds				SRAM/AI2 sec	00-59
19h-1Fh	User SRAM (7 bytes)								SRAM	

1. AF2 will always read 0 if the AL2E bit is set to 0.

0 = Must be set to zero
ABE = Alarm in battery backup enable bit
A1IE = Alarm1 interrupt enable bit
AC0-AC6 = analog calibration bits
ACS = analog calibration sign bit
AF1, AF2 = Alarm flag
AL2E = Alarm 2 enable bit
BL = Battery low bit
BMB0-BMB4 = Watchdog multiplier bits
CB0, CB1 = Century bits
DC0-DC4 = Digital calibration bits
DCS = Digital calibration sign bit
FT = Frequency test bit
HT = Halt update bit
OF = Oscillator fail bit
OUT= Output level
OFIE = Oscillator fail interrupt enable
OTP = OTP control bit
RB0-RB2 = Watchdog resolution bits
RPT11-RPT15 = Alarm 1 repeat mode bits
RPT21-RPT25 = Alarm 2 repeat mode bits
RS0-RS3 = SQW frequency
SQWE = Square wave enable
SRAM/$\overline{ALM2}$ = SRAM/Alarm 2 bit
ST = Stop bit
TD0, TD1 = Timer frequency bits
TE = Timer enable bit
TF = Timer flag
$\overline{TI}$/TP = Timer interrupt or pulse
TIE = Timer interrupt enable
WDF = Watchdog flag

3.3 Real-time clock accuracy

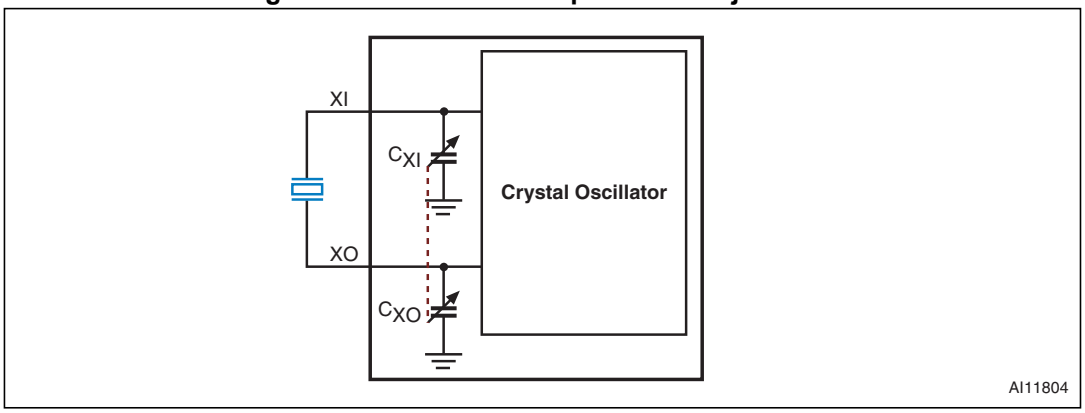
The M41T93 is driven by a quartz controlled oscillator with a nominal frequency of 32,768 Hz. The accuracy of the real-time clock is dependent upon the accuracy of the crystal, and the match between the capacitive load of the oscillator circuit and the capacitive load for which the crystal was trimmed. Temperature also affects the crystal frequency, causing additional error (see *Figure 11 on page 26*).

The M41T93 provides the option of clock correction through either manufacturing calibration or in-application calibration. The total possible compensation is typically –93 ppm to +156 ppm. The two compensation circuits that are available are:

1. The analog calibration register (12h) can be used to adjust internal (on-chip) load capacitors for oscillator capacitance trimming. There are two load capacitors C_{XI} and C_{XO} (see *Figure 10*), nominally 25 pF each, one on either side of the crystal. The effective load capacitance is the series equivalent of C_{XI} and C_{XO}. For the nominal 25 pF, the effective load capacitance is 12.5pF.
   Writing to the analog calibration register adjusts both capacitors by the same amount. That is, the two capacitors will always have the same value. They can be adjusted up or down in 0.25 pF steps. The maximum adjustment up is +9.75 pF for a total of 34.75 pF (17.4 pF effective load) to slow the oscillator. The maximum downward adjustment is –18 pF for a total of 7 pF (3.5 pF effective load) to speed up the oscillator.
2. A digital calibration register (08h) can also be used to adjust the clock counter by adding or subtracting a pulse at the 512 Hz divider stage. This approach provides periodic compensation of approximately –63 ppm to +126 ppm (see *Digital calibration (periodic counter correction) on page 22*).

This range of load values translates to an approximate frequency range adjustment of –15 to +95 ppm (see *Analog calibration (programmable load capacitance) on page 25*).

Figure 10. Internal load capacitance adjustment



3.4 Clock calibration

The M41T93 oscillator is designed for use with a 12.5 pF crystal load capacitance. When the calibration circuit is properly employed, accuracy improves to better than ±1 ppm at 25 °C.

The M41T93 design provides the following two methods for clock error correction.

3.4.1 Digital calibration (periodic counter correction)

This method employs the use of periodic counter correction by adjusting the ratio of the 100 Hz divider stage to the 512 Hz divider stage. Under normal operation, the 100Hz divider stage outputs precisely 100 pulses for every 512 pulses of the 512 Hz input stage to provide the input frequency to the fraction of seconds clock register. By adjusting the number of 512 Hz input pulses used to generate 100 output pulses, the clock can be sped up or slowed down, as shown in *Figure 13 on page 29*.

When a non-zero value is loaded into the five calibration bits (DC4 – DC0) found in the digital calibration register (08h) and the sign bit is 1, (indicating positive calibration), the 100 Hz stage outputs 100 pulses for every 511 input pulses instead of the normal 512. Since the 100 pulses are now being output in a shorter window, this has the effect of speeding up the clock by 1/512 seconds for each second the circuit is active. Similarly, when the sign bit is 0, indicating negative calibration, the block outputs 100 pulses for every 513 input pulses. Since the 100 pulses are then being output in a longer window, this has the effect of slowing down the clock by 1/512 seconds for each second the circuit is active.

The amount of calibration is controlled by using the value in the calibration register (N) to generate the adjustment in one second increments. This is done for the first N seconds once every *eight* minutes for positive calibration, and for N seconds once every *sixteen* minutes for negative calibration (see *Table 4 on page 24*).

For example, if the calibration register is set to '100010,' then the adjustment will occur for two seconds in every minute. Similarly, if the calibration register is set to '000011,' then the adjustment will occur for 3 seconds in every alternating minute.

The digital calibration bits (DC4 – DC0) occupy the five lower order bits in the digital calibration register (08h). These bits can be set to represent any value between 0 and 31 in binary form. The sixth bit (DCS) is a sign bit; '1' indicates positive calibration, '0' indicates negative calibration. Calibration occurs within an 8-minute (positive) or 16-minute (negative) cycle. Therefore, each calibration step has an effect on clock accuracy of +4.068 or –2.034 ppm. Assuming that the oscillator is running at exactly 32,768 Hz, each of the 31 increments in the calibration byte would represent +10.7 or –5.35 seconds per month, which corresponds to a total range of +5.5 or –2.75 minutes per month.

One method of determining the amount of digital calibration required is to use the frequency test output (FT) of the device (see *Section 3.14: IRQ/FT/OUT pin, frequency test, interrupts and the OUT bit on page 38* for more information on enabling the FT output).

When FT is enabled, a 512 Hz signal is output on the $\overline{\text{IRQ}}$/FT/OUT pin. This signal can be measured using a highly accurate timing device such as a frequency counter. The measured value is then compared to 512 Hz and the oscillator error in ppm is then determined.

The user should keep in mind that changes in the digital calibration value will not affect the signal measured on the FT pin. While the analog calibration circuit does affect the oscillator,

the digital calibration circuitry uses periodic counter correction which occurs downstream of the 512 Hz divider chain and hence has no effect on the FT pin.

Note: 1 The modified pulses are not observable on the frequency test (FT) output, nor will the effect of the calibration be measurable real-time, due to the periodic nature of the error compensation.

2 Positive digital calibration is performed on an eight minute cycle, therefore the value in the calibration register should not be modified more frequently than once every eight minutes for positive values of calibration. Negative digital calibration is performed on a sixteen minute cycle, therefore negative values in the calibration register should not be modified more frequently than once every sixteen minutes.

Table 4. Digital calibration values

Calibration value (binary)	Calibration value rounded to the nearest ppm	
DC4 – DC0	Negative calibration (DCS = 0) to slow a fast clock	Positive calibration (DCS = 1) to speed up a slow clock
0 (00000)	0	0
1 (00001)	–2	4
2 (00010)	–4	8
3 (00011)	–6	12
4 (00100)	–8	16
5 (00101)	–10	20
6 (00110)	–12	24
7 (00111)	–14	28
8 (01000)	–16	33
9 (01001)	–18	37
10 (01010)	–20	41
11 (01011)	–22	45
12 (01100)	–24	49
13 (01101)	–26	53
14 (01110)	–28	57
15 (01111)	–31	61
16 (10000)	–33	65
17 (10001)	–35	69
18 (10010)	–37	73
19 (10011)	–39	77
20 (10100)	–41	81
21 (10101)	–43	85
22 (10110)	–45	90
23 (10111)	–47	94
24 (11000)	–49	98
25 (11001)	–51	102
26 (11010)	–53	106
27 (11011)	–55	110
28 (11100)	–57	114
29 (11101)	–59	118
30 (11110)	–61	122
31 (11111)	–63	126
N	N/491520 (per minute)	N/245760 (per minute)

3.4.2 Analog calibration (programmable load capacitance)

A second method of calibration employs the use of programmable internal load capacitors to adjust (or trim) the oscillator frequency. As discussed in *Section 3.4.1*, the 512 Hz frequency test output can be used to determine the amount of frequency error in the oscillator. Changes in the analog calibration value will affect the frequency test output, thus the user can immediately see the effects of these changes (see *Section 3.14 on page 38* for more information on enabling the FT output).

By design, the oscillator is intended to be 0 ppm (± crystal accuracy) at room temperature (25 °C, see *Figure 11 on page 26*) when a 12.5 pF crystal is connected. Referring to *Figure 12 on page 28*, the device has two load capacitors, C_{XI} and C_{XO}, connected from the XI and XO pins to ground. These are nominally 25 pF each. The effective load capacitance is the series equivalent of these two:

$$C_{LOAD} = \frac{C_{XI} \bullet C_{XO}}{C_{XI} + C_{XO}}$$

For the nominal case of $C_{XI} = C_{XO} = 25$ pF,

$$C_{LOAD} = \frac{25 \bullet 25}{25 + 25} = 12.5\text{pF}$$

Thus, the nominal effective load capacitance matches the crystal specification of 12.5 pF.

The analog calibration register can be digitally adjusted, up or down, in increments of 0.25 pF, to change the capacitance of C_{XI} and C_{XO}. The default value is 25 pF. The maximum is 34.75 pF, to slow the clock, and the minimum is 7 pF, to speed up the clock.

The analog calibration value is in sign-magnitude format with the most significant bit the sign bit. The table below shows the approximate weighting for each of the bits.

b7	b6	b5	b4	b3	b2	b1	b0	
sign	16	8	4	2	1	0.5	0.25	pF

While the 7 bits plus sign suggest a total adjustment range of ±31.75 pF, the logic inside the device limits this to the range +9.75 pF / –18 pF. The table below summarizes the nominal, upper and lower limits of the load capacitance and the expected effect on the operating frequency of the oscillator.

C_{LOAD} (pF)	C_{XI}, C_{XO} (pF)	ACAL (Addr 0x12)	Oscillator frequency
12.5	25 (default)	0x00	0 ppm
17.4	34.75 (+9.75)	0x27	–15 ppm (slow)
3.5	7 (–18)	0xC8	+95 ppm (fast)

The asymmetrical nature of the adjustment range (+9.75 pF / –18 pF) is due to the nature of the frequency versus temperature curve (*Figure 11*) of 32.768 kHz watch crystals. The oscillator will slow down at temperatures both above and below room level (~25 °C). Hence, it usually needs to be sped up, so more adjustment range is provided to remove capacitance than to increase it.