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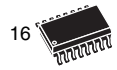
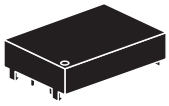
M41T94

Serial real-time clock with 44 bytes NVRAM and reset

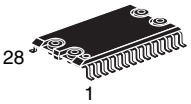
Datasheet - production data



SO16 (MQ)



SNAPHAT® (SH)
battery & crystal



SOH28 (MH)

Features

- Counters for tenths/hundredths of seconds, seconds, minutes, hours, day, date, month, year, and century
- 32 KHz crystal oscillator integrating load capacitance (12.5 pF) providing exceptional oscillator stability and high crystal series resistance operation
- Serial peripheral interface (2 MHz SPI)
- Ultralow battery supply current of 500 nA (max)
- 2.7 to 5.5 V operating voltage
- 2.5 to 5.5 V oscillator operating voltage
- Battery low flag
- Automatic switchover and deselect circuitry
- 44 bytes of general purpose RAM
- Programmable alarm and interrupt function (valid even during battery backup mode)
- Accurate programmable watchdog timer (from 62.5 ms to 128 s)
- Microprocessor power-on reset
- Choice of power-fail deselect voltages (V_{CC} = 2.7 to 5.5 V):
  - THS = V_{SS}; 2.55 V ≤ V_{PFD} ≤ 2.70 V
  - THS = V_{CC}; 4.20 V ≤ V_{PFD} ≤ 4.50 V
- Packaging includes a 28-lead SOIC and SNAPHAT® top (to be ordered separately) or 16-lead SOIC
- 28-lead SOIC package provides direct connection for a SNAPHAT® top which contains the battery and crystal
- RoHS compliant
  - Lead-free second level interconnect

Contents

List of tables

List of figures

1 Description

The M41T94 is a serial real-time clock with 44 bytes of NVRAM and a RESET output. A built-in 32,768 Hz oscillator (external crystal controlled) and 8 bytes of the SRAM (see *Table 4 on page 18*) are used for the clock/calendar function and are configured in binary coded decimal (BCD) format.

An additional 12 bytes of RAM provide status/control of alarm, watchdog and square wave functions. Addresses and data are transferred serially via a serial SPI interface. The built-in address register is incremented automatically after each WRITE or READ data byte. The M41T94 has a built-in power sense circuit which detects power failures and automatically switches to the battery supply when a power failure occurs. The energy needed to sustain the SRAM and clock operations can be supplied by a small lithium button-cell supply when a power failure occurs. Functions available to the user include a non-volatile, time-of-day clock/calendar, alarm interrupts, watchdog timer and programmable square wave output. Other features include a power-on reset as well as two additional debounced inputs ($\overline{\text{RSTIN1}}$ and $\overline{\text{RSTIN2}}$) which can also generate an output reset ($\overline{\text{RST}}$). The eight clock address locations contain the century, year, month, date, day, hour, minute, second and tenths/hundredths of a second in 24-hour BCD format. Corrections for 28, 29 (leap year - valid until year 2100), 30 and 31 day months are made automatically. The ninth clock address location controls user access to the clock information and also stores the clock software calibration setting.

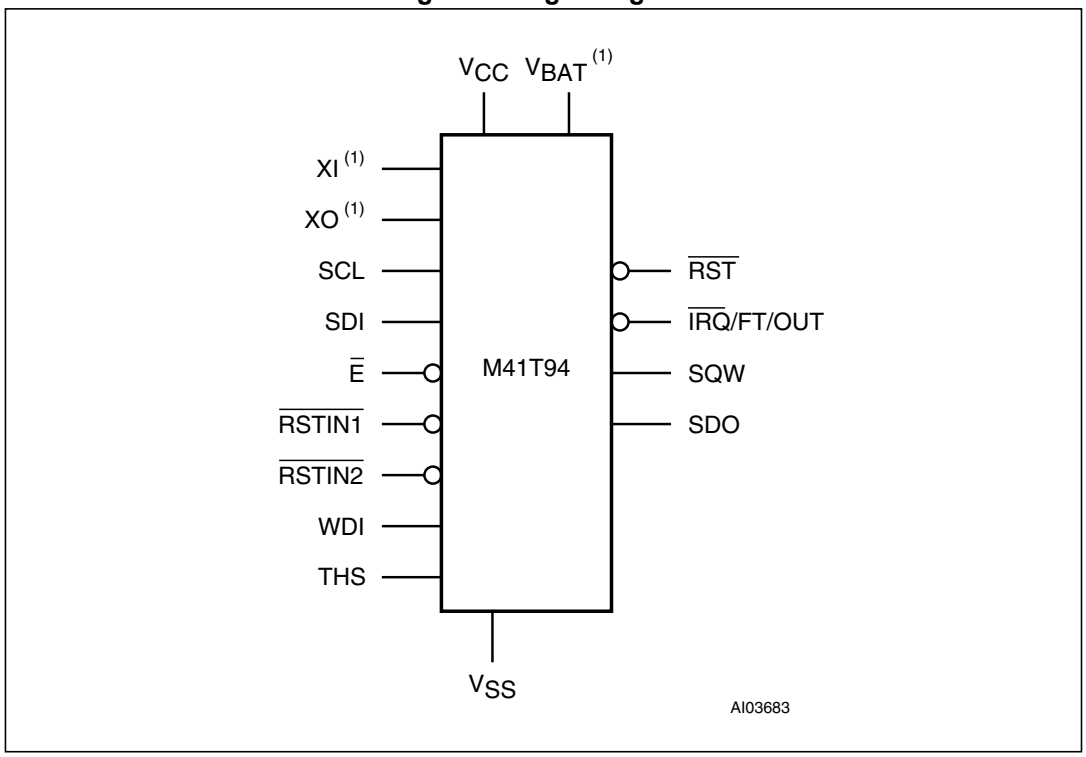
The M41T94 is supplied in either a 16-lead plastic SOIC (requiring user supplied crystal and battery) or a 28-lead SOIC SNAPHAT® package (which integrates both crystal and battery in a single SNAPHAT top). The 28-pin, 330 mil SOIC provides sockets with gold plated contacts at both ends for direct connection to a separate SNAPHAT housing containing the battery and crystal. The unique design allows the SNAPHAT battery/crystal package to be mounted on top of the SOIC package after the completion of the surface mount process.

Insertion of the SNAPHAT housing after reflow prevents potential battery and crystal damage due to the high temperatures required for device surface-mounting. The SNAPHAT housing is also keyed to prevent reverse insertion.

The SOIC and battery/crystal packages are shipped separately in plastic anti-static tubes or in tape & reel form. For the 28-lead SOIC, the battery/crystal package (e.g., SNAPHAT) part number is “M4TXX-BR12SH” (see *Table 21 on page 36*).

Caution: Do not place the SNAPHAT battery/crystal top in conductive foam, as this will drain the lithium button-cell battery.

Figure 1. Logic diagram



1. For SO16 package only.

Figure 2. 16-pin SOIC connections

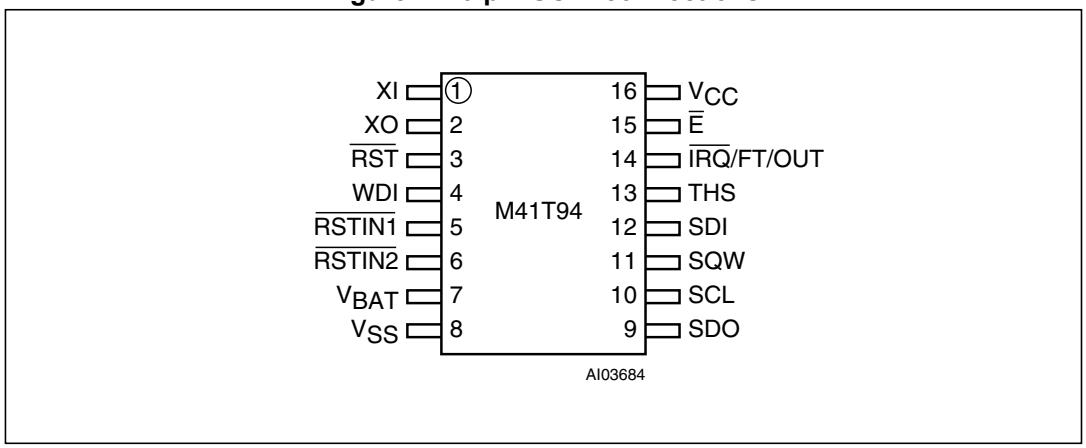


Table 1. Signal names

$\overline{E}$	Chip enable
$\overline{IRQ}$/FT/OUT	Interrupt/frequency test/out output (open drain)
$\overline{RST}$	Reset output (open drain)
$\overline{RSTIN1}$	Reset 1 input
$\overline{RSTIN2}$	Reset 2 input
SCL	Serial clock input
SDI	Serial data input
SDO	Serial data output
SQW	Square wave output
THS	Threshold select pin
WDI	Watchdog input
XI (1)	Oscillator input
XO (1)	Oscillator output
V_{BAT} (1)	Battery supply voltage
V_{CC}	Supply voltage
V_{SS}	Ground

1. For SO16 package only.

Figure 3. 28-pin SOIC connections

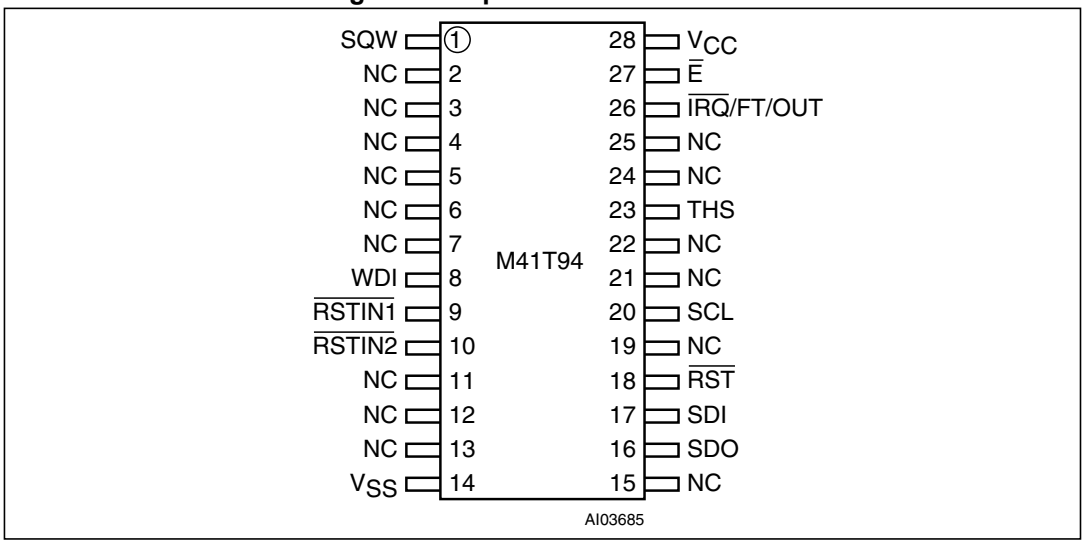
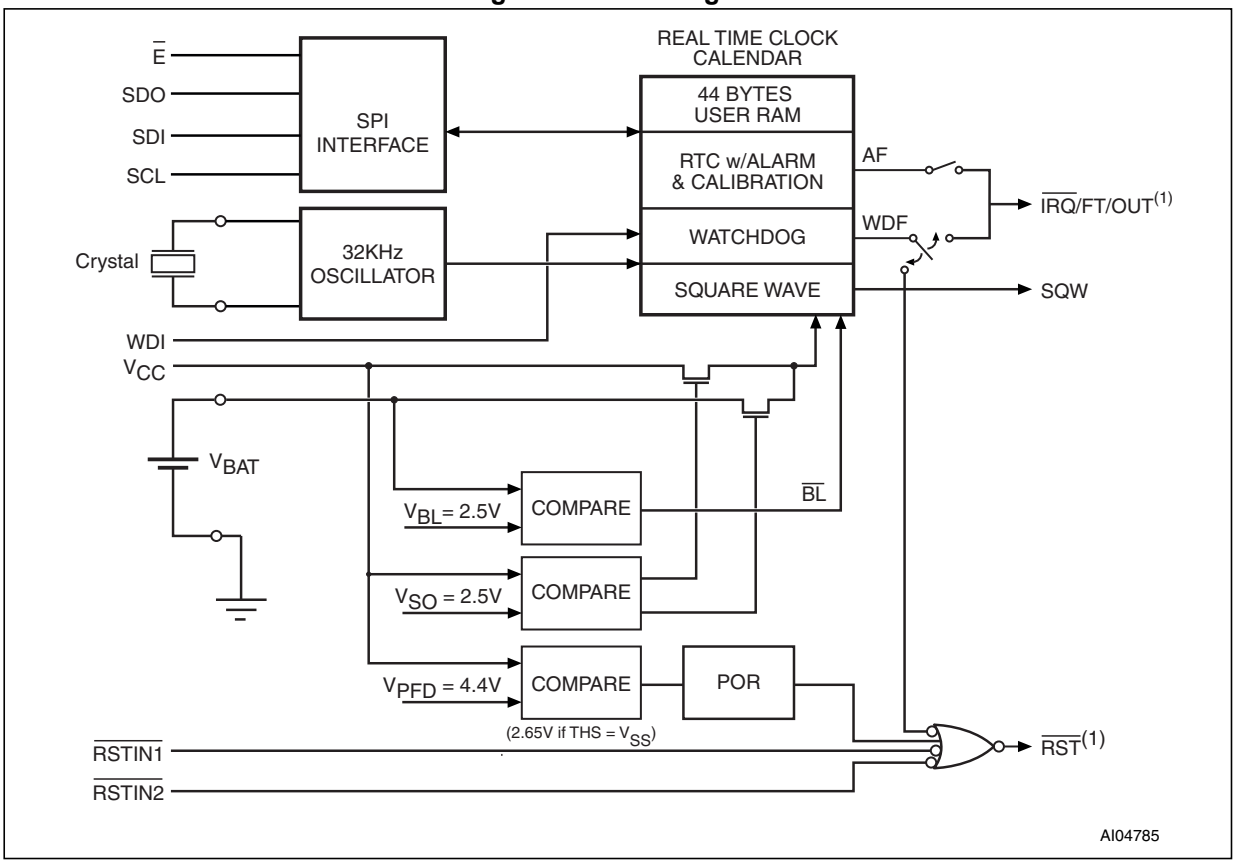
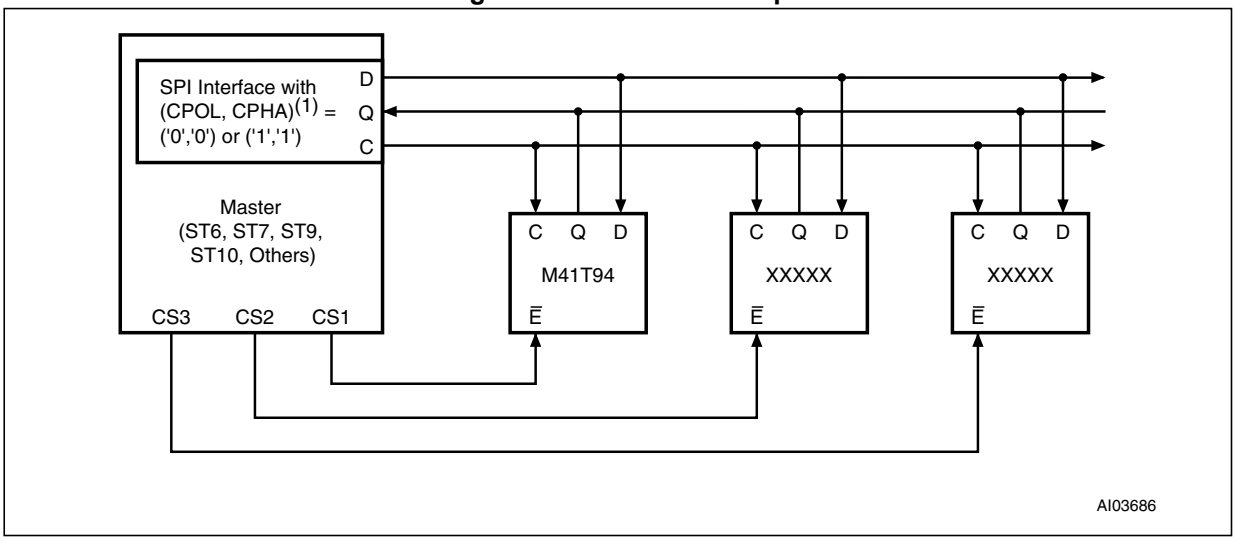


Figure 4. Block diagram



1. Open drain output

Figure 5. Hardware hookup



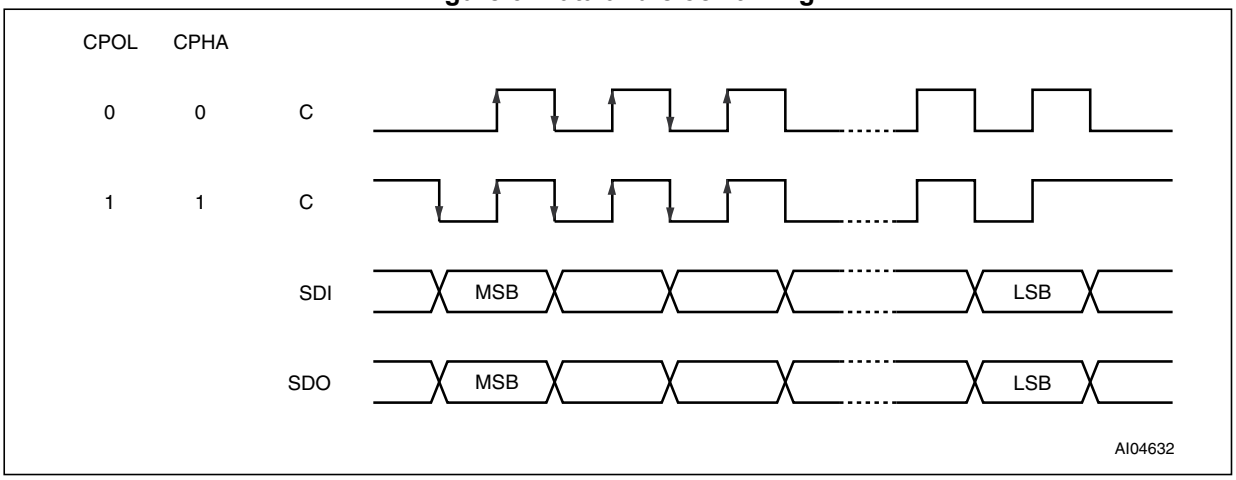
1. CPOL (clock polarity) and CPHA (clock phase) are bits that may be set in the SPI control register of the MCU.

Table 2. Function table

Mode	$\overline{E}$	SCL	SDI	SDO
Disable reset	H	Input disabled	Input disabled	High Z
WRITE	L		Data bit latch	High Z
READ	L		X	Next data bit shift (1)

1. SDO remains at High Z until eight bits of data are ready to be shifted out during a READ.

Figure 6. Data and clock timing



2 Signal description

2.1 Serial data output (SDO)

The output pin is used to transfer data serially out of the memory. Data is shifted out on the falling edge of the serial clock.

2.2 Serial data input (SDI)

The input pin is used to transfer data serially into the device. Instructions, addresses, and the data to be written, are each received this way. Input is latched on the rising edge of the serial clock.

2.3 Serial clock (SCL)

The serial clock provides the timing for the serial interface (as shown in *Figure 7 on page 13* and *Figure 8 on page 14*). The W/R bit, addresses, or data are latched, from the input pin, on the rising edge of the clock input. The output data on the SDO pin changes state after the falling edge of the clock input.

The M41T94 can be driven by a microcontroller with its SPI peripheral running in either of the two following modes:

- (CPOL, CPHA) = ('0', '0') or
- (CPOL, CPHA) = ('1', '1').

For these two modes, input data (SDI) is latched in by the low-to-high transition of clock SCL, and output data (SDO) is shifted out on the high-to-low transition of SCL (see *Table 2 on page 10* and *Figure 6 on page 10*).

2.4 Chip enable ($\overline{E}$)

When $\overline{E}$ is high, the memory device is deselected, and the SDO output pin is held in its high impedance state. After power-on, a high-to-low transition on $\overline{E}$ is required prior to the start of any operation.

3 Operation

The M41T94 clock operates as a slave device on the SPI serial bus. Each memory device is accessed by a simple serial interface that is SPI bus compatible. The bus signals are SCL, SDI and SDO (see *Table 1 on page 8* and *Figure 5 on page 9*). The device is selected when the chip enable input ($\overline{E}$) is held low. All instructions, addresses and data are shifted serially in and out of the chip. The most significant bit is presented first, with the data input (SDI) sampled on the first rising edge of the clock (SCL) after the chip enable ($\overline{E}$) goes low. The 64 bytes contained in the device can then be accessed sequentially in the following order:

- 1st byte: tenths/hundredths of a second register
- 2nd byte: seconds register
- 3rd byte: minutes register
- 4th byte: century/hours register
- 5th byte: day register
- 6th byte: date register
- 7th byte: month register
- 8th byte: year register
- 9th byte: control register
- 10th byte: watchdog register
- 11th - 16th bytes: Alarm registers
- 17th - 19th bytes: reserved
- 20th byte: square wave register
- 21st - 64th bytes: user RAM

The M41T94 clock continually monitors V_{CC} for an out-of tolerance condition. Should V_{CC} fall below V_{PFD}, the device terminates an access in progress and resets the device address counter. Inputs to the device will not be recognized at this time to prevent erroneous data from being written to the device from a an out-of-tolerance system. When V_{CC} falls below V_{SO}, the device automatically switches over to the battery and powers down into an ultra low current mode of operation to conserve battery life. As system power returns and V_{CC} rises above V_{SO}, the battery is disconnected, and the power supply is switched to external V_{CC}.

Write protection continues until V_{CC} reaches V_{PFD} (min) plus t_{REC} (min). For more information on battery storage life refer to application note AN1012.

3.1 SPI bus characteristics

The serial peripheral interface (SPI) bus is intended for synchronous communication between different ICs. It consists of four signal lines: serial data input (SDI), serial data output (SDO), serial clock (SCL) and a chip enable ($\overline{E}$).

By definition a device that gives out a message is called “transmitter,” the receiving device that gets the message is called “receiver.” The device that controls the message is called “master.” The devices that are controlled by the master are called “slaves.”

The $\overline{E}$ input is used to initiate and terminate a data transfer. The SCL input is used to synchronize data transfer between the master (micro) and the slave (M41T94) devices.

The SCL input, which is generated by the microcontroller, is active only during address and data transfer to any device on the SPI bus (see *Figure 5 on page 9*).

The M41T94 can be driven by a microcontroller with its SPI peripheral running in either of the two following modes:

- (CPOL, CPHA) = ('0', '0') or
- (CPOL, CPHA) = ('1', '1').

For these two modes, input data (SDI) is latched in by the low-to-high transition of clock SCL, and output data (SDO) is shifted out on the high-to-low transition of SCL (see *Table 2 on page 10* and *Figure 6 on page 10*).

There is one clock for each bit transferred. Address and data bits are transferred in groups of eight bits. Due to memory size the second most significant address bit is a Don’t Care (address bit 6).

Figure 7. Input timing requirements

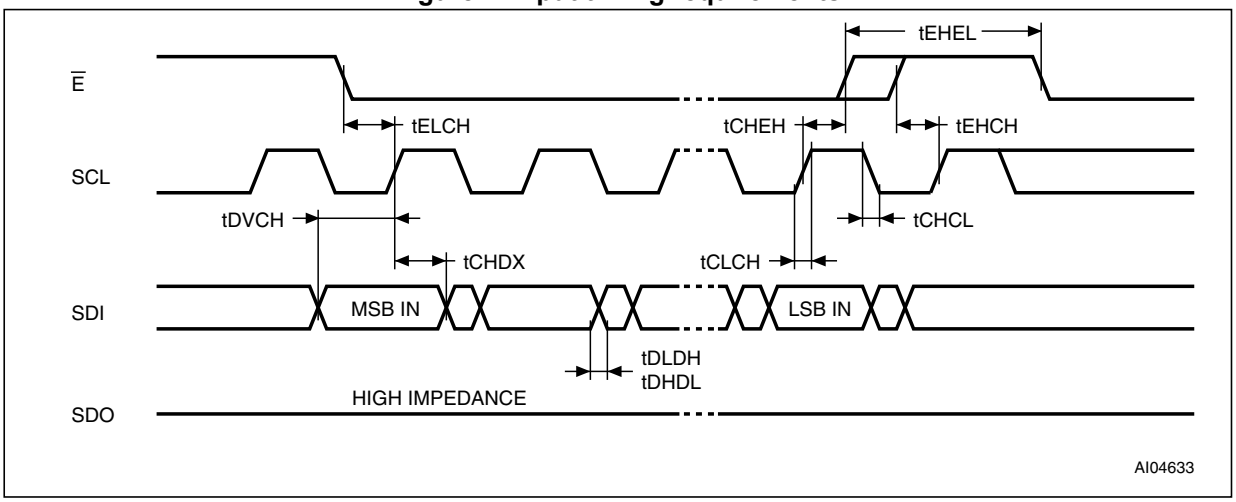


Figure 8. Output timing requirements

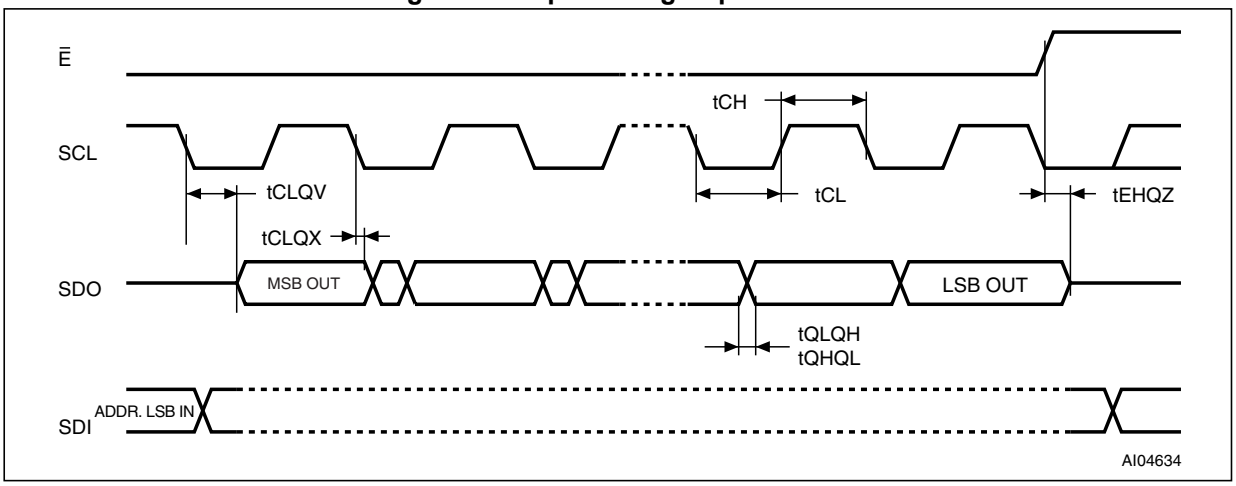


Table 3. AC characteristics

Symbol	Parameter[1]	Min	Max	Unit
f_{SCL}	Serial clock input frequency	DC	2	MHz
t_{CH}[2]	Clock high	200		ns
t_{CHCL}[3]	Clock transition (fall time)		1	µs
t_{CHDX}	Serial clock input high to input data transition	50		ns
t_{CHEH}	Serial clock input high to chip enable high	200		ns
t_{CL}[2]	Clock low	200		ns
t_{CLCH}[3]	Clock transition (rise time)		1	µs
t_{CLQV}	Serial clock input low to output valid		150	ns
t_{CLQX}	Serial clock input low to output data transition	0		ns
t_{DHDL}[3]	Input data transition (fall time)		1	µs
t_{DLDH}[3]	Input data transition (rise time)		1	µs
t_{DVCH}	Input data to serial clock input high	40		ns
t_{EHCH}	Chip enable high to serial clock input high	200		ns
t_{EHEL}	Chip enable high to chip enable low	200		ns
t_{EHQZ}[3]	Chip enable high to output high-z		250	ns
t_{ELCH}	Chip enable low to serial clock input high	200		ns
t_{QHQL}[3]	Output data transition (fall time)		100	ns
t_{QLQH}[3]	Output data transition (rise time)		100	ns

1. Valid for ambient operating temperature: T_A = –40 to 85°C; V_{CC} = 2.7 to 5.5 V (except where noted).
2. $t_{CH} + t_{CL} \geq 1/f_{SCL}$
3. Value guaranteed by design, not 100% tested in production.

3.2 Read and write cycles

Address and data are shifted MSB first into the serial data input (SDI) and out of the serial data output (SDO). Any data transfer considers the first bit to define whether a READ or WRITE will occur. This is followed by seven bits defining the address to be read or written. Data is transferred out of the SDO for a READ operation and into the SDI for a WRITE operation. The address is always the second through the eighth bit written after the Enable ($\overline{E}$) pin goes low. If the first bit is a '1,' one or more WRITE cycles will occur. If the first bit is a '0,' one or more READ cycles will occur (see Figure *Figure 9 on page 16* and *Figure 10 on page 16*).

Data transfers can occur one byte at a time or in multiple byte burst mode, during which the address pointer will be automatically incremented. For a single byte transfer, one byte is read or written and then $\overline{E}$ is driven high. For a multiple byte transfer all that is required is that $\overline{E}$ continue to remain low. Under this condition, the address pointer will continue to increment as stated previously. Incrementing will continue until the device is deselected by taking $\overline{E}$ high. The address will wrap to 00h after incrementing to 3Fh.

The system-to-user transfer of clock data will be halted whenever the address being read is a clock address (00h to 07h). Although the clock continues to maintain the correct time, this will prevent updates of time and date during either a READ or WRITE of these address locations by the user. The update will resume either due to a deselect condition or when the pointer increments to an non-clock or RAM address (08h to 3Fh).

Note: This is true both in READ and WRITE mode.

3.3 Data retention mode

With valid V_{CC} applied, the M41T94 can be accessed as described above with READ or WRITE cycles. Should the supply voltage decay, the M41T94 will automatically deselect, write protecting itself when V_{CC} falls between V_{PFD} (max) and V_{PFD} (min) (see *Figure 17 on page 30*). At this time, the reset pin ($\overline{RST}$) is driven active and will remain active until V_{CC} returns to nominal levels. When V_{CC} falls below the switchover voltage (V_{SO}), power input is switched from the V_{CC} pin to the SNAPHAT battery (or external battery for SO16) at this time, and the clock registers are maintained from the attached battery supply. All outputs become high impedance. On power-up, when V_{CC} returns to a nominal value, write protection continues for t_{REC} by internally inhibiting $\overline{E}$. The $\overline{RST}$ signal also remains active during this time (see *Figure 17 on page 30*). Before the next active cycle, chip enable should be taken high for at least t_{EHEL}, then low.

For a further more detailed review of battery lifetime calculations, please see application note AN1012.

Figure 9. Read mode sequence

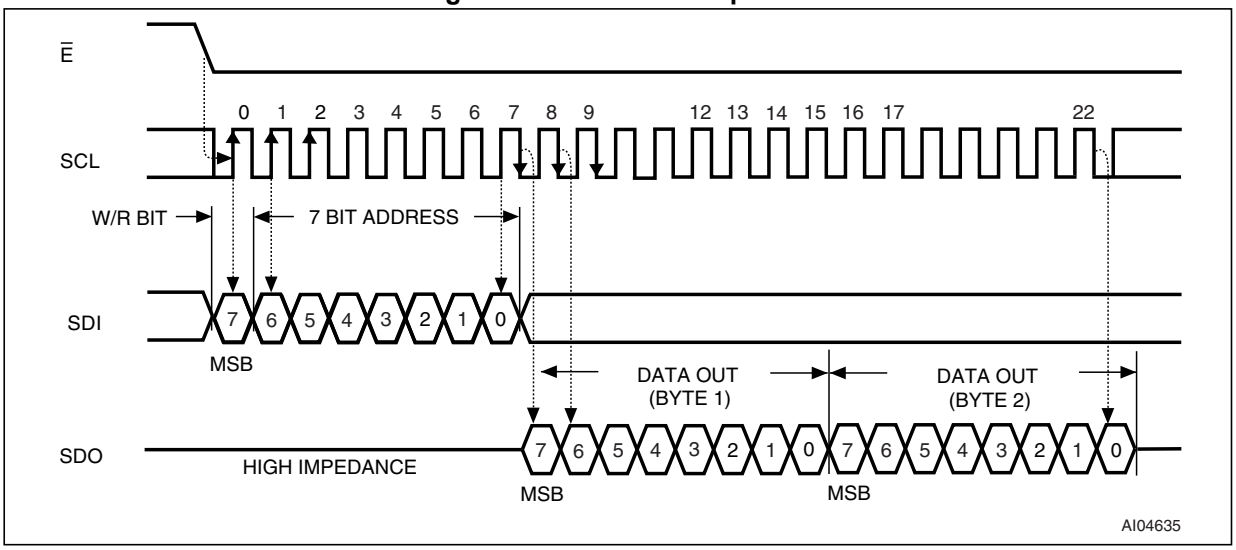
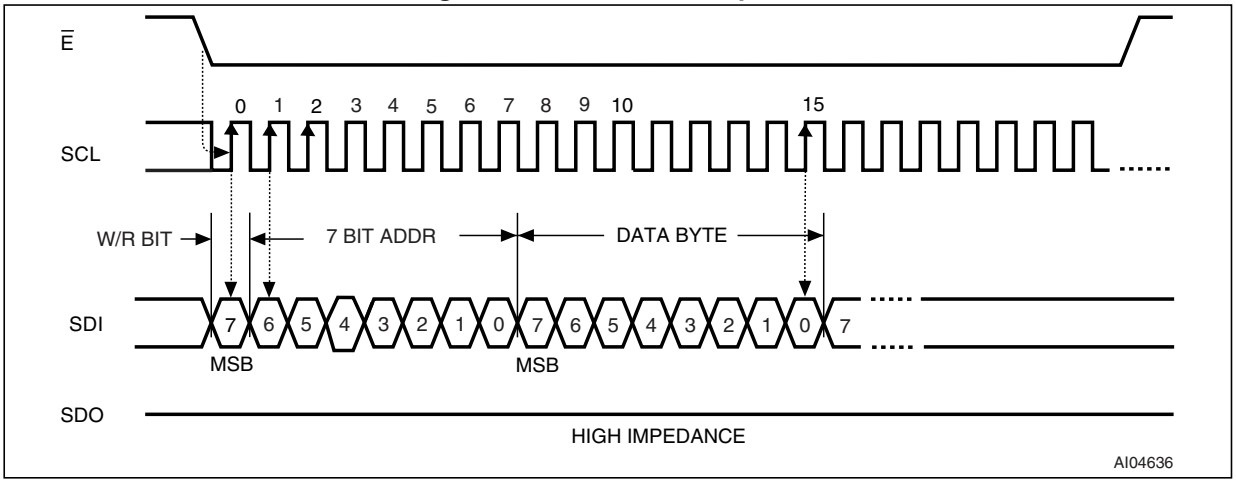


Figure 10. Write mode sequence



4 Clock operations

The eight byte clock register (see *Table 4 on page 18*) is used to both set the clock and to read the date and time from the clock, in a binary coded decimal format. Tenths/hundredths of seconds, seconds, minutes, and hours are contained within the first four registers. Bits D6 and D7 of clock register 03h (century/hours register) contain the CENTURY ENABLE bit (CEB) and the CENTURY bit (CB). Setting CEB to a '1' will cause CB to toggle, either from '0' to '1' or from '1' to '0' at the turn of the century (depending upon its initial state). If CEB is set to a '0,' CB will not toggle. Bits D0 through D2 of register 04h contain the day (day of week). Registers 05h, 06h, and 07h contain the date (day of month), month and years. The ninth clock register is the control register (this is described in the clock calibration section). Bit D7 of register 01h contains the STOP bit (ST). Setting this bit to a '1' will cause the oscillator to stop. If the device is expected to spend a significant amount of time on the shelf, the oscillator may be stopped to reduce current drain. When reset to a '0' the oscillator restarts within one second.

The eight clock registers may be read one byte at a time, or in a sequential block. The control register (address location 08h) may be accessed independently. Provision has been made to assure that a clock update does not occur while any of the eight clock addresses are being read. If a clock address is being read, an update of the clock registers will be halted. This will prevent a transition of data during the READ.

4.1 Power-down time-stamp

When a power failure occurs, the halt update bit (HT) will automatically be set to a '1.' This will prevent the clock from updating the clock registers, and will allow the user to read the exact time of the power-down event. Resetting the HT bit to a '0' will allow the clock to update the clock registers with the current time. For more information, see application note AN1572.

4.2 Clock registers

The M41T94 offers 20 internal registers which contain clock, alarm, watchdog, flag, square wave and control data (see *Table 4 on page 18*). These registers are memory locations which contain external (user accessible) and internal copies of the data (usually referred to as BiPORT™ cells). The external copies are independent of internal functions except that they are updated periodically by the simultaneous transfer of the incremented internal copy. The internal divider (or clock) chain will be reset upon the completion of a WRITE to any clock address.

The system-to-user transfer of clock data will be halted whenever the clock addresses (00h to 07h) are being written. The update will resume either due to a deselect condition or when the pointer increments to a non-clock or RAM address.

Clock and alarm registers store data in BCD. Control, watchdog and square wave registers store data in binary format.

Table 4. Clock register map(1)

Addr	D7	D6	D5	D4	D3	D2	D1	D0	Function/range BCD format	
00h	0.1 seconds				0.01 seconds				Seconds	00-99
01h	ST	10 seconds			Seconds				Seconds	00-59
02h	0	10 minutes			Minutes				Minutes	00-59
03h	CEB	CB	10 Hours		Hours (24 hour format)				Century/hours	0-1/00-23
04h	TR	0	0	0	0	Day of week			Day	01-7
05h	0	0	10 date		Date: day of month				Date	01-31
06h	0	0	0	10M	Month				Month	01-12
07h	10 Years				Year				Year	00-99
08h	OUT	FT	S	Calibration					Control	
09h	WDS	BMB4	BMB3	BMB2	BMB1	BMB0	RB1	RB0	Watchdog	
0Ah	AFE	SQWE	ABE	AI 10M	Alarm month				AI month	01-12
0Bh	RPT4	RPT5	AI 10 date		Alarm date				AI date	01-31
0Ch	RPT3	HT	AI 10 hour		Alarm hour				AI hour	00-23
0Dh	RPT2	Alarm 10 minutes			Alarm minutes				AI min	00-59
0Eh	RPT1	Alarm 10 seconds			Alarm seconds				AI sec	00-59
0Fh	WDF	AF	0	BL	0	0	0	0	Flags	
10h	0	0	0	0	0	0	0	0	Reserved	
11h	0	0	0	0	0	0	0	0	Reserved	
12h	0	0	0	0	0	0	0	0	Reserved	
13h	RS3	RS2	RS1	RS0	0	0	0	0	SQW	

1. Keys:
S = Sign bit
FT = Frequency test bit
ST = Stop bit
0 = Must be set to zero
BL = Battery low flag (read only)
BMB0-BMB4 = Watchdog multiplier bits
CEB = Century enable bit
CB = Century bit
OUT = Output level
AFE = Alarm flag enable flag
RB0-RB1 = Watchdog resolution bits
WDS = Watchdog steering bit
ABE = Alarm in battery back-up mode enable bit
RPT1-RPT5 = Alarm repeat mode bits
WDF = Watchdog flag (read only)
WDF = Watchdog flag (read only)
AF = Alarm flag (read only)
SQWE = Square wave enable
RS0-RS3 = SQW frequency
HT = Halt update bit
TR = t_{REC} bit

4.3 Setting alarm clock registers

Address locations 0Ah-0Eh contain the alarm settings. The alarm can be configured to go off at a prescribed time on a specific month, date, hour, minute, or second, or repeat every year, month, day, hour, minute, or second. It can also be programmed to go off while the M41T94 is in the battery backup to serve as a system wake-up call.

Bits RPT5-RPT1 put the alarm in the repeat mode of operation. *Table 5 on page 19* shows the possible configurations. Codes not listed in the table default to the once per second mode to quickly alert the user of an incorrect alarm setting.

When the clock information matches the alarm clock settings based on the match criteria defined by RPT5-RPT1, the AF (alarm flag) is set. If AFE (alarm flag enable) is also set, the alarm condition activates the $\overline{IRQ}$/FT/OUT pin.

Note: ***If** the address pointer is allowed to increment to the flag register address, an alarm condition will not cause the interrupt/flag to occur until the address pointer is moved to a different address. It should also be noted that if the last address written is the "Alarm Seconds," the address pointer will increment to the flag address, causing this situation to occur.*

To disable the alarm, write '0' to the alarm date register and to RPT1–5. The $\overline{IRQ}$/FT/OUT output is cleared by a READ to the flags register. This READ of the flags register will also reset the alarm flag (D6; register 0Fh). See *Figure 11 on page 19*.

The $\overline{IRQ}$/FT/OUT pin can also be activated in the battery backup mode. The $\overline{IRQ}$/FT/OUT will go low if an alarm occurs and both ABE (alarm in battery backup mode enable) and AFE are set. The ABE and AFE bits are reset during power-up, therefore an alarm generated during power-up will only set AF. The user can read the flag register at system boot-up to determine if an alarm was generated while the M41T94 was in the deselect mode during power-up. *Figure 12 on page 20* illustrates the backup mode alarm timing.

Table 5. Alarm repeat mode

RPT5	RPT4	RPT3	RPT2	RPT1	Alarm setting
1	1	1	1	1	Once per second
1	1	1	1	0	Once per minute
1	1	1	0	0	Once per hour
1	1	0	0	0	Once per day
1	0	0	0	0	Once per month
0	0	0	0	0	Once per year

Figure 11. Alarm interrupt reset waveforms

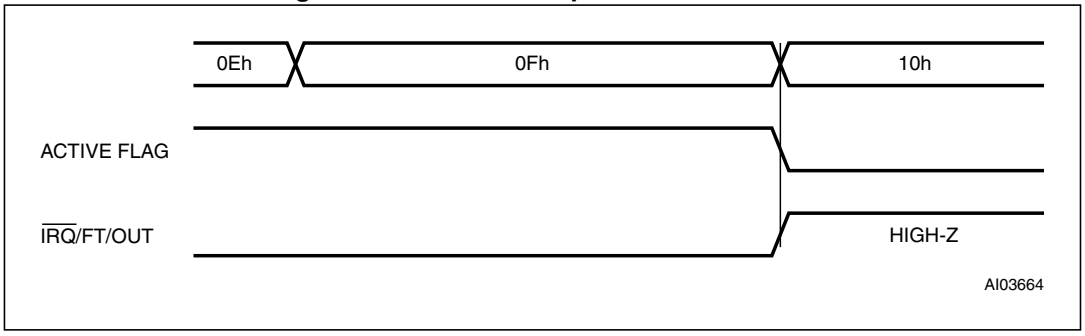
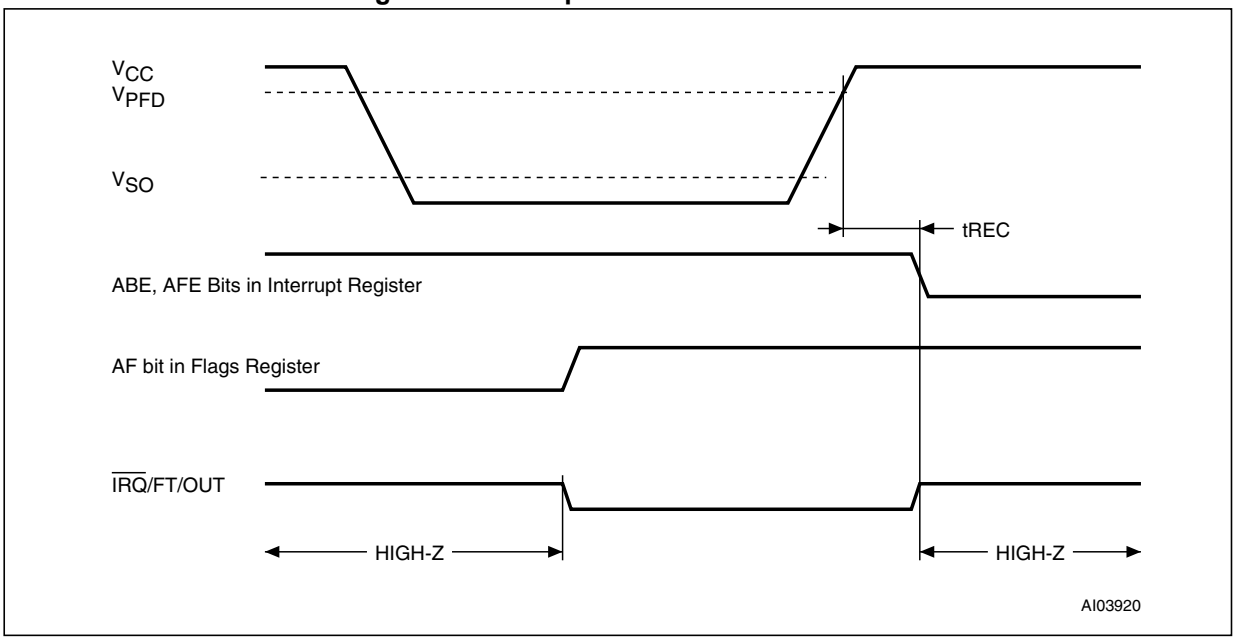


Figure 12. Backup mode alarm waveforms



4.4 Watchdog timer

The watchdog timer can be used to detect an out-of-control microprocessor. The user programs the watchdog timer by setting the desired amount of time-out into the Watchdog register, address 09h. bits BMB4-BMB0 store a binary multiplier and the two lower order bits RB1-RB0 select the resolution, where 00 = $^1/_{16}$ second, 01 = $^1/_4$ second, 10 = 1 second, and 11 = 4 seconds. The amount of time-out is then determined to be the multiplication of the five-bit multiplier value with the resolution. (For example: writing 00001110 in the Watchdog register = 3*1 or 3 seconds).

Note: Accuracy of timer is within ± the selected resolution.

If the processor does not reset the timer within the specified period, the M41T94 sets the WDF (watchdog flag) and generates a watchdog interrupt or a microprocessor reset. WDF is reset by reading the flags register (0Fh).

The most significant bit of the watchdog register is the watchdog steering bit (WDS). When set to a '0,' the watchdog will activate the $\overline{\text{IRQ}}$/FT/OUT pin when timed-out. When WDS is set to a '1,' the watchdog will output a negative pulse on the RST pin for t_{REC}. The watchdog register and the AFE, ABE, SQWE, and FT bits will reset to a '0' at the end of a watchdog time-out when the WDS bit is set to a '1.'

The watchdog timer can be reset by two methods:

1. a transition (high-to-low or low-to-high) can be applied to the watchdog input pin (WDI), or
2. the microprocessor can perform a WRITE of the watchdog register.

The time-out period then starts over. The WDI pin should be tied to V_{SS} if not used. In order to perform a software reset of the watchdog timer, the original time-out period can be written into the watchdog register, effectively restarting the count-down cycle.

Should the watchdog timer time-out, and the WDS bit is programmed to output an interrupt, a value of 00h needs to be written to the watchdog register in order to clear the $\overline{\text{IRQ}}$/FT/OUT pin. This will also disable the watchdog function until it is again programmed correctly. A READ of the flags register will reset the watchdog flag (bit D7; register 0Fh).

The watchdog function is automatically disabled upon power-up and the watchdog register is cleared. If the watchdog function is set to output to the $\overline{\text{IRQ}}$/FT/OUT pin and the frequency test (FT) function is activated, the watchdog function prevails and the frequency test function is denied.

4.5 Square wave output

The M41T94 offers the user a programmable square wave function which is output on the SQW pin. RS3-RS0 bits located in 13h establish the square wave output frequency. These frequencies are listed in Table *Table 6 on page 22*. Once the selection of the SQW frequency has been completed, the SQW pin can be turned on and off under software control with the square wave enable bit (SQWE) located in register 0Ah.

Table 6. Square wave output frequency

Square wave bits				Square wave	
RS3	RS2	RS1	RS0	Frequency	Units
0	0	0	0	None	–
0	0	0	1	32.768	kHz
0	0	1	0	8.192	kHz
0	0	1	1	4.096	kHz
0	1	0	0	2.048	kHz
0	1	0	1	1.024	kHz
0	1	1	0	512	Hz
0	1	1	1	256	Hz
1	0	0	0	128	Hz
1	0	0	1	64	Hz
1	0	1	0	32	Hz
1	0	1	1	16	Hz
1	1	0	0	8	Hz
1	1	0	1	4	Hz
1	1	1	0	2	Hz
1	1	1	1	1	Hz

4.6 Power-on reset

The M41T94 continuously monitors V_{CC}. When V_{CC} falls to the power fail detect trip point, the $\overline{RST}$ pulls low (open drain) and remains low on power-up for t_{REC} after V_{CC} passes V_{PFD} (max). The $\overline{RST}$ pin is an open drain output and an appropriate pull-up resistor should be chosen to control rise time.

4.7 Reset inputs ($\overline{RSTIN1}$ & $\overline{RSTIN2}$)

The M41T94 provides two independent inputs which can generate an output reset. The duration and function of these resets is identical to a reset generated by a power cycle. *Table 7 on page 23* and *Figure 13 on page 23* illustrate the AC reset characteristics of this function. Pulses shorter than t_{RLRH1} and t_{RLRH2} will not generate a reset condition. $\overline{RSTIN1}$ and $\overline{RSTIN2}$ are each internally pulled up to V_{CC} through a 100 kΩ resistor.

Figure 13. $\overline{\text{RSTIN1}}$ and $\overline{\text{RSTIN2}}$ timing waveforms

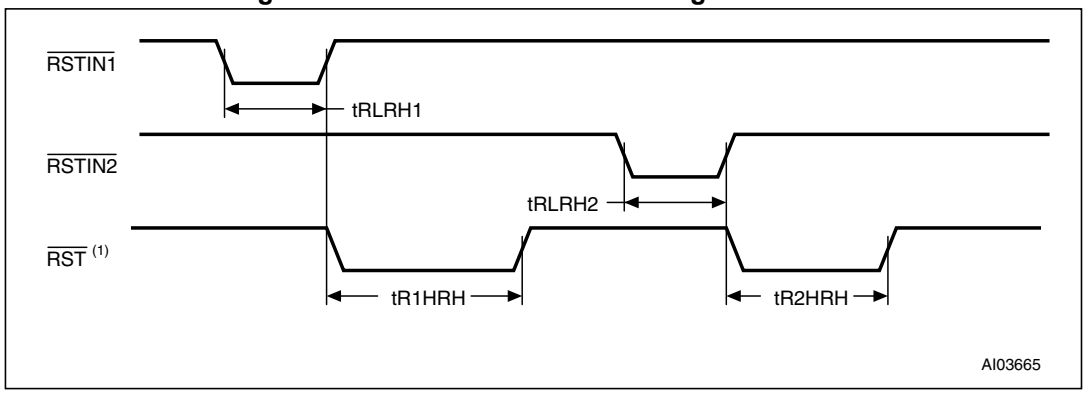


Table 7. Reset AC characteristics(1)

Symbol	Parameter	Min	Max	Unit
t_{RLRH1}(2)	$\overline{\text{RSTIN1}}$ low to $\overline{\text{RSTIN1}}$ high	200		ns
t_{RLRH2}(3)	$\overline{\text{RSTIN2}}$ low to $\overline{\text{RSTIN2}}$ high	100		ms
t_{R1HRH}(4)	$\overline{\text{RSTIN1}}$ high to $\overline{\text{RST}}$ high	40	200	ms
t_{R2HRH}(4)	$\overline{\text{RSTIN2}}$ high to $\overline{\text{RST}}$ high	40	200	ms

1. Valid for ambient operating temperature: T_A = –40 to 85°C; V_{CC} = 2.7 to 5.5 V (except where noted).
2. Pulse width less than 50 ns will result in no RESET (for noise immunity).
3. Pulse width less than 20 ms will result in no RESET (for noise immunity).
4. Programmable (see *Table on page 26*).

4.8 Calibrating the clock

The M41T94 is driven by a quartz-controlled oscillator with a nominal frequency of 32,768 Hz. Uncalibrated clock accuracy will not exceed ±35 ppm (parts per million) oscillator frequency error at 25°C, which equates to about ±1.53 minutes per month. When the Calibration circuit is properly employed, accuracy improves to better than ±2 ppm at 25°C.

The oscillation rate of crystals changes with temperature (see *Figure 14 on page 24*). Therefore, the M41T94 design employs periodic counter correction. The calibration circuit adds or subtracts counts from the oscillator divider circuit at the divide by 256 stage, as shown in *Figure 15 on page 25*. The number of times pulses are blanked (subtracted, negative calibration) or split (added, positive calibration) depends upon the value loaded into the five calibration bits found in the control register. Adding counts speeds the clock up, subtracting counts slows the clock down.

The calibration bits occupy the five lower order bits (D4-D0) in the control register (8h). These bits can be set to represent any value between 0 and 31 in binary form. Bit D5 is a sign bit; '1' indicates positive calibration, '0' indicates negative calibration. Calibration occurs within a 64 minute cycle. The first 62 minutes in the cycle may, once per minute, have one second either shortened by 128 or lengthened by 256 oscillator cycles. If a binary '1' is loaded into the register, only the first 2 minutes in the 64 minute cycle will be modified; if a binary 6 is loaded, the first 12 will be affected, and so on.

Therefore, each calibration step has the effect of adding 512 or subtracting 256 oscillator cycles for every 125,829,120 actual oscillator cycles, that is +4.068 or –2.034 ppm of

adjustment per calibration step in the calibration register. Assuming that the oscillator is running at exactly 32,768 Hz, each of the 31 increments in the calibration byte would represent +10.7 or –5.35 seconds per month which corresponds to a total range of +5.5 or –2.75 minutes per month.

Two methods are available for ascertaining how much calibration a given M41T94 may require.

The first involves setting the clock, letting it run for a month and comparing it to a known accurate reference and recording deviation over a fixed period of time. Calibration values, including the number of seconds lost or gained in a given period, can be found in application note AN934: TIMEKEEPER® calibration. This allows the designer to give the end user the ability to calibrate the clock as the environment requires, even if the final product is packaged in a non-user serviceable enclosure. The designer could provide a simple utility that accesses the calibration byte.

The second approach is better suited to a manufacturing environment, and involves the use of the $\overline{IRQ}$/FT/OUT pin. The pin will toggle at 512 Hz, when the stop bit (ST, D7 of 1h) is '0,' the frequency test bit (FT, D6 of 8h) is '1,' the alarm flag enable bit (AFE, D7 of Ah) is '0,' and the watchdog steering bit (WDS, D7 of 9h) is '1' or the watchdog register (9h = 0) is reset.

Any deviation from 512 Hz indicates the degree and direction of oscillator frequency shift at the test temperature. For example, a reading of 512.010124 Hz would indicate a +20 ppm oscillator frequency error, requiring a –10 (XX001010) to be loaded into the calibration byte for correction.

Note: Setting or changing the calibration byte does not affect the frequency test output frequency.

The $\overline{IRQ}$/FT/OUT pin is an open drain output which requires a pull-up resistor for proper operation. A 500 to 10 kΩ resistor is recommended in order to control the rise time. The FT bit is cleared on power-down.

Figure 14. Crystal accuracy across temperature

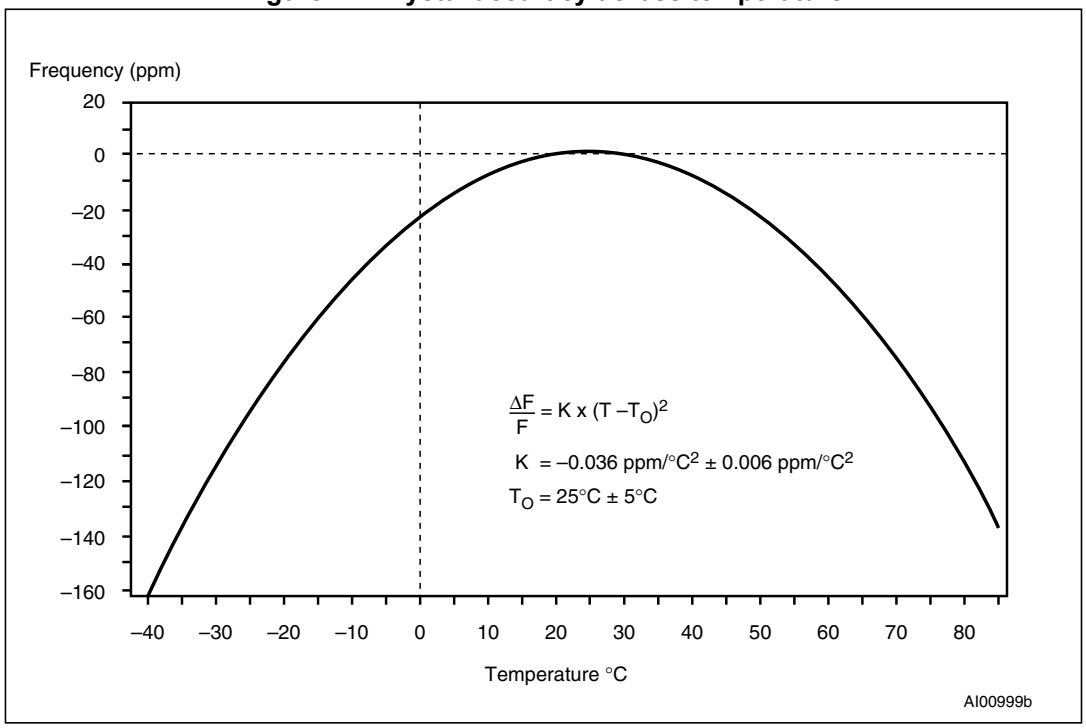
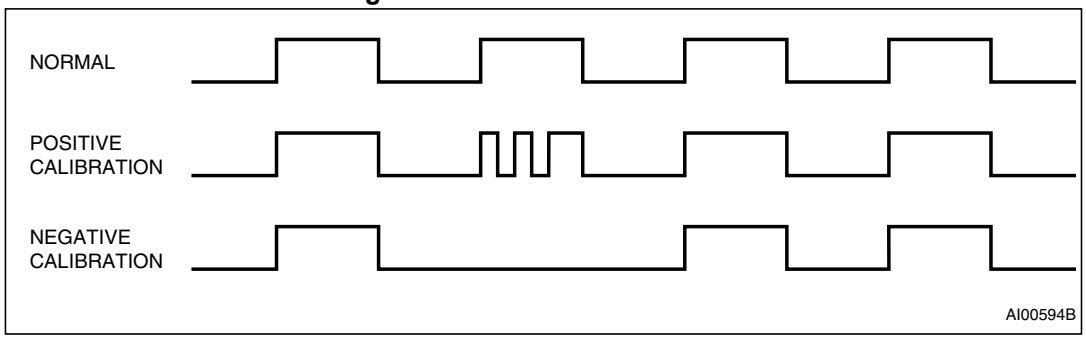


Figure 15. Calibration waveform



4.9 Century bit

Bits D7 and D6 of clock register 03h contain the CENTURY ENABLE bit (CEB) and the CENTURY bit (CB). Setting CEB to a '1' will cause CB to toggle, either from a '0' to '1' or from '1' to '0' at the turn of the century (depending upon its initial state). If CEB is set to a '0,' CB will not toggle.

4.10 Output driver pin

When the FT bit, AFE bit and watchdog register are not set, the $\overline{IRQ}$/FT/OUT pin becomes an output driver that reflects the contents of D7 of the control register. In other words, when D7 (OUT bit) and D6 (FT bit) of address location 08h are a '0,' then the $\overline{IRQ}$/FT/OUT pin will be driven low.

Note: The $\overline{IRQ}$/FT/OUT pin is an open drain which requires an external pull-up resistor.

4.11 Battery low warning

The M41T94 automatically performs battery voltage monitoring upon power-up and at factory-programmed time intervals of approximately 24 hours. The battery low (BL) bit, bit D4 of flags register 0Fh, will be asserted if the battery voltage is found to be less than approximately 2.5 V. The BL bit will remain asserted until completion of battery replacement and subsequent battery low monitoring tests, either during the next power-up sequence or the next scheduled 24-hour interval.

If a battery low is generated during a power-up sequence, this indicates that the battery is below approximately 2.5 volts and may not be able to maintain data integrity in the SRAM. Data should be considered suspect and verified as correct. A fresh battery should be installed.

If a battery low indication is generated during the 24-hour interval check, this indicates that the battery is near end of life. However, data is not compromised due to the fact that a nominal V_{CC} is supplied. In order to insure data integrity during subsequent periods of battery backup mode, the battery should be replaced. The SNAPHAT® top may be replaced while V_{CC} is applied to the device.

Note: This will cause the clock to lose time during the interval the SNAPHAT® battery/crystal top is disconnected.