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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
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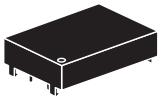
M48T201Y
M48T201V

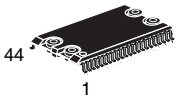
5.0 or 3.3 V TIMEKEEPER® supervisor

Features

- Converts low power SRAM into NVRAMs
- Year 2000 compliant
- Battery low flag
- Integrated real time clock, power-fail control circuit, battery and crystal
- Watchdog timer
- Choice of write protect voltages (V_{PFD} = power-fail deselect voltage):
  - M48T201Y: V_{CC} = 4.5 to 5.5 V
    $4.1V \leq V_{PFD} \leq 4.5$ V
  - M48T201V: V_{CC} = 3.0 to 3.6 V
    $2.7\ V \leq V_{PFD} \leq 3.0$ V
- Microprocessor power-on reset (valid even during battery backup mode)
- Programmable alarm output active in the battery backed-up mode
- Packaging includes a 44-lead SOIC and SNAPHAT® top (to be ordered separately)
- SOIC package provides direct connection for a SNAPHAT® top which contains the battery and crystal
- RoHS compliant
  - Lead-free second level interconnect

SNAPHAT® (SH)
crystal/battery





SOH44 (MH)
44-pin SOIC

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1 Description

The M48T201Y/V are self-contained devices that include a real time clock (RTC), programmable alarms, a watchdog timer, and a square wave output which provides control of up to 512 K x 8 of external low-power static RAM. Access to all RTC functions and the external RAM is the same as conventional bytewide SRAM. The 16 TIMEKEEPER® registers offer year, month, date, day, hour, minute, second, calibration, alarm, century, watchdog, and square wave output data. Externally attached static RAMs are controlled by the M48T201Y/V via the $\overline{G}_{CON}$ and $\overline{E}_{CON}$ signals.

The 44-pin, 330 mil SOIC provides sockets with gold plated contacts at both ends for direct connection to a separate SNAPHAT® housing containing the battery and crystal. The unique design allows the SNAPHAT battery package to be mounted on top of the SOIC package after the completion of the surface mount process.

Insertion of the SNAPHAT housing after reflow prevents potential battery damage due to the high temperatures required for device surface-mounting. The SNAPHAT housing is keyed to prevent reverse insertion. The SOIC and battery packages are shipped separately in plastic anti-static tubes or in tape & reel form. For the 44-lead SOIC, the battery/crystal package (e.g., SNAPHAT) part number is “M4Txx-BR12SH” (see *Table 19 on page 34*).

Caution: Do not place the SNAPHAT battery/crystal top in conductive foam as this will drain the lithium button-cell battery.

Figure 1. Logic diagram

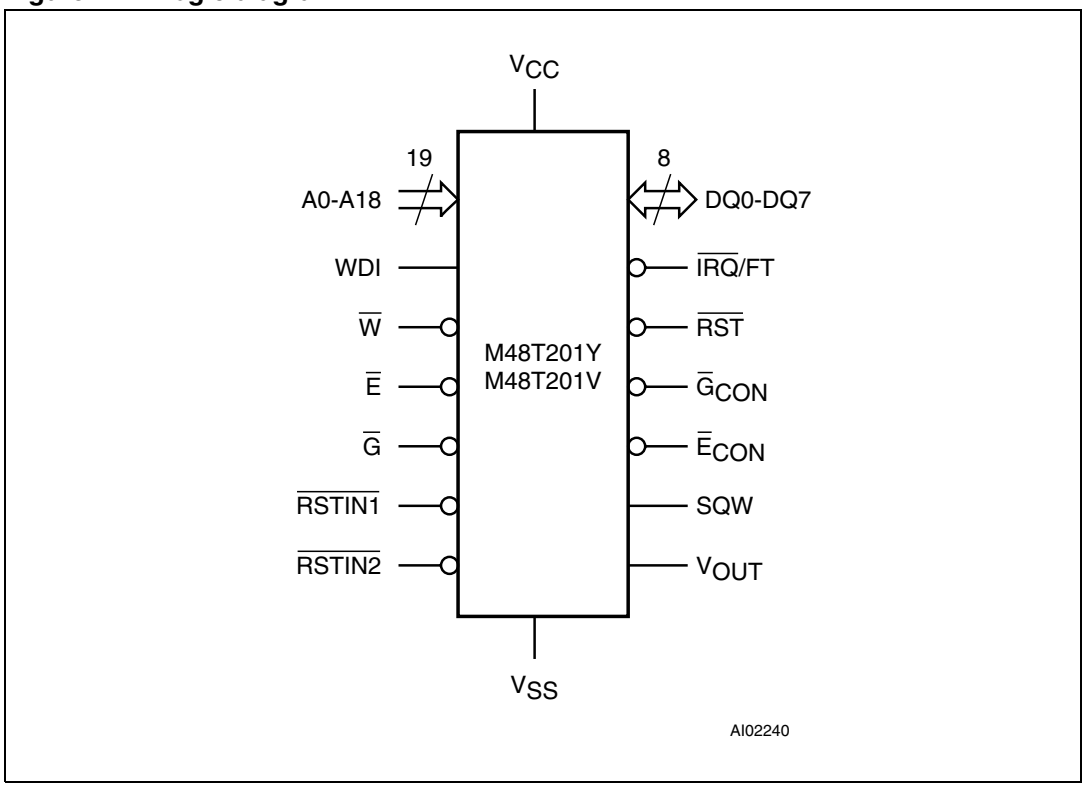


Table 1. Signal names

A0-A18	Address inputs
DQ0-DQ7	Data inputs / outputs
$\overline{RSTIN1}$	Reset 1 input
$\overline{RSTIN2}$	Reset 2 Input
$\overline{RST}$	Reset output (open drain)
WDI	Watchdog input
$\overline{E}$	Chip enable input
$\overline{G}$	Output enable Input
$\overline{W}$	WRITE enable input
$\overline{E}_{CON}$	RAM chip enable output
$\overline{G}_{CON}$	RAM enable output
$\overline{IRQ}$/FT	Interrupt / frequency test output (open drain)
SQW	Square wave output
V_{OUT}	Supply voltage output
V_{CC}	Supply voltage
V_{SS}	Ground
NC	Not connected internally

Figure 2. SOIC connections

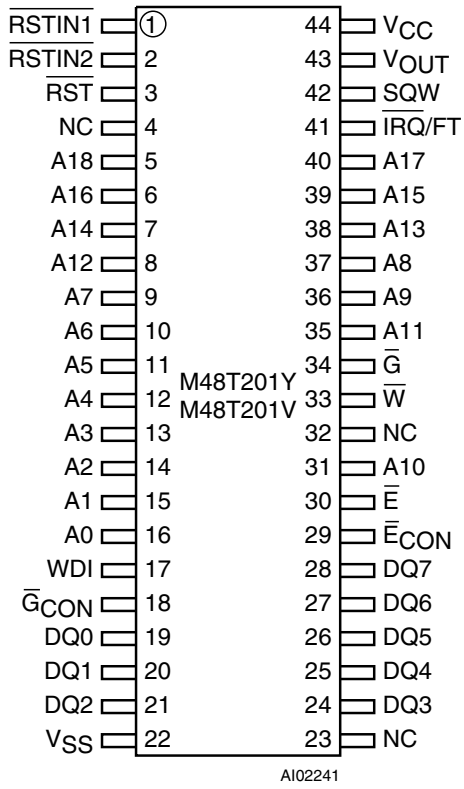
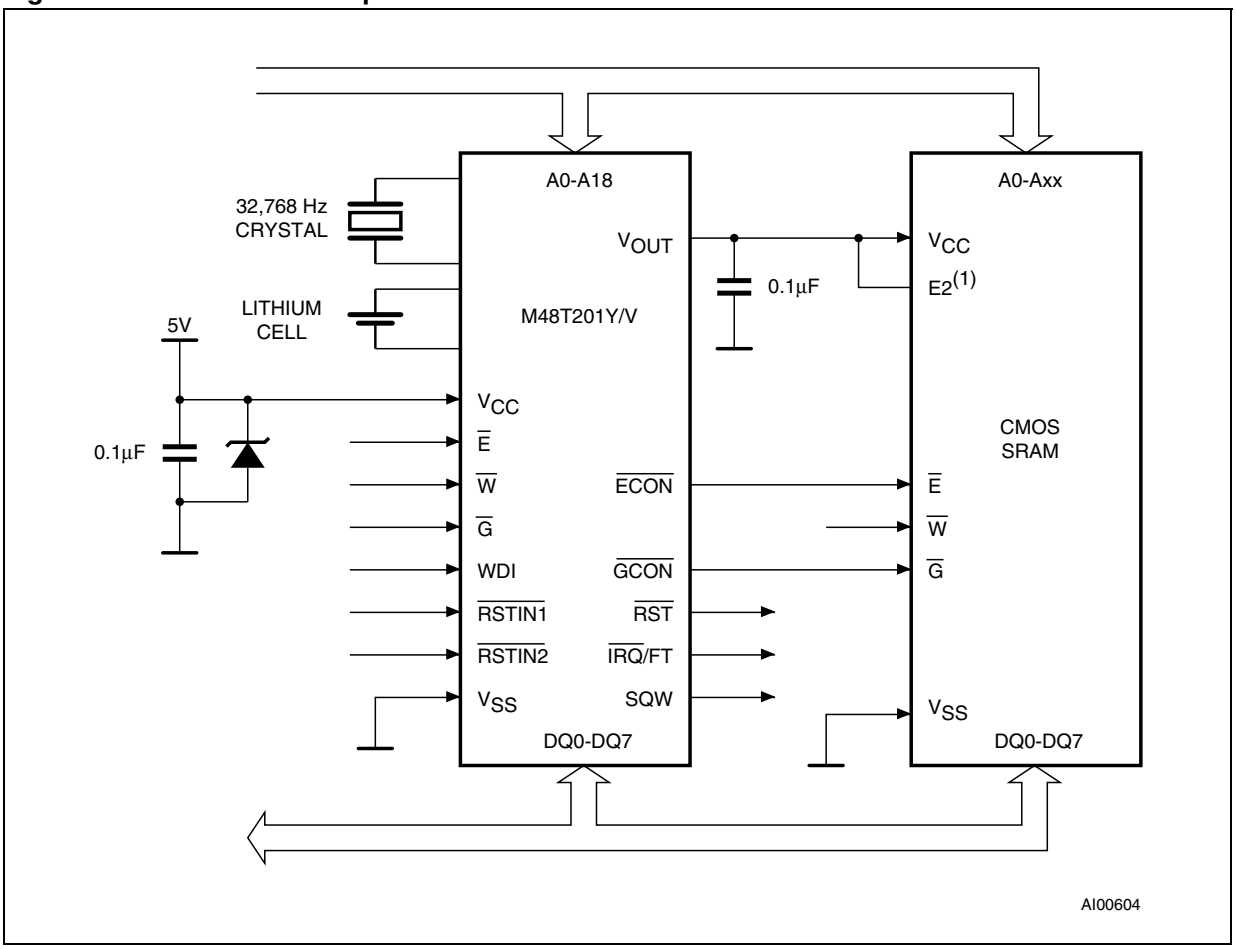


Figure 3. Hardware hookup



1. If the second chip enable pin (E2) is unused, it should be tied to V_{OUT}.

2 Operation

Automatic backup and write protection for an external SRAM is provided through V_{OUT}, $\overline{E}_{CON}$, and $\overline{G}_{CON}$ pins. (Users are urged to insure that voltage specifications, for both the supervisor chip and external SRAM chosen, are similar.) The SNAPHAT® containing the lithium energy source is used to retain the RTC and RAM data in the absence of V_{CC} power through the V_{OUT} pin. The chip enable output to RAM ($\overline{E}_{CON}$) and the output enable output to RAM ($\overline{G}_{CON}$) are controlled during power transients to prevent data corruption. The date is automatically adjusted for months with less than 31 days and corrects for leap years (valid until 2100). The internal watchdog timer provides programmable alarm windows.

The nine clock bytes (7FFFFh-7FFF9h and 7FFF1h) are not the actual clock counters, they are memory locations consisting of BiPORT™ READ/WRITE memory cells within the static RAM array. Clock circuitry updates the clock bytes with current information once per second. The information can be accessed by the user in the same manner as any other location in the static memory array. Byte 7FFF8h is the clock control register. This byte controls user access to the clock information and also stores the clock calibration setting.

Byte 7FFF7h contains the watchdog timer setting. The watchdog timer can generate either a reset or an interrupt, depending on the state of the watchdog steering bit (WDS). Bytes 7FFF6h-7FFF2h include bits that, when programmed, provide for clock alarm functionality. Alarms are activated when the register content matches the month, date, hours, minutes, and seconds of the clock registers. Byte 7FFF1h contains century information. Byte 7FFF0h contains additional flag information pertaining to the watchdog timer, the alarm condition, the battery status and square wave output operation. 4 bits are included within this register (RS0-RS3) that are used to program the square wave output frequency (see *Table 7 on page 21*). The M48T201Y/V also has its own power-fail detect circuit. This control circuitry constantly monitors the supply voltage for an out of tolerance condition. When V_{CC} is out of tolerance, the circuit write protects the TIMEKEEPER® register data and external SRAM, providing data security in the midst of unpredictable system operation. As V_{CC} falls below the battery backup switchover voltage (V_{SO}), the control circuitry automatically switches to the battery, maintaining data and clock operation until valid power is restored.

2.1 Address decoding

The M48T201Y/V accommodates 19 address lines (A0-A18) which allow direct connection of up to 512 K bytes of static RAM. Regardless of SRAM density used, timekeeping, watchdog, alarm, century, flag, and control registers are located in the upper RAM locations. All TIMEKEEPER registers reside in the upper RAM locations without conflict by inhibiting the $\overline{G}_{CON}$ (output enable RAM) signal during clock access. The RAM's physical locations are transparent to the user and the memory map looks continuous from the first clock address to the upper most attached RAM addresses.

Table 2. Operating modes

Mode	V_{CC}	E	G	W	DQ7-DQ0	Power
Deselect	4.5 V to 5.5 V or 3.0 V to 3.6 V	V_{IH}	X	X	High-Z	Standby
WRITE		V_{IL}	X	V_{IL}	D_{IN}	Active
READ		V_{IL}	V_{IL}	V_{IH}	D_{OUT}	Active
READ		V_{IL}	V_{IH}	V_{IH}	High-Z	Active
Deselect	V_{SO} to V_{PFD} (min)(1)	X	X	X	High-Z	CMOS standby
Deselect	$\leq V_{SO}$(1)	X	X	X	High-Z	Battery backup

1. See *Table 14 on page 30* for details.

Note: X = V_{IH} or V_{IL}; V_{SO} = battery backup switchover voltage

2.2 Read mode

The M48T201Y/V executes a READ cycle whenever $\overline{W}$ (WRITE enable) is high and $\overline{E}$ (chip enable) is low. The unique address specified by the address inputs (A0-A18) defines which one of the on-chip TIMEKEEPER® registers or external SRAM locations is to be accessed. When the address presented to the M48T201Y/V is in the range of 7FFFFh-7FFF0h, one of the on-board TIMEKEEPER registers is accessed and valid data will be available to the eight data output drivers within t_{AVQV} after the address input signal is stable, providing that the $\overline{E}$ and $\overline{G}$ access times are also satisfied. If they are not, then data access must be measured from the latter occurring signal ($\overline{E}$ or $\overline{G}$) and the limiting parameter is either t_{ELQV} for $\overline{E}$ or t_{GLQV} for $\overline{G}$ rather than the address access time. When one of the on-chip TIMEKEEPER registers is selected for READ, the $\overline{G}_{CON}$ signal will remain inactive throughout the READ cycle.

When the address value presented to the M48T201Y/V is outside the range of TIMEKEEPER registers, an external SRAM location will be selected. In this case the $\overline{G}$ signal will be passed to the $\overline{G}_{CON}$ pin, with the specified delay times of t_{AOEL} or t_{OERL}.

Figure 4. $\overline{G}_{CON}$ timing when switching between RTC and external SRAM

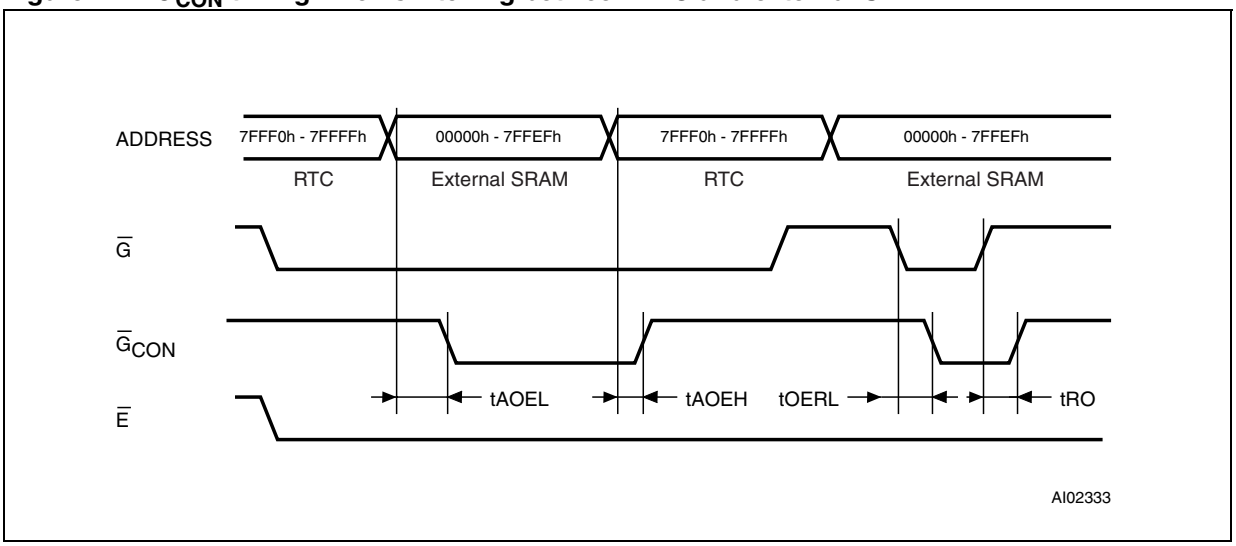


Figure 5. Read cycle timing: RTC and external RAM control signals

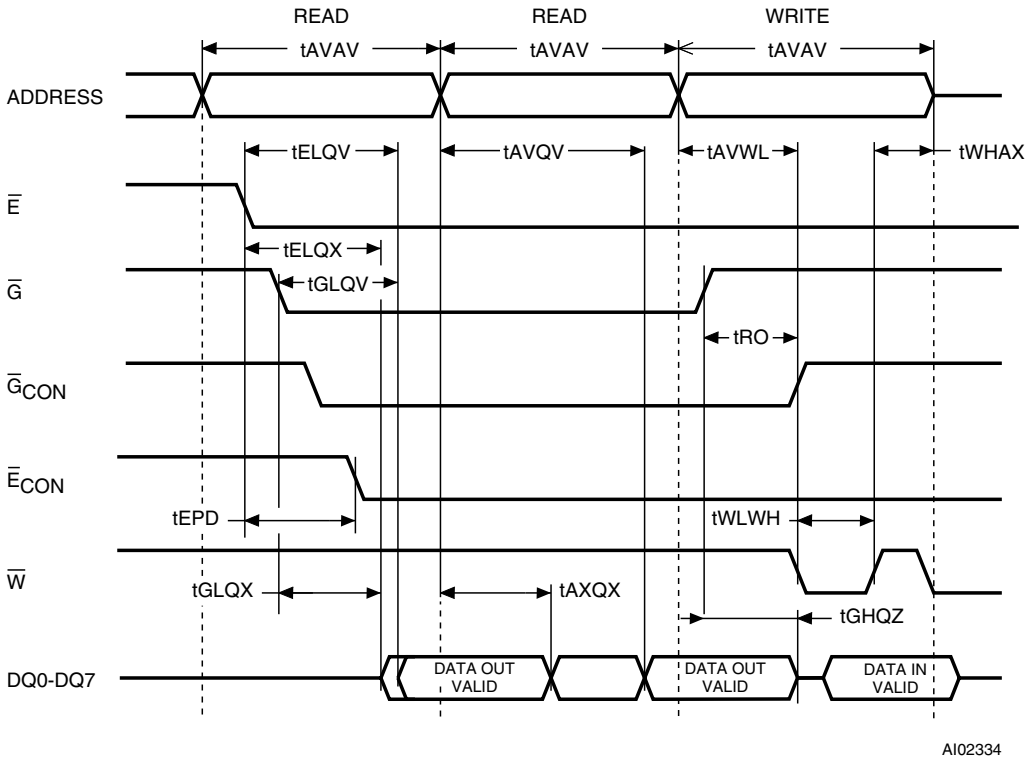


Table 3. Read mode AC characteristics

Symbol	Parameter[1]	M48T201Y		M48T201V		Unit
		–70		–85		
		Min	Max	Min	Max	
t_{AVAV}	READ cycle time	70		85		ns
t_{AVQV}	Address valid to output valid		70		85	ns
t_{ELQV}	Chip enable low to output valid		70		85	ns
t_{GLQV}	Output enable low to output valid		25		35	ns
t_{ELQX}[2]	Chip enable low to output transition	5		5		ns
t_{GLQX}[2]	Output enable low to output transition	0		0		ns
t_{EHQZ}[2]	Chip enable high to output Hi-Z		20		25	ns
t_{GHQZ}[2]	Output enable high to output Hi-Z		20		25	ns
t_{AXQX}	Address transition to output transition	5		5		ns
t_{AOEL}	External SRAM address to $\overline{G}_{CON}$ low		20		30	ns
t_{AOEH}	Supervisor SRAM address to $\overline{G}_{CON}$ high		20		30	ns
t_{EPD}	$\overline{E}$ to $\overline{E}_{CON}$ low or high		10		15	ns
t_{OERL}	$\overline{G}$ low to $\overline{G}_{CON}$ low		15		20	ns
t_{RO}	$\overline{G}$ high to $\overline{G}_{CON}$ high		10		15	ns

1. Valid for ambient operating temperature: T_A = 0 to 70°C; V_{CC} = 4.5 to 5.5 V or 3.0 to 3.6 V (except where noted).
2. C_L = 5 pF.

2.3 Write mode

The M48T201Y/V is in the WRITE mode whenever $\overline{W}$ (WRITE enable) and $\overline{E}$ (chip enable) are low state after the address inputs are stable. The start of a WRITE is referenced from the latter occurring falling edge of $\overline{W}$ or $\overline{E}$. A WRITE is terminated by the earlier rising edge of $\overline{W}$ or $\overline{E}$. The addresses must be held valid throughout the cycle. $\overline{E}$ or $\overline{W}$ must return high for a minimum of t_{EHAX} from chip enable or t_{WHAX} from WRITE enable prior to the initiation of another READ or WRITE cycle. Data-in must be valid t_{DVWH} prior to the end of WRITE and remain valid for t_{WHDX} afterward. $\overline{G}$ should be kept high during WRITE cycles to avoid bus contention; although, if the output bus has been activated by a low on $\overline{E}$ and $\overline{G}$ a low on $\overline{W}$ will disable the outputs t_{WLQZ} after $\overline{W}$ falls.

When the address value presented to the M48T201Y/V during the WRITE is in the range of 7FFFFh-7FFF0h, one of the on-board TIMEKEEPER® registers will be selected and data will be written into the device. When the address value presented to M48T201Y/V is outside the range of TIMEKEEPER registers, an external SRAM location is selected.

Figure 6. Write cycle timing: RTC and external RAM control signals

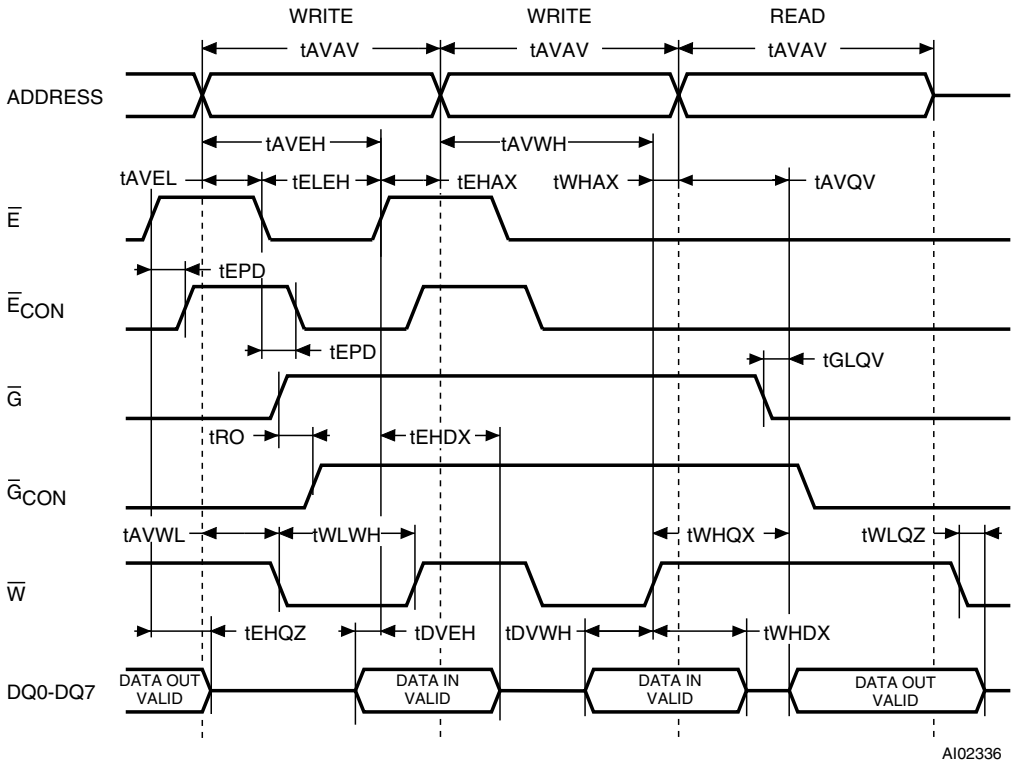


Table 4. Write mode AC characteristics

Symbol	Parameter[1]	M48T201Y		M48T201V		Unit
		–70		–85		
		Min	Max	Min	Max	
t_{AVAV}	WRITE cycle time	70		85		ns
t_{AVWL}	Address valid to WRITE enable low	0		0		ns
t_{AVEL}	Address valid to chip enable low	0		0		ns
t_{WLWH}	WRITE enable pulse width	45		55		ns
t_{ELEH}	Chip enable low to chip enable high	50		60		ns
t_{WHAX}	WRITE enable high to address transition	0		0		ns
t_{EHAX}	Chip enable high to address transition	0		0		ns
t_{DVWH}	Input valid to WRITE enable high	25		30		ns
t_{DVEH}	Input valid to chip enable high	25		30		ns
t_{WHDX}	WRITE enable high to input transition	0		0		ns
t_{EHDX}	Chip enable high to input transition	0		0		ns
t_{WLQZ}[2][3]	WRITE enable low to output High-Z		20		25	ns
t_{AVWH}	Address valid to WRITE enable high	55		65		ns
t_{AVEH}	Address valid to chip enable high	55		65		ns
t_{WHQX}[2][3]	WRITE enable high to output transition	5		5		ns

1. Valid for ambient operating temperature: T_A = 0 to 70°C; V_{CC} = 4.5 to 5.5 V or 3.0 to 3.6 V (except where noted).
2. C_L = 5 pF
3. If $\overline{E}$ goes low simultaneously with $\overline{W}$ going low, the outputs remain in the high impedance state.

2.4 Data retention mode

With valid V_{CC} applied, the M48T201Y/V can be accessed as described above with READ or WRITE cycles. Should the supply voltage decay, the M48T201Y/V will automatically deselect, write protecting itself (and any external SRAM) when V_{CC} falls between V_{PFD} (max) and V_{PFD} (min). This is accomplished by internally inhibiting access to the clock registers via the $\overline{E}$ signal. At this time, the reset pin ($\overline{RST}$) is driven active and will remain active until V_{CC} returns to nominal levels. External RAM access is inhibited in a similar manner by forcing $\overline{E}_{CON}$ to a high level. This level is within 0.2 V of the V_{BAT}. $\overline{E}_{CON}$ will remain at this level as long as V_{CC} remains at an out-of-tolerance condition. When V_{CC} falls below the level of the battery (V_{BAT}), power input is switched from the V_{CC} pin to the SNAPHAT® battery and the clock registers are maintained from the attached battery supply. External RAM is also powered by the SNAPHAT battery. All outputs except $\overline{G}_{CON}$, $\overline{E}_{CON}$, $\overline{RST}$, $\overline{IRQ}$/FT and V_{OUT}, become high impedance. The V_{OUT} pin is capable of supplying 100 µA of current to the attached memory with less than 0.3 V drop under this condition. On power up, when V_{CC} returns to a nominal value, write protection continues for 200 ms (max) by inhibiting $\overline{E}_{CON}$. The $\overline{RST}$ signal also remains active during this time (see *Figure 14 on page 30*).

Note: Most low power SRAMs on the market today can be used with the M48T201Y/V TIMEKEEPER® SUPERVISOR. There are, however some criteria which should be used in making the final choice of an SRAM to use.

The SRAM must be designed in a way where the chip enable input disables all other inputs to the SRAM. This allows inputs to the M48T201Y/V and SRAMs to be “Don't care” once V_{CC} falls below V_{PFD} (min). The SRAM should also guarantee data retention down to V_{CC} = 2.0 V. The chip enable access time must be sufficient to meet the system needs with the chip enable (and output enable) output propagation delays included.

3 Clock operation

3.1 TIMEKEEPER® registers

The M48T201Y/V offers 16 internal registers which contain TIMEKEEPER®, alarm, watchdog, flag, and control data (see *Table 5 on page 18*). These registers are memory locations which contain external (user accessible) and internal copies of the data (usually referred to as BiPORT™ TIMEKEEPER cells). The external copies are independent of internal functions except that they are updated periodically by the simultaneous transfer of the incremented internal copy. TIMEKEEPER and alarm registers store data in BCD. control, watchdog and flags (bits D0 to D3) registers store data in binary format.

3.2 Reading the clock

Updates to the TIMEKEEPER registers should be halted before clock data is read to prevent reading data in transition. The BiPORT TIMEKEEPER cells in the RAM array are only data registers and not the actual clock counters, so updating the registers can be halted without disturbing the clock itself.

Updating is halted when a '1' is written to the READ bit, D6 in the control register (7FFF8h). As long as a '1' remains in that position, updating is halted. After a halt is issued, the registers reflect the count; that is, the day, date, and time that were current at the moment the halt command was issued.

All of the TIMEKEEPER registers are updated simultaneously. A halt will not interrupt an update in progress. Updating occurs approximately 1 second after the READ bit is reset to a '0.'

3.3 Setting the clock

Bit D7 of the control register (7FFF8h) is the WRITE bit. Setting the WRITE bit to a '1,' like the READ bit, halts updates to the TIMEKEEPER registers. The user can then load them with the correct day, date, and time data in 24-hour BCD format (see *Table 5 on page 18*).

Resetting the WRITE bit to a '0' then transfers the values of all time registers (7FFFFh-7FFF9h, 7FFF1h) to the actual TIMEKEEPER counters and allows normal operation to resume. After the WRITE bit is reset, the next clock update will occur approximately one second later.

Note: Upon power-up following a power failure, both the WRITE bit and the READ bit will be reset to '0.'

3.4 Stopping and starting the oscillator

The oscillator may be stopped at any time. If the device is going to spend a significant amount of time on the shelf, the oscillator can be turned off to minimize current drain on the battery. The STOP bit is located at bit D7 within the seconds register (7FFF9h). Setting it to a '1' stops the oscillator. When reset to a '0,' the M48T201Y/V oscillator starts within one second.

Note: It is not necessary to set the WRITE bit when setting or resetting the FREQUENCY TEST bit (FT) or the STOP bit (ST).

Table 5. TIMEKEEPER® register map

Address	Data								Function/range BCD format	
	D7	D6	D5	D4	D3	D2	D1	D0		
7FFFFh	10 years				Year				Year	00-99
7FFFEh	0	0	0	10 M	Month				Month	01-12
7FFFDh	0	0	10 date		Date: Day of month				Date	01-31
7FFFCh	0	FT	0	0	0	Day			Day	01-07
7FFFBh	0	0	10 hours		Hours (24-hour format)				Hours	00-23
7FFFAh	0	10 minutes			Minutes				Minutes	00-59
7FFF9h	ST	10 seconds			Seconds				Seconds	00-59
7FFF8h	W	R	S	Calibration					Control	
7FFF7h	WDS	BMB4	BMB3	BMB2	BMB1	BMB0	RB1	RB0	Watchdog	
7FFF6h	AFE	SQWE	ABE	Al.10M	Alarm month				Al. month	01-12
7FFF5h	RPT4	RPT5	Al. 10 date		Alarm date				Al. date	01-31
7FFF4h	RPT3	0	Al. 10 hours		Alarm hours				Al. hours	00-23
7FFF3h	RPT2	Alarm 10 minutes			Alarm minutes				Al. minutes	00-59
7FFF2h	RPT1	Alarm 10 seconds			Alarm seconds				Al. seconds	00-59
7FFF1h	1000 years				100 years				Century	00-99
7FFF0h	WDF	AF	0	BL	RS3	RS2	RS1	RS0	Flags	

Keys:

S = Sign bit
FT = Frequency test bit
R = READ bit
W = WRITE bit
ST = Stop bit
0 = Must be set to '0'
WDS = Watchdog steering bit
AF = Alarm flag
BL = Battery low flag
SQWE = Square wave enable bit
BMB0-BMB4 = Watchdog multiplier bits
RB0-RB1 = Watchdog resolution bits
AFE = Alarm flag enable flag
ABE = Alarm in battery backup mode enable bit
RPT1-RPT5 = Alarm repeat mode bits
WDF = Watchdog flag
RS0-RS3 = SQW frequency

3.5 Setting the alarm clock

Registers 7FFF6h-7FFF2h contain the alarm settings. The alarm can be configured to go off at a prescribed time on a specific month, day of month, hour, minute, or second or repeat every month, day of month, hour, minute, or second.

It can also be programmed to go off while the M48T201Y/V is in the battery backup to serve as a system wake-up call.

Bits RPT5-RPT1 put the alarm in the repeat mode of operation. *Table 6* shows the possible configurations. Codes not listed in the table default to the once per second mode to quickly alert the user of an incorrect alarm setting.

Note: User must transition address (or toggle chip enable) to see flag bit change.

When the clock information matches the alarm clock settings based on the match criteria defined by RPT5-RPT1, the AF (alarm flag) is set. If AFE (alarm flag enable) is also set, the alarm condition activates the $\overline{IRQ}$/FT pin. To disable alarm, write '0' to the alarm-date register and RPT1-5. The $\overline{IRQ}$/FT output is cleared by a READ to the flags register as shown in *Figure 7*. A subsequent READ of the flags register is necessary to see that the value of the alarm flag has been reset to '0.'

The $\overline{IRQ}$/FT pin can also be activated in the battery backup mode. The $\overline{IRQ}$/FT will go low if an alarm occurs and both ABE (alarm in battery backup mode enable) and AFE are set. The ABE and AFE bits are reset during power-up, therefore an alarm generated during power-up will only set AF. The user can read the flag register at system boot-up to determine if an alarm was generated while the M48T201Y/V was in the deselect mode during power-up. *Figure 8 on page 20* illustrates the backup mode alarm timing.

Figure 7. Alarm interrupt reset waveforms

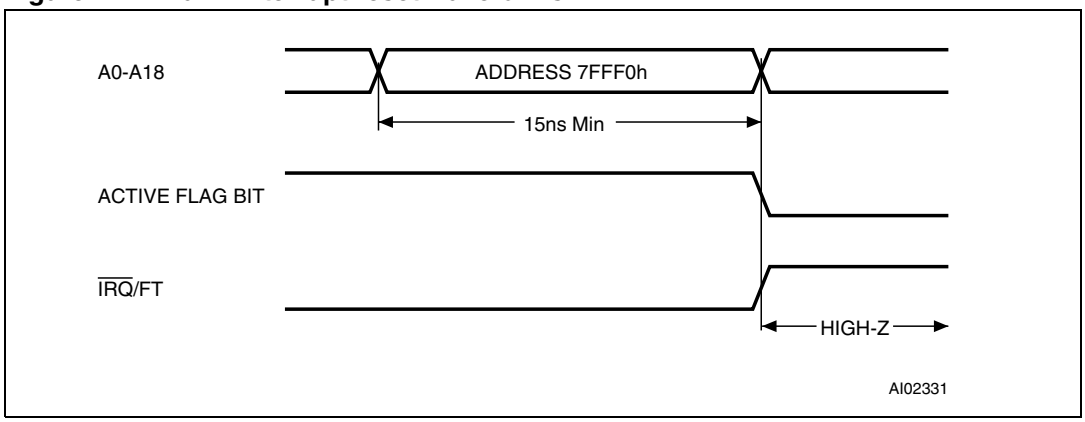
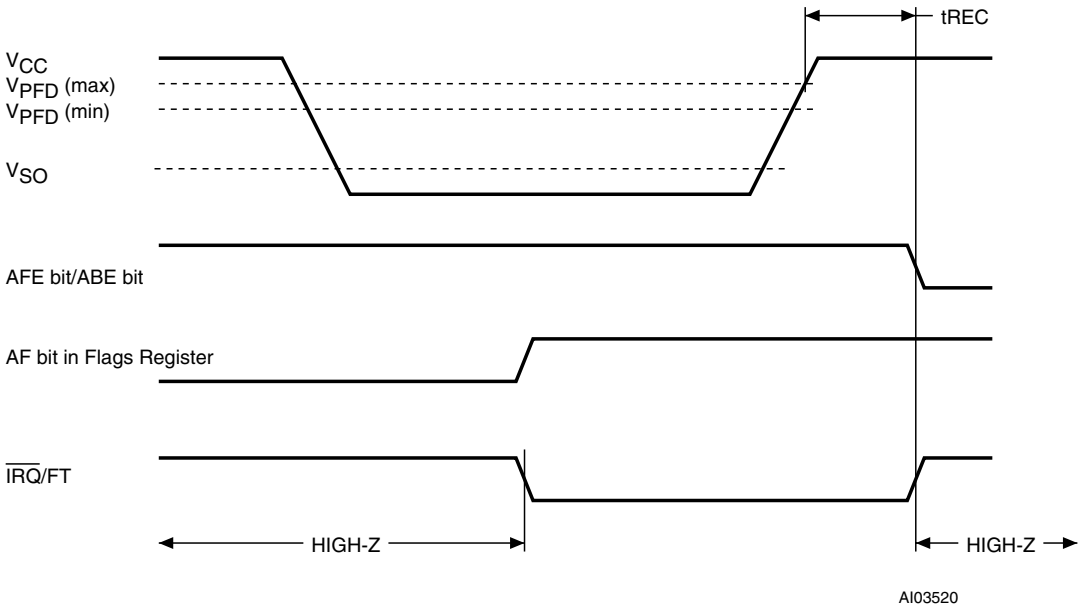


Table 6. Alarm repeat modes

RPT5	RPT4	RPT3	RPT2	RPT1	Alarm setting
1	1	1	1	1	Once per second
1	1	1	1	0	Once per minute
1	1	1	0	0	Once per hour
1	1	0	0	0	Once per day
1	0	0	0	0	Once per month
0	0	0	0	0	Once per year

Figure 8. Backup mode alarm waveforms



3.6 Watchdog timer

The watchdog timer can be used to detect an out-of-control microprocessor. The user programs the watchdog timer by setting the desired amount of timeout into the Watchdog Register, address 7FFF7h. Bits BMB4-BMB0 store a binary multiplier and the two lower order bits RB1-RB0 select the resolution, where 00 = 1/16 second, 01 = 1/4 second, 10 = 1 second, and 11 = 4 seconds. The amount of timeout is then determined to be the multiplication of the five-bit multiplier value with the resolution. (For example: writing 00001110 in the watchdog register = 3*1 or 3 seconds).

Note: Accuracy of timer is within ± the selected resolution.

If the processor does not reset the timer within the specified period, the M48T201Y/V sets the WDF (watchdog flag) and generates a watchdog interrupt or a microprocessor reset. WDF is reset by reading the flag register (address 7FFF0h).

The most significant bit of the watchdog register is the watchdog steering bit (WDS). When set to a '0', the watchdog will activate the $\overline{IRQ}$/FT pin when timed-out. When WDS is set to a '1,' the watchdog will output a negative pulse on the $\overline{RST}$ pin for t_{REC}. The watchdog register and the AFE, SQWE, ABE, and FT bits will reset to a '0' at the end of a watchdog timeout when the WDS bit is set to a '1.'

The watchdog timer can be reset by two methods:

1. a transition (high-to-low or low-to-high) can be applied to the watchdog input pin (WDI) or
2. the microprocessor can perform a WRITE of the watchdog register.

The timeout period then starts over. The WDI pin should be tied to V_{SS} if not used. The watchdog will be reset on each transition (edge) seen by the WDI pin.

In order to perform a software reset of the watchdog timer, the original timeout period can be written into the watchdog register, effectively restarting the countdown cycle.

Should the watchdog timer time out, and the WDS bit is programmed to output an interrupt, a value of 00h needs to be written to the watchdog register in order to clear the $\overline{IRQ}$/FT pin. This will also disable the watchdog function until it is again programmed correctly. A READ of the flags register will reset the watchdog flag (bit D7; register 7FFF0h).

The watchdog function is automatically disabled upon power-down and the watchdog register is cleared. If the watchdog function is set to output to the $\overline{IRQ}$/FT pin and the frequency test function is activated, the watchdog or alarm function prevails and the frequency test function is denied.

Note: The user must transition the address (or toggle chip enable) to see the flag bit change.

3.7 Square wave output

The M48T201Y/V offers the user a programmable square wave function which is output on the SQW pin. RS3-RS0 bits located in 7FFF0h establish the square wave output frequency. These frequencies are listed in *Table 7*. Once the selection of the SQW frequency has been completed, the SQW pin can be turned on and off under software control with the square wave enable bit (SQWE) located in register 7FFF6h.

Table 7. Square wave output frequency

Square wave bits				Square wave	
RS3	RS2	RS1	RS0	Frequency	Units
0	0	0	0	Hi-Z	-
0	0	0	1	32.768	kHz
0	0	1	0	8.192	kHz
0	0	1	1	4.096	kHz
0	1	0	0	2.048	kHz
0	1	0	1	1.024	kHz
0	1	1	0	512	Hz
0	1	1	1	256	Hz
1	0	0	0	128	Hz
1	0	0	1	64	Hz
1	0	1	0	32	Hz
1	0	1	1	16	Hz
1	1	0	0	8	Hz
1	1	0	1	4	Hz
1	1	1	0	2	Hz
1	1	1	1	1	Hz

3.8 Power-on reset

The M48T201Y/V continuously monitors V_{CC}. When V_{CC} falls to the power fail detect trip point, the $\overline{RST}$ pulls low (open drain) and remains low on power-up for t_{REC} after V_{CC} passes V_{PFD} (max). The $\overline{RST}$ pin is an open drain output and an appropriate pull-up resistor to V_{CC} should be chosen to control rise time.

3.9 Reset inputs ($\overline{RSTIN1}$ & $\overline{RSTIN2}$)

The M48T201Y/V provides two independent inputs which can generate an output reset. The duration and function of these resets is identical to a reset generated by a power cycle. *Figure 9* and *Table 8* illustrate the AC reset characteristics of this function. Pulses shorter than t_{R1} and t_{R2} will not generate a reset condition. $\overline{RSTIN1}$ and $\overline{RSTIN2}$ are each internally pulled up to V_{CC} through a 100 KΩ resistor.

Figure 9. $\overline{RSTIN1}$ and $\overline{RSTIN2}$ timing waveforms

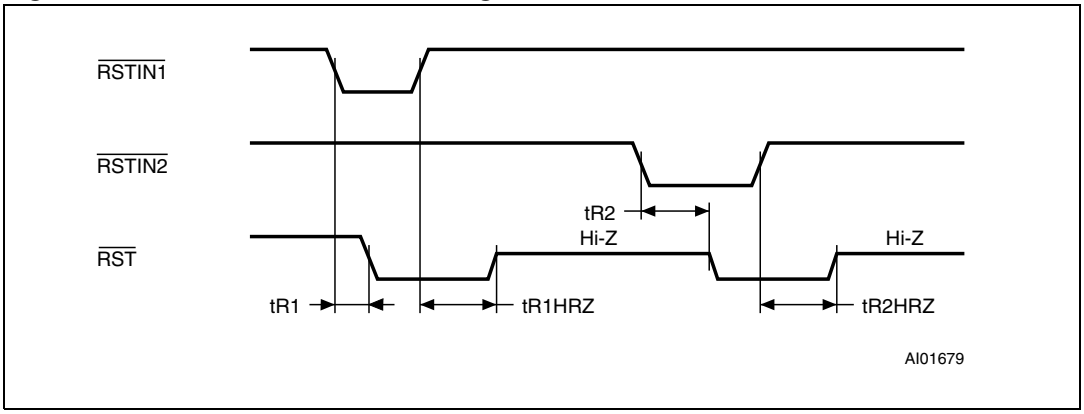


Table 8. Reset AC characteristics

Symbol	Parameter[1]	Min	Max	Unit
t_{R1}	$\overline{RSTIN1}$ low to $\overline{RST}$ low	50	200	ns
t_{R2}	$\overline{RSTIN2}$ low to $\overline{RST}$ low	20	100	ms
t_{R1HRZ}[2]	$\overline{RSTIN1}$ high to $\overline{RST}$ Hi-Z	40	200	ms
t_{R2HRZ}[2]	$\overline{RSTIN2}$ high to $\overline{RST}$ Hi-Z	40	200	ms

1. Valid for ambient operating temperature: T_A = 0 to 70°C; V_{CC} = 4.5 to 5.5 V or 3.0 to 3.6 V (except where noted).
2. C_L = 5 pF (see *Figure 13 on page 28*).

3.10 Calibrating the clock

The M48T201Y/V is driven by a quartz controlled oscillator with a nominal frequency of 32,768 Hz. The devices are factory calibrated at 25°C and tested for accuracy. Clock accuracy will not exceed ±35 ppm (parts per million) oscillator frequency error at 25°C, which equates to about ±1.53 minutes per month. When the calibration circuit is properly employed, accuracy improves to better than +1/–2 ppm at 25°C.

The oscillation rate of crystals changes with temperature (see *Figure 10 on page 24*). The M48T201Y/V design employs periodic counter correction. The calibration circuit adds or subtracts counts from the oscillator divider circuit at the divide by 256 stage, as shown in *Figure 11 on page 24*.

The number of times pulses which are blanked (subtracted, negative calibration) or split (added, positive calibration) depends upon the value loaded into the five calibration bits found in the control register. Adding counts speeds the clock up, subtracting counts slows the clock down.

The calibration bits occupy the five lower order bits (D4-D0) in the control register 7FFF8h. These bits can be set to represent any value between 0 and 31 in binary form. Bit D5 is a sign bit; '1' indicates positive calibration, '0' indicates negative calibration (see *Figure 11 on page 24*). Calibration occurs within a 64 minute cycle. The first 62 minutes in the cycle may, once per minute, have one second either shortened by 128 or lengthened by 256 oscillator cycles. If a binary '1' is loaded into the register, only the first 2 minutes in the 64 minute cycle will be modified; if a binary 6 is loaded, the first 12 will be affected, and so on.

Therefore, each calibration step has the effect of adding 512 or subtracting 256 oscillator cycles for every 125,829,120 actual oscillator cycles, that is +4.068 or –2.034 ppm of adjustment per calibration step in the calibration register. Assuming that the oscillator is running at exactly 32,768 Hz, each of the 31 increments in the calibration byte would represent +10.7 or –5.35 seconds per month which corresponds to a total range of +5.5 or –2.75 minutes per month.

Two methods are available for ascertaining how much calibration a given M48T201Y/V may require. The first involves setting the clock, letting it run for a month and comparing it to a known accurate reference and recording deviation over a fixed period of time. Calibration values, including the number of seconds lost or gained in a given period, can be found in the STMicroelectronics application note AN934, “TIMEKEEPER® calibration.” This allows the designer to give the end user the ability to calibrate the clock as the environment requires, even if the final product is packaged in a non-user serviceable enclosure. The designer could provide a simple utility that accesses the calibration byte.

The second approach is better suited to a manufacturing environment, and involves the use of the $\overline{\text{IRQ}}$/FT pin. The pin will toggle at 512 Hz, when the stop bit (ST, D7 of 7FFF9h) is '0,' the frequency test bit (FT, D6 of 7FFFCh) is '1,' the alarm flag enable bit (AFE, D7 of 7FFF6h) is '0,' and the watchdog steering bit (WDS, D7 of 7FFF7h) is '1' or the watchdog register (7FFF7h=0) is reset.

Note: A 4-second settling time must be allowed before reading the 512 Hz output.

Any deviation from 512 Hz indicates the degree and direction of oscillator frequency shift at the test temperature. For example, a reading of 512.010124 Hz would indicate a +20 ppm oscillator frequency error, requiring a –10 (WR001010) to be loaded into the calibration byte for correction. Note that setting or changing the calibration byte does not affect the frequency test output frequency.

The $\overline{\text{IRQ}}$/FT pin is an open drain output which requires a pull-up resistor to V_{CC} for proper operation. A 500-10 kΩ resistor is recommended in order to control the rise time. The FT bit is cleared on power-down.

Figure 10. Crystal accuracy across temperature

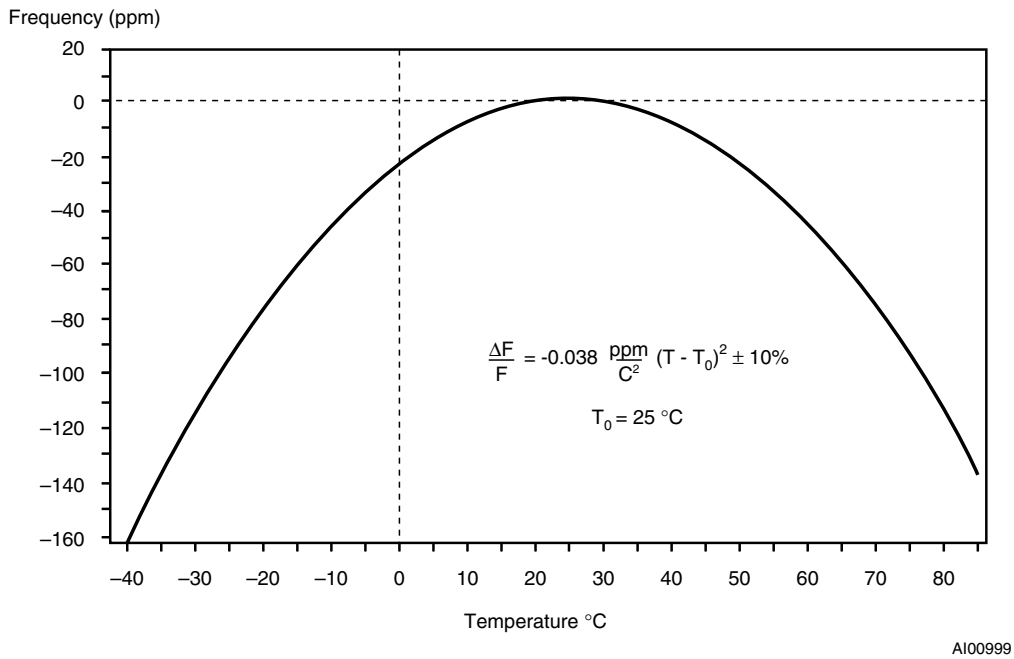
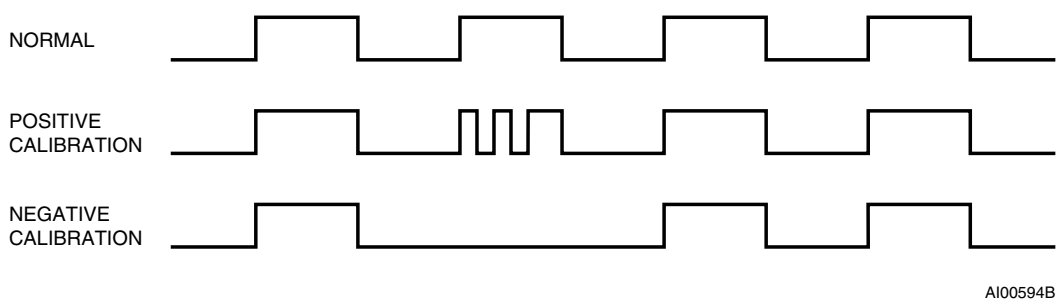


Figure 11. Calibration waveform



3.11 Battery low warning

The M48T201Y/V automatically performs battery voltage monitoring upon power-up and at factory-programmed time intervals of approximately 24 hours. The battery low (BL) bit, bit D4 of flags register 7FFF0h, will be asserted if the battery voltage is found to be less than approximately 2.5 V. The BL bit will remain asserted until completion of battery replacement and subsequent battery low monitoring tests, either during the next power-up sequence or the next scheduled 24-hour interval.

If a battery low is generated during a power-up sequence, this indicates that the battery is below approximately 2.5 V and may not be able to maintain data integrity in the SRAM. Data should be considered suspect and verified as correct. A fresh battery should be installed.

If a battery low indication is generated during the 24-hour interval check, this indicates that the battery is near end of life. However, data is not compromised due to the fact that a nominal V_{CC} is supplied. In order to insure data integrity during subsequent periods of battery backup mode, the battery should be replaced. The SNAPHAT® top may be replaced while V_{CC} is applied to the device.

Note: This will cause the clock to lose time during the interval the battery/crystal is removed.

The M48T201Y/V only monitors the battery when a nominal V_{CC} is applied to the device. Thus applications which require extensive durations in the battery backup mode should be powered-up periodically (at least once every few months) in order for this technique to be beneficial. Additionally, if a battery low is indicated, data integrity should be verified upon power-up via a checksum or other technique.

3.12 Initial power-on defaults

Upon application of power to the device, the following register bits are set to a '0' state: WDS; BMB0-BMB4; RB0-RB1; AFE; ABE; SQWE; W; R; FT (see *Table 9*).

Table 9. Default values

Condition	W	R	FT	AFE	ABE	SQWE	Watchdog register(1)
Initial power-up (Battery attach for SNAPHAT)(2)	0	0	0	0	0	0	0
RESET(3)	0	0	0	0	0	0	0
Power-down(4)	0	0	0	1	1	1	0

1. WDS, BMB0-BMB4, RB0, RB1.
2. State of other control bits undefined.
3. State of other control bits remains unchanged.
4. Assuming these bits set to '1' prior to power-down.