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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
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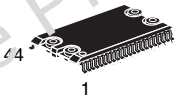
M48T212V

3.3V TIMEKEEPER® supervisor

Features

- Integrated real-time clock, power-fail control circuit, battery and crystal
- Converts low power SRAM into NVRAMs
- Year 2000 compliant (4-digit year)
- Battery low flag
- Microprocessor power-on reset
- Programmable alarm output active in the battery backed-up mode
- Watchdog timer
- Automatic power-fail chip deselect and WRITE protection
- WRITE protect voltage (V_{PFD} = Power-fail deselect voltage):
  - M48T212V: V_{CC} = 3.0 to 3.6V
    $2.7V \leq V_{PFD} \leq 3.0V$
- Packaging includes a 44-lead SOIC and SNAPHAT® top (to be ordered separately)
- RoHS compliant
  - Lead-free second level interconnect

SNAPHAT (SH)
Crystal/battery



SOH44 (MH)

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1 Description

The M48T212V is a self-contained device that includes a real-time clock (RTC), programmable alarms, a watchdog timer, and two external chip enable outputs which provide control of up to four (two in parallel) external low-power static RAMs.

Access to all TIMEKEEPER® functions and the external RAM is the same as conventional byte-wide SRAM. The 16 TIMEKEEPER Registers offer Century, Year, Month, Date, Day, Hour, Minute, Second, Calibration, Alarm, Watchdog, and Flags. Externally attached static RAMs are controlled by the M48T212V via the $\overline{E1}_{CON}$ and $\overline{E2}_{CON}$ signals (see *Table 3 on page 10*).

The 44-pin, 330mil SOIC provides sockets with gold plated contacts at both ends for direct connection to a separate SNAPHAT® housing containing the battery and crystal. The unique design allows the SNAPHAT battery package to be mounted on top of the SOIC package after the completion of the surface mount process.

Insertion of the SNAPHAT housing after reflow prevents potential battery and crystal damage due to the high temperatures required for device surface-mounting. The SNAPHAT housing is keyed to prevent reverse insertion.

The SOIC and battery/crystal packages are shipped separately in plastic anti-static tubes or in Tape & Reel form. For the-44 lead SOIC, the battery/crystal package (e.g., SNAPHAT) part number is “M4TXX-BR12SH” (see *Table 20 on page 33*).

Caution: Do not place the SNAPHAT battery/crystal top in conductive foam, as this will drain the lithium button-cell battery.

Figure 1. Logic diagram

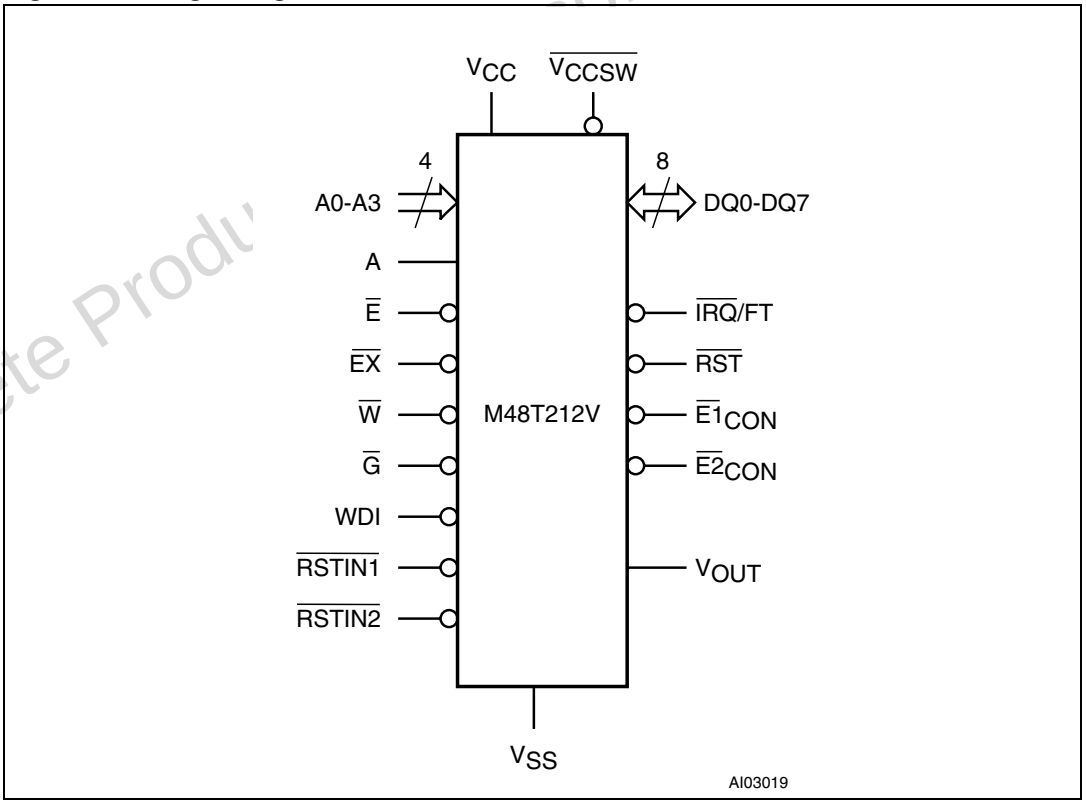


Table 1. Signal names

A0-A3	Address inputs
DQ0-DQ7	Data inputs/outputs
$\overline{RSTIN1}$	Reset 1 input
$\overline{RSTIN2}$	Reset 2 input
$\overline{RST}$	Reset output (open drain)
WDI	Watchdog input
A	Bank select input
$\overline{E}$	Chip enable input
$\overline{EX}$	External chip enable input
$\overline{G}$	Output enable input
$\overline{W}$	WRITE enable input
$\overline{E1}_{CON}$	RAM chip enable 1 output
$\overline{E2}_{CON}$	RAM chip enable 2 output
$\overline{IRQ}$/FT	Int/freq test output (open drain)
$\overline{V}_{\overline{CCSW}}$	V_{CC} switch output
V_{OUT}	Supply voltage output
V_{CC}	Supply voltage
V_{SS}	Ground
NC	Not connected internally

Figure 2. SOIC connections

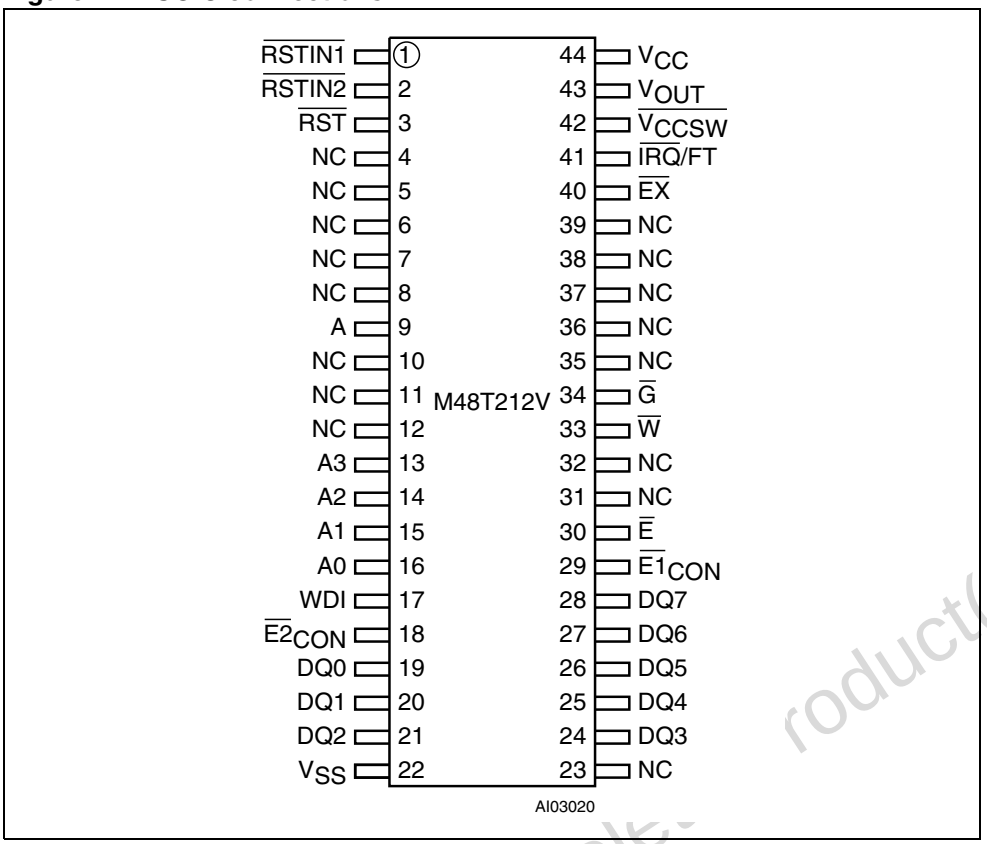
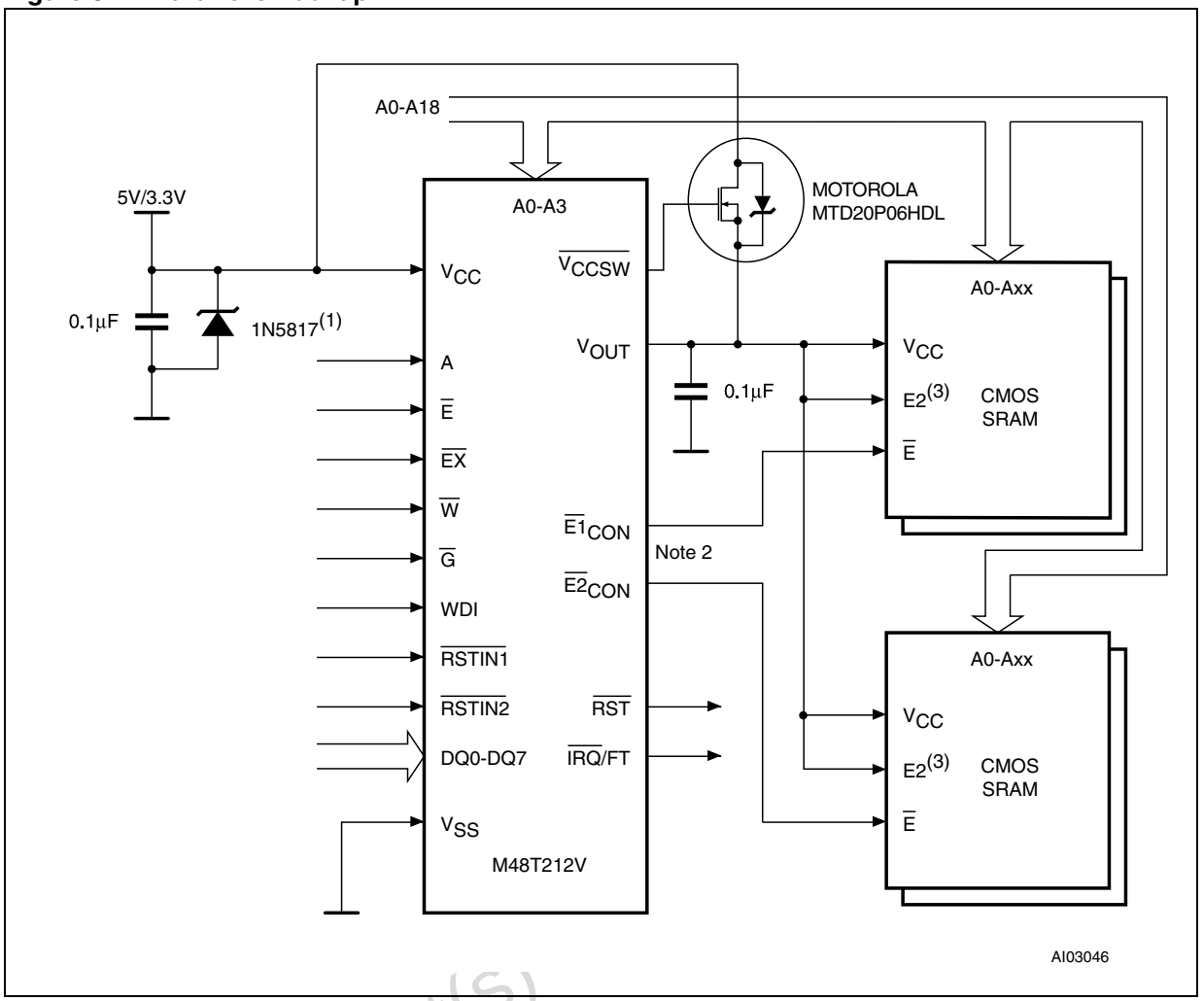


Figure 3. Hardware hookup



1. Traces connecting $\overline{E1}_{CON}$ and $\overline{E2}_{CON}$ to external SRAM should be as short as possible.
2. If the second chip enable pin (E2) is unused, it should be tied to V_{OUT}.

Note: See description in Power Supply Decoupling and Undershoot Protection.

2 Operation

Automatic backup and write protection for an external SRAM is provided through V_{OUT}, $\overline{E1}_{CON}$ and $\overline{E2}_{CON}$ pins. (Users are urged to ensure that voltage specifications, for both the SUPERVISOR chip and external SRAM chosen, are similar). The SNAPHAT® containing the lithium energy source used to permanently power the real-time clock is also used to retain RAM data in the absence of V_{CC} power through the V_{OUT} pin.

The chip enable outputs to RAM ($\overline{E1}_{CON}$ and $\overline{E2}_{CON}$) are controlled during power transients to prevent data corruption. The date is automatically adjusted for months with less than 31 days and corrects for leap years (valid until 2100). The internal watchdog timer provides programmable alarm windows.

The nine clock bytes (Fh-9h and 1h) are not the actual clock counters, they are memory locations consisting of BiPORT™ READ/WRITE memory cells within the static RAM array. Clock circuitry updates the clock bytes with current information once per second. The information can be accessed by the user in the same manner as any other location in the static memory array.

Byte 8h is the clock control register. This byte controls user access to the clock information and also stores the clock calibration setting. Byte 7h contains the watchdog timer setting. The watchdog timer can generate either a reset or an interrupt, depending on the state of the Watchdog Steering Bit (WDS). Bytes 6h-2h include bits that, when programmed, provide for clock alarm functionality.

Alarms are activated when the register content matches the month, date, hours, minutes, and seconds of the clock registers. Byte 1h contains century information. Byte 0h contains additional flag information pertaining to the watchdog timer, alarm and battery status.

The M48T212V also has its own Power-Fail Detect circuit. This control circuitry constantly monitors the supply voltage for an out of tolerance condition. When V_{CC} is out of tolerance, the circuit write protects the TIMEKEEPER® register data and external SRAM, providing data security in the midst of unpredictable system operation. As V_{CC} falls below V_{SO}, the control circuitry automatically switches to the battery, maintaining data and clock operation until valid power is restored.

2.1 Address decoding

The M48T212YV accommodates 4 address lines (A3-A0) which allow access to the sixteen bytes of the TIMEKEEPER clock registers. All TIMEKEEPER registers reside in the SUPERVISOR chip itself. All TIMEKEEPER registers are accessed by enabling $\overline{E}$ (Chip Enable).

Table 2. Operating modes

Mode	V_{CC}	E	G	W	DQ7-DQ0	Power
Deselect	3.0V to 3.6V	V_{IH}	X	X	High-Z	Standby
WRITE		V_{IL}	X	V_{IL}	D_{IN}	Active
READ		V_{IL}	V_{IL}	V_{IH}	D_{OUT}	Active
READ		V_{IL}	V_{IH}	V_{IH}	High-Z	Active
Deselect	V_{SO} to V_{PFD} (min)(1)	X	X	X	High-Z	CMOS standby
Deselect	$\leq V_{SO}$(1)	X	X	X	High-Z	Battery back-up

1. See *Table 14 on page 28* for details.

Note: X = V_{IH} or V_{IL}; V_{SO} = Battery back-up switchover voltage

Table 3. Truth table for SRAM bank select

Mode	V_{CC}	$\overline{EX}$	A	$\overline{E1}_{CON}$	$\overline{E2}_{CON}$	Power
Select	3.0V to 3.6V	Low	Low	Low	High	Active
		Low	High	High	Low	Active
Deselect		High	X	High	High	Standby
Deselect	V_{SO} to V_{PFD} (min)(1)(	X	X	High	High	CMOS standby
Deselect	$\leq V_{SO}$(1)	X	X	High	High	Battery back-up

1. See *Table 14 on page 28* for details.

Note: X = V_{IH} or V_{IL}; V_{SO} = Battery back-up switchover voltage

Figure 4. Chip enable control and bank select timing

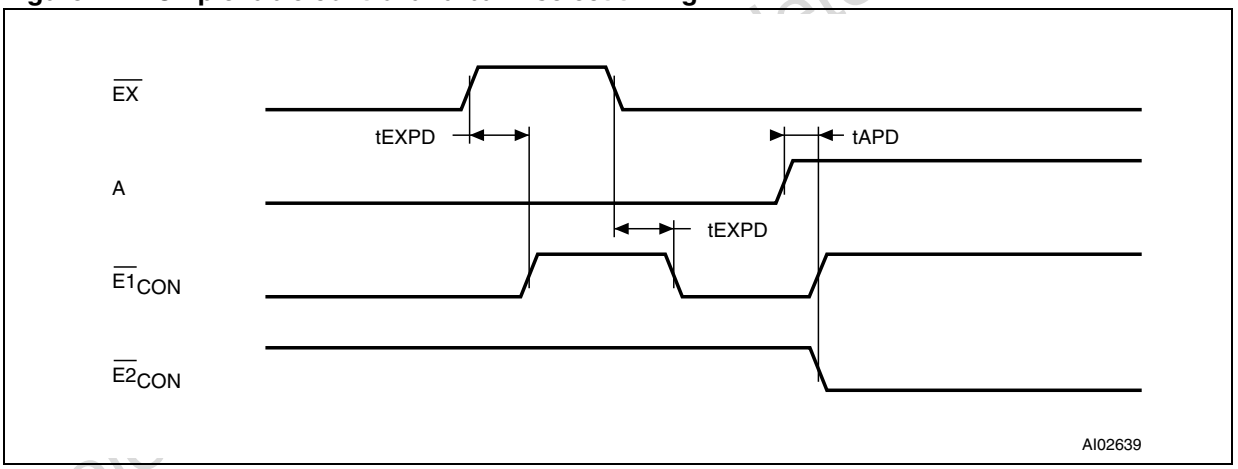


Table 4. Chip enable control and bank select characteristics

Symbol	Parameter	M48T212V		Unit
		–85		
		Min	Max	
t_{EXPD}	$\overline{EX}$ to $\overline{E1}_{CON}$ or $\overline{E2}_{CON}$ (low or high)		15	ns
t_{APD}	A to $\overline{E1}_{CON}$ or $\overline{E2}_{CON}$ (low or high)		15	ns

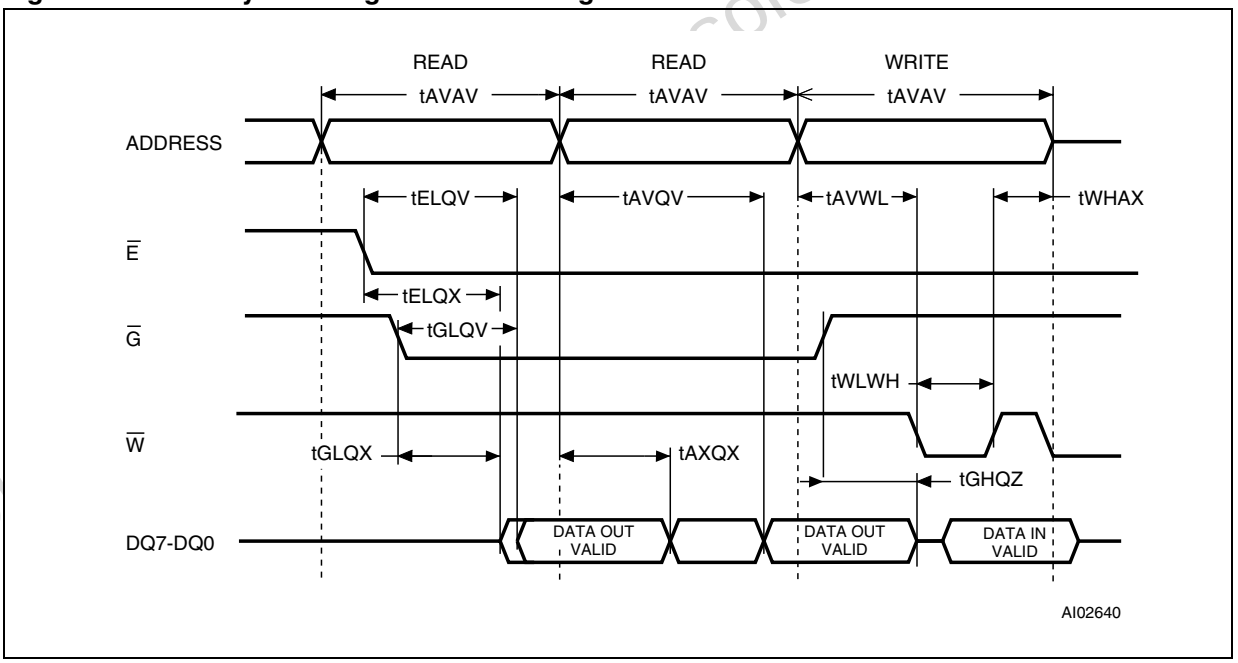
2.2 Read mode

The M48T212V executes a READ cycle whenever $\overline{W}$ (WRITE Enable) is high and $\overline{E}$ (Chip Enable) is low. The unique address specified by the address inputs (A3-A0) defines which one of the on-chip TIMEKEEPER® registers is to be accessed. When the address presented to the M48T212V is in the range of 0h-Fh, one of the on-board TIMEKEEPER registers is accessed and valid data will be available to the eight data output drivers within t_{AVQV} after the address input signal is stable, providing that the $\overline{E}$ and $\overline{G}$ access times are also satisfied.If they are not, then data access must be measured from the latter occurring signal ($\overline{E}$ or $\overline{G}$) and the limiting parameter is either t_{ELQV} for $\overline{E}$ or t_{GLQV} for $\overline{G}$ rather than the address access time.

When $\overline{EX}$ input is low, an external SRAM location will be selected.

Note: Care should be taken to avoid taking both $\overline{E}$ and $\overline{EX}$ low simultaneously to avoid bus contention.

Figure 5. Read cycle timing: RTC control signal waveforms



Note: $\overline{EX}$ is assumed high.

Table 5. Read mode AC characteristics

Symbol	Parameter[1]	M48T212V		Unit
		–85		
		Min	Max	
t_{AVAV}	Read cycle time	85		ns
t_{AVQV}	Address valid to output valid		85	ns
t_{ELQV}	Chip enable low to output valid		85	ns
t_{GLQV}	Output enable low to output valid		35	ns
t_{ELQX}[2]	Chip enable low to output transition	5		ns
t_{GLQX}[2]	Output enable low to output transition	0		ns
t_{EHQZ}[2]	Chip enable high to output Hi-Z		25	ns
t_{GHQZ}[2]	Output enable high to output Hi-Z		25	ns
t_{AXQX}	Address transition to output transition	5		ns

1. Valid for ambient operating temperature: T_A = 0 to 70°C; V_{CC} = 3.0 to 3.6V (except where noted).
2. C_L = 5pF.

2.3 Write mode

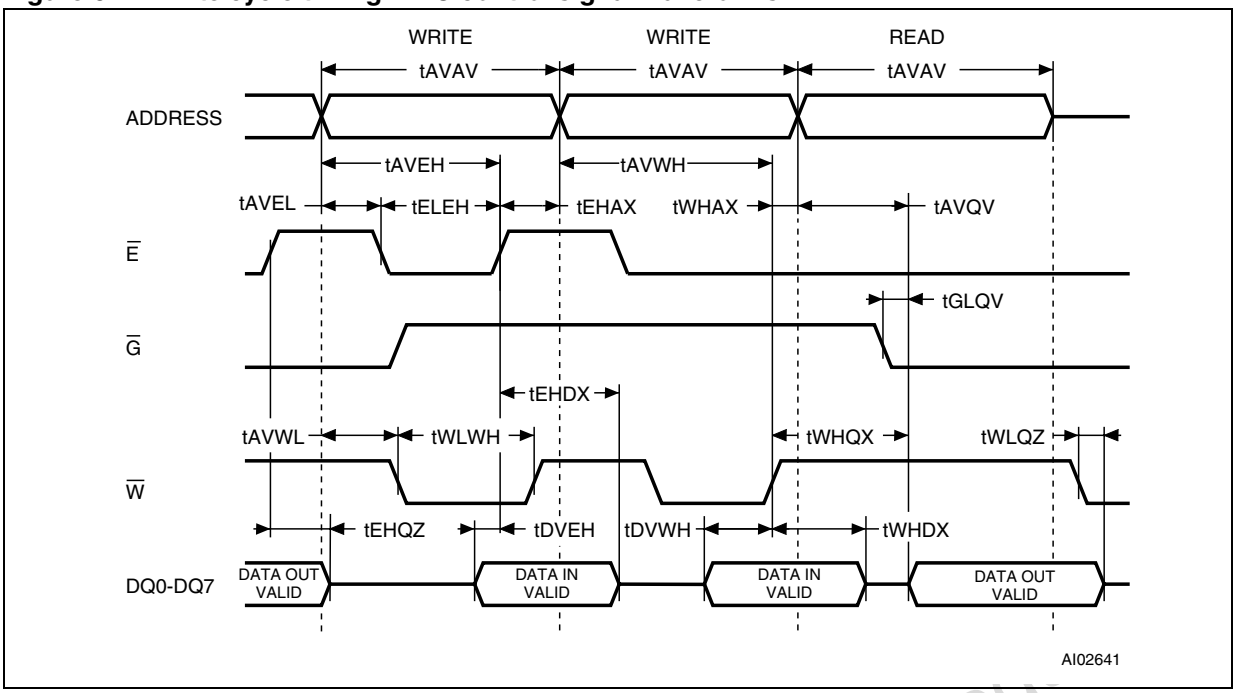
The M48T212V is in the WRITE Mode whenever $\overline{W}$ (WRITE Enable) and $\overline{E}$ (Chip Enable) are in a low state after the address inputs are stable. The start of a WRITE is referenced from the latter occurring falling edge of $\overline{W}$ or $\overline{E}$. A WRITE is terminated by the earlier rising edge of $\overline{W}$ or $\overline{E}$. The addresses must be held valid throughout the cycle. $\overline{E}$ or $\overline{W}$ must return high for a minimum of t_{EHAX} from Chip Enable or t_{WHAX} from WRITE Enable prior to the initiation of another READ or WRITE cycle. Data-in must be valid t_{DVWH} prior to the end of WRITE and remain valid for t_{WHDX} afterward.

$\overline{G}$ should be kept high during WRITE cycles to avoid bus contention; although, if the output bus has been activated by a low on $\overline{E}$ and $\overline{G}$ a low on $\overline{W}$ will disable the outputs t_{WLQZ} after $\overline{W}$ falls.

When $\overline{E}$ is low during the WRITE, one of the on-board TIMEKEEPER® registers will be selected and data will be written into the device. When $\overline{EX}$ is low (and $\overline{E}$ is high) an external SRAM location is selected.

Note: Care should be taken to avoid taking both $\overline{E}$ and $\overline{EX}$ low simultaneously to avoid bus contention.

Figure 6. Write cycle timing: RTC control signal waveforms



Note: $\overline{EX}$ is assumed high.

Table 6. Write mode AC characteristics

Symbol	Parameter[1]	M48T212V		Unit
		–85		
		Min	Max	
t_{AVAV}	Write cycle time	85		ns
t_{AVWL}	Address valid to write enable low	0		ns
t_{AVEL}	Address valid to chip enable low	0		ns
t_{WLWH}	Write enable pulse width	55		ns
t_{ELEH}	Chip enable low to chip enable high	60		ns
t_{WHAX}	Write enable high to address transition	0		ns
t_{EHAX}	Chip enable high to address transition	0		ns
t_{DVWH}	Input valid to write enable high	30		ns
t_{DVEH}	Input valid to chip enable high	30		ns
t_{WHDX}	Write enable high to input transition	0		ns
t_{EHDX}	Chip enable high to input transition	0		ns
t_{WLQZ}[2][3]	Write enable low to output High-Z		25	ns
t_{AVWH}	Address valid to write enable high	65		ns
t_{AVEH}	Address valid to chip enable high	65		ns
t_{WHQX}[2][3]	Write enable high to output transition	5		ns

1. Valid for ambient operating temperature: T_A = 0 to 70°C; V_{CC} = 3.0 to 3.6V (except where noted).
2. C_L = 5pF
3. If $\overline{E}$ goes low simultaneously with $\overline{W}$ going low, the outputs remain in the high impedance state.

2.4 Data retention mode

With valid V_{CC} applied, the M48T212V can be accessed as described above with READ or WRITE cycles. Should the supply voltage decay, the M48T212V will automatically deselect, write protecting itself (and any external SRAM) when V_{CC} falls between V_{PFD} (max) and V_{PFD} (min). This is accomplished by internally inhibiting access to the clock registers via the $\overline{E}$ signal. At this time, the Reset pin ($\overline{RST}$) is driven active and will remain active until V_{CC} returns to nominal levels.

External RAM access is inhibited in a similar manner by forcing $\overline{E1}_{CON}$ and $\overline{E2}_{CON}$ to a high level. This level is within 0.2 volts of the V_{BAT}. $\overline{E1}_{CON}$ and $\overline{E2}_{CON}$ will remain at this level as long as V_{CC} remains at an out-of-tolerance condition.

When V_{CC} falls below battery back-up switchover voltage (V_{SO}), power input is switched from the V_{CC} pin to the SNAPHAT® battery and the clock registers and external SRAM are maintained from the attached battery supply. All outputs become high impedance. The V_{OUT} pin is capable of supplying 100µA of current to the attached memory with less than 0.3V drop under this condition. On power up, when V_{CC} returns to a nominal value, write protection continues for 200ms (max) by inhibiting $\overline{E1}_{CON}$ or $\overline{E2}_{CON}$.

The $\overline{RST}$ signal also remains active during this time (see *Figure 14 on page 29*).

Note: Most low power SRAMs on the market today can be used with the M48T212V TIMEKEEPER® SUPERVISOR. There are, however some criteria which should be used in

making the final choice of an SRAM to use. The SRAM must be designed in a way where the chip enable input disables all other inputs to the SRAM. This allows inputs to the M48T212V and SRAMs to be "Don't care" once V_{CC} falls below V_{PFD}(min). The SRAM should also guarantee data retention down to V_{CC} = 2.0V. The chip enable access time must be sufficient to meet the system needs with the chip enable output propagation delays included.

If the SRAM includes a second chip enable pin ($\overline{E2}$), this pin should be tied to V_{OUT}.

If data retention lifetime is a critical parameter for the system, it is important to review the data retention current specifications for the particular SRAMs being evaluated. Most SRAMs specify a data retention current at 3.0V. Manufacturers generally specify a typical condition for room temperature along with a worst case condition (generally at elevated temperatures). The system level requirements will determine the choice of which value to use.

The data retention current value of the SRAMs can then be added to the I_{BAT} value of the M48T212V to determine the total current requirements for data retention. The available battery capacity for the SNAPHAT® of your choice can then be divided by this current to determine the amount of data retention available (see *Table 20 on page 33*).

For a further more detailed review of lifetime calculations, please see Application Note AN1012.

3 Clock operation

3.1 TIMEKEEPER® registers

The M48T212V offers 16 internal registers which contain TIMEKEEPER®, Alarm, Watchdog, Flag, and Control data. These registers are memory locations which contain external (user accessible) and internal copies of the data (usually referred to as BiPORT™ TIMEKEEPER cells).

The external copies are independent of internal functions except that they are updated periodically by the simultaneous transfer of the incremented internal copy. TIMEKEEPER and Alarm Registers store data in BCD. Control, Watchdog and Flags Registers store data in Binary Format.

3.2 Reading the clock

Updates to the TIMEKEEPER registers should be halted before clock data is read to prevent reading data in transition. The BiPORT TIMEKEEPER cells in the RAM array are only data registers and not the actual clock counters, so updating the registers can be halted without disturbing the clock itself.

Updating is halted when a '1' is written to the READ Bit, D6 in the Control Register (8h). As long as a '1' remains in that position, updating is halted. After a halt is issued, the registers reflect the count; that is, the day, date, and time that were current at the moment the halt command was issued.

All of the TIMEKEEPER registers are updated simultaneously. A halt will not interrupt an update in progress. Updating occurs 1 second after the READ Bit is reset to a '0.'

3.3 Setting the clock

Bit D7 of the Control Register (8h) is the WRITE Bit. Setting the WRITE Bit to a '1,' like the READ Bit, halts updates to the TIMEKEEPER registers. The user can then load them with the correct day, date, and time data in 24 hour BCD format (see *Table 7 on page 18*).

Resetting the WRITE Bit to a '0' then transfers the values of all time registers (Fh-9h, 1h) to the actual TIMEKEEPER counters and allows normal operation to resume. After the WRITE Bit is reset, the next clock update will occur one second later.

Note: Upon power-up following a power failure, the READ Bit will automatically be set to a '1.' This will prevent the clock from updating the TIMEKEEPER registers, and will allow the user to read the exact time of the power-down event.

Resetting the READ Bit to a '0' will allow the clock to update these registers with the current time. The WRITE Bit will be reset to a '0' upon power-up.

3.4 Stopping and starting the oscillator

The oscillator may be stopped at any time. If the device is going to spend a significant amount of time on the shelf, the oscillator can be turned off to minimize current drain on the battery. The STOP Bit is located at Bit D7 within the Seconds Register (9h). Setting it to a '1' stops the oscillator. When reset to a '0,' the M48T212V oscillator starts within one second.

Note: It is not necessary to set the WRITE Bit when setting or resetting the FREQUENCY TEST Bit (FT) or the STOP Bit (ST).

Table 7. TIMEKEEPER® register map

Address	D7	D6	D5	D4	D3	D2	D1	D0	Function/range BCD format	
Fh	10 Years				Year				Year	00-99
Eh	0	0	0	10M	Month				Month	01-12
Dh	0	0	10 date		Date: Day of month				Date	01-31
Ch	0	FT	0	0	0	Day of week			Day	01-7
Bh	0	0	10 hours		Hours (24 hour format)				Hours	00-23
Ah	0	10 minutes			Minutes				Min	00-59
9h	ST	10 seconds			Seconds				Sec	00-59
8h	W	R	S	Calibration					Control	
7h	WDS	BMB4	BMB3	BMB2	BMB1	BMB0	RB1	RB0	Watchdog	
6h	AFE	0	ABE	AI 10M	Alarm month				A month	01-12
5h	RPT4	RPT5	AI 10 date		Alarm date				A date	01-31
4h	RPT3	0	AI 10 hour		Alarm hour				A hour	00-23
3h	RPT2	Alarm 10 minutes			Alarm minutes				A min	00-59
2h	RPT1	Alarm 10 seconds			Alarm seconds				A sec	00-59
1h	1000 year				100 year				Century	00-99
0h	WDF	AF	Y	BL	Y	Y	Y	Y	Flag	

Keys:

S = Sign bit
FT = Frequency test bit
R = READ bit
W = WRITE bit
ST = Stop bit
0 = Must be set to '0'
BL = Battery low flag (read only)
BMB0-BMB4 = Watchdog multiplier bits
AFE = Alarm flag enable flag
RB0-RB1 = Watchdog resolution bits
WDS = Watchdog steering bit
ABE = Alarm in battery back-up mode enable bit
RPT1-RPT5 = Alarm repeat mode bits
WDF = Watchdog flag (read only)
AF = Alarm flag (read only)
Y = '1' or '0'

3.5 Setting the alarm clock

Address locations 6h-2h contain the alarm settings. The alarm can be configured to go off at a prescribed time on a specific month, date, hour, minute, or second or repeat every year, month, day, hour, minute, or second. It can also be programmed to go off while the M48T212V is in the battery back-up to serve as a system wake-up call.

Bits RPT5-RPT1 put the alarm in the repeat mode of operation. *Table 8* shows the possible configurations. Codes not listed in the table default to the once per second mode to quickly alert the user of an incorrect alarm setting.

Note: User must transition address (or toggle chip enable) to see Flag Bit change.

When the clock information matches the alarm clock settings based on the match criteria defined by RPT5-RPT1, the AF (Alarm Flag) is set.

If AFE (Alarm Flag Enable) is also set, the alarm condition activates the $\overline{IRQ}$/FT pin. To disable alarm, write '0' to the Alarm Date registers and RPT1-5. The $\overline{IRQ}$/FT output is cleared by a READ to the Flags Register as shown in *Figure 7*. A subsequent READ of the Flags Register is necessary to see that the value of the Alarm Flag has been reset to '0.'

The $\overline{IRQ}$/FT pin can also be activated in the battery back-up mode. The $\overline{IRQ}$/FT will go low if an alarm occurs and both ABE (Alarm in Battery Back-up Mode Enable) and AFE are set. The ABE and AFE Bits are reset during power-up, therefore an alarm generated during power-up will only set AF. The user can read the Flag Register at system boot-up to determine if an alarm was generated while the M48T212V was in the deselect mode during power-up. *Figure 8 on page 20* illustrates the back-up mode alarm timing.

Figure 7. Alarm interrupt reset waveforms

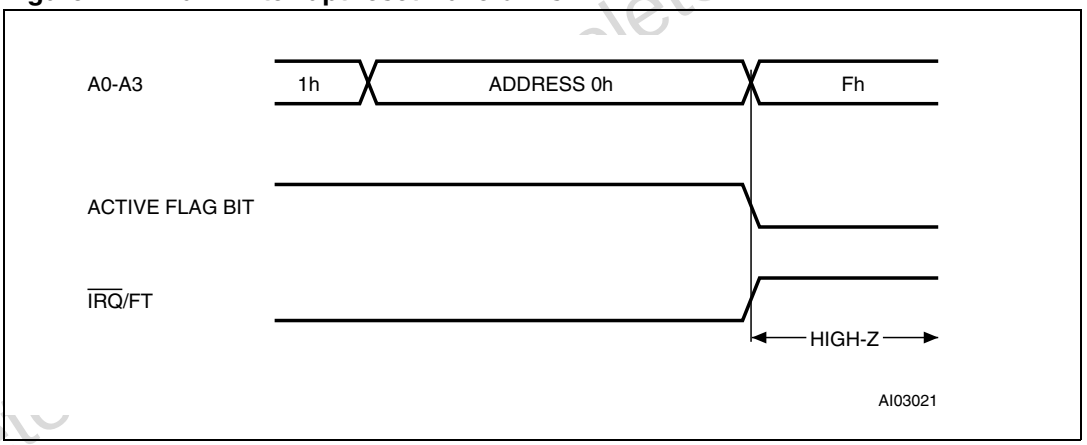
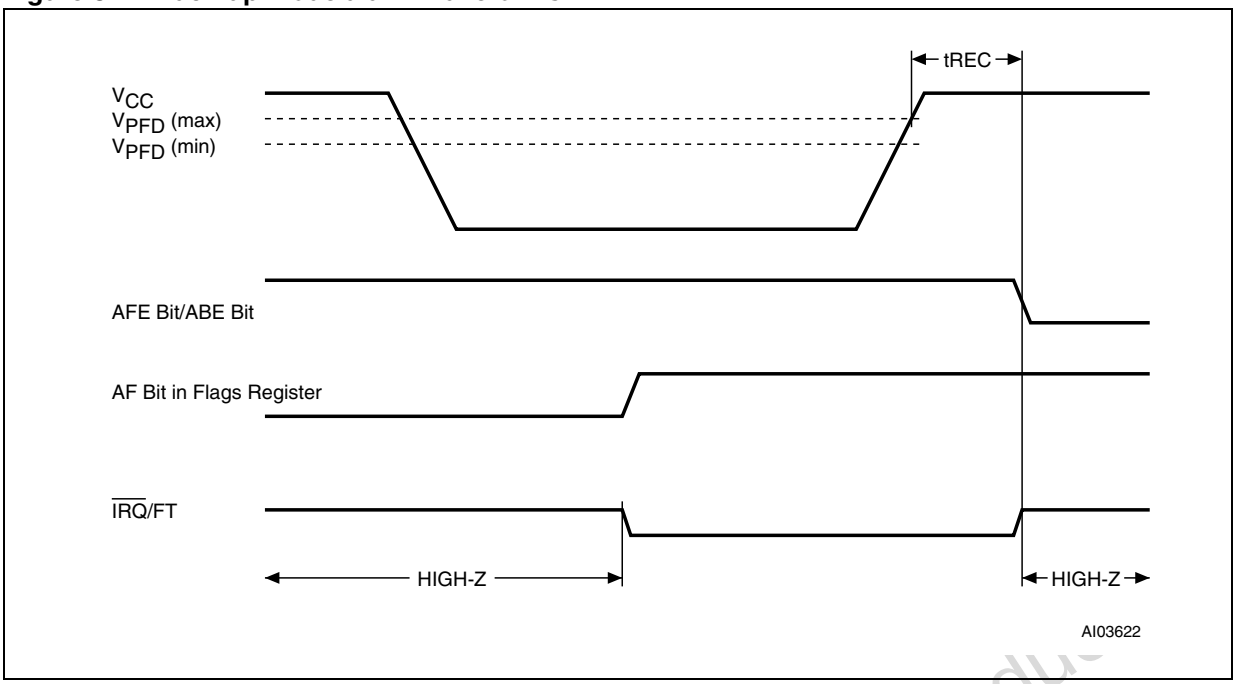


Table 8. Alarm repeat modes

RPT5	RPT4	RPT3	RPT2	RPT1	Alarm setting
1	1	1	1	1	Once per second
1	1	1	1	0	Once per minute
1	1	1	0	0	Once per hour
1	1	0	0	0	Once per day
1	0	0	0	0	Once per month
0	0	0	0	0	Once per year

Figure 8. Back-up mode alarm waveforms



3.6 Watchdog timer

The watchdog timer can be used to detect an out-of-control microprocessor. The user programs the watchdog timer by setting the desired amount of time-out into the Watchdog Register, address 7h.

Bits BMB4-BMB0 store a binary multiplier and the two lower-order bits RB1-RB0 select the resolution, where 00=1/16 second, 01=1/4 second, 10=1 second, and 11=4 seconds. The amount of time-out is then determined to be the multiplication of the five-bit multiplier value with the resolution. (For example: writing 00001110 in the Watchdog Register = 3*1 or 3 seconds).

Note: Accuracy of timer is within ± the selected resolution.

If the processor does not reset the timer within the specified period, the M48T212V sets the WDF (Watchdog Flag) and generates a watchdog interrupt or a microprocessor reset. WDF is reset by reading the Flags Register (Address 0h).

The most significant bit of the Watchdog Register is the Watchdog Steering Bit (WDS). When set to a '0.' the watchdog will activate the $\overline{IRQ}$/FT pin when timed-out. When WDS is set to a '1,' the watchdog will output a negative pulse on the $\overline{RST}$ pin for 40 to 200 ms. The Watchdog register, AFE, ABE, and FT Bits will reset to a '0' at the end of a Watchdog time-out when the WDS Bit is set to a '1.'

The watchdog timer can be reset by two methods:

1. a transition (high-to-low or low-to-high) can be applied to the Watchdog Input pin (WDI) or
2. the microprocessor can perform a WRITE of the Watchdog Register.

The time-out period then starts over. The WDI pin should be tied to V_{SS} if not used. The watchdog will be reset on each transition (edge) seen by the WDI pin. In the order to

perform a software reset of the watchdog timer, the original time-out period can be written into the Watchdog Register, effectively restarting the count-down cycle.

Should the watchdog timer time-out, and the WDS Bit is programmed to output an interrupt, a value of 00h needs to be written to the Watchdog Register in order to clear the $\overline{IRQ}$/FT pin. This will also disable the watchdog function until it is again programmed correctly. A READ of the Flags Register will reset the Watchdog Flag (Bit D7; Register 0h).

The watchdog function is automatically disabled upon power-down and the Watchdog Register is cleared. If the watchdog function is set to output to the $\overline{IRQ}$/FT pin and the frequency test function is activated, the watchdog or alarm function prevails and the frequency test function is denied.

3.7 V_{CC} switch output

$\overline{Vccsw}$ output goes low when V_{OUT} switches to V_{CC} turning on a customer supplied P-Channel MOSFET (see *Figure 3 on page 8*). The Motorola MTD20P06HDL is recommended. This MOSFET in turn connects V_{OUT} to a separate supply when the current requirement is greater than I_{OUT1} (see *Table 14 on page 28*). This output may also be used simply to indicate the status of the internal battery switchover comparator, which controls the source (V_{CC} or battery) of the V_{OUT} output.

3.8 Power-on reset

The M48T212V continuously monitors V_{CC}. When V_{CC} falls to the power fail detect trip point, the $\overline{RST}$ pulls low (open drain) and remains low on power-up for t_{rec} after V_{CC} passes V_{PFD} (max). The $\overline{RST}$ pin is an open drain output and an appropriate pull-up resistor to V_{CC} should be chosen to control rise time.

Note: If the $\overline{RST}$ output is fed back into either of the $\overline{RSTIN}$ inputs (for a microprocessor with a bi-directional reset) then a 1kΩ (max) pull-up resistor is recommended.

3.9 Reset inputs ($\overline{RSTIN1}$ & $\overline{RSTIN2}$)

The M48T212V provides two independent inputs which can generate an output reset. The duration and function of these resets is identical to a reset generated by a power cycle. *Table 9* and *Figure 9* illustrate the AC reset characteristics of this function. During the time $\overline{RST}$ is enabled (t_{R1HRH} & t_{R2HRH}), the Reset Inputs are ignored.

Note: $\overline{RSTIN1}$ and $\overline{RSTIN2}$ are each internally pulled up to V_{CC} through a 100KΩ resistor.

Figure 9. ($\overline{\text{RSTIN1}}$ & $\overline{\text{RSTIN2}}$) timing waveforms

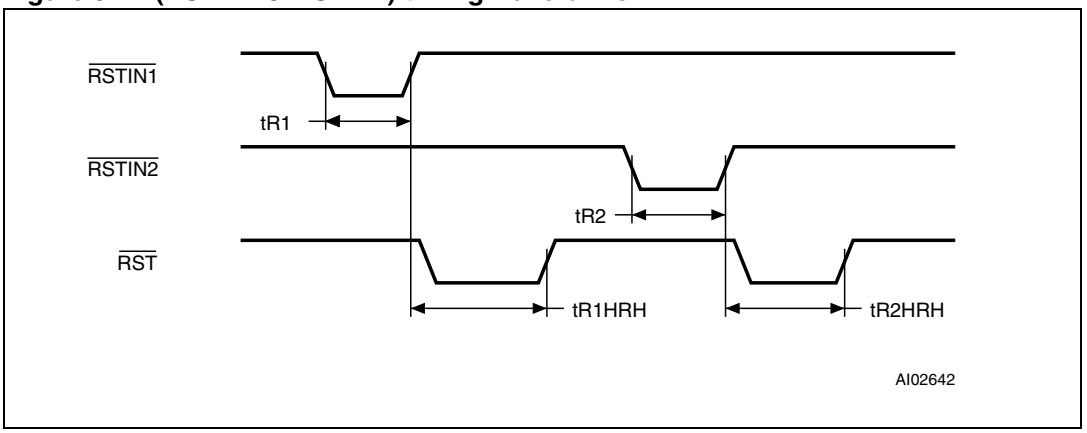


Table 9. Reset AC characteristics

Symbol	Parameter(1)	Min	Max	Unit
t_{R1}(2)	$\overline{\text{RSTIN1}}$ low to $\overline{\text{RSTIN1}}$ high	200		ns
t_{R2}(3)	$\overline{\text{RSTIN2}}$ low to $\overline{\text{RSTIN2}}$ high	100		ms
t_{R1HRH}(4)	$\overline{\text{RSTIN1}}$ high to $\overline{\text{RST}}$ high	40	200	ms
t_{R2HRH}(4)	$\overline{\text{RSTIN2}}$ high to $\overline{\text{RST}}$ high	40	200	ms

1. Valid for ambient operating temperature: T_A = 0 to 70°C or –40 to 85°C; V_{CC} = 4.5 to 5.5V or 3.0 to 3.6V (except where noted).
2. Pulse width less than 50ns will result in no $\overline{\text{RESET}}$ (for noise immunity).
3. Pulse width less than 20ms will result in no $\overline{\text{RESET}}$ (for noise immunity).
4. C_L = 5pF (see *Figure 13 on page 27*).

3.10 Calibrating the clock

The M48T212V is driven by a quartz controlled oscillator with a nominal frequency of 32,768 Hz. The devices are tested not to exceed ±35 ppm (parts per million) oscillator frequency error at 25°C, which equates to about ±1.53 minutes per month (see *Figure 10 on page 24*). When the Calibration circuit is properly employed, accuracy improves to better than +1/–2 ppm at 25°C.

The oscillation rate of crystals changes with temperature. The M48T212V design employs periodic counter correction. The calibration circuit adds or subtracts counts from the oscillator divider circuit at the divide by 256 stage, as shown in *Figure 11 on page 25*. The number of times pulses which are blanked (subtracted, negative calibration) or split (added, positive calibration) depends upon the value loaded into the five Calibration bits found in the Control Register. Adding counts speeds the clock up, subtracting counts slows the clock down.

The Calibration bits occupy the five lower-order bits (D4-D0) in the Control Register 8h. These bits can be set to represent any value between 0 and 31 in binary form. Bit D5 is a Sign Bit; '1' indicates positive calibration, '0' indicates negative calibration. Calibration occurs within a 64 minute cycle. The first 62 minutes in the cycle may, once per minute, have one second either shortened by 128 or lengthened by 256 oscillator cycles.

If a binary '1' is loaded into the register, only the first 2 minutes in the 64 minute cycle will be modified; if a binary 6 is loaded, the first 12 will be affected, and so on.

Therefore, each calibration step has the effect of adding 512 or subtracting 256 oscillator cycles for every 125,829,120 actual oscillator cycles, that is +4.068 or –2.034 ppm of adjustment per calibration step in the calibration register. Assuming that the oscillator is running at exactly 32,768 Hz, each of the 31 increments in the Calibration byte would represent +10.7 or –5.35 seconds per month which corresponds to a total range of +5.5 or –2.75 minutes per month.

Two methods are available for ascertaining how much calibration a given M48T212Y/V may require. The first involves setting the clock, letting it run for a month and comparing it to a known accurate reference and recording deviation over a fixed period of time. Calibration values, including the number of seconds lost or gained in a given period, can be found in Application Note, “AN934, TIMEKEEPER® Calibration.”

This allows the designer to give the end user the ability to calibrate the clock as the environment requires, even if the final product is packaged in a non-user serviceable enclosure. The designer could provide a simple utility that accesses the Calibration byte.

The second approach is better suited to a manufacturing environment, and involves the use of the $\overline{IRQ}$/FT pin. The pin will toggle at 512Hz, when the Stop Bit (ST, D7 of 9h) is '0,' the Frequency Test Bit (FT, D6 of Ch) is '1,' the Alarm Flag Enable Bit (AFE, D7 of 6h) is '0,' and the Watchdog Steering Bit (WDS, D7 of 7h) is '1' or the Watchdog Register (7h=0) is reset.

Any deviation from 512 Hz indicates the degree and direction of oscillator frequency shift at the test temperature. For example, a reading of 512.010124 Hz would indicate a +20 ppm oscillator frequency error, requiring a –10 (WR001010) to be loaded into the Calibration Byte for correction. Note that setting or changing the Calibration Byte does not affect the Frequency test output frequency.

The $\overline{IRQ}$/FT pin is an open drain output which requires a pull-up resistor to V_{CC} for proper operation. A 500-10kΩ resistor is recommended in order to control the rise time. The FT Bit is cleared on power-up.

3.11 Battery low warning

The M48T212V automatically performs battery voltage monitoring upon power-up and at factory-programmed time intervals of approximately 24 hours. The Battery Low (BL) Bit, Bit D4 of Flags Register 0h, will be asserted if the battery voltage is found to be less than approximately 2.5V. The BL Bit will remain asserted until completion of battery replacement and subsequent battery low monitoring tests, either during the next power-up sequence or the next scheduled 24-hour interval.

If a battery low is generated during a power-up sequence, this indicates that the battery is below approximately 2.5 volts and may not be able to maintain data integrity in the SRAM. Data should be considered suspect and verified as correct. A fresh battery should be installed.

If a battery low indication is generated during the 24-hour interval check, this indicates that the battery is near end of life. However, data is not compromised due to the fact that a nominal V_{CC} is supplied. In order to ensure data integrity during subsequent periods of battery back-up mode, the battery should be replaced. The SNAPHAT® battery/crystal top should be replaced with V_{CC} powering the device to avoid data loss.

Note: This will cause the clock to lose time during the time interval the battery crystal is removed.

The M48T212V only monitors the battery when a nominal V_{CC} is applied to the device. Thus applications which require extensive durations in the battery back-up mode should be

powered-up periodically (at least once every few months) in order for this technique to be beneficial.

Additionally, if a battery low is indicated, data integrity should be verified upon power-up via a checksum or other technique.

3.12 Initial power-on defaults

Upon application of power to the device, the following register bits are set to a '0' state: WDS, BMB0-BMB4, RB0-RB1, AFE, ABE, W, and FT (see *Table 10*).

Table 10. Default values

Condition	W	R	FT	AFE	ABE	Watchdog register(1)
Initial power-up (Battery attach for SNAPHAT)(2)	0	0	0	0	0	0
RESET (3)	0	0	0	0	0	0
Power-down (4)	0	1	0	1	1	0
Subsequent power-up	0	1	0	0	0	0

1. WDS, BMB0-BMB4, RB0, RB1.
2. State of other control bits undefined.
3. State of other control bits remains unchanged.
4. Assuming these bits set to '1' prior to power-down.

Figure 10. Crystal accuracy across temperature

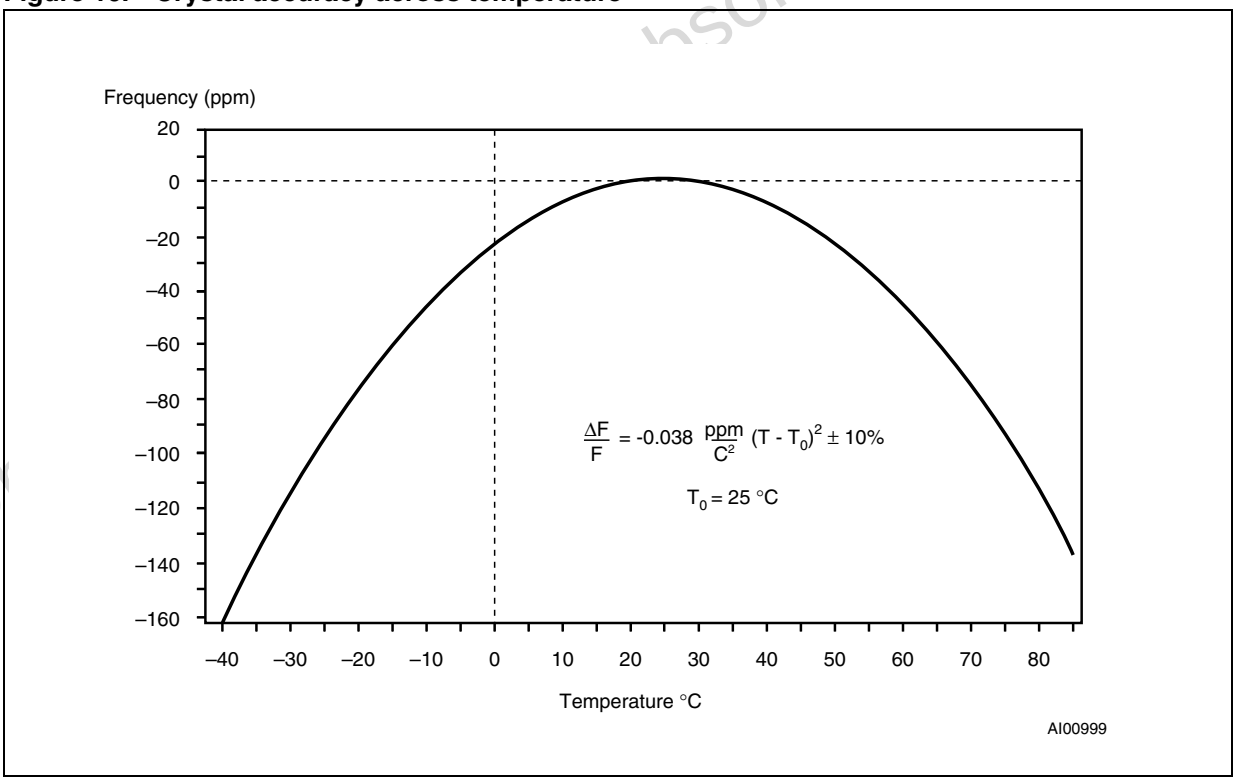
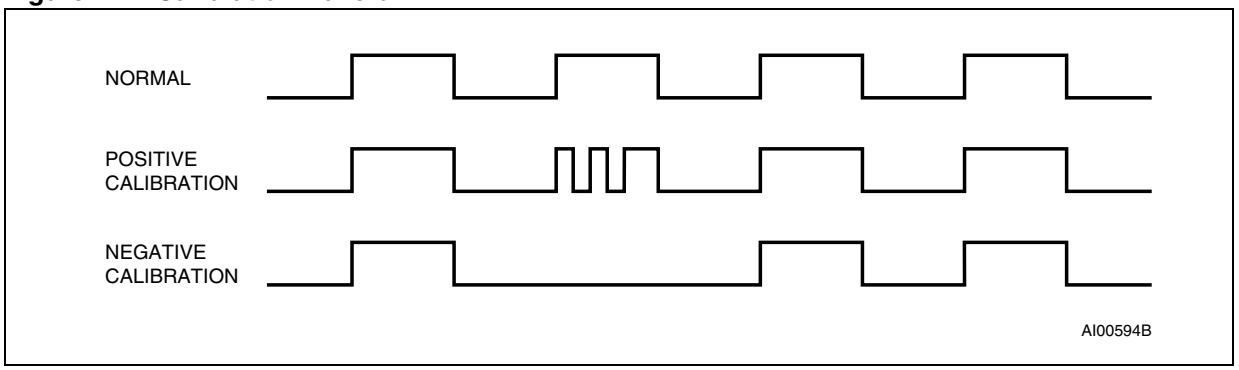


Figure 11. Calibration waveform



3.13 V_{CC} noise and negative going transients

I_{CC} transients, including those produced by output switching, can produce voltage fluctuations, resulting in spikes on the V_{CC} bus. These transients can be reduced if capacitors are used to store energy which stabilizes the V_{CC} bus. The energy stored in the bypass capacitors will be released as low going spikes are generated or energy will be absorbed when overshoots occur. A ceramic bypass capacitor value of 0.1µF (as shown in *Figure 12*) is recommended in order to provide the needed filtering.

In addition to transients that are caused by normal SRAM operation, power cycling can generate negative voltage spikes on V_{CC} that drive it to values below V_{SS} by as much as one volt. These negative spikes can cause data corruption in the SRAM while in battery backup mode. To protect from these voltage spikes, STMicroelectronics recommends connecting a Schottky diode from V_{CC} to V_{SS} (cathode connected to V_{CC}, anode to V_{SS}). Schottky diode 1N5817 is recommended for through hole and MBRS120T3 is recommended for surface mount.

Figure 12. Supply voltage protection