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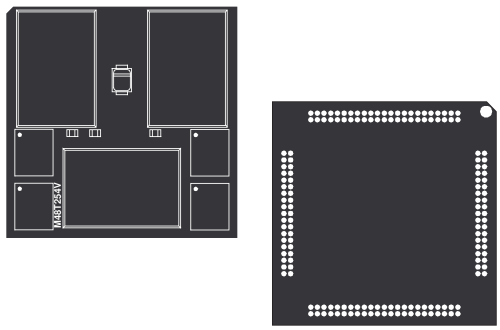
M48T254V

3.3V, 16 Mbit (2 Mb x 8 bit) TIMEKEEPER®
SRAM WITH PHANTOM CLOCK

FEATURES SUMMARY

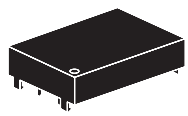
- 3.3V ± 10%
- INTEGRATED ULTRA LOW POWER SRAM, REAL TIME CLOCK, POWER-FAIL CONTROL CIRCUIT, BATTERY AND CRYSTAL
- REAL TIME CLOCK KEEPS TRACK OF TENTHS/HUNDREDTHS OF SECONDS, SECONDS, MINUTES, HOURS, DAYS, DATE, MONTHS, and YEARS.
- CLOCK FUNCTION IS TRANSPARENT TO RAM OPERATION.
- PRECISION POWER MONITORING and POWER SWITCHING CIRCUITRY
- AUTOMATIC WRITE-PROTECTION WHEN V_{CC} IS OUT-OF-TOLERANCE
- POWER-FAIL DESELECT VOLTAGE:
  - V_{CC} = 3.3V ± 10%; 2.8V ≤ V_{PFD} ≤ 2.97V
- BATTERY LOW ($\overline{BL}$)
- 10 YEARS of DATA RETENTION and CLOCK OPERATION IN THE ABSENCE OF POWER
- SNAPHAT HOUSING (BATTERY/CRYSTAL) IS REPLACEABLE
- 100ns ACCESS (READ = WRITE)

Figure 1. 168-ball PBGA Module



168-ball PBGA
Module (ZA)

Figure 2. SNAPHAT Crystal/Battery



SNAPHAT (SH)
Crystal/Battery

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SUMMARY DESCRIPTION

The M48T254V TIMEKEEPER® RAM is a 2Mbit x 8 non-volatile static RAM and real time clock organized as 2,097,152 words by 8 bits. The special BGA package provides a fully integrated battery back-up memory and real time clock solution. In the event of power instability or absence, a self-contained battery maintains the timekeeping operation and provides power for a CMOS static RAM. Control circuitry monitors V_{CC} and invokes write protection to prevent data corruption in the memory and RTC.

The clock keeps track of tenths/hundredths of seconds, seconds, minutes, hours, day, date, month, and year information. The last day of the month is automatically adjusted for months with less than 31 days, including leap year correction.

The clock operates in one of two formats:

– a 12-hour mode with an AM/PM indicator; or

– a 24-hour mode

The M48T254V is a 168-ball PBGA module that integrates the RTC, the battery, and SRAM in one package.

Figure 3. Logic Diagram

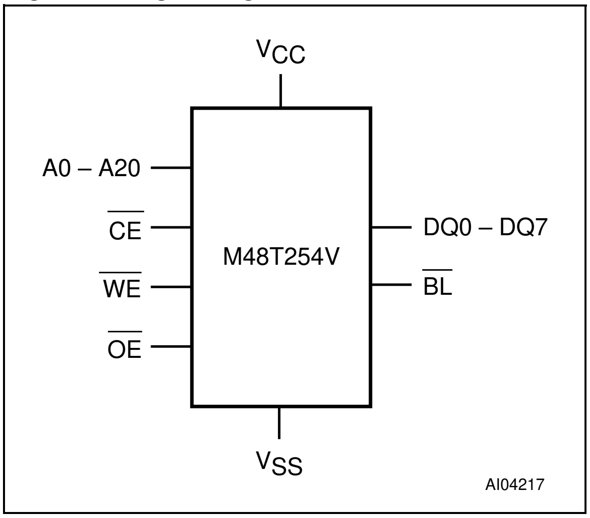
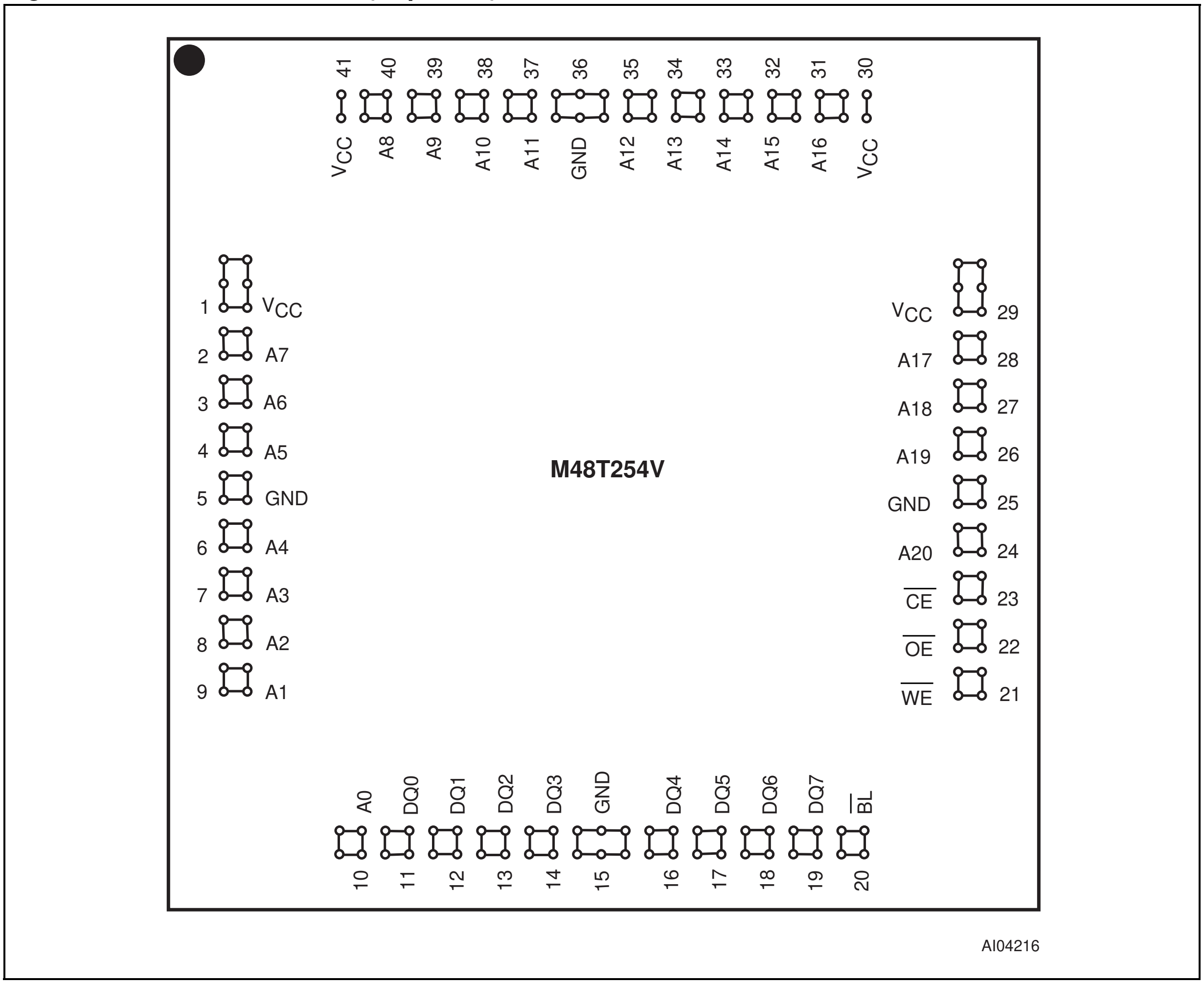


Table 1. Signal Names

A0 - A20	Address Inputs
DQ0 - DQ7	Data Input/Output
$\overline{CE}$	Chip Enable
$\overline{WE}$	WRITE Enable Inputs
$\overline{OE}$	Output Enable
$\overline{BL}$	Battery Low Output (Open Drain)
NC	No Connect
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 4. PBGA Connections (Top View)



Note: This diagram is TOP VIEW perspective (view through package).

Figure 5. Hardware Hookup

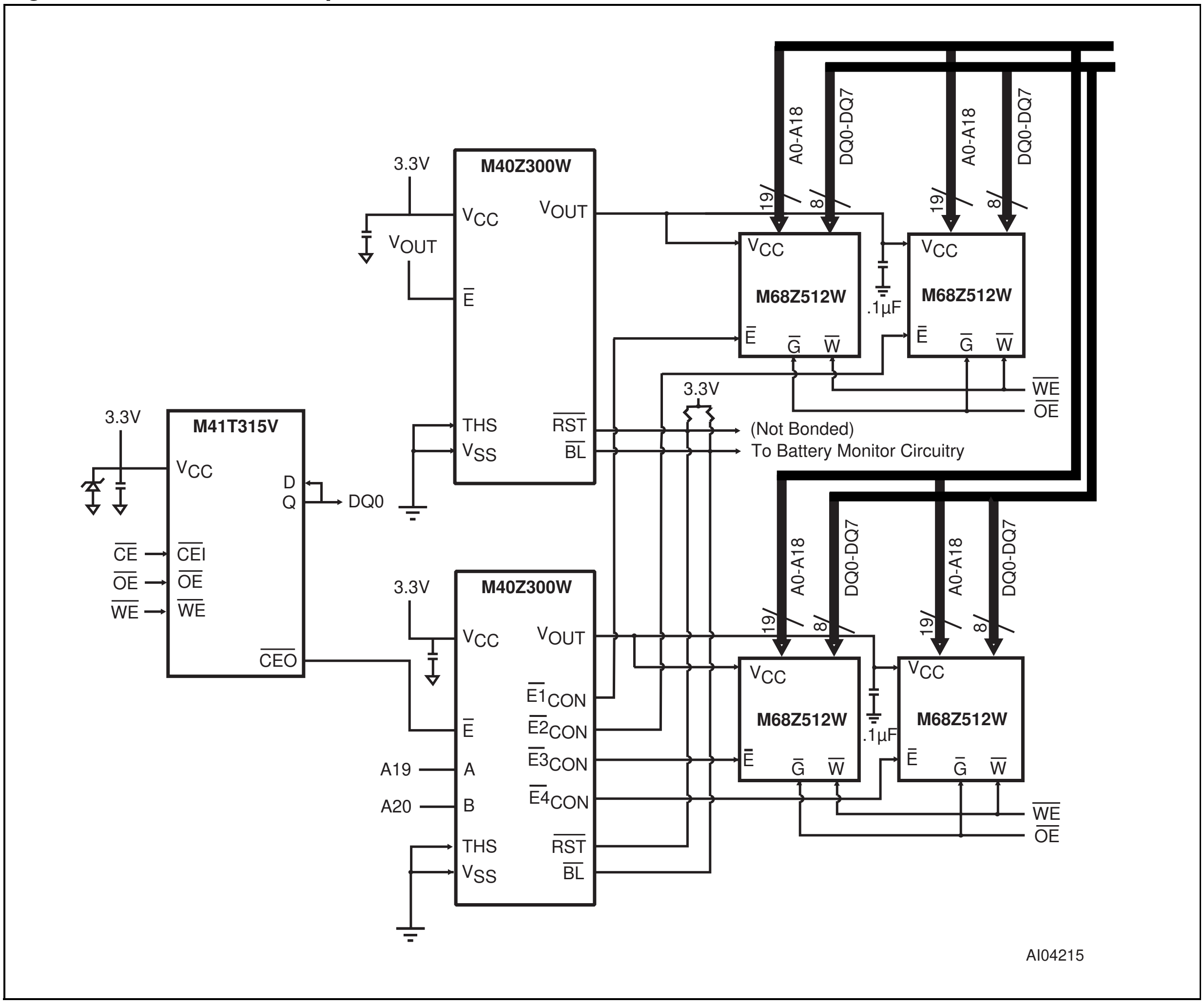
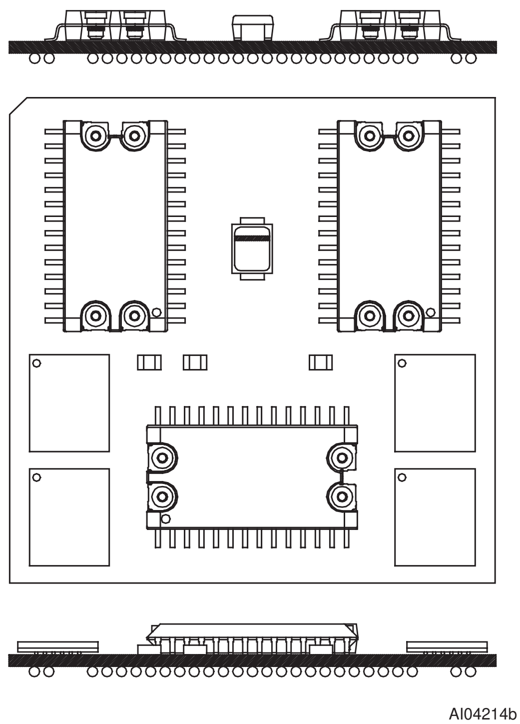


Figure 6. M48T254V PBGA Module Solution (Side/Top)



MAXIMUM RATING

Stressing the device above the rating listed in the "Absolute Maximum Ratings" table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_A	Operating Temperature	0 to 70	°C
T_{STG}	Storage Temperature (V_{CC}, Oscillator Off)	–40 to 85	°C
T_{SLD}	Lead Solder Temperature for 10 seconds	260	°C
V_{CC}	Supply Voltage (on any pin relative to Ground)	–0.3 to +4.6	V
V_{IO}	Input or Output Voltages	–0.3 to V_{CC} + 0.3	V
I_O	Output Current	20	mA
P_D	Power Dissipation	1	W

CAUTION! *Negative undershoots below –0.3V are not allowed on any pin while in the Battery Back-up Mode.*

DC AND AC PARAMETERS

This section summarizes the operating and measurement conditions, as well as the DC and AC characteristics of the device. The parameters in the following DC and AC Characteristic tables are derived from tests performed under the Measurement Conditions listed in the relevant tables. Designers should check that the operating conditions in their projects match the measurement conditions when using the quoted parameters.

Table 3. DC and AC Measurement Conditions

Parameter	M41T254V
V_{CC} Supply Voltage	3.0 to 3.6V
Ambient Operating Temperature	0 to 70°C
Load Capacitance (C_L)	50pF
Input Rise and Fall Times	≤ 5ns
Input Pulse Voltages	0 to 3V
Input and Output Timing Ref. Voltages	1.5V

Note: Output Hi-Z is defined as the point where data is no longer driven.

Figure 7. AC Testing Load Circuit

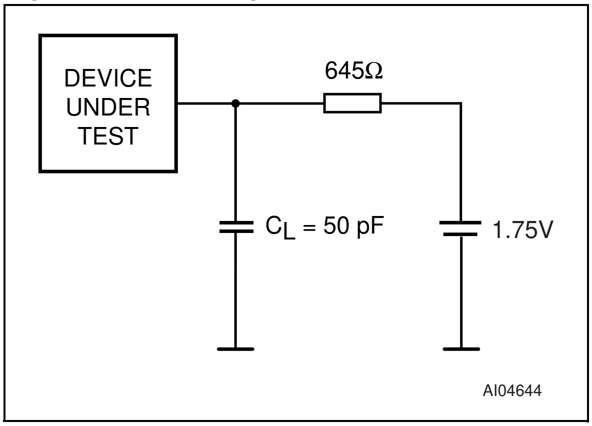


Table 4. Capacitance

Symbol	Parameter[1,2]	Min	Max	Unit
C_{IN}	Input Capacitance (A0-A18, $\overline{OE}$, $\overline{WE}$, $\overline{CE}$)		40	pF
	Input Capacitance (A19-A20)		10	pF
C_{OUT}	Output Capacitance ($\overline{BL}$)		20	pF
C_{IO}[3]	Input / Output Capacitance		40	pF

Note: 1. Effective capacitance measured with power supply at 3V. Sampled only; not 100% tested.
2. At 25°C, f = 1MHz.
3. Outputs were deselected.

Table 5. DC Characteristics

Sym	Parameter	Test Condition[1]	M48T254V			Unit
			Min	Typ	Max	
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$			±4	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$			±4	µA
I_{CC1}	Supply Current				50	mA
I_{CC2}	Supply Current (TTL Standby)	$\overline{CE} = V_{IH}$		5	7	mA
I_{CC3}	V_{CC} Power Supply Current	$\overline{CE} = V_{CCI} - 0.2$		2	3	mA
V_{IL}[2]	Input Low Voltage		–0.3		0.6	V
V_{IH}[2]	Input High Voltage		2.2		$V_{CC} + 0.3$	V
V_{OL}[3]	Output Low Voltage (Open Drain)	$I_{OL} = 10mA$			0.4	V
	Output Low Voltage	$I_{OL} = 2.0mA$			0.4	V
V_{OH}	Output High Voltage	$I_{OH} = -1.0mA$	2.4			V
V_{PFD}[2]	Power Fail Deselect		2.80		2.97	V
V_{SO}[2]	Battery Back-up Switchover			2.5		V

Note: 1. Valid for Ambient Operating Temperature: T_A = 0 to 70°C; V_{CC} = 3.0 to 3.6V (except where noted).
2. All voltages are referenced to Ground.
3. For $\overline{BL}$ pin (Open Drain).

OPERATION MODES

READ

A READ cycle executes whenever WRITE Enable ($\overline{WE}$) is high and Chip Enable ($\overline{CE}$) is low (see Figure 8, page 10). The distinct address defined by the 21 address inputs (A0-A20) specifies which of the 2M bytes of data is to be accessed. Valid data will be accessed by the eight data output drivers within the specified Access Time (t_{ACC}) after the last address input signal is stable, the $\overline{CE}$ and $\overline{OE}$ access times, and their respective parameters are satisfied. When $\overline{CE}$ t_{ACC} and $\overline{OE}$ t_{ACC} are not satisfied, then data access times must be measured from the more recent $\overline{CE}$ and $\overline{OE}$ signals, with the limiting parameter being t_{CO} (for $\overline{CE}$) or t_{OE} (for $\overline{OE}$) instead of address access.

WRITE

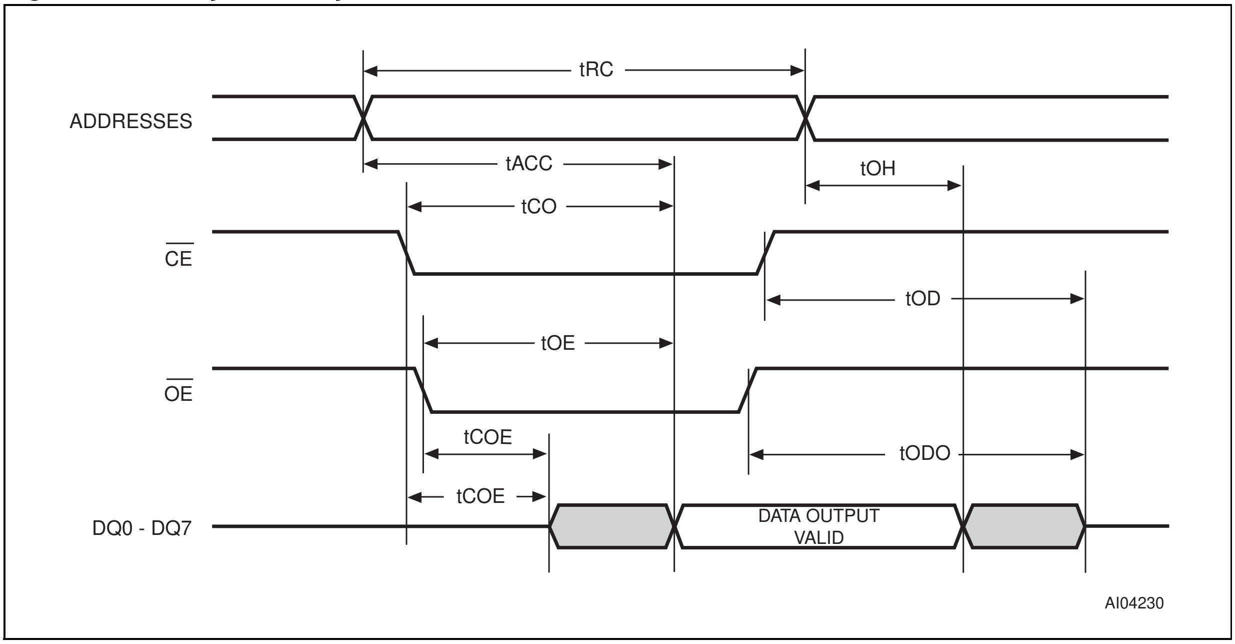
WRITE Mode occurs whenever $\overline{CE}$ and $\overline{WE}$ signals are low (after address inputs are stable, see Figure 9, page 10 and Figure 10, page 11). The most recent falling edge of $\overline{CE}$ and $\overline{WE}$ will determine when the WRITE cycle begins (the earlier, rising edge of $\overline{CE}$ or $\overline{WE}$ determines cycle termination). All address inputs must be kept stable throughout the WRITE cycle. $\overline{WE}$ must be high (inactive) for a minimum recovery time (t_{WR}) before a subsequent cycle is initiated. The $\overline{OE}$ control signal should be kept high (inactive) during the WRITE cycles to avoid bus contention. If $\overline{CE}$ and $\overline{OE}$ are low (active), $\overline{WE}$ will disable the outputs for Output Data WRITE Time (t_{ODW}) from its falling edge.

Table 6. Operating Modes

Mode	V_{CC}	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	DQ7-DQ0	Power
Deselect	3.0V to 3.6V	V_{IH}	X	X	High-Z	Standby
WRITE		V_{IL}	X	V_{IL}	D_{IN}	Active
READ		V_{IL}	V_{IL}	V_{IH}	D_{OUT}	Active
READ		V_{IL}	V_{IH}	V_{IH}	High-Z	Active
Deselect	V_{SO} to V_{PFD} (min)[1]	X	X	X	High-Z	CMOS Standby
Deselect	$\leq V_{SO}$[1]	X	X	X	High-Z	Battery Back-Up

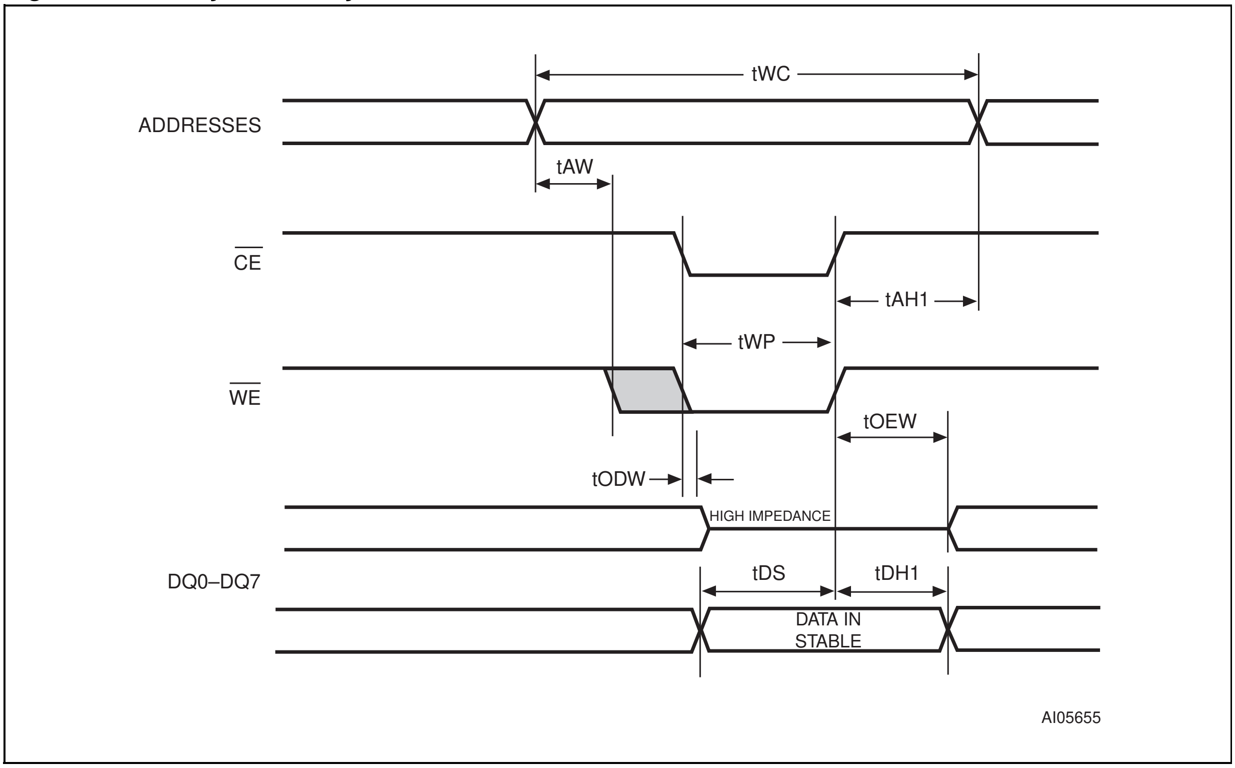
Note: X = V_{IH} or V_{IL}; V_{SO} = Battery Back-up Switchover Voltage
1. See Table 8, page 13 for details.

Figure 8. Memory READ Cycle



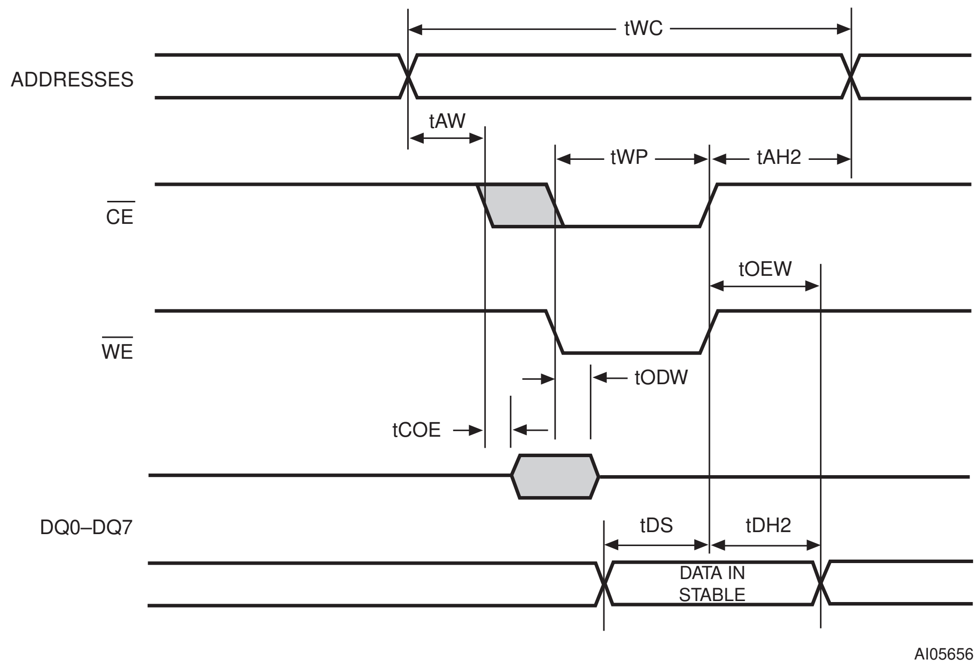
Note: $\overline{WE}$ is high for a READ cycle.

Figure 9. Memory WRITE Cycle, WRITE Enable Controlled



Note: 1. $\overline{OE} = V_{IH}$ or V_{IL}. If $\overline{OE} = V_{IH}$ during a WRITE cycle, the output buffers remain in a high impedance state.
2. If the $\overline{CE}$ low transition occurs simultaneously with or later than the $\overline{WE}$ low transition in $\overline{WE}$ Controlled WRITE, the output buffers remain in a high impedance state during this period.
3. If the $\overline{CE}$ high transition occurs simultaneously with the $\overline{WE}$ high transition, the output buffers remain in a high impedance state during this period.

Figure 10. Memory WRITE Cycle, Chip Enable Controlled



Note: 1. $\overline{OE}$ = V_{IH} or V_{IL}. If $\overline{OE}$ = V_{IH} during a WRITE cycle, the output buffers remain in a high impedance state.
2. If $\overline{WE}$ is low or the $\overline{WE}$ low transition occurs prior to or simultaneously with the $\overline{CE}$ low transition, the output buffers remain in a high impedance state during this period.

Table 7. AC Electrical Characteristics

Symbol		Parameter[1]	M48T254V		Unit
			Min	Max	
t_{AVAV}	t_{RC}	READ Cycle Time	100		ns
t_{AVQV}	t_{ACC}	Access Time		100	ns
t_{ELQV}	t_{CO}	Chip Enable Low to Output Valid		100	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid		55	ns
t_{ELQX}	t_{COE}[2]	Chip Enable or Output Enable Low to Output Transition	5		ns
t_{AXQX}	t_{OH}	Output Hold from Address Change	5		ns
t_{EHQZ}	t_{OD}[2]	Chip Enable High to Output Hi-Z		35	ns
t_{GHQZ}	t_{ODO}[2]	Output Enable High to Output Hi-Z		35	ns
t_{WLQZ}	t_{ODW}[2]	Output Hi-Z from $\overline{WE}$		35	ns
t_{AVAV}	t_{WC}	WRITE Cycle Time	100		ns
t_{WLWH} t_{ELEH}	t_{WP}[3]	$\overline{WE}$, $\overline{CE}$ Pulse Width	70		ns
t_{AVEL}	t_{AW}	Address Setup Time	0		ns
t_{WHAX}	t_{AH1}	Address Hold Time from $\overline{WE}$	5		ns
t_{EHAX}	t_{AH2}	Address Hold Time from $\overline{CE}$	25		ns
t_{WHQX}	t_{OEW}[2]	Output Active from $\overline{WE}$	5		ns
t_{DVEH} t_{DVWH}	t_{DS}	Data Setup Time	40		ns
t_{WHDX}	t_{DH1}	Data Hold Time from $\overline{WE}$	0		ns
t_{EHDX}	t_{DH2}	Data Hold Time from $\overline{CE}$	20		ns
	t_{RR}	READ Recovery (Clock Access Only)	20		ns
	t_{WR}[4]	WRITE Recovery (Clock Access Only)	20		ns

Note: 1. Valid for Ambient Operating Temperature: T_A = 0 to 70°C; V_{CC} = 3.0 to 3.6V (except where noted).
2. These parameters are sampled with a 5 pF load are not 100% tested.
3. t_{WP} is specified as the logical AND of $\overline{CE}$ and $\overline{WE}$. t_{WP} is measured from the latter of $\overline{CE}$ or $\overline{WE}$ going low to the earlier of $\overline{CE}$ or $\overline{WE}$ going high.
4. t_{WR} is a function of the latter occurring edge of $\overline{WE}$ or $\overline{CE}$.

Data Retention Mode

Data can be read or written only when V_{CC} is greater than V_{PFD}. When V_{CC} is below V_{PFD} (the point at which write protection occurs), the clock registers and the SRAM are blocked from any access. When V_{CC} falls below the Battery Switch Over threshold (V_{SO}), the device is switched from V_{CC} to battery backup (V_{BAT}). RTC operation and SRAM data are maintained via battery backup until power is stable. All control, data, and address signals must be powered down when V_{CC} is powered down.

The lithium power source is designed to provide power for RTC activity as well as RTC and RAM data retention when V_{CC} is absent or unstable. The capability of this source is sufficient to power the device continuously for the life of the equipment into which it has been installed. For specification purposes, life expectancy is ten (10) years at 25°C with the internal oscillator running without V_{CC}. The actual life expectancy will be much longer if no battery energy is used (e.g., when V_{CC} is present).

Figure 11. Power Down/Up Mode AC Waveforms

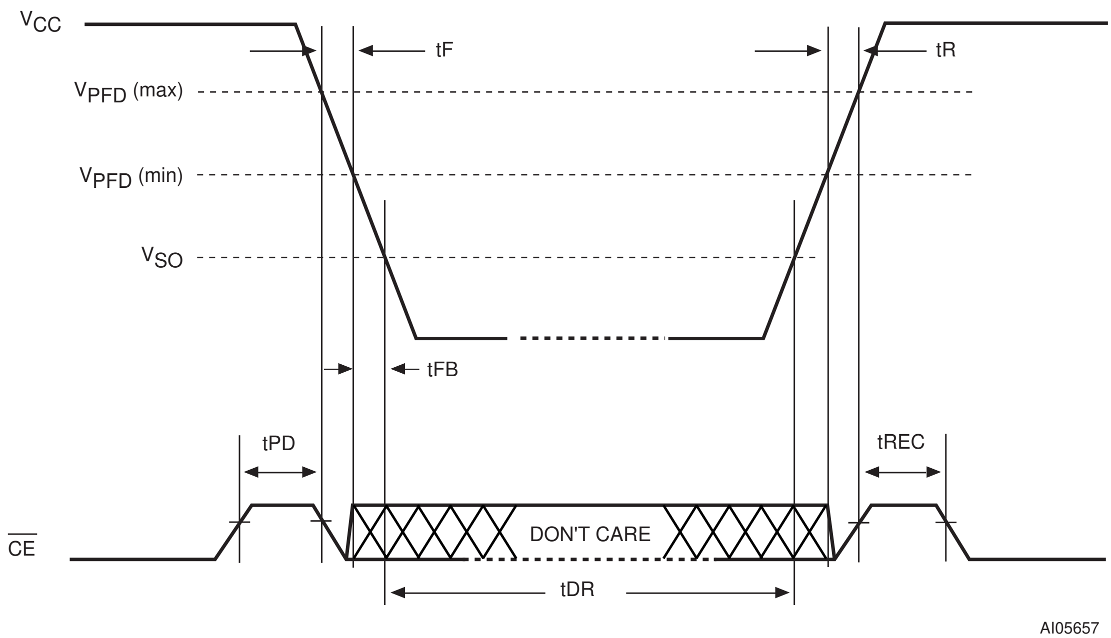


Table 8. Power Down/Up Trip Points DC Characteristics

Symbol	Parameter(1)	Min	Max	Unit
t_{REC}	V_{PFD} (max) to $\overline{CE}$ low	40	120	ms
t_F	V_{PFD} (max) to V_{PFD} (min) V_{CC} Fall Time	300		µs
t_{FB}	V_{PFD} (min) to V_{SO} V_{CC} Fall Time	10		µs
t_R	V_{PFD} (min) to V_{PFD} (max) V_{CC} Rise Time	0		µs
t_{PD}	$\overline{CE}$ High to Power-Fail	0		µs
t_{DR}(2)	Expected Data Retention Time	10		Years

Note: 1. Valid for Ambient Operating Temperature: T_A = 0 to 70°C; V_{CC} = 3.0 to 3.6V (except where noted).
2. At 25°C, V_{CC} = 0V; the expected t_{DR} is defined as cumulative time in the absence of V_{CC} with the clock oscillator running. (Requires use of three M4T32-BR12SH SNAPHAT® tops.)

PHANTOM CLOCK OPERATION

Communication with the Phantom Clock is established by pattern recognition of a serial bit-stream of 64 bits which must be matched by executing 64 consecutive WRITE cycles containing the proper data on DQ0.

All accesses which occur prior to recognition of the 64-bit pattern are directed to memory.

After recognition is established, the next 64 READ or WRITE cycles either extract or update data in the clock while disabling the memory.

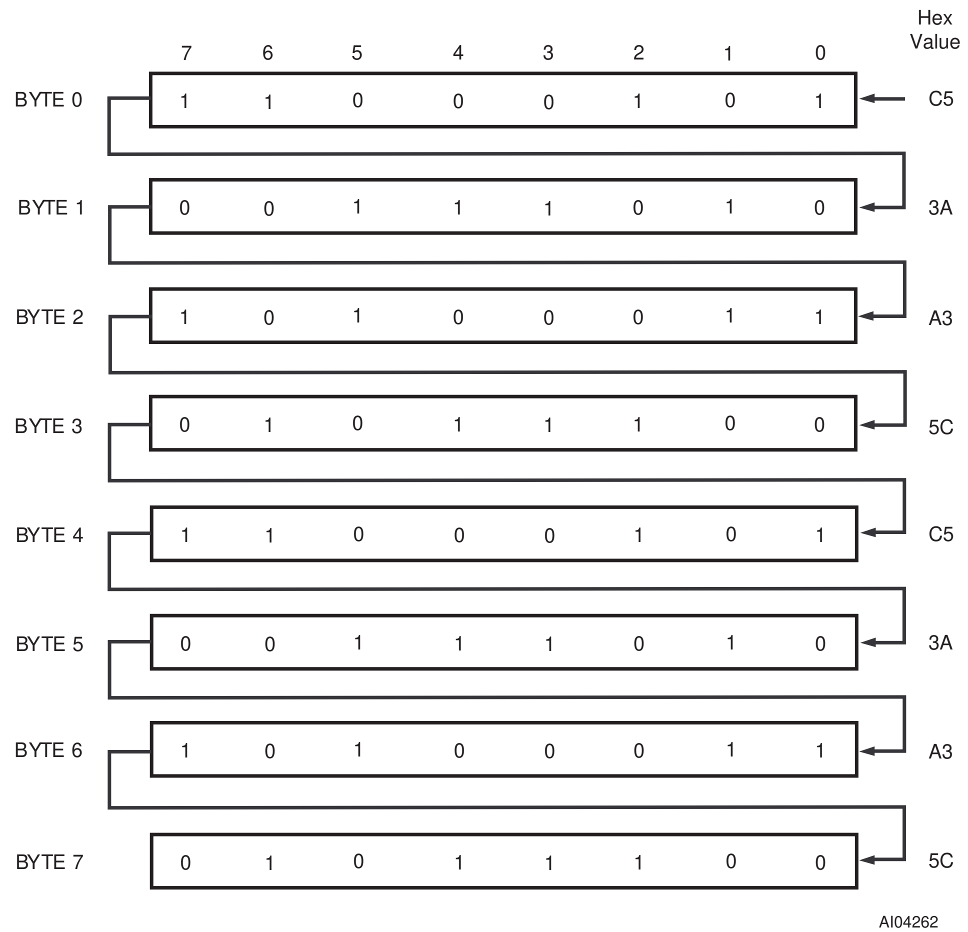
Data transfer to and from the timekeeping function is accomplished with a serial bit-stream under control of Chip Enable ($\overline{CE}$), Output Enable ($\overline{OE}$), and WRITE Enable ($\overline{WE}$). Initially, a READ cycle using the $\overline{CE}$ and $\overline{OE}$ control of the clock starts the pattern recognition sequence by moving the pointer to the first bit of the 64-bit comparison register (see Figure 12, page 15).

Next, 64 consecutive WRITE cycles are executed using the $\overline{CE}$ and $\overline{WE}$ control of the device. These 64 WRITE cycles are used only to gain access to the clock. Therefore, any address to the memory is acceptable. However, the WRITE cycles generated to gain access to the Phantom Clock are also writing data to a location in the mated RAM. The preferred way to manage this requirement is to set aside just one address location in RAM as a Phantom Clock scratch pad.

When the first WRITE cycle is executed, it is compared to Bit 1 of the 64-bit comparison register. If a match is found, the pointer increments to the next location of the comparison register and awaits the next WRITE cycle.

If a match is not found, the pointer does not advance and all subsequent WRITE cycles are ignored. If a READ cycle occurs at any time during pattern recognition, the present sequence is aborted and the comparison register pointer is reset. Pattern recognition continues for a total of 64 WRITE cycles as described above until all of the bits in the comparison register have been matched. With a correct match for 64-bits, the Phantom Clock is enabled and data transfer to or from the timekeeping registers can proceed. The next 64 cycles will cause the Phantom Clock to either receive or transmit data on DQ0, depending on the level of the $\overline{OE}$ pin or the $\overline{WE}$ pin. Cycles to other locations outside the memory block can be interleaved with $\overline{CE}$ cycles without interrupting the pattern recognition sequence or data transfer sequence to the Phantom Clock.

Figure 12. Comparison Register Definition



Note: The odds of this pattern being accidentally duplicated and sending aberrant entries to the RTC is less than 1 in 10^{19}. This pattern is sent to the clock LSB to MSB.

Clock Register Information

Clock information is contained in eight registers of 8 bits, each of which is sequentially accessed one (1) bit at a time after the 64-bit pattern recognition sequence has been completed. When updating the clock registers, each must be handled in groups of 8 bits. Writing and reading individual bits within a register could produce erroneous results. These READ/WRITE registers are defined in the clock register map (see Table 9).

Data contained in the clock registers is in Binary Coded Decimal format (BCD). Reading and writing the registers is always accomplished by stepping through all eight registers, starting with Bit 0 of Register 0 and ending with Bit 7 of Register 7.

AM-PM/12/24 Mode

Bit 7 of the hours register is defined as the 12-hour or 24-hour mode select bit. When it is high, the 12-hour mode is selected. In the 12-hour mode, Bit 5 is the AM/PM bit with the logic high being “PM.” In the 24-hour mode, Bit 5 is the second 10-hour bit (20-23 hours).

Oscillator Bit

Bit 5 controls the oscillator. When set to logic '0,' the oscillator turns on and the RTC/calendar begins to increment.

Zero Bits

Registers 1, 2, 3, 4, 5, and 6 contain one (1) or more bits that will always read logic '0.' When writing to these locations, either a logic '1' or '0' is acceptable.

Table 9. RTC Register Map

Register	D7	D6	D5	D4	D3	D2	D1	D0	Function/Range BCD Format	
0	0.1 Seconds				0.01 Seconds				Seconds	00-99
1	0	10 Seconds			Seconds				Seconds	00-59
2	0	10 Minutes			Minutes				Minutes	00-59
3	12/24	0	10/ A/P	Hrs	Hours (24 Hour Format)				Hours	01-12/ 00-23
4	0	0	$\overline{OSC}$	1	0	Day of the Week			Day	01-7
5	0	0	10 date		Date: Day of the Month				Date	01-31
6	0	0	0	10M	Month				Month	01-12
7	10 Years				Year				Year	00-99

Keys:

A/P = AM/PM Bit
12/24 = 12 or 24-hour mode Bit
$\overline{OSC}$ = Oscillator Bit
$\overline{RST}$ = Reset Bit
0 = Must be set to '0'
1 = Must be set to '1'

Figure 13. Phantom Clock READ Cycle

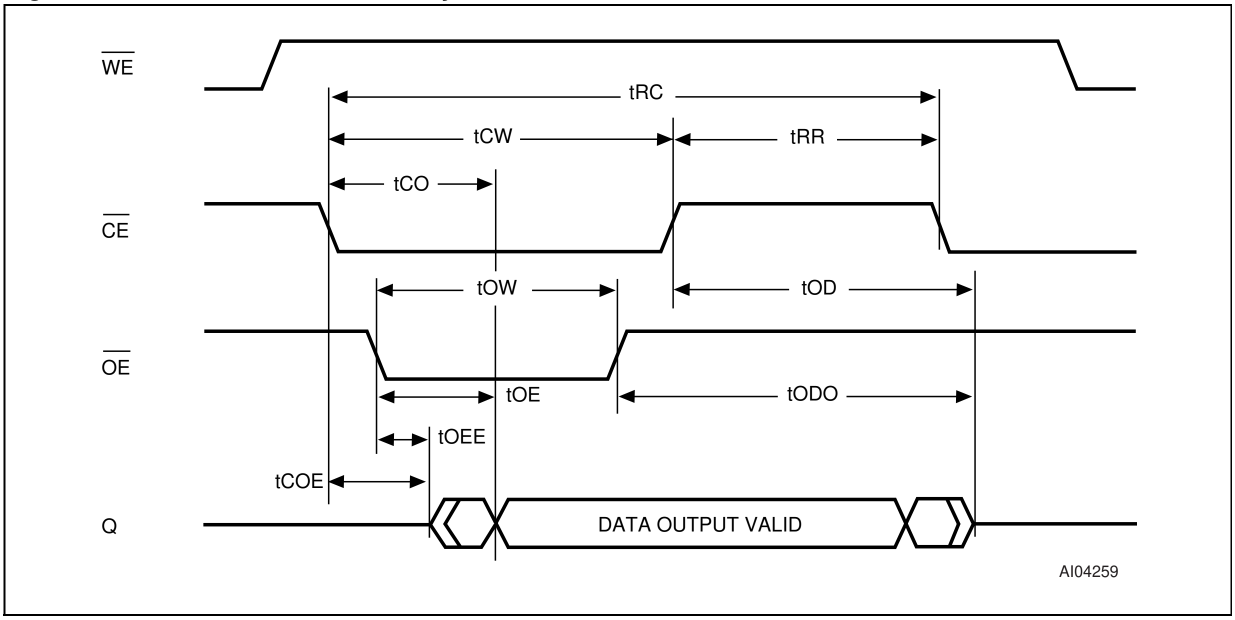
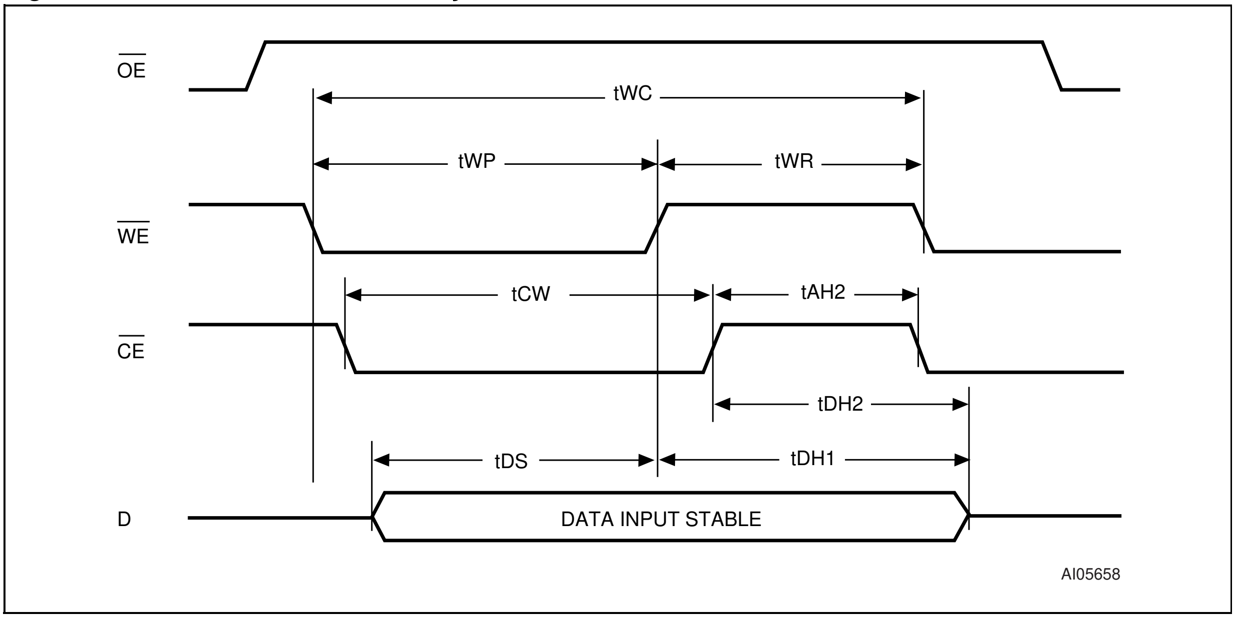


Figure 14. Phantom Clock WRITE Cycle



Battery Low

The M48T254V automatically performs battery voltage monitoring upon power-up, and at factory-programmed time intervals of at least 24 hours. The Battery Low ($\overline{BL}$) signal will be asserted if the battery voltage is found to be less than approximately 2.5V. The $\overline{BL}$ signal will remain asserted until completion of battery replacement and subsequent battery low monitoring tests, either during the next power-up sequence or the next scheduled 24-hour interval.

If a battery low is generated during a power-up sequence, this indicates that one of the batteries is below 2.5V and may not be able to maintain data integrity in the SRAM. Data should be considered suspect, and verified as correct. All three SNAPHAT® tops should be replaced.

If a battery low indication is generated during the 24-hour interval check, this indicates that one of the batteries is near end of life. However, data is not compromised due to the fact that a nominal V_{CC} is supplied. In order to insure data integrity during subsequent periods of battery back-up mode, the batteries should be replaced. The SNAPHAT top should be replaced with valid V_{CC} applied to the device.

The M48T254V only monitors the batteries when a nominal V_{CC} is applied to the device. Thus applications which require extensive durations in the battery back-up mode should be powered-up periodically (at least once every few months) in order for this technique to be beneficial. Additionally, if a battery low is indicated, data integrity should be verified upon power-up via a checksum or other technique. The $\overline{BL}$ signal is an open drain output and an appropriate pull-up resistor should be chosen to control the rise time.

Note: The $\overline{BL}$ signal is available only for the external SRAM, not for the Real-Time Clock.

PART NUMBERING

Table 10. Ordering Information Scheme

Example: M48T 254V –10 ZA 1

Device Type

M48T

Supply Voltage and Write Protect Voltage

254V = V_{CC} = 3.0 to 3.6V; V_{PFD} = 2.8 to 2.97V

Speed

–10 = 100ns

Package(1)

ZA = 42.5mm x 42.5mm(2), 1.27mm Ball Pitch, BGA Module

Temperature Range

1 = 0 to 70°C

Note: 1. The SOIC packages (SO28/SO44) require the battery/crystal package (SNAPHAT) which is ordered separately under the part number “M4T32-BR12SH” in plastic tube or “M4T32-BR12SHTR” in Tape and Reel form.

2. Where “Z” is the symbol for BGA packages and “A” denotes 1.27mm ball pitch

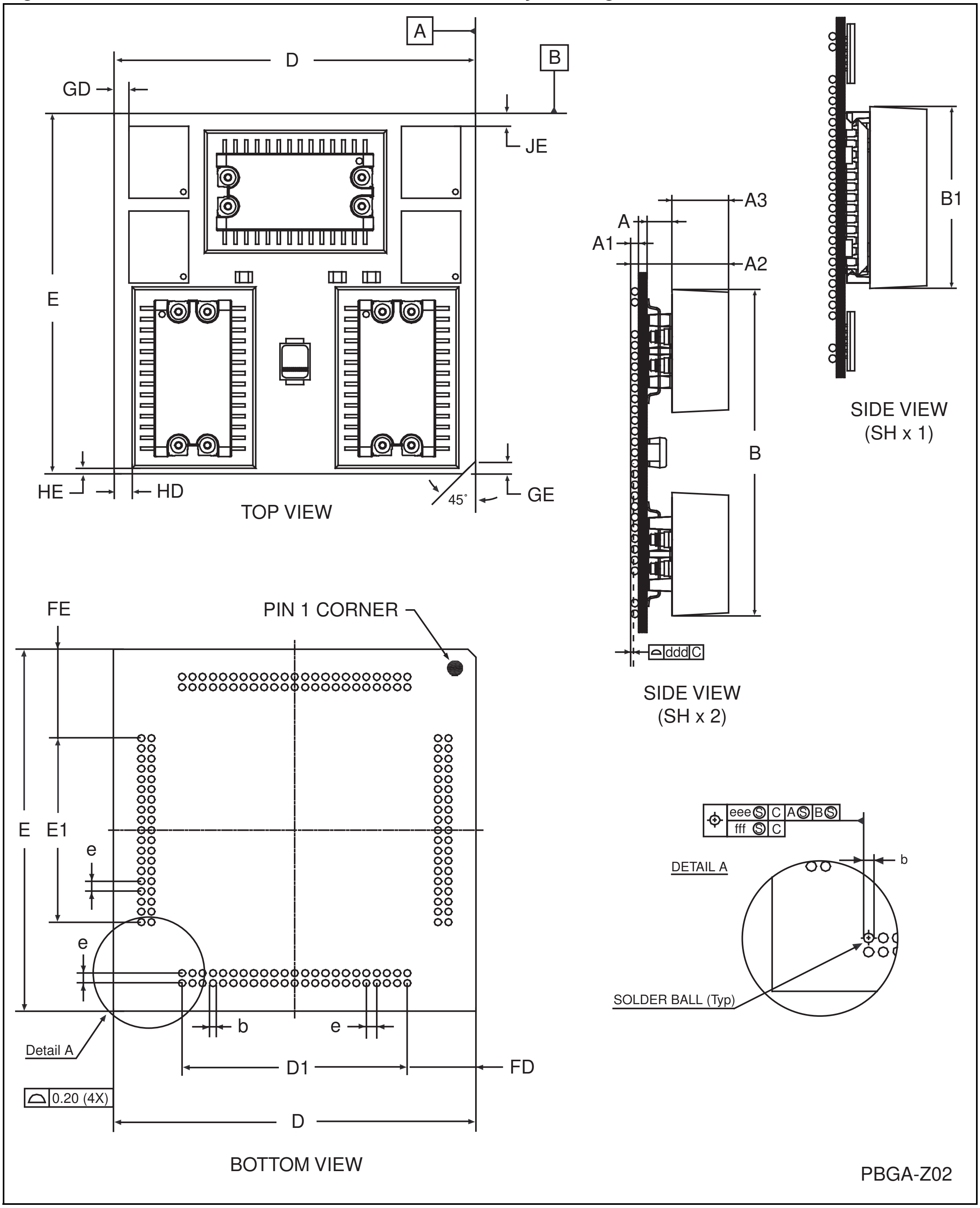
For a list of available options (e.g., Speed, Package) or for further information on any aspect of this device, please contact the ST Sales Office nearest to you.

Table 11. SNAPHAT Battery Table

Part Number	Description	Package
M4T32-BR12SH	Lithium Battery (120mAh) SNAPHAT	SH

PACKAGE MECHANICAL INFORMATION

Figure 15. PBGA-ZA – 168-ball Plastic Ball Grid Array Package Outline

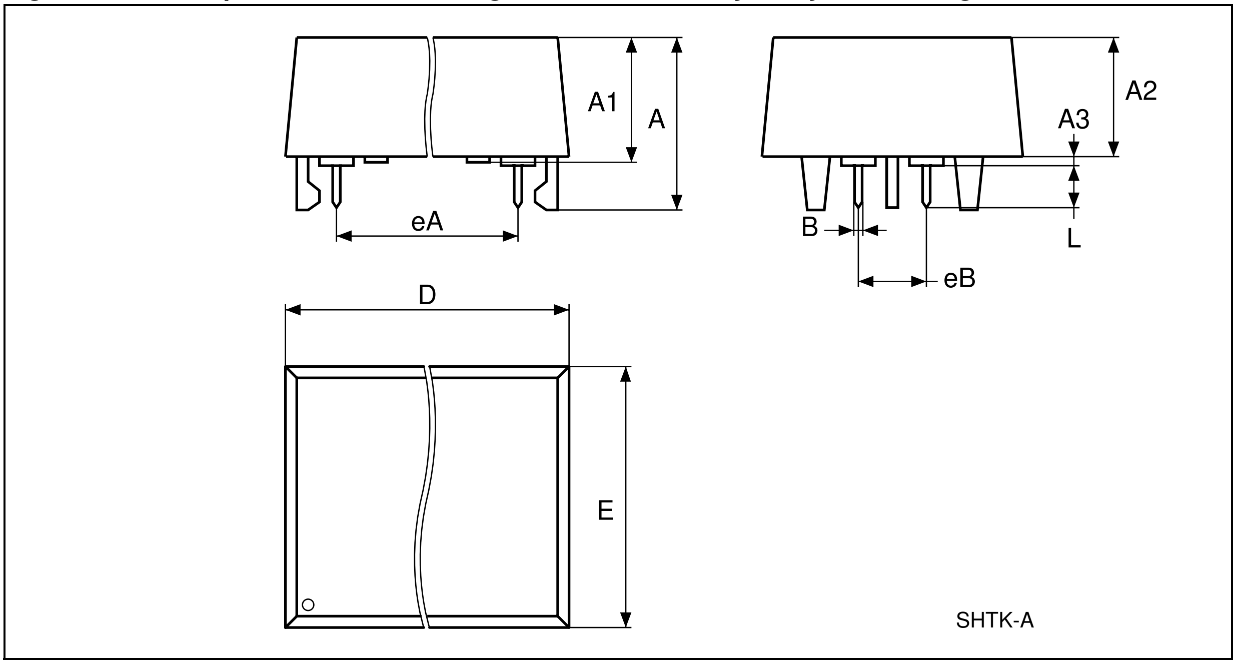


Note: Drawing is not to scale.

Table 12. PBGA-ZA – 168-ball Plastic Ball Grid Array Package Mechanical Data

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A	2.94	2.74	3.14	0.116	0.108	0.124
A1	0.89	0.69	1.09	0.035	0.027	0.043
A2	11.53	11.18	11.88	0.454	0.440	0.468
A3		7.24	8.00		0.285	0.315
B	38.54	38.34	38.74	1.517	1.509	1.525
B1		21.21	21.84		0.835	0.860
b	0.76	0.71	0.81	0.030	0.028	0.032
D	42.50	42.30	42.70	1.673	1.665	1.681
D1	27.94			1.100		
E	42.50	42.30	42.70	1.673	1.665	1.681
E1	22.86			0.900		
e	1.27			0.050		
FD	7.28	7.18	7.38	0.287	0.283	0.291
FE	9.82	9.72	9.92	0.387	0.383	0.391
GD	1.75	1.55	1.95	0.069	0.061	0.077
GE	1.50	1.30	1.70	0.059	0.051	0.067
HD	1.98	1.78	2.18	0.078	0.070	0.086
HE	0.51	0.31	0.71	0.020	0.012	0.028
JE	1.50	1.30	1.70	0.059	0.051	0.067
n	168			168		
	Tolerance			**Tolerance**		
ddd	0.15			0.006		
eee	0.30			0.012		
fff	0.15			0.006		

Figure 16. SH – 4-pin SNAPHAT Housing for 120mAh Battery & Crystal, Package Outline



Note: Drawing is not to scale.

Table 13. SH – 4-pin SNAPHAT Housing for 120mAh Battery & Crystal, Package Mechanical Data

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			10.54			0.415
A1		8.00	8.51		0.315	.0335
A2		7.24	8.00		0.285	0.315
A3			0.38			0.015
B		0.46	0.56		0.018	0.022
D		21.21	21.84		0.835	0.860
E		17.27	18.03		0.680	.0710
eA		15.55	15.95		0.612	0.628
eB		3.20	3.61		0.126	0.142
L		2.03	2.29		0.080	0.090

REVISION HISTORY

Table 14. Document Revision History

Date	Rev. #	Revision Details
September 2002	1.0	First Issue
31-Mar-03	1.1	Updated test condition (Table 8)
19-May-03	2.0	v2.2 template update; modify package dimensions (Table 12)

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