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:: MCF5329-10 Fire Engine ::

NOMO N

LOGIC

freescale semiconductor

Hardware Specification www.logicpd.com

REVISION HISTORY

REV	EDITOR	REVISION DESCRIPTION	CARD ENGINE REV	APPROVAL	DATE
1	Nathan Kro	Draft	Alpha	--	--
A	Kurt Larson	Initial Release	Beta	KL	12/06/05

REV	EDITOR	REVISION DESCRIPTION	SCHEMATIC REV	APPROVAL	DATE
B	Jed Anderson	Added “Schematic Rev” to Revision History table; Updated Hirose PNs in Section 6.1 to reflect available parts; Added second Important Note to Section 6.1; General grammatical and formatting changes	1001664 Rev A	JCA	11/08/06
C	Jed Anderson	Removed 8 MB option for NOR flash; Removed Section 1.4 “Fire Engine Advantages”	1001664 Rev B	JCA	04/09/07

Please check www.logicpd.com for the latest revision of this manual, product change notifications, and additional application notes.

Table of Contents

Table of Figures

PRODUCT BRIEF:
Logic :: Freescale

MCF5329 FIRE ENGINE System on Module

The MCF5329 Fire Engine is a compact, product-ready hardware and software solution that fast forwards your embedded product design.

The MCF5329 Fire Engine is a complete System on Module (SOM) that offers essential features for handheld and embedded networking applications. Use of custom baseboards makes the Fire Engine the ideal foundation for OEMs developing handheld and compact products. The Fire Engine provides a common reference pin-out on its expansion connectors, which enables easy scalability to next generation microprocessor Fire Engines when new functionality or performance is required.

Application development is performed right on the product-ready MCF5329 Fire Engine and software Board Support Packages (BSPs), which enables you to seamlessly transfer your application code and hardware into production.

The MCF5329 Fire Engine is ideal for applications in the medical, point-of-sale, industrial, and security markets. From patient monitoring and medical imaging, to card payment terminals and bar code readers, to CCTV cameras and intruder alarms, the MCF5329 Fire Engine allows for powerful versatility and long-life products.

FREESCALE MCF5329 FIRE ENGINE

MCF5329 FIRE ENGINE :: HIGHLIGHTS:

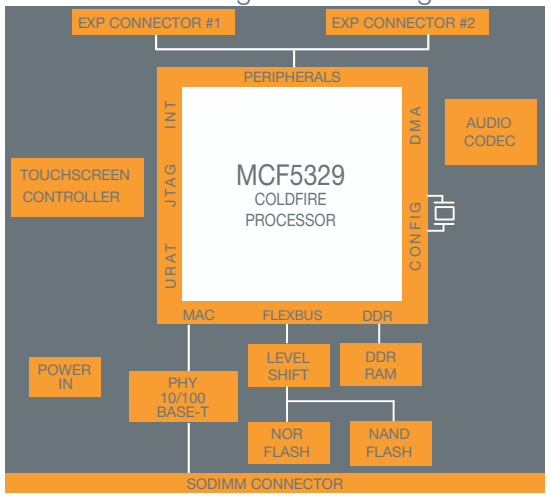
+ Product-ready System on Module with the MCF5329 ColdFire processor running at 240 MHz
+ Compact form factor 60.2 mm x 67.8 mm x 4.4 mm
+ Long product lifecycle
+ Multiple third-party software options
+ 0 ˚C to 70 ˚C (commercial temp)
+ RoHS compliant

ZOOM™ COLDFIRE M5329EVB :: FEATURES:

+ Application baseboard
+ MCF5329 Fire Engine (M5329BFEE)
+ Necessary accessories to immediately get up and running
+ Kit available from Freescale (M5329EVBE)
+ See Zoom™ ColdFire SDK product brief for more information

LOGIC

MCF5329 Fire Engine Block Diagram



MCF5329 Fire Engine Ordering Information

Freescale P/N	Speed (MHz)	DDR Mem (MB)	NOR Flash (MB)	NAND Flash (MB)	Touch	Audio	Ethernet
MCF5329AFEE	240	32	2	0	Y	Y	Y
MCF5329BFEE	240	32	2	16	Y	Y	Y

ZOOM™ ColdFire M5329EVB Ordering Information

Freescale P/N	SOM Configuration	Recommended Resale
M5329EVBE	M5329BFEE	$699

LOGIC WEBSITE :: DESIGN RESOURCES:

+Logic Technical Support : http://www.logicpd.com/support/
+Technical Discussion Group : http://www.logicpd.com/support/tdg/
+Frequently Asked Questions (FAQ) : http://www.logicpd.com/support/faq/
+For more information contact Logic Sales : product.sales@logicpd.com

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freescale™ semiconductor

Product Features

Processor
+Freescale MCF5329 32-bit ColdFire RISC microprocessor running at 240 MHz

SDRAM Memory
+32 MB DDR SDRAM standard

Flash Memory
+2–4 MB scalable NOR flash (2 MB standard)
+Scalable NAND flash (16 MB standard)

Display
+Programmable color LCD controller
+Built-in driver supports up to 800x600 with 16-bit LCD interface

Touch Screen
+Integrated 4-wire touch screen controller

Network Support
+10/100 Base-T Ethernet controller for application/debug (National Semiconductor DP83848 PHY)

Audio
+I2S compliant audio codec (Texas Instruments TLV320AIC23)

PC Card Expansion
+CompactFlash Type I card (memory-mapped mode only)

USB
+USB 2.0 full-speed host and device interface

Serial Ports
+Three 16C550 compatible UARTs
+Queued SPI interface w/selectable bit patterns

CAN
+CAN 2.0B interface muxed with I2C interface

GPIO
+Programmable I/O depending on peripheral requirements

Software
+LogicLoader™ (bootloader/monitor)
+Freescale dBUG ROM monitor
+Multiple third-party software options

Mechanical
+60.2 mm wide x 67.8 mm long x 4.4 mm high

RoHS Compliant

PN: 1004114 Rev F

1.2 Acronyms

ACI	Audio CODEC Interface
ADC	Analog to Digital Converter
AFE	Analog Front End Interface
AHB	Advanced Hardware Bus
BSP	Board Support Package
CDK	ColdFire® Development Kit
CPLD	Complex Programmable Logic Device
DAC	Digital to Analog Converter
DC	Direct Current
DDR	Double Data Rate (RAM)
DMA	Direct Memory Access
DRAM	Dynamic Random Access Memory
ENDEC	Encoder Decoder
ESD	Electro Static Dissipative
FEC	Fast Ethernet Controller
FET	Field Effect Transistor
FIQ	Fast Interrupt Request
FIFO	First In First Out
GPIO	General Purpose Input Output
HAL	Hardware Abstraction Layer
IC	Integrated Circuit
I2S	Inter-IC Sound
IDK	Integrated Development Kit
I/O	Input/Output
IRQ	Interrupt Request
LCD	Liquid Crystal Display
LoLo	LogicLoader™
MMC	Multi Media Card
NC	No Connect
PCB	Printed Circuit Board
PHY	Physical Layer
PLL	Phase Lock Loop
PMOS	P Metal Oxide Semiconductor
RISC	Reduced Instruction Set Computer
RTC	Real Time Clock
SDK	Starter Development Kit
SDRAM	Synchronous Dynamic Random Access Memory
SIR	Serial Infrared
SoC	System on Chip
SOM	System on Module
SSP	Synchronous Serial Port
SPI	Standard Programming Interface
TSC	Touch Screen Controller
TTL	Transistor-Transistor Logic
UART	Universal Asynchronous Receive Transmit
UHCI	Universal Host Controller Interface
VIC	Vectored Interrupt Controller

1.3 Technical Specification

Please refer to the following component specifications and data sheets.

LogicLoader User's Manual (available from Logic at http://www.logicpd.com)
MCF5329 Reference Manual (available from Freescale® at http://www.freescale.com/coldfire)
Texas Instruments™ TLV320DAC23 Audio codec data sheet (available at http://www.TI.com)

1.4 Fire Engine Interface

Logic's common Fire Engine interface allows for easy migration to new processors and technology. Logic is constantly researching and developing new technologies to improve performance, lower cost, and increase feature capabilities. By using the common SOM footprint, it is possible to take advantage of Logic's work without having to re-spin the old design. Contact Logic sales for more information.

In fact, encapsulating a significant amount of your design onto the Fire Engine reduces any long-term risk of obsolescence. If a component on the Fire Engine design becomes obsolete, Logic will simply design for an alternative part that is transparent to your product. Furthermore, Logic tests all Fire Engines prior to delivery, decreasing time-to-market and ensuring a simpler and less costly manufacturing process.

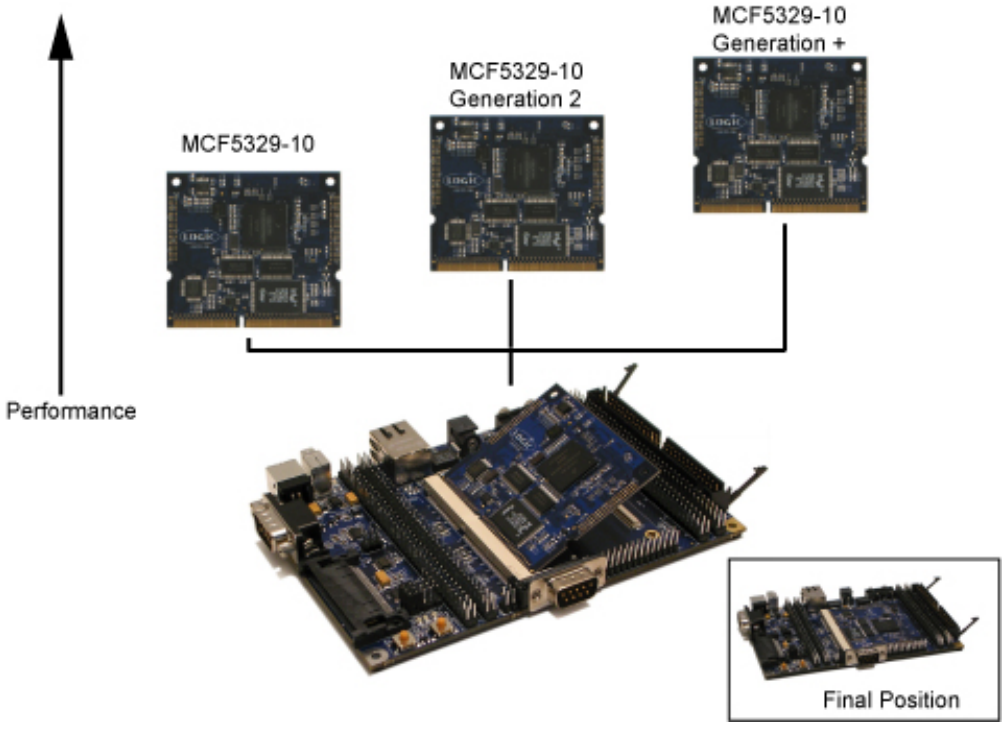

Figure 1.1: Fire Engine Advantages

1.5 MCF5329-10 Fire Engine Block Diagram

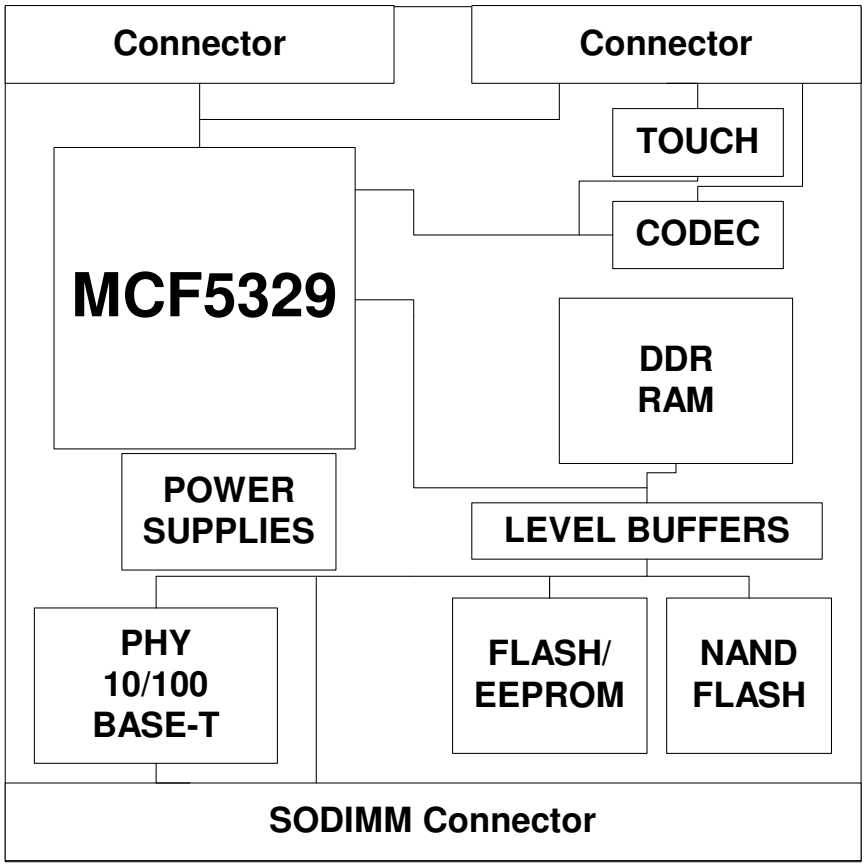

Figure 1.2: MCF5329-10 Fire Engine Block Diagram

1.6 Electrical, Mechanical, and Environmental Specifications

1.6.1 Absolute Maximum Ratings

Parameter	Symbol	Rating	unit
DC IO and Peripheral Supply Voltage	3.3V	VSS-0.3 to 3.6	V
DC Core Supply Voltage	VCORE	VSS-0.3 to 2.7	V

NOTE: These stress ratings are only for transient conditions. Operation at, or beyond, absolute maximum rating conditions may affect reliability and cause permanent damage to the Fire Engine and its components.

1.6.1.1 Recommended Operating Conditions

Parameter	Min	Typical	Max	Unit	Notes
DC IO and Peripheral Supply Voltage	3.0	3.3	3.6	V	
DC 3.3V Active Current	68	236		mA	2,5,6
DC 3.3V Suspend Current				mA	2
DC 3.3V Standby Current				mA	2
DC Core Voltage	2.3	2.5	2.7	V	
DC Core Active Current	22	58		mA	2,5,6
DC Core Suspend Current				mA	2
DC Core Standby Current				mA	2
Commercial Operating Temperature	0	25	70	°C	
Industrial Operating Temperature	-40	25	85	°C	3
Storage Temperature	-40	25	85	°C	
Dimensions		2.35 x 2.6		Inches	
Weight		17		Grams	4
Connector Insertion/removal		50		Cycles	
Input Signal High Voltage	0.8 x VCC			V	
Input Signal Low Voltage			0.2 x VCC	V	
Output Signal High Voltage	VCC – 0.3		VCC	V	
Output Signal Low Voltage	GND		GND + 0.3	V	

1. VCORE, SRAM, PLL, and 3.3V power are sequenced on the module.
2. Power consumption dependent on software state.
3. Contact Logic for more information on an industrial temperature MCF5329-10 Fire Engine.
4. May vary depending on Fire Engine configuration.
5. Minimum is average while CPU is in reset.
6. Typical is idle in LoLo bootloader with no activity and no display, Ethernet powered.

2 Electrical Specification

2.1 Microcontroller

2.1.1 MCF5329 Microcontroller

The MCF5329-10 Fire Engine uses Freescale's highly integrated MCF5329 ColdFire Microprocessor. This device features the V3 ColdFire core and provides many integrated on-chip peripherals, including:

Integrated ColdFire V3 Core
- 32-bit ColdFire V3 Core
- 4 stage instruction fetch pipeline
- 8 entry instruction buffer acceleration
- 16 kBytes instruction/data cache
- 32 kBytes on-chip SRAM

Integrated LCD Controller
- Up to 800 x 600 resolution at 16-bit color
- Supports STN, TFT, and HR-TFT
- Up to 256k colors

Three UARTs
AC97/I2S Codec Interface
One USB Client and One USB Host Interface (USB 2.0)
Many General Purpose I/O Signals
16 Independent DMA Channels
Four Programmable Timers
RTC
Low Power Modes

See Freescale's *MCF5329 Reference Manual* for additional information.
http://www.freescale.com/

IMPORTANT NOTE: Please visit http://www.freescale.com/ for errata on the MCF5329.

2.1.2 MCF5329 Microcontroller Block Diagram

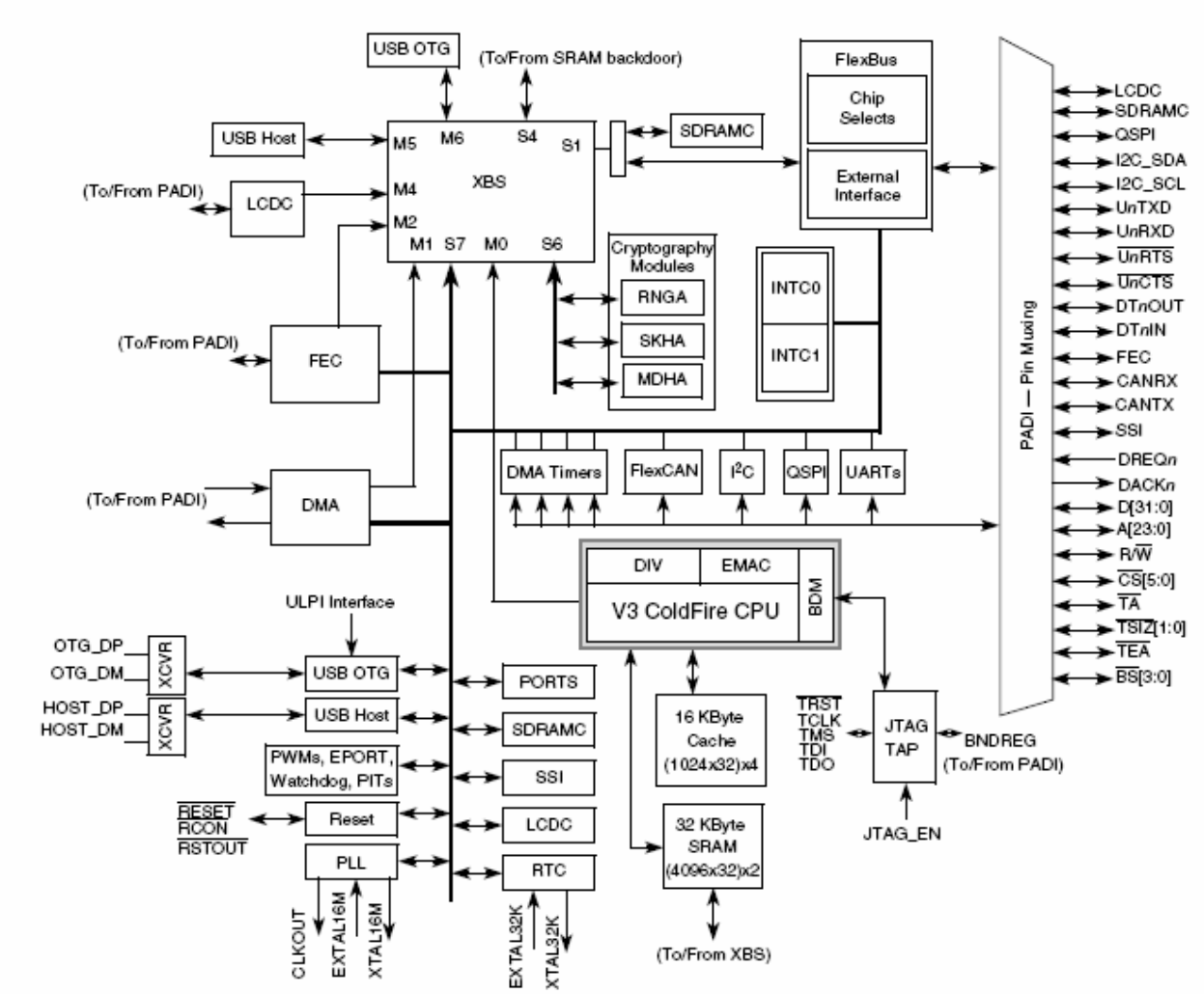

Figure 2.1: MCF5329 Microcontroller Block Diagram

2.2 Clocks

The MCF5329 requires 2 crystals in order to enable proper internal timing. A 16.000 MHz crystal is used to generate many of the processor's internal clocks via a series of PLLs and signal dividers. To generate the core CPU clock, the 16.000 MHz signal is run through a PLL controlled by the PLL Feedback Divider Register (PFDR). Divisors are used to divide down the internal bus frequency to set the LCD, memory controller, quick capture interface, and DMA controller.

IMPORTANT NOTE: Please see Freescale's *MCF5329 Reference Manual* for additional information about processor clocking.

The second required crystal runs at 32.768 kHz. The 32.768 kHz clock is used as a reference clock for the Real Time Clock (RTC) Module.

The MCF5329's microcontroller core clock speed is initialized to 240 MHz on the Fire Engine. The SDRAM bus speed is set at 80 MHz in LogicLoader. Other clock speeds can be supported and modified in software for specific user applications, like specific serial baud rates.

The MCF5329-10 Fire Engine provides an external bus clock, uP_BUS_CLK, on the 144-pin SO-DIMM connector. The uP_BUS_CLK, which is connected to the processor's FB_CLK, is set to a

default of 80 MHz. uP_SD_CLK and uP_SD_nCLK serve as the SDRAM clocks on the MCF5329-10 Fire Engine.

MCF5329 Microcontroller Signal Name	MCF5329-10 Fire Engine Net Name	Default Software Value in LogicLoader
CORE	N/A	240 MHz
Internal bus	N/A	80 MHz
SD_CLK	uP_SD_CLK	80 MHz
SD_CLK_b	uP_SD_nCLK	80 MHz

2.3 Memory

2.3.1 DDR Synchronous DRAM

The MCF5329-10 Fire Engine uses a 16-bit memory bus to interface to DDR SDRAM. The memory can be configured as 16, 32, or 64 MBytes in order to meet the user's memory requirements and cost constraints. Logic's default memory configuration on the CDK board is specified as 32 MBytes.

2.3.2 Direct Memory Access (DMA)

The Freescale MCF5329 microcontroller has an internal DMA controller. These channels can be used to interface streams from internal peripherals to the system memory (including USB, I2S, etc.). The DMA controller can also be used to interface streams from Memory-to-Memory or Memory-to-External Peripheral using two dedicated external channels. External handshake signals are available to support transfers to and from external peripherals. For more information on using the DMA interface refer to the *MCF5329 Reference Manual*.

2.3.3 NOR Flash

The MCF5329-10 Fire Engine uses a 16-bit memory bus to interface to NOR flash memory chips. The onboard Fire Engine memory can be configured as 1, 2, or 4 MBytes to meet the user's flash requirements and cost constraints. Logic's default flash configuration is 2 MBytes on the CDK. Because flash is one of the most expensive components on the MCF5329-10 Fire Engine, it is important to contact Logic when determining the necessary flash size for final product configuration. NAND flash is a lower cost alternative that should be considered for final product configuration.

It is possible to expand the system's non-volatile storage capability by adding external flash ICs, CompactFlash®, or NAND flash. See the MCF5329-10 ColdFire Development Kit for reference designs or contact Logic for other possible peripheral designs.

2.3.4 NAND Flash

The MCF5329-10 Fire Engine uses an 8-bit memory bus to interface to NAND flash. The product supports configurations of 16, 32, 64 MBytes, and other sizes, depending on NAND availability. The standard development kit is provided with 16 MBytes of NAND flash. Please contact Logic for more information.

2.3.5 CompactFlash (memory-mapped mode only)

The MCF5329-10 Fire Engine supports a CompactFlash memory-mapped mode only slot. The MCF5329-10 Fire Engine uses internal logic to provide the necessary signals for a CompactFlash card interface in memory-mapped mode only. The internal logic delays the rising edge of CF_nCE by two clock cycles to meet CompactFlash timing. The address hold time for uP_nCS1 must be extended two clock cycles beyond deassertion of uP_nCS1 to prevent bus conflicts. The

nCHRDY input signal to the Fire Engine can be asserted by CompactFlash. When pulled low, the nCHRDY signal generates a low on the uP_nWAIT signal to the processor, extending the length of the current cycle beyond the programmed internal wait states. See section 2.13 for further information on the CompactFlash interface. The Zoom™ ColdFire Development Kit reference design includes a CompactFlash connector for memory-mapped mode, but does not support hot-swappable capability. If hot-swappable capability is desired, it can be achieved by adding additional hardware to the user's baseboard.

2.4 10/100 Ethernet Controller

The MCF5329-10 Fire Engine uses the Fast Ethernet Controller (FEC) on the MCF5329 processor combined with the National Semiconductor® DP83848 10/100 single-chip Ethernet Transceiver to provide an easy-to-use networking interface. To facilitate use, six signals from the DP83848 are mapped to external connectors: transmit plus/minus, receive plus/minus, and two status LEDs. The four analog PHY interface signals (transmit/receive) each require an external impedance matching circuit to operate properly. Logic provides an example circuit schematic in the MCF5329-10 ColdFire Development Kit for reference. Please note the TX+/- and RX+/- pairs must be routed as differential pairs on the PCB.

2.5 Audio Codec

The MCF5329 processor has a Synchronous Serial Interface (SSI) controller that can support AC97 and I2S formats. This SSI controller implements a 5-pin serial interface to the I2S audio codec, in this case the Texas Instruments (TI) TLV320DAC23. From the TI codec on the MCF5329-10 Fire Engine, the outputs are CODEC_OUTL and CODEC_OUTR. These signals are available from the 80-pin expansion connectors.

The TI codec on the MCF5329 Fire Engine performs up to full-duplex 24-bit codec functions and supports variable sample rates from 8-96k samples per second.

NOTE: The Freescale MCF5329 Fire Engine also offers an SSI interface for other codec devices. This interface provides a digital interface that is multiplexed with the signals from the SSI controller. If you are looking for a different codec option, Logic has previously interfaced different high-performance audio codecs into other Fire Engines. Contact Logic for assistance in selecting an appropriate audio codec for your application.

2.6 Display Interface

Freescale's MCF5329 microcontroller has a built in LCD controller supporting STN, color STN, HR-TFT, and TFT panels at up to 800 x 600 x 18-bit color resolution. See the *MCF5329 Reference Manual* for further information on the integrated LCD controller. The signals from the MCF5329's LCD controller are organized by bit and color and can be interfaced through the J1A expansion connectors. Logic has written drivers for numerous panels of different types and sizes. Please contact Logic before selecting a panel for your application.

IMPORTANT NOTE: Using the internal graphics controller will affect processor performance. Selecting display resolutions and color bits per pixel will vary processor busload.

2.7 Serial Interface

The MCF5329-10 Fire Engine comes with the following serial channels: UARTA, UARTB, UART2, and QSPI. If additional serial channels are required, please contact Logic for reference designs. Please see the *MCF5329 Reference Manual* for further information regarding serial communications.

2.7.1 UARTA

UARTA has been configured to be the MCF5329-10 development kit's main serial port. It is an asynchronous 16C550-compatible UART. This UART provides a high-speed serial interface that uses FIFO and is capable of sending and receiving serial data simultaneously. The signals from the Fire Engine are TTL level signals not RS232 level signals. The user must provide an external RS232 transceiver for RS232 applications. Logic has provided an example reference design with the ColdFire Development Kit. When choosing an RS232 transceiver, the user should keep in mind cost, availability, ESD protection, and data rates.

UARTA's baud rate is set by default to 115.2Kbits/sec, though it supports most common serial baud rates. UARTA is available off the J1C 144-pin SO-DIMM connector.

2.7.2 UARTB

Serial Port UARTB is an asynchronous 16C550-compatible UART. This UART is a high-speed serial interface that uses FIFO and is capable of sending and receiving serial data simultaneously. The signals from the Fire Engine are TTL level signals, not RS232 level signals. The CDK baseboard has a RS232 level shifter and can be accessed on P3 when the J9 jumpers are installed connecting pins 1-2, 3-4, and 5-6. UARTB's baud rate can also be set to most common serial baud rates. UARTB is available off the J1B 80-pin expansion connector.

2.7.3 QSPI

The Queued SPI interface is used on the Fire Engine to communicate with the onboard touch interface, as well as the onboard audio codec.

There is an additional uP_SPI_FRM signal brought off-board for customer use. The serial format is used to interface between the parallel data inside the SoC and synchronous serial communications on peripheral devices. The signals are available off the 144-pin SO-DIMM connector. Please see the *MCF5329 Reference Manual* for further information.

2.8 USB Interface

The MCF5329 Fire Engine is configured with both USB host and device functionality. The USB device interface is compliant to the USB 2.0 and the EHCI 1.0 specifications. This USB client supports full-speed (12 Mbits/sec) operation. The USB device interface on the MCF5329 is able to transmit data, receive data, or control information over the bus, and is available for external use off the J1A 80-pin connector.

The USB host interface is compatible with both the USB 2.0 and EHCI 1.0 specifications. This controller also supports both low-speed and full-speed USB devices. The USB connector signals are available off the J1A 80-pin connector. For more information on using both the USB device and host interfaces, please see the *MCF5329 Reference Manual*.

IMPORTANT NOTE: In order for USB to be correctly implemented on the MCF5329 Fire Engine, additional impedance matching circuitry is required on the USBP and USBM signals before they can be used. USB 2.0 requirements specify that the impedance on each driver must be between 28 Ω and 44 Ω. For reference, see the impedance matching circuit on the Logic CDK.

2.9 ADC/Touch Interface

The MCF5329-10 Fire Engine uses the Texas Instruments ADS7843 touch screen controller (TSC) for a 12-bit analog-to-digital converter (ADC). This TSC is used to support standard 4-wire resistive touch panels. The TSC has 2 A/D signals that are available externally off the J1A 80-pin connector. The device is connected to the CPU by the QSPI interface. Please see the *ADS7843 Datasheet* for more information.

2.10 General Purpose I/O

Logic designed the MCF5329-10 Fire Engine to be flexible and provided multiple options for analog and digital GPIO. There are numerous digital GPIO pins on the Fire Engine that interface to the MCF5329. See the "Pin Descriptions" section of this data sheet for more information. If certain peripherals are not desired, such as the LCD controller, chip selects, IRQs, or UARTS, then multiple GPIO pins become available. Please see the table in Section 5.4 "Multiplexed Signal Trade-Offs" for a list of the available GPIO trade-offs.

2.11 Onboard Logic Interfaces

The onboard Logic interfaces are used to create additional functionality on the Fire Engine with the support of a few discrete logic components. The logic interface serves four main purposes: modify MCF5329 flex-bus signal timing to support standard CompactFlash cards, add 8 general purpose inputs and 8 general purpose outputs, provide memory map selection between the GPIO interface and the CompactFlash interface, and provide chip select qualified read and write signals for onboard NAND flash.

Memory Map:
The onboard Logic creates a 2-part memory map for the CPU's chip select 1 area. The base address is determined by the CSAR1 register. The base address of chip select 1 is also the base address of the CompactFlash interface. When chip select 1 is asserted and A19 is low, onboard logic modifies the flex-bus hardware signal timing to meet the CompactFlash specification. The recommended flex-bus settings for accessing CompactFlash and the external general purpose input/output bits are:
CSCR1 = 0x002A3780
CSMR1 = 0x001F0001

Chip Select	Offset	Device/feature
nCS1	+ 0x00	CompactFlash Interface
nCS1	+ 0x80000	External 8 bit GPIO port
nCS2	+ 0x00	NAND flash area

Accessing chip select area 1 with an address that asserts address line 19 high will cause an access to the external onboard 8-bit GPIO port. The GPIO port bits are listed here and correspond to actual external signals on the Fire Engine PCB. Note that reading and writing to a single bit may have different functions. For example, reading from bit 7 returns the state of the nSTANDBY signal, but writing to bit 7 changes the state of the uP_STATUS_1 signal.

Bit	7	6	5	4
Input (read)	nSTANDBY	nSUSPEND	LATCH_GPO_1	LCD_VEEEN
Output (write)	uP_STATUS_1	uP_STATUS_2	LATCH_GPO_1	LCD_VEEEN
Output Reset value	tri-state	tri-state	tri-state	tri-state

Bit	3	2	1	0
Input (read)	LATCH_GPO_2	WRLAN_nINT	nIRQD	uP_MODE2
Output (write)	LATCH_GPO_2	NAND_nGPIO	uP_USB2_PWR_EN	uP_USB1_PWR_EN
Output Reset value	tri-state	tri-state	tri-state	tri-state

GPIO port initialization:
The 8 GPIO outputs are in tri-state by default after a CPU reset. To enable the GPIO outputs, first write the desired state of the outputs to the GPIO port at address chip select 1 + 0x80000. Then the processor GPIO TIN3/PTIMER3 signal should be driven low, which will enable all 8 GPIO

outputs. This can be accomplished by clearing bits 6 and 7 in the PAR_TIMER register and clearing bit 3 in the PODR_TIMER register.

GPIO port signal definitions:

uP_MODE2 - Read only. Logic Loader software reads this pin to determine whether or not to skip user abort from any stored scripts. Tying this signal low will disable user aborts from scripts over the serial port. Refer to the *LogicLoader User's Manual* for additional information. This pin can also be used as a General Purpose input and read from the 8-bit GPIO port. This signal is pulled up to 3.3V through a 1.5K resistor.

uP_USB1_PWR_EN – Write only. Active low. Enables power supply for USB port 1.

nIRQD – Input only. Software can use as a hardware interrupt on MCF5329-10. This signal is pulled up to 3.3V through a 1.5k resistor. If driven low, this signal will drive the processor's IRQ5 low. The ISR that services IRQ5 should read the 8-bit GPIO port to determine which interrupt source is active.

uP_USB2_PWR_EN – Write only. Active high. Enables USB port 2.

WRLAN_nINT – Read only. Active low. Hardware interrupt from the onboard Ethernet PHY. This signal is pulled up to 3.3V through a 1.5k resistor. If driven low, this signal will drive the processor's IRQ5 low. The ISR that services IRQ5 should read the 8-bit GPIO port to determine which interrupt source is active.

NAND_nGPIO – Write only. Active low. Driving this signal low will hold the NAND flash chip select low (NAND_nCE). See the following section for more details.

LATCH_GPO_2 – Read/Write. Writing to this bit will drive the external signal LATCH_GPO_2 to the desired state. Reading from this bit will return the current state of the LATCH_GPO_2 output.

LCD_VEEEN – Read/Write. Writing to this bit will drive the external signal LCD_VEEEN to the desired state. Reading from this bit will return the current state of the LCD_VEEEN output. This signal is typically used for controlling power to LCD backlight displays.

LATCH_GPO_1 – Read/Write. Writing to this bit will drive the external signal LATCH_GPO_1 to the desired state. Reading from this bit will return the current state of the LATCH_GPO_1 output.

nSUSPEND – Read only. Software can use as a hardware interrupt on MCF5329-10. See Section 3.5.4.2 for suggested software implementation of the nSUSPEND signal. This signal is pulled up to 3.3V through a 1.5k resistor. If driven low, this signal will drive the processor's IRQ5 low. The ISR that services IRQ5 should read the 8-bit GPIO port to determine which interrupt source is active.

uP_STATUS_2 – Write only. Writing to this bit will drive the external signal uP_STATUS_2 to the desired state. The uP_STATUS_1 and uP_STATUS_2 signals are used to drive the LEDs on the CDK baseboard. Driving this signal low will turn on the LED.

nSTANDBY - Read only. Software can use as a hardware interrupt on MCF5329-10. See section 3.5.4.3 for suggested software implementation of the nSTANDBY signal. This signal is pulled up to 3.3V through a 1.5k resistor. If driven low, this signal will drive the processor's IRQ5 low. The ISR that services IRQ5 should read the 8-bit GPIO port to determine which interrupt source is active.

uP_STATUS_1 – Write only. Writing to this bit will drive the external signal uP_STATUS_1 to the desired state. The uP_STATUS_1 and uP_STATUS_2 signals are used to drive the LEDs on the CDK baseboard. Driving this signal low will turn on the LED.

NAND flash:

The NAND flash chip base address is defined by chip select 2. Any reads or writes to the NAND flash chip are qualified by AND gates in U16. Using the NAND_nGPIO output defined in the onboard "GPIO port signal definitions" section above, software can hold the NAND chip select (NAND_nCE) signal low to allow for devices which require the chip select to be active during address pointer changes. The onboard logic allows the NAND address pointer change to occur without issues even while other devices chip selects are active.

2.12 Expansion/Feature Options

The MCF5329-10 Fire Engine was designed for expansion and a variable feature set, providing all the necessary control signals and bus signals to expand the user's design. Some of these signals are buffered and brought out to the 144-pin SO-DIMM connector and two 80-pin expansion connectors. It is possible for a user to expand the Fire Engine's functionality even further by adding host bus or ISA bus devices. Some features that are implemented on the MCF5329, but are not discussed herein, include: RTC, pulse width modulation (PWM), crypto unit, random number generator, enhanced multiply-accumulate (EMAC), and the debug module. See the *MCF5329 Reference Manual* and the MCF5329-10 Fire Engine schematics for more details. Logic has experience implementing additional options, including other audio codecs, Ethernet ICs, co-processors, and components on Fire Engine boards. Please contact Logic for potential reference designs before selecting your peripherals.

3 System Integration

3.1 Configuration

The MCF5329-10 Fire Engine was designed to meet multiple applications for specific users and budget requirements. As a result, this Fire Engine supports a variety of embedded operating systems and comes with the following hardware configurations:

- Flexible memory footprint: 16, 32, or 64 MBytes DDR SDRAM
- Flexible NOR flash footprint: 1, 2, or 4 MBytes NOR flash
- Flexible NAND flash footprint: 0, 16, 32, 64 MBytes, or larger NAND flash.
- Optional National Semiconductor DP83848 10/100 Ethernet controller
- Optional Texas Instruments TLV320DAC23 audio codec
- Optional Texas Instruments ADS7843 touch controller

Please contact Logic for additional hardware configurations to meet your application needs.

3.2 Resets

3.2.1 Master Reset (Hard Reset)

All hardware peripherals should connect their hardware-reset pin to the MSTR_nRST signal on the SODIMM connector. Internally all Fire Engine peripheral hardware reset pins are connected to the MSTR_nRST_INT net. The MSTR_nRST signal is an open-drain output, enabling the user to assert the MSTR_nRST signal externally. Logic suggests that custom designs implemented with the MCF5329-10 Fire Engine use the MSTR_nRST signal as the “pin hole” reset used in commercial embedded systems. The MSTR_nRST triggers a power on reset event to the MCF5329 and resets the entire CPU.

If the output of the reset chip, MSTR_nRST, is asserted (active low), the user can expect to lose information stored in SDRAM. The data loss occurs because the external signals uP_BUS_CLK and uP_AUX_CLK are interrupted during the assertion of the MSTR_nRST signal.

IMPORTANT NOTE: Any custom reset circuit design should guard the assertion of the reset lines during a low power state so as to prevent power-up in a low or bad power condition (which will cause data corruption and possible temporary system lockup). See the section entitled “Power Management” for further details. The following two conditions will cause a system-wide reset: power on or a low pulse on the MSTR_nRST signal.

Power On:
At power on, the MSTR_nRST signal is asserted low when the supply voltage (VDD) of the reset chip is between 1.0V and 3.08V. Once the 3.3V supply surpasses 3.08V the reset chip will trigger a rising edge of MSTR_nRST after a 140-460 ms delay (240 ms typical).

Low Pulse on MSTR_nRST Signal:
A low pulse on the MSTR_nRST signal of the reset chip, asserted by an external source (for example, the reset button on the custom design application) will bring MSTR_nRST low until the assertion source is de-asserted. There is no delay beyond the de-assertion of the external MSTR_nRST signal source, so the custom design must ensure that the assertion time is sufficient for all related peripherals.

Logic suggests that for any external assertion source that triggers the MSTR_nRST signal, analog or digital, de-bouncing be used to generate a clean, one-shot reset signal.

3.3 Interrupts

The MCF5329 incorporates two interrupt controllers (INTC0 and INTC1). Through these two interrupt controllers the MCF5329 can prioritize and process up to 128 interrupts (not all used on this device). Each interrupt has its own unique vector number and its own unique interrupt control register (ICRnx) to define software-assigned levels. Refer to Freescale's *MCF5329 Reference Manual* for further information on using IRQ interrupts.

3.4 JTAG Debugger Interface

The JTAG connection on the MCF5329 allows recovery of corrupted flash memory and real-time application debug. When choosing a debugger board, remember that many different third-party JTAG debuggers are available for Freescale ColdFire microcontrollers. The following signals make up the JTAG interface to the MCF5329: PST[3:0], DDATA[3:0], uP_TDI, uP_TMS, uP_TCK, and uP_TDO. These signals should interface directly to a 26-pin 0.1" through-hole connector as shown on the CDK baseboard reference schematics.

IMPORTANT NOTE: When laying out the 26-pin connector, realize it may not be numbered as a standard 26-pin 0.1" IDC through-hole connector. See MCF5329-10 ColdFire Development Kit reference design for further details. Different JTAG tool vendors define the 26-pin IDC connector pin-out differently.

3.5 Power Management

3.5.1 System Power Supplies

In order to ensure a flexible design, the MCF5329-10 Fire Engine was designed to have the following power areas: 3.3V, 3.3VA, 3.3V_WRLAN, and 2.5V. All power areas are inputs to the Fire Engine with the exception of 3.3V_WRLAN, which is an output from the Fire Engine.

3.5.1.1 2.5V

The 2.5V input pins are connected to a 2.5V power supply with an optional backup battery. If the design is required to maintain SDRAM contents in a critical power situation (low battery, loss of power), the 2.5V supply should be maintained above the minimum level at all costs (see "Electrical Specification", Section 2). Logic suggests using Standby mode to prepare the system for a critical power condition. In this way, the SDRAM is placed into self-refresh and processor is placed into the Standby state. Please note the description of Standby mode in Section 3.5.4.3 below.

3.5.1.2 3.3V

The power nets connected to the 3.3V power plane handle the majority of the peripheral supply pins (digital) on the MCF5329-10 Fire Engine. This supply must stay within the acceptable levels specified in Section 2 of this manual, "Electrical Specification", unless experiencing power down or critical power conditions.

Under critical power conditions, Logic suggests notifying the system through the assertion of a Standby sequence first, and then powering this supply off.

3.5.1.3 3.3VA

The power nets connected to the 3.3VA power plane handles all peripheral supply pins (analog), but not the MCF5329 processor on the MCF5329-10 Fire Engine. The 3.3VA supply must stay within the acceptable levels specified in Section 2 of this manual, “Electrical Specification”, unless powering down the board or under critical power conditions.

Under critical power conditions, Logic suggests first notifying the system through the assertion of a Standby sequence and then powering this supply off.

3.5.1.4 3.3V_WRLAN

This “power” supply net is an output from the Fire Engine. The custom application board should use the 3.3V_WRLAN output pin to supply the Ethernet impedance matching resistors with power. These resistors should not be connected to 3.3V directly or the entire Ethernet controller circuit on the Fire Engine will try to power itself through the impedance matching resistors. Please see Logic’s CDK reference design schematics for details.

3.5.1.5 1.5V (Internal to Fire Engine Only)

The module creates a 1.5V power plane for the CORE_VDD inputs on the MCF5329. The 1.5V plane is powered from the 3.3V supply and is always on when 3.3V is available.

3.5.2 System Power Management

Good power management design is important in any system development and embedded system design is no exception. In embedded system design, power management is typically one of the most complicated areas due to the dramatic effect it has on the product cost, performance, usability, and overall customer satisfaction. Many factors affect a power-efficient hardware design: power supply selection (efficiency), clocking design, IC and component selection, etc. The MCF5329-10 Fire Engine was designed to keep these aspects in mind and provide maximum flexibility in software and system integration.

On the MCF5329 there are many different software configurations that drastically effect power consumption: microcontroller core clock frequency, microcontroller bus clock frequency, microcontroller peripheral clocks, microcontroller bus modes, microcontroller power management states (Run, Wait, Doze, and Stop), peripheral power states and modes, product user scenarios, interrupt handling, and display settings (resolution, backlight, refresh, bits per pixel, etc). These settings are typically initialized in the startup software routines and may be later modified in the operating system and application software. Information for these items can be found in the appropriate documents such as the *LogicLoader User’s Manual* or the specific BSP manual.

3.5.3 Peripherals

Most peripherals provide software programmable power states. However, sometimes these programmable power states may not be the best solution.

The MCF5329-10 Fire Engine was designed to have the following four power areas: 3.3V, 3.3V_WRLAN, 3.3VA, and 2.5V for a flexible hardware design. See Figure 3.1, below.

Logic Net Name	Required Input VDC	Notes
3.3V	3.3 VDC	Connects to the digital peripherals on the Fire Engine.
3.3VA	3.3 VDC	Connects to the Audio Codec on the Fire Engine to provide a clean analog plane. The user may choose not to provide a clean analog plane depending on their performance requirements.
2.5V	2.5 VDC	Connects to the onboard memory bus and DDR RAM.
3.3V_WRLAN	3.3 V (This Pin is an output, see section 3.5.1.4)	Output from the Fire Engine that provides power to the offboard Ethernet circuitry.

Figure 3.1: Power Plane Diagram

3.5.4 Microcontroller

The MCF5329 processor power management's scheme was designed to be easy to use. There are four power management modes provided in the MCF5329 microcontroller: Run, Wait, Doze, and Stop. Logic Product Development BSPs have simplified the power management scheme to three power states: Run, Suspend, and Standby. Please see the descriptions of all three states below, as well as the *MCF5329 Reference Manual*, for more details.

3.5.4.1 Run State

Run is the MCF5329-10 Fire Engine's normal operating state in which both oscillator inputs and all clocks are hardware enabled. The MCF5329 can enter Run mode from any state. A Standby to Run transition occurs on any valid wake up event. The assertion of MSTR_nRST or any enabled interrupt signal qualify. All power supplies are active in this state. Please see the *MCF5329 Reference Manual* for further information.

3.5.4.2 Suspend State

Suspend state is the MCF5329 Fire Engine's hardware power down state, allowing for lower power consumption. The Suspend state is designed to reduce power consumption while the MCF5329 is waiting for an event such as a keyboard input. The Suspend state is entered using Logic BSPs by asserting the nSUSPEND signal or through software. The Stop, Wait, or Doze state is entered. All power supplies remain active. System context is retained. An internal or external wakeup event can cause the processor to transition back to Run Mode. Please see the *MCF5329 Reference Manual* for further information.

3.5.4.3 Standby State

Standby state is the MCF5329 Fire Engine's lowest power state. This state is entered in Logic BSPs by asserting the nSTANDBY signal or through software. The MCF5329 processor is put into Stop state. All clocks are stopped. System reboot is required if 3.3V power is removed. 3.3V power can be removed from the Fire Engine. The 2.5V power rail should be maintained if the DDR SDRAM contents wish to be retained. Internal or external wakeup events can cause

transition back to run state if 3.3V is not powered down, otherwise a system reset is required because context is lost when 3.3V power is removed.

3.6 ESD Considerations

The MCF5329-10 Fire Engine was designed to interface to a customer's peripheral board. The Fire Engine was designed to be low cost and adaptable to many different applications. The MCF5329-10 Fire Engine does not provide any onboard ESD protection circuitry – this must be provided by the product it is used in. Logic has extensive experience in designing products with ESD requirements. Please contact Logic if you need any assistance in ESD design considerations.

4 Memory & I/O Mapping

On the Freescale ColdFire MCF5329 microcontroller, all address mapping is accomplished through the use of several Address pointer registers. Please consult the *MCF5329 Reference Manual* for details.

FlexBus:

Mapped “Chip Select” signals for the FlexBus are available as outputs from the microcontroller and are assigned as follows:

FB_CS0# = NOR flash (boot, 1 MB, 2 MB, or 4 MB)
FB_CS1# = CompactFlash and registers
FB_CS2# = NAND flash (16 MB, 32 MB, or 64 MB)
FB_CS3# = Available for use by an external device (VIDEO_nCS, host board)
FB_CS4# = Available for use by an external device (FAST_nCS, host board)
FB_CS5# = Available for use by an external device (SLOW_nCS, host board)

DDR RAM Chip Select lines:
SD_CS0 = DDR RAM
SD_CS1 = Not used

Please consult the *LogicLoader User’s Manual* and the *LogicLoader User’s Manual Addendum* for the MCF5329 for complete memory map information.

