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# M54455EVB User's Manual

by:   Microcontroller Solutions Group

# 1      Introduction

## 1.1      Purpose

This document provides design and usage information for the Freescale M54455EVB evaluation, development and reference platform.

The M54455EVB platform provides an evaluation system for the Freescale MCF5445*x* ColdFire® V4m embedded microprocessor family. The MCF54455 is the superset device in the family and is the processor featured on this platform. This allows evaluation and development for the entire family on a single hardware platform.

## 1.2      Related Documents

- *MCF54455 Reference Manual*
- *M54455EVB Quick Start Guide*
- *M54455EVB Schematics*
- *MC34702 Switch-Mode with Linear Power Supply Datasheet*

**Contents**

*freescale*™
semiconductor

- *Universal Serial Bus Specification, Revision 2.0*
- *PCI Local Bus Specification, Revision 2.2*
- *DDR2 SDRAM Specification (JESD79-2C)*

# 2 Overview

## 2.1 MCF54455 Overview

The MCF54455 is the host processor for the M54455EVB. Figure 1 shows a top-level block diagram of the MCF54455 superset device. The following is a brief summary of the functional blocks in the MCF54455 superset device.

- Version 4 ColdFire Core with MMU and EMAC
  — Up to 410 Dhrystone 2.1 MIPS @ 266 MHz
- 16 KBytes instruction cache and 16 KBytes data cache
- 32 Kbytes internal SRAM
- Support for booting from SPI-compatible flash, EEPROM, and FRAM devices
- Crossbar switch technology (XBS) for concurrent access to peripherals or RAM from multiple bus masters
- 16 channel DMA controller
- 16-bit 133MHz DDR/mobile-DDR/DDR2 Controller
- USB 2.0 On-the-Go controller with ULPI support
- 32-bit PCI controller @ 66MHz
- ATA/ATAPI controller
- Two 10/100 Fast Ethernet Controllers (FEC*n*)
- Cryptographic acceleration unit (CAU)
- Random number generator
- Synchronous serial interface
- Four periodic interrupt timers
- Four 32-bit timers with DMA support
- DMA-supported serial peripheral interface (DSPI)
- Three UARTs
- $I^2C$ bus interface
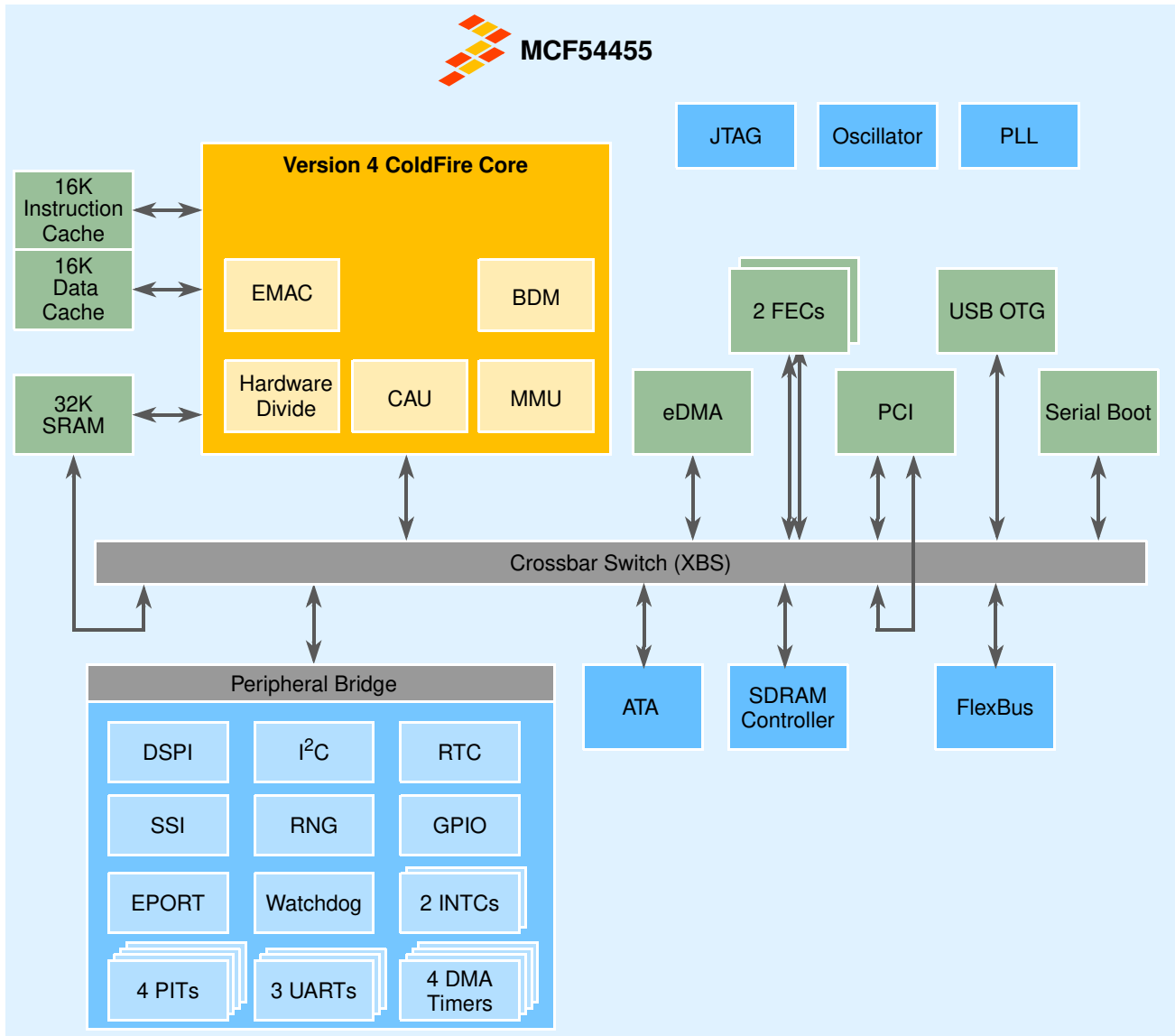
**LEGEND**

| | | | |
|---|---|---|---|
| **ATA** | – Advanced Technology Attachment Controller | **INTC** | – Interrupt controller |
| **BDM** | – Background debug module | **JTAG** | – Joint Test Action Group interface |
| **CAU** | – Cryptography acceleration unit | **MMU** | – Memory management unit |
| **DSPI** | – DMA serial peripheral interface | **PCI** | – Peripheral Component Interconnect |
| **eDMA** | – Enhanced direct memory access | **PIT** | – Programmable interrupt timers |
| **EMAC** | – Enhanced multiply-accumulate unit | **PLL** | – Phase locked loop module |
| **EPORT** | – Edge port module | **RNG** | – Random Number Generator |
| **FEC** | – Fast Ethernet Controller | **RTC** | – Real time clock |
| **GPIO** | – General Purpose Input/Output | **SSI** | – Synchronous Serial Interface |
| **I²C** | – Inter-Integrated Circuit | **USB OTG** | – Universal Serial Bus On-the-Go controller |

**Figure 1. MCF54455 Block Diagram**

## 2.2    M54455EVB Overview

The M54455EVB provides hardware to evaluate as many of the configurations of the MCF5445$x$ family as possible. The M54455EVB features:

- Freescale MCF54455 ColdFire microprocessor
- DDR2 SDRAM (256 MByte)
- Two NOR flash memory devices (16 MByte, 512 KByte)
- Serial flash
- MRAM (512 KByte, accessible through FPGA Flexbus interface)
- Four PCI slots (32-bit, for MCF5445$x$ as a PCI host system)
- Two-port Ethernet interface
- 40-pin ATA connector
- Audio interface ($I^2S$ mode of SSI module connected to audio codec)
- Multiple USB interface options
  — FS/LS Host via on-chip transceiver with host support (Type A receptacle)
  — HS/FS/LS dual-role via external ULPI PHY (Mini-AB receptacle)
- Two RS232 serial ports (RS232 transceivers on UART0 & UART1)
- One USB serial port (UART0 serial converted to USB converted on UART0)
- Built-in P&E Micro USB Multilink debug interface
- Standard 26-pin BDM header
- Serial interface header for access to timers, interrupts, DSPI, $I^2C$, and more
- Clock generation logic adjustable via $I^2C$
- LEDs and 7-segment display programmable via CPLD and FPGA
- Low-profile, micro-ATX computer case with built-in power supply



**Figure 2. M54455EVB Kit**

## Figure 3. M54455EVB Block Diagram

**PCI Clock Buffer**

**Programmable Clock Generator**

Clocks for FPGA, Eth PHY, USB

**SSI Audio Interface**

**USB Full-speed Interface**

**BDM & JTAG 26-pin Connector**

PCI Slot 3

PCI Slot 2

PCI Slot 1

PCI Slot 0

3.3V PCI Bus

3.3V

1.8V

**DDR2 Term Reg**

0.9V VTT

0.9V VREF

EXTAL

PCI Arbi Cntrl and Interrupts

**Interfaces for RS232, RS232-to-USB, DSPI, I2C, Timers, etc.**

**Serial Flash**

Serial I/O, Interrupts, Timers, etc.

**DDR2 4 x 512Kbit (64M8)**

**DDR2 Parallel Termination**

SDRAM Bus

VREF

VTT

**FPGA**

PCI Arbitration and Interrupts

PCI Arbitration and Interrupts

**ColdFire MCF5445x**

Buffered Flexbus

**MRAM**

**CPLD**

FlexBus

**Reset Configuration Latch**

ATA_DATA[7:0], Control

**Compression Logic Analyzer Connectors surrounding processor for access to all switching signals**

CPLD Switchable Options

Chip Selects

**512K Flash 8-bit data bus Flash0**

Boot Mode Selection

**ATA**

**ATA Buffer**

ATA_DATA[15:8]

ATA_DATA[15:8]

**16MB Flash 8-bit data bus Flash1**

ULPI

FEC0 RMII

FEC1 RMII / ATA_DATA[8:15]

5V

**ATX Power Supply**

**MC34702**

**MC34702**

**Barrel Pwr Connector**

3.3V

1.8V

1.5V

1.2V

**USB ULPI Interface**

**Dual FEC PHY (RMII mode) and 2xRJ45 w/ integrated magnetics and LEDs**
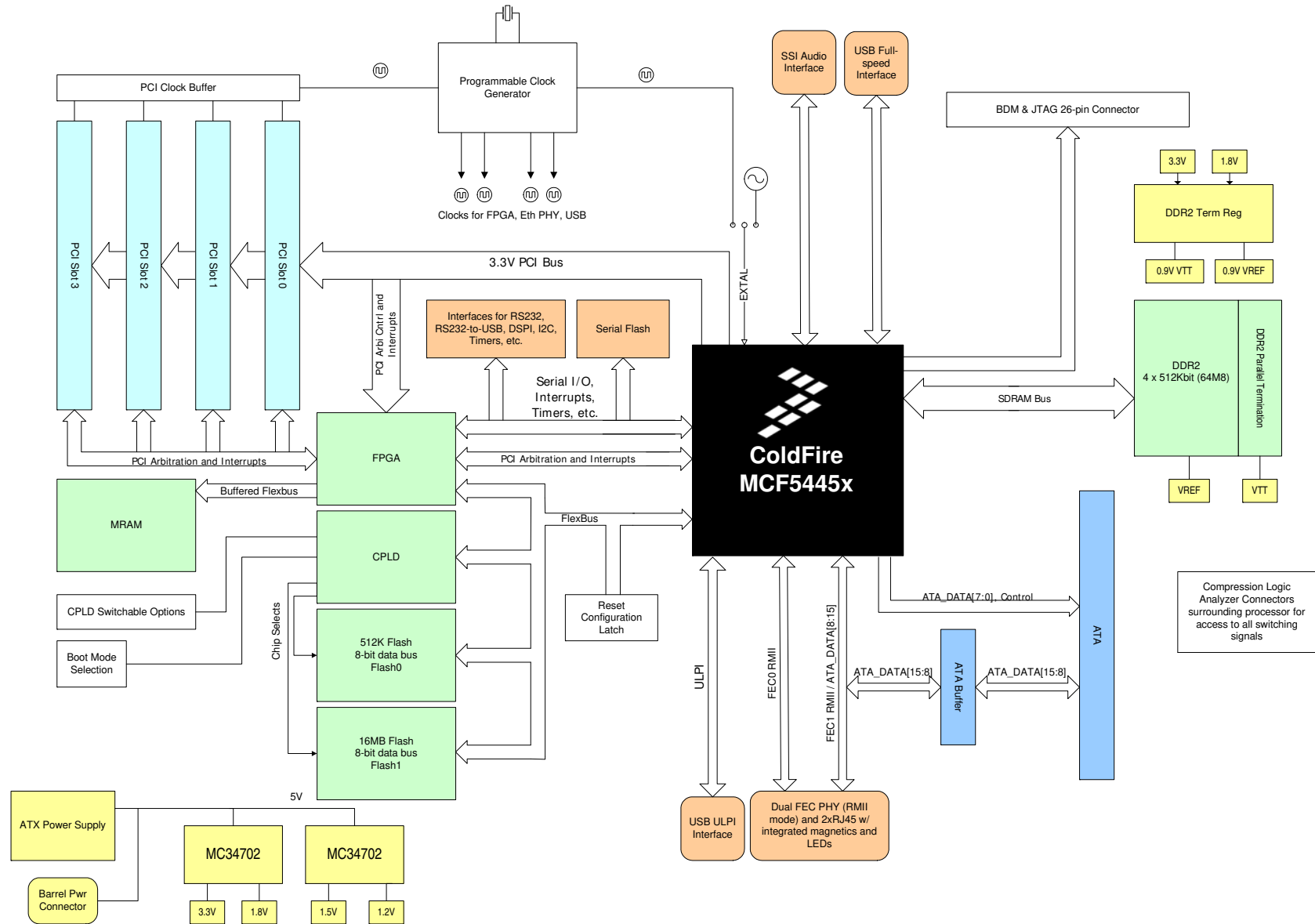
## 2.3 Memory Map Overview

Figure 1 illustrates the overall memory map for the MCF54455 and M54455EVB.

**Table 1. M54455EVB Memory Map**

| Function | Start Address | End Address | Size |
|---|---|---|---|
| Flexbus—Flash1 | 0x0000_0000 | 0x00FF_FFFF | 16 MB |
| Flexbus—Flash0 | 0x0400_0000 | 0x0407_FFFF | 512 KB |
| Flexbus—CPLD[1] | 0x0800_0000 | 0x08FF_FFFF | 16 MB |
| Flexbus—FPGA/MRAM[1] | 0x0900_0000 | 0x09FF_FFFF | 16 MB |
| DDR2 SDRAM | 0x4000_0000 | 0x4FFF_FFFF | 256 MB |
| MCF5445x Internal SRAM | 0x8000_0000 | 0x8000_7FFF | 32 KB |
| ATA | 0x9000_0000 | 0x9FFF_FFFF | 256 MB |
| PCI | 0xA000_0000 | 0xBFFF_FFFF | 512 MB |
| Flexbus—Unused | 0xC000_0000 | 0xDFFF_FFFF | 512 MB |
| Reserved | 0xE000_0000 | 0xEFFF_FFFF | 256 MB |
| Internal Peripheral Space | 0xF000_0000 | 0xFFFF_FFFF | 256 MB |

[1] The CPLD and FPGA sections contain details on the memory-mapped registers within these address spaces.

Much of the memory map is dictated by the MCF5445x memory map. Refer to the "Overview" and "Crossbar Switch" sections of the *MCF54455 Reference Manual* for more details.

## 2.4    I/O Back Panel

Refer to Figure 4 for the I/O back panel descriptions.
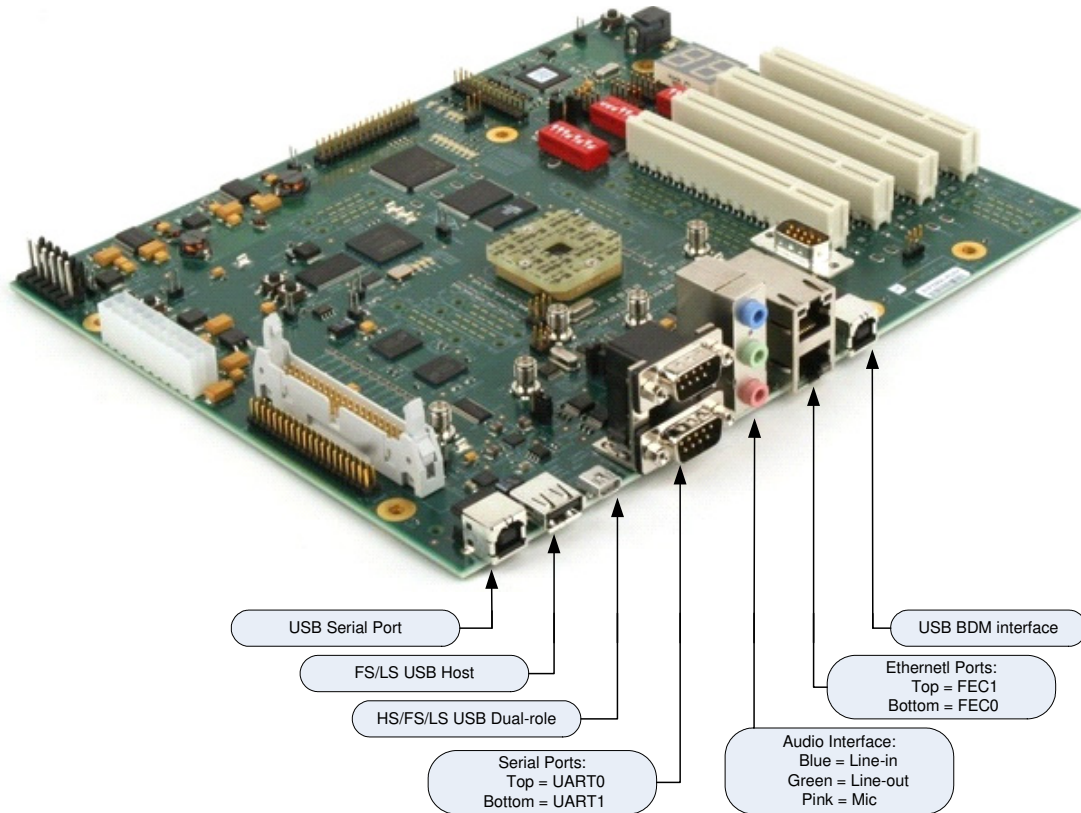


**Figure 4. M54455EVB I/O Back Panel Port Locations**

# 3    Installation and Configuration

The M54455EVB comes pre-programmed with U-Boot and Linux pre-configured to run a demo application. This section describes how to setup the evaluation board to access the bootloader to start Linux.

The default communication interface with the M54455EVB is a simple serial port console. A terminal emulator on a host PC and the supplied serial cable is required to interact with the serial port. Alternately, a USB cable can be used if the USB serial port is configured for use (refer to Section 4.17, "Serial Ports" for details).

The basic installation steps are as follows:

1. Plug in the case's power supply with the power cable provided.
2. Connect one end of the provided serial cable to the DB9 serial port connector labelled UART0 (Refer to Figure 4).
3. Connect the other end of the serial cable to a free DB9 serial port connector on a host PC.
4. Open the terminal emulator of your choice (e.g. HyperTerminal, Tera Term, minicom, etc.).

5. Configure the COM port as follows:

**Table 2. Default Serial Console Settings**

| Parameter | Setting |
|---|---|
| Baud Rate | 115,200 bps |
| Data bits | 8 |
| Parity | None |
| Stop bits | 1 |
| Flow Control | None or Software (Xon/Xoff) |

6. Press the power switch on the front of the computer case and the U-Boot banner (example below) should appear in the terminal window.

```
U-Boot 1.2.0-g4a442d31-dirty (Aug 23 2007 - 11:14:19)

CPU:    Freescale MCF54455 (Mask:48 Version:1)
        CPU CLK 266 Mhz BUS CLK 133 Mhz FLB CLK 33 Mhz
        INP CLK 33 Mhz VCO CLK 533 Mhz
Board: Freescale M54455 EVB
I2C:    ready
DRAM:   256 MB
FLASH: 16.5 MB
In:     serial
Out:    serial
Err:    serial
Net:    FEC0, FEC1
IDE:    Bus 0: not available  Status = 0x60
->
```

Linux and a root file system are preprogrammed into the second Flash device (Flash1) at address 0x0000_0000. A demo application automatically runs when Linux is started. A network connection is required for the web server portion of the demo to work.

7. Plug one end of the provided Ethernet cable into a network or host PC with a DHCP server running. Plug the other end of the cable into the FEC0 interface (bottom RJ45 receptacle) of the M54455EVB.

8. To boot Linux, issue the following U-Boot command.

```
-> bootm 0
```

9. The demo application prints out a banner message including the IP address that it obtained from the DHCP server. Launch a web client (e.g. Firefox or Internet Explorer) and copy this IP address into the web browser. The M54455EVB serves up a web page with more information on the available demos.

# 4    Hardware Submodules

The following sections describe the hardware submodules of the M54455EVB.

## 4.1 DDR SDRAM Interface

The MCF5445*x* DDR SDRAM controller has the following features:

- Supports a glueless interface to DDR, DDR2, and mobile/low-power DDR SDRAM devices
- Support for 16-bit fixed memory port width
- 16-byte critical word first burst transfer
- Up to 14 lines of row address, up to 11 column address lines, 2 bits of bank address, and two chip selects.
- Supports up to 512 MByte of memory; minimum memory configuration of 8 MByte
- Supports page mode to maximize the data rate
- Supports sleep mode and self-refresh mode

The M54455EVB features 256 MBytes of DDR2 SDRAM. Four 8-bit wide Micron MT47H64M8 (512 Mbit) devices are arranged as two 16 M × 8 × 4 banks per SDRAM controller chip select. This results in two 16-bit wide, 128 MBytes blocks of DDR2 memory

The SDRAM interface is terminated with parallel termination resistors. The MCF5445*x* does not provide control for the DDR2 on-die termination. The ODT pins on the DDR2 devices are connected to control signals from the CPLD for test purposes only. These signals are disabled in the normal functional mode.

## 4.2 Reset Controller

The reset controller on the M54455EVB is implemented in a Xilinx XC95144XL CPLD. The CPLD controls the state of the system reset signal (SYSRESET) gathers reset information from a pushbutton reset (SW2), the BDM interface, and the FPGA (FPGA_DONE). At system power-on, the CPLD holds SYSRESET asserted until the FPGA has loaded its image from the platform flash PROM and asserted the FPGA_DONE signal. After system power-on, the CPLD asserts SYSRESET when it detects the assertion of any of the reset sources.

## 4.3 MCF5445*x* Boot Options

During a system reset, the CPLD also drives the boot mode configuration signals into the MCF5445*x*. The MCF5445*x* has three boot mode options:

- Boot with default configuration constants specified in the RCON register,
- Boot with configuration data specified by the Flexbus FB_AD[7:0] pins, and
- Boot with configuration data obtained from an external SPI memory through the serial boot facility.

In all of these cases, the boot code is fetched from an external memory connected to the Flexbus on FB_CS0 with the possible exception of the serial boot mode. In serial boot mode, if the boot load length field (BLL) in the reset configuration data stored in the SPI memory is non-zero, then boot code is loaded from the SPI memory instead of from Flexbus.

The MCF5445*x* boot mode is determined by the state of the BOOTMOD[1:0] input pins during the rising edge of RSTOUT (MCF5445*x* reset output signal). The CPLD drives BOOTMOD[1:0] to the values that

are set on the CPLD mode signals (CPLD_MODE[1:0]). The CPLD_MODE signals are set by the CPLD configuration switch, SW1. See Section 4.14, "CPLD" for more details. Table 3 shows the SW1 settings and their corresponding boot mode configurations.

**Table 3. M54455EVB Boot Mode Selection**

| BOOTMOD[1:0] | SW1[2:1] | Meaning |
|---|---|---|
| 00 | ON:ON | Boot from Flexbus with defaults (from RCON register) |
| 01 | ON:OFF | Reserved |
| 10 | OFF:ON | Boot from Flexbus and override defaults via data bus (FB_AD[7:0]) |
| 11 | OFF:OFF | Boot from Flexbus and override defaults via serial boot facility (SPI memory) |

## 4.3.1 Default Configuration (SW1[2:1] = ON:ON)

If the BOOTMOD pins are 00 during reset, the MCF5445*x* RCON register determines the chip configuration after reset, regardless of the states of the external data pins. The RCON register specifies the following default configuration for the MCF54455:

- PCI enabled, muxed Flexbus address/data, 8-bit port-size boot
- PLL enabled
- PCI host mode
- 66MHz PCI slew rate mode
- PLL multiplier: $f_{VCO} = 6 \times f_{REF}$

## 4.3.2 Parallel Configuration (SW1[2:1] = OFF:ON)

If the BOOTMOD pins are 10 during reset, the MCF5445*x* configuration after reset is determined according to the levels driven onto the FB_AD[7:0] pins. On the M54455EVB, the FB_AD[7:0] pins are actively driven by an 8-bit buffer enabled when the MCF5445*x* $\overline{RSTOUT}$ signal is asserted. The values driven by the buffer are set by the SW3 DIP switch settings. Refer to Table 4 for the configuration setting information.

**Table 4. MCF54455 Parallel Configuration During Reset**

| Pin(s) Affected | Corresponding SW3 Settings | | | Function |
|---|---|---|---|---|
| | SW3[8] | SW3[7] | SW3[6] | **Flexbus, PCI, Port Size Mode** |
| | ON | ON | ON | PCI, muxed FB addr/data, 8-bit boot[1] |
| | ON | ON | OFF | No PCI, muxed FB addr/data, 16-bit boot |
| | ON | OFF | ON | No PCI, muxed FB addr/data, 8-bit boot |
| FB_AD[31:0], PCI_* | ON | OFF | OFF | No PCI, muxed FB addr/data, 32-bit boot |
| | OFF | ON | ON | PCI, muxed FB addr/data, 16-bit boot |
| | OFF | ON | OFF | No PCI, non-muxed FB addr/data, 16-bit boot |
| | OFF | OFF | ON | No PCI, non-muxed FB addr/data, 8-bit boot |
| | OFF | OFF | OFF | No PCI, non-muxed FB addr/data, 32-bit boot |
| | SW3[5] | | | **PLL Mode** |
| Output Clocks | ON | | | Limp mode |
| | OFF | | | PLL mode |
| | SW3[4] | | | **PCI Host/Agent Mode (when in a PCI mode)** |
| (none) | ON | | | PCI host mode |
| | OFF | | | PCI agent mode |
| | SW3[4] | | | **Oscillator Mode (when in a No PCI mode)** |
| (none) | ON | | | Oscillator bypass mode |
| | OFF | | | Crystal oscillator mode |
| | SW3[3] | | | **PCI Slew Rate Mode (when in a PCI mode)** |
| PCI_* | ON | | | 66 MHz slew rate mode |
| | OFF | | | 33 MHz slew rate mode |
| | SW3[3] | SW3[2] | SW3[1] | **PLL Multiplier (when in a No PCI mode)** |
| | ON | ON | ON | $f_{VCO} = 8 \times f_{REF}$ |
| | ON | ON | OFF | $f_{VCO} = 16 \times f_{REF}$ |
| | ON | OFF | ON | $f_{VCO} = 6 \times f_{REF}$ |
| (none) | ON | OFF | OFF | $f_{VCO} = 12 \times f_{REF}$ |
| | OFF | ON | ON | $f_{VCO} = 18 \times f_{REF}$ |
| | OFF | ON | OFF | $f_{VCO} = 24 \times f_{REF}$ |
| | OFF | OFF | ON | $f_{VCO} = 10 \times f_{REF}$ |
| | OFF | OFF | OFF | $f_{VCO} = 20 \times f_{REF}$ |

Table 4. MCF54455 Parallel Configuration During Reset (continued)

| Pin(s) Affected | Corresponding SW3 Settings | | Function |
|---|---|---|---|
| | SW3[2] | SW3[1] | PLL Multiplier (when in a PCI mode) |
| (none) | ON | ON | $f_{VCO} = 8 \times f_{REF}$<br>e.g. CPU = 266 MHz; PCI = 66 MHz |
| | ON | OFF | $f_{VCO} = 16 \times f_{REF}$<br>e.g. CPU = 266 MHz; PCI = 33 MHz |
| | OFF | ON | $f_{VCO} = 6 \times f_{REF}$<br>e.g. CPU = 200 MHz; PCI = 66 MHz |
| | OFF | OFF | $f_{VCO} = 12 \times f_{REF}$<br>e.g. CPU = 200 MHz; PCI = 33 MHz |

[1] This setting is required if booting from Flash device, Flash0, or Flash1.

### 4.3.3 Serial Configuration (SW1[2:1] = OFF:OFF)

If the BOOTMOD pins are 11 during reset, then the chip configuration after reset is determined by data obtained from an external SPI memory through serial boot using the SBF_DI, SBF_DO, $\overline{SBF\_CS}$, and SBF_CK signals. The internal configuration signals are driven to reflect the data being received from the external SPI memory to allow for module configuration. See "Serial Boot Facility" and "Chip Configuration Module" chapters of the *MCF54455 Reference Manual* for more details.

## 4.4 System Clocks

A single Cypress CY22393 device generates all of the clock signals on the M54455EVB. Alternatively, you can supply the clock signals using external SMA connectors for test purposes. The different clock signals and configurations are described below. Please refer to the *MCF54455 Reference Manual* for further information on the clocking requirements for the MCF5445*x* family.

The CY22393 is programmed prior to assembly on the M54455EVB PCB. There is an $I^2C$ interface on this device that allows it to be reprogrammed. However, these settings are not retained following a power-on reset.

The state of the CY22393's S2 frequency control input pin is controlled by a jumper (H4[3:4]) and the system FPGA signal, CLK_GEN_S2. The FPGA uses two conditions to determine how to drive the CLK_GEN_S2 signal: the M66EN signal and a programmable bit in the PCICLKCFG register. The M66EN signal is a PCI bus signal that is tied to logic 0 if a 33MHz PCI card is installed in any one of the four PCI slots. By default, the PCICLKCFG[CLKGENS2EN] bit is cleared, which forces the clocks to 33 MHz. Table 5 summarizes the three controls over the state of the S2 pin.

**Table 5. PCI Clocks and MCF5445*x* Input Clock Speed Selection**

| M66EN signal | FPGA_PCICLKCFG [CLKGENS2EN] | H4[3:4] Jumper | Resulting S2 Value | CPU input and PCI Bus Speed |
|---|---|---|---|---|
| 0 | — | — | 0 | 33 MHz |
| — | 0[1] | — | 0[1] | 33 MHz[1] |
| — | — | Jumper Shunt ON | 0 | 33 MHz |
| 1[1] | 1 | Jumper Shunt OFF[1] | 1 | 66 MHz |

[1] **Indicates the default values.**

The following pseudocode illustrates the input clock determination logic:

```
if ((H4[3:4] shunt is not installed) and
        (no 33MHz PCI cards installed (M66EN logic 1)) and
        (FPGA_PCICLKCFG[CLKGENS2EN] is set))
{
        S2 = 1; PCI Clocks and MCF5445x input clock are 66MHz
}
else
{
        S2 = 0; PCI Clocks and MCF5445x input clock are 33MHz
}
```

Refer to Section 4.13, "FPGA" for details on the FPGA_PCICLKCFG register. Table 6 shows the default system clock frequencies generated by the CY22393.

**Table 6. Clock Generator Outputs**

| Clock | CY22393 Output | S2 Value | Default Clock Frequency (MHz) | Description |
|---|---|---|---|---|
| MCF5445*x* Input Clock | CLKA | 0 | 33 | Clock driven into the EXTAL pin on the MCF5445*x*. This is the operating frequency in limp mode and the PLL reference when the PLL is enabled. |
| | | 1 | 66 | |
| PCI Clock | CLKB | 0 | 33 | Duplicate of the MCF5445*x* input clock. This is driven to clock buffers and on to each PCI slot, the FPGA, and the CPLD. |
| | | 1 | 66 | |
| MCF5445*x* USB Clock | CLKC | N/A | Disabled[1] | MCF5445*x* USB clock[1] |
| ULPI PHY Clock | CLKD | N/A | 24 | Reference clock for the external ULPI PHY |
| RMII Ethernet Clocks | CLKE | N/A | 50 | Duplicate, matched clocks driven to each MCF5445*x* FEC RMII clock input and to the external dual Ethernet PHY |

[1] CLKC is disabled by default. Instead, USBCLKIN is driven by the 60MHz clock output of the ULPI PHY. However, JP918 provides an option to select CLKC as the source for USBCLKIN. If this is selected, the CY22393 must be programmed via I$^2$C to generate a 60MHz clock signal.

There is a provision on the M54455EVB for clocking the MCF5445*x* with a 25MHz crystal instead of the 33/66MHz external clock. A cut-trace (CT11) can be modified to route the provided 25MHz crystal oscillator circuit to the EXTAL input. Refer to Figure 5 for details on how to make this modification.

**Figure 5. MCF5445*x* Input Clock Selection Cut-Trace**

## 4.5 SPI Flash

A 16 Mbit SPI flash is connected to the MCF5445*x* via the DSPI interface. This same SPI flash can be used to store reset configuration parameters and boot code when using the serial boot facility. Refer to Section 4.3, "MCF5445x Boot Options" for more information on how to configure the M54455EVB for serial boot.

## 4.6 Flash

The M54455EVB features two flash devices connected to the FlexBus expansion bus. The smaller of the two flashes is a 512KByte, 8-bit wide AT49BV040 (or compatible) device referred to as Flash0. This device contains the U-Boot bootloader. The larger of the two flashes is a 16 MByte, 8-bit wide 28F128J3D (or compatible) device referred to as Flash1. By default, this flash device is programmed with a Linux image, but it can be reprogrammed and used as a boot device if desired.

The selection of a boot flash device is achieved with a CPLD mode switch setting, specifically CPLD_MODE2 which is controllable by DIP switch SW1[3]. The device that is connected to the global chip-select from the MCF5445*x* ($\overline{\text{FB\_CS0}}$) is the boot device. The other device is connected to $\overline{\text{FB\_CS1}}$. Table 7 shows the boot device selection settings.

**Table 7. Flash Chip Select Configuration**

| SW1[3] | Meaning | Application |
|--------|---------|-------------|
| OFF | Flash1 is the boot device<br>$\overline{\text{FLASH1\_CS}} = \overline{\text{FB\_CS0}}$<br>$\overline{\text{FLASH0\_CS}} = \overline{\text{FB\_CS1}}$ | Boot custom image |
| ON | Flash0 is the boot device<br>$\overline{\text{FLASH1\_CS}} = \overline{\text{FB\_CS1}}$<br>$\overline{\text{FLASH0\_CS}} = \overline{\text{FB\_CS0}}$ | Boot U-Boot |

## 4.7 PCI

The MCF5445*x* processor's PCI controller module has the following features:

- Compatible with PCI 2.2 specification
- Supports up to four external PCI masters
- 32-bit target and initiator operation
- 33–66 MHz operation with PCI bus to internal bus divider ratios of 1:1, 1:2, 1:3, 2:3, 1:4, and 1:5.
- Support for host and agent configurations.

The M54455EVB is designed to feature the MCF5445*x* as a PCI host. It provides four, 32-bit, 3.3V PCI slots. The IDSEL pins on each of the slots and the MCF5445*x* is connected to a different PCI_AD signal. Table 8 shows the IDSEL connections.

**Table 8. PCI IDSEL Assignments**

| PCI Slot | IDSEL Assignment |
|----------|------------------|
| Slot 0 | PCI_AD17 |
| Slot 1 | PCI_AD18 |
| Slot 2 | PCI_AD19 |
| Slot 3 | PCI_AD20 |
| MCF5445*x* | PCI_AD16 |

### 4.7.1 PCI Clocking

The MCF5445*x* does not output a PCI clock. The PCI controller of the MCF5445*x* is timed to the input reference clock on EXTAL. Therefore, the input reference clock to the MCF5445*x* is matched to each of the PCI slots on the M54455EVB to maintain clock phase alignment and ensure proper PCI timings.

The M54455EVB is designed to support 33- and 66-MHz 32-bit PCI cards. However, the speed of the PCI clocks and input clock is limited to that of the slowest device by logic on the M54455EVB. The frequency of these clocks is controlled by an input (S2) into the clock generator logic. The FPGA automatically adjusts this control signal based on the M66EN signal from each PCI slot. The S2 signal is also controllable by a jumper and a memory mapped register in the FPGA. See Section 4.4, "System Clocks" and Section 4.13, "FPGA" for more information. Table 5 provides a summary of the PCI bus speed controls.

### 4.7.2 PCI Power

The PCI is only available if an ATX supply is used to power the board. If the optional barrel power connector is used, then the ATX3V3 supply is not available. This also affects the clocking of the MCF5445*x*. The M66EN signal is pulled-up to the ATX3V3 supply. Without this supply, the M66EN signal is detected as a logic 0 and the CPU input reference frequency is forced to 33MHz.

## 4.7.3    PCI Arbitration

By default, the EVB uses the MCF5445*x* on-chip PCI arbiter, and the request/grant signals from the PCI slots are routed directly to the MCF5445*x*. The board does provide cut-trace options to allow you to route these PCI arbitration signals to the FPGA. It would then be left to you to implement an external arbitration scheme in the FPGA.

The following figures describe how to alter the M54455EVB to route the PCI arbitration signals to the FPGA. Reference designators for the cut-trace board footprints are CT1-CT10. CT1-CT2, CT5-CT7 and CT9 can be found near the PCI slots (J14, J15, J16, J17), and CT8, CT10, CT3 and CT4 can be found near the MCF5445*x* (U1).
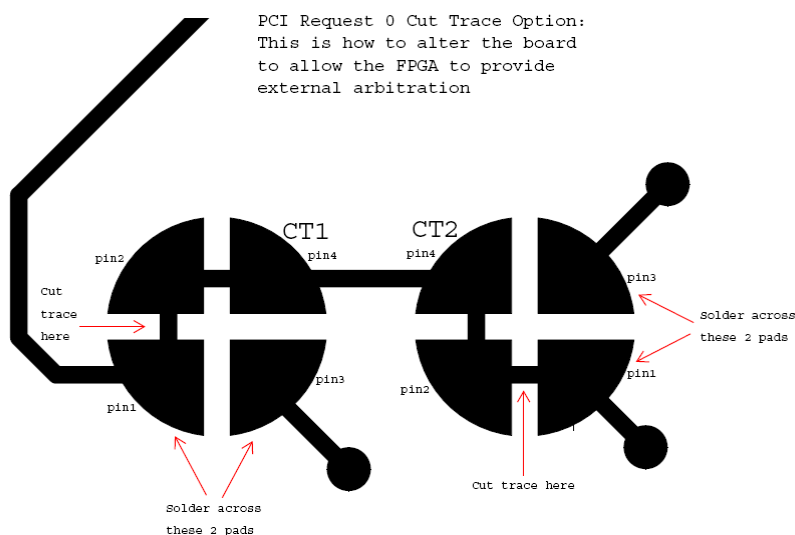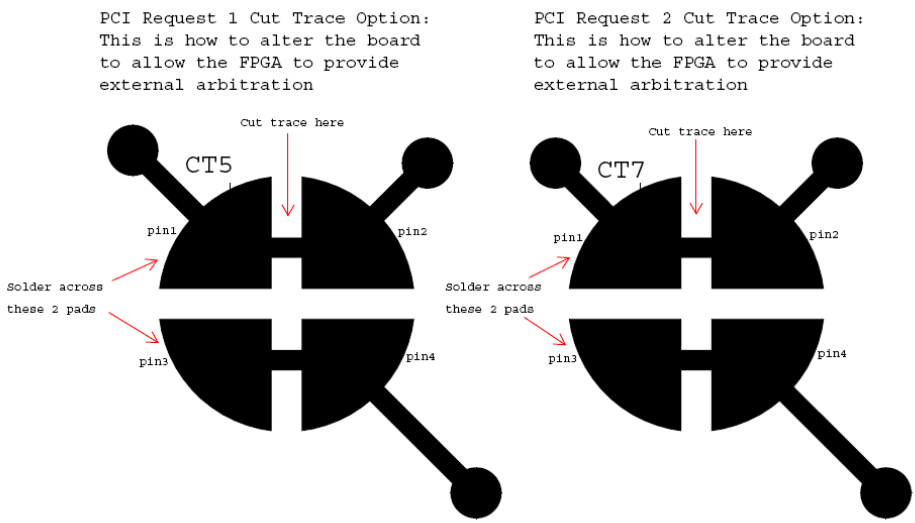


**Figure 6. PCI Request 0 Cut Trace Option—Use FPGA for Arbitration**

**Figure 7. PCI Request 1 and Request 2 Cut Trace Option—Use FPGA for Arbitration**



**Figure 8. PCI Request 3 Cut Trace Option—Use FPGA for Arbitration**

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PCI Grant 0 Cut Trace Option:
This is how to alter the board
to allow the FPGA to provide
external arbitration

**Figure 9. PCI Grant 0 Cut Trace Option—Use FPGA for Arbitration**

PCI Grant 1 Cut Trace Option:
This is how to alter the board
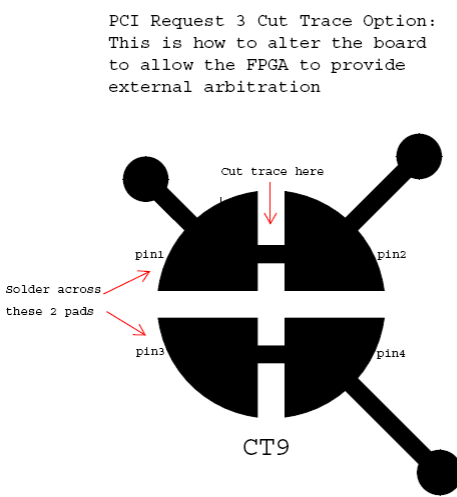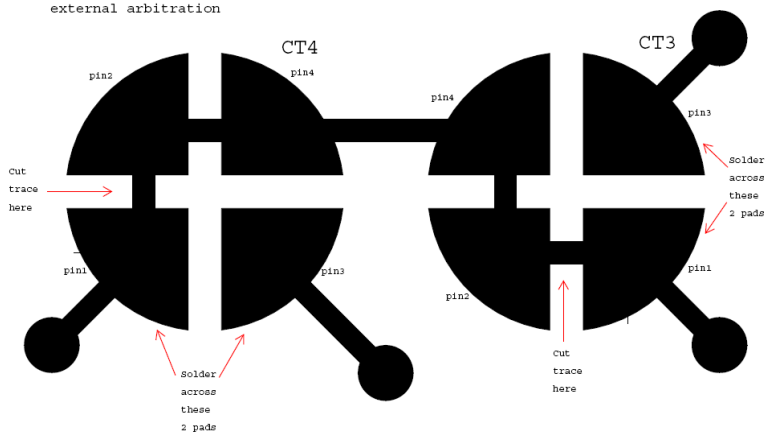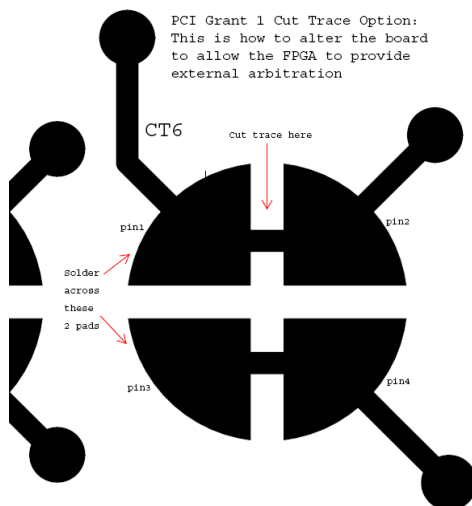to allow the FPGA to provide
external arbitration

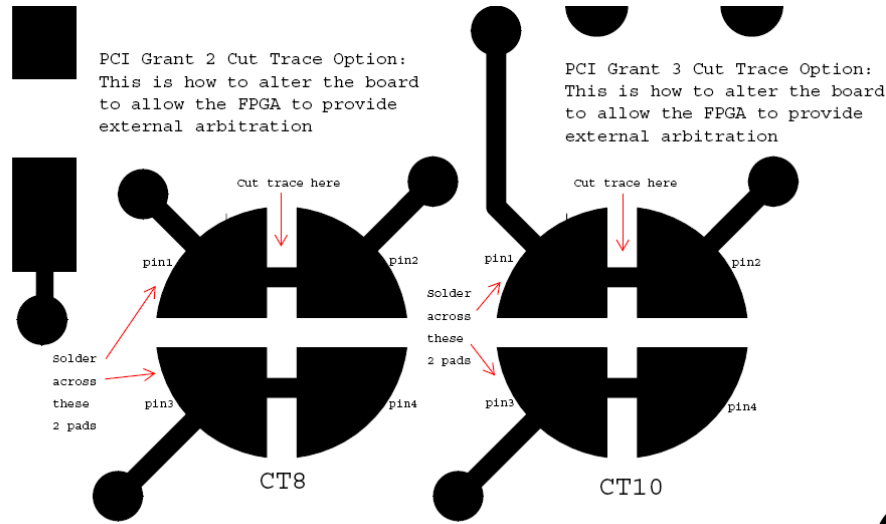**Figure 10. PCI Grant 1 Cut Trace Option—Use FPGA for Arbitration**

**Figure 11. PCI Grant 2 and Grant 3 Cut Trace Option—Use FPGA for Arbitration**

## 4.7.4   PCI Interrupts

The four interrupt signals on each PCI slot (INTA–INTD) are wire ORed together to form one interrupt source per slot. These four interrupt sources are routed to the system FPGA. The FPGA routes these interrupts to the MCF5445*x* as programmed by you. Please refer to Section 4.13.1, "FPGA Registers" for details on how to program the FPGA's interrupt controller.

## 4.8   Audio

A stereo audio codec is connected to the MCF5445*x*'s SSI interface. The SSI operates in I$^2$S mode to transfer audio data to and from a TLV320AIC23B device. The codec's control communications SPI channel is accessed through the MCF5445*x*'s DSPI interface using DSPI_PCS5. The line-in, line-out, and microphone inputs of the codec are brought to a 3.5-mm triple audio connector with PC-99 standard color coding. Refer to Section 2.4, "I/O Back Panel" for location and connection information.

For accessibility ease, all the SSI signals from the MCF5445*x* are brought to a header, J910.

**Table 9. SSI Signals on J910**

| Signal Name | Pin | Pin | Signal Name |
|:-----------:|:---:|:---:|:-----------:|
| SSI_RXD | 1 | 2 | SSI_TXD |
| SSI_MCLK | 3 | 4 | SSI_BCLK |
| SSI_FS | 5 | 6 | GND |

## 4.9    BDM and JTAG

The primary debug port on the MCF5445*x* is referred to as the background debug module or BDM. The standard 26-pin BDM header (J24) is provided on the M54455EVB for attachment of an external BDM control interface. However, the M54455EVB also features a built-in P&E USB ColdFire Multilink. This interface is brought out to the I/O back panel to a standard Type-B USB receptacle. Refer to Section 2.4, "I/O Back Panel" for the location of the connector. This allows for run-control debugging with a standard USB cable (provided in the M54455EVB kit).

The MCF5445*x* also features IEEE 1149.1 Test Access Port (JTAG) test logic that can be used for boundary-scan testability. The access pins for JTAG are multiplexed over the BDM control signals and are available on J24.

The JTAG_EN input signal to the MCF5445*x* determines the debug mode: BDM or JTAG. This signal is controllable by JP903 as shown below.

**Table 10. Debug Mode Selection**

| JP903 Setting | Debug Mode |
|---------------|------------|
| Shunt on 1-2  | JTAG       |
| Shunt on 2-3  | BDM        |

The TCLK and PSTCLK signals are the only two multiplexed signals that switch input/output state depending on which debug mode is selected. In BDM mode, the PSTCLK is an output from the MCF5445*x* to the external BDM control interface. In JTAG mode, TCLK is the test clock input. The standard 26-pin BDM header defines pin 24 as PSTCLK. A common practice is to place TCLK on pin 6 of this header. JP904 is available to control the routing of the multiplexed TCLK_PSTCLK signal to the 26-pin debug header (J24) as shown below.

**Table 11. TCLK/PSTCLK Routing Control**

| JP904 Setting | TCLK_PSTCLK Routing |
|---------------|---------------------|
| Shunt on 1-2  | TCLK/PSTCLK on J24[24][1] |
| Shunt on 2-3  | TCLK/PSTCLK on J24[6][2]  |

[1]   This setting is required if an external BDM control interface is used. If the on-board USB Multilink is used, this jumper setting is ignored.

[2]   This pin was previously specified by Freescale as Developer Reserved. External BDM control cables may be able to make use of this pin for JTAG instructions. There is a 10-kΩ pull-down resistor on the TCK_PSTCLK signal when this setting is selected.

## 4.10 USB

The MCF5445*x* integrates a USB 2.0 dual-role module with the following features:

- Support for host and device modes
- Support for full speed (FS) and low speed (LS) via an on-chip FS/LS transceiver
- Optional UTMI+ Low Pin Count Interface (ULPI) to support high speed (HS) transfers as well as FS and LS
- Uses 60 MHz reference clock based off of the system clock or from an external pin

The M54455EVB provides two interfaces to the single MCF5445*x* USB controller. Only one of these interfaces can be used at any one time.

### 4.10.1 On-Chip FS/LS Transceiver

The on-chip FS/LS transceiver signals are brought out to a type-A USB connector and are intended to be used for USB host applications. 15-kΩ pull-down and 33-Ω series resistors are provided on the D+ and D- data signals. Power to the connector is provided by an external dual-channel power distribution switch (MIC2026-1YM, U928). The B-channel of this device supplies the power for the type-A connector and is controlled by the MCF5445*x* USB_VBUS_EN output control signal.

When the on-chip FS/LS transceiver is used, the ULPI PHY can be put into its reset state. Refer to Section 4.14, "CPLD" for details.

### 4.10.2 ULPI PHY

The ULPI interface of the MCF5445*x* is also featured on the M54455EVB. An external ULPI physical layer device, the SMSC USB3300 (U927), connects directly to the MCF5445*x* ULPI interface. The USB signals from the ULPI PHY are brought out to a mini-AB USB connector. The ID pin on the mini-AB connector connects to the ULPI PHY's ID pin and indicates whether a host or device is connected. The ULPI PHY has an enable signal connected to the A-channel of the MIC2026 power distribution switch that is used to supply VBUS when operating as a host.

The RESET signal input to the ULPI PHY is controlled by the system's CPLD. Refer to Section 4.14, "CPLD" for details.

## 4.11 Ethernet

The MCF5445*x* processor features two Fast Ethernet controllers (FEC) with MII and RMII interface options. The M54455EVB provides a dual 10/100 Mbps Ethernet PHY to interface with the processor's FECs. The PHY operates in dual RMII mode. The board also provides two RJ45 connectors with integrated magnetics and LEDs.

The dual-port 10/100 Mbps provides a power-down feature for each port. You can control these power down signals via the system's CPLD.

**NOTE**

The FEC1 RMII interface signals on the MCF5445*x* are multiplexed with the upper eight bits of the ATA data bus. You must select between using the FEC1 interface or the full ATA interface. The system's CPLD provides control for this selection. Refer to Section 4.14, "CPLD" for details.

## 4.12 ATA

The M54455EVB provides a standard 40-pin ATA connector, as well as an external ATA data buffer that interfaces with the MCF5445*x* processor's ATA interface.

A device connected to the ATA Interface must be powered by a separate supply. Several peripheral power connectors are provided by the ATX power supply inside the case of the M54455EVB.

**NOTE**

Some of the ATA interface signals on the MCF5445*x* are multiplexed with the FEC1 RMII interface signals. To have access to the full 16-bit ATA data bus, the FEC1 interface must be disabled. The system's CPLD provides control for this selection. Refer to Section 4.14, "CPLD" for details.

## 4.13 FPGA

The M54455EVB FPGA is a Xilinx Spartan 3 FPGA that provides interrupt control for the four PCI slots and the pushbuttons SW6 and SW7. It also provides a buffered FlexBus interface to the external 256K × 16bit MRAM and an interface to a seven-segment display and two LEDs.

### 4.13.1 FPGA Registers

The FPGA implements several FlexBus accessible memory-mapped registers. Table 12 shows the memory map and the following sections provide details on each register.

**NOTE**

Use only 32-bit reads and writes to these registers.

**Table 12. FPGA Memory Map**

| Address | Register | Width (bits) | Access | Reset Value | Section/Page |
|---------|----------|--------------|--------|-------------|--------------|
| 0x0900_0000 | FPGA interrupt request enable register (FPGA_IRQEN) | 32 | R/W | 0x0000_0000 | 4.13.1.1/23 |
| 0x0900_0004 | FPGA interrupt request status register (FPGA_IRQSTATUS) | 32 | R | 0x0000_0000 | 4.13.1.2/23 |
| 0x0900_0008 | FPGA PCI clock configuration register (FPGA_PCICLKCFG) | 32 | R/W | 0x0000_0004 | 4.13.1.3/24 |
| 0x0900_000C | FPGA interrupt request routing register (FPGA_IRQROUTE) | 32 | R/W | 0x0000_0039 | 4.13.1.4/24 |
| 0x0900_0010 | FPGA version register (FPGA_VERSION) | 32 | R | 0x1A00_0102 | 4.13.1.5/25 |
| 0x0900_0014 | FPGA seven segment display register (FPGA_7SEGMENT) | 32 | R/W | 0x0000_0000 | 4.13.1.6/26 |
| 0x0900_0018 | FPGA LED control register (FPGA_LEDS) | 32 | R/W | 0x0000_0000 | 4.13.1.7/26 |

### 4.13.1.1 FPGA Interrupt Request Enable Register (FPGA_IRQEN)

Address: 0x0900_0000 (FPGA_IRQEN)

| | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|------|------|-----|-----|-----|----|
| R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | SW7 | SW6 | PCI | | | |
| W | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Figure 4-12. FPGA_IRQEN Register**

**Table 13. FPGA_IRQEN Field Descriptions**

| Field | Description |
|-------|-------------|
| 31–6 | Reserved, must be cleared. |
| 5<br>SW7 | Setting this bit allows the SW7 pushbutton interrupt source to be passed through to the IRQ line determined by FPGA_IRQROUTE.<br>1 SW7 interrupt is enabled<br>0 SW7 interrupt source does not assert an IRQ |
| 4<br>SW6 | Setting this bit allows the SW6 pushbutton interrupt source to be passed through to the IRQ line determined by FPGA_IRQROUTE.<br>1 SW6 interrupt is enabled<br>0 SW6 interrupt source does not assert an IRQ |
| 3–0<br>PCI | Setting these bits allow the corresponding PCI interrupt source to be passed through to the IRQ line determined by FPGA_IRQROUTE.<br>1 Corresponding PCI interrupt is enabled<br>0 Corresponding PCI interrupt source does not assert an IRQ |

### 4.13.1.2 FPGA Interrupt Request Status Register (FPGA_IRQSTATUS)

Address: 0x0900_0004 (FPGA_IRQSTATUS)

| | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|------|------|-----|-----|-----|----|
| R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | SW7 | SW6 | PCI | | | |
| W | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**Figure 13. FPGA_IRQSTATUS Register**

**Table 14. FPGA_IRQSTATUS Field Descriptions**

| Field | Description |
|-------|-------------|
| 31–6 | Reserved, must be cleared. |
| 5<br>SW7 | Indicates the SW7_b signal is asserted. This bit shows the status of the interrupt, even if FPGA_IRQEN[SW7] is cleared. |
| 4<br>SW6 | Indicates the SW6_b signal is asserted. This bit shows the status of the interrupt, even if FPGA_IRQEN[SW6] is cleared. |
| 3–0<br>PCI | Indicates the corresponding interrupt $\overline{\text{PCI\_IRQ}}$ line is asserted. These bits show the status of interrupt, even if the corresponding FPGA_IRQEN[PCI] bit is cleared. |

### 4.13.1.3 FPGA PCI Clock Configuration Register (FPGA_PCICLKCFG)

Address: 0x0900_0008 (PCI_CLK_CFG)

| | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | M66 EN | CLKGEN S2 | CLKGEN S2EN |
| W | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1[1] | 0 | 0 |

**Figure 14. FPGA_PCICLKCFG Register**

[1] This value is reset to 0 if not using the ATX power supply.

**Table 15. FPGA_PCICLKCFG Field Descriptions**

| Field | Description |
|---|---|
| 31–3 | Reserved, must be cleared. |
| 2 M66EN | State of the M66EN pin from the PCI slots.<br>0  33MHz card is installed in a PCI slot. The input clock and PCI clocks is 33MHz<br>1  Non 33MHz cards are installed. PCI speed is determined by CLKGENS2EN and/or external jumper on header H4[3:4] |
| 1 CLKGENS2 | State of the S2 control input to the CY22393 clock generator. For the S2 pin to assert, M66EN must be set, the jumper across pins 3 and 4 on H4 must be removed, and CLKGENS2EN must be set.<br>0  Input clock and PCI clocks are operating at 33MHz<br>1  Input clock and PCI clocks are operating at 66MHz |
| 0 CLKGENS2EN | Assert the S2 control input to the CY22393 clock generator. If the M66EN pin is pulled-low, this bit is ignored. A jumper shunt across H4[3:4] also overrides this setting and force 33MHz operation. The CLKGENS2 bit always reflects the current state of the S2 signal.<br>0  Set input clock and PCI clocks to 33MHz<br>1  Set input clock and PCI clocks to 66MHz |

### 4.13.1.4 FPGA Interrupt Request Routing Register (FPGA_IRQROUTE)

Address: 0x0900_000C (FPGA_IRQROUTE)

| | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | SW7 | | SW6 | | PCI | |
| W | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 |

**Figure 15. FPGA IRQROUTE Register**

**Table 16. FPGA_IRQROUTE Field Descriptions**

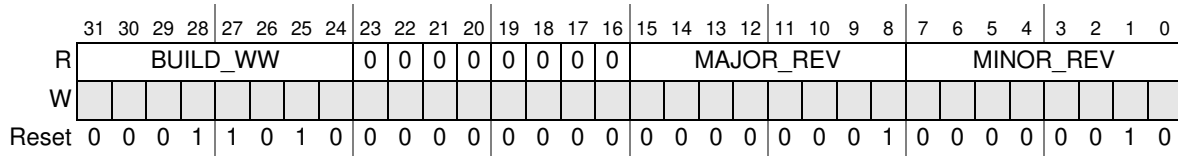| Field | Description |
|---|---|
| 31–6 | Reserved, must be cleared. |
| 5–4 SW7 | SW7 IRQ selection (pushbutton)<br>00  IRQ1<br>01  IRQ3<br>10  IRQ4<br>11  IRQ7 |

**Table 16. FPGA_IRQROUTE Field Descriptions (continued)**

| Field | Description |
|---|---|
| 3–2<br>SW6 | SW6 IRQ selection (pushbutton)<br>00  IRQ1<br>01  IRQ3<br>10  IRQ4<br>11  IRQ7 |
| 1–0<br>PCI | PCI IRQ selection<br>00  IRQ1<br>01  IRQ3<br>10  IRQ4<br>11  IRQ7 |

## 4.13.1.5   FPGA Version Register (FPGA_VERSION)

The FPGA_VERSION register reflects the version of the FPGA code image.

Address:  0x0900_0010 (FPGA_VERSION)

| | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R | BUILD_WW | | | | | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | MAJOR_REV | | | | | | | | MINOR_REV | | | | | | | |
| W | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

**Figure 16. FPGA Version Register**

**Table 17. FPGA_VERSION Field Descriptions**

| Field | Description |
|---|---|
| 31–24<br>BUILD_WW | Build date work week |
| 23–16 | Reserved, must be cleared. |
| 15–8<br>MAJOR_REV | Major revision number.<br>Example: Revision 1.2 of the FPGA code. MAJOR_REV = 0x01, MINOR_REV = 0x02 |
| 7–0<br>MINOR_REV | Minor revision number.<br>Example: Revision 1.2 of the FPGA code. MAJOR_REV = 0x01, MINOR_REV = 0x02 |