M5450
M5451

LED DISPLAY DRIVERS

FEATURES SUMMARY

- M5450 34 OUTPUTS/15mA SINK
- M5451 35 OUTPUTS/15mA SINK
- CURRENT GENERATOR OUTPUTS (NO EXTERNAL RESISTORS REQUIRED)
- CONTINUOUS BRIGHTNESS CONTROL
- SERIAL DATA INPUT
- ENABLE (ON M5450)
- WIDE SUPPLY VOLTAGE OPERATION
- TTL COMPATIBILITY

Application Examples:

- MICROPROCESSOR DISPLAYS
- INDUSTRIAL CONTROL INDICATOR
- RELAY DRIVER
- INSTRUMENTATION READOUTS

DESCRIPTION

The M5450 and M5451 are monolithic MOS integrated circuits produced with an N-channel silicon gate technology. They are available in 40-pin dual in-line plastic packages.

A single pin controls the LED display brightness by setting a reference current through a variable resistor connected to V_{DD} or to a separate supply of 13.2V maximum.

Figure 1. Packages

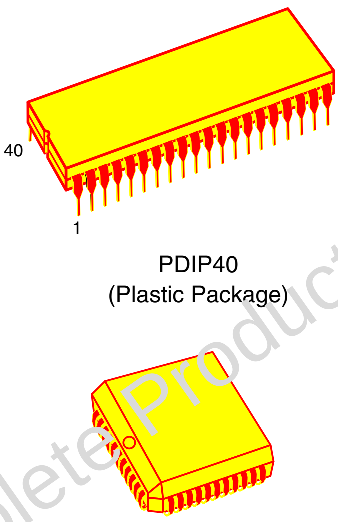


Figure 2. Pin Connection

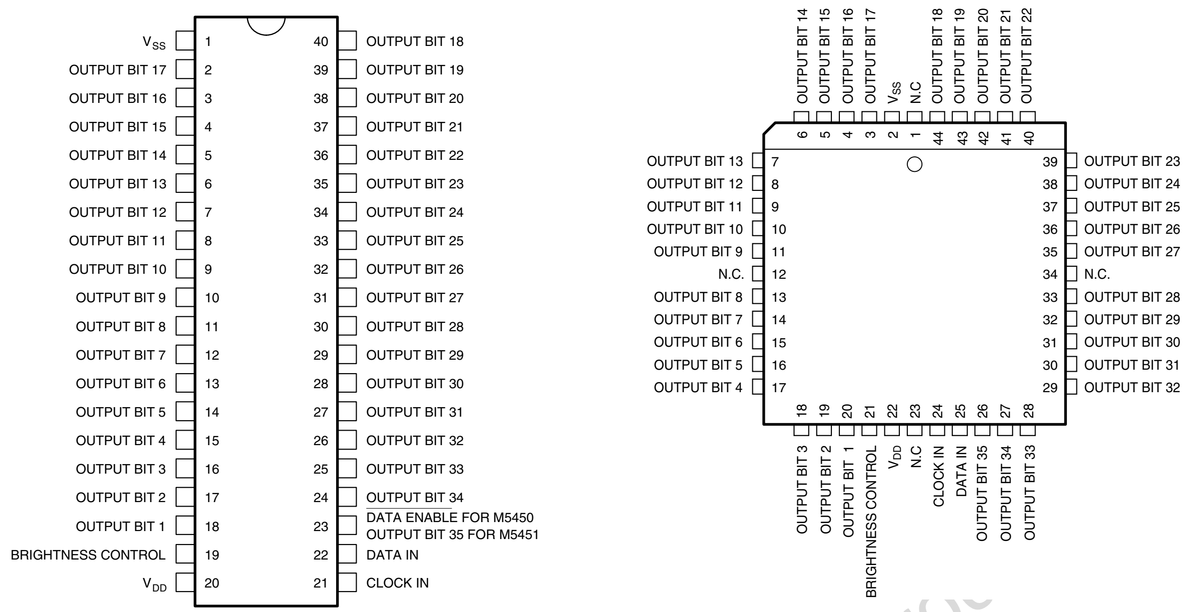


Figure 3. Block Diagram

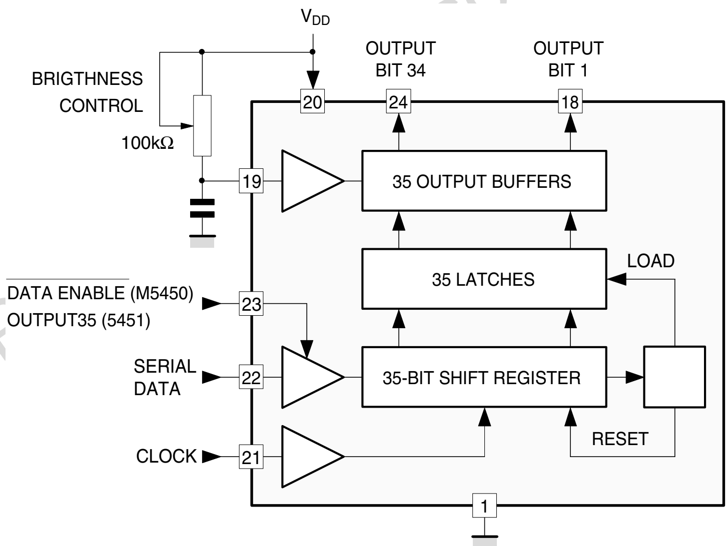


Table 1. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	– 0.3 to 15	V
V_I	Input Voltage	– 0.3 to 15	V
$V_{O(off)}$	Off State Output Voltage	15	V
I_O	Output Sink Current	40	mA
P_{TOT}	Total Package Power Dissipation at 25°C	1	W
	Total Package Power Dissipation at 85°C	560	mW
T_j	Junction Temperature	150	°C
T_{OP}	Operating Temperature Range	– 25 to 85	°C
T_{STG}	Storage Temperature Range	– 65 to 150	°C

Note: Stresses above those listed under "Absolute Maximum Ratings" may causes permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

FUNCTIONAL DESCRIPTION

Both the M5450 and the M5451 are specially designed to operate 4 or 5-digit alphanumeric displays with minimal interface with the display and the data source. Serial data transfer from the data source to the display driver is accomplished with 2 signals, serial data and clock. Using a format of a leading "1" followed by the 35 data bits allows data transfer without an additional load signal. The 35 data bits are latched after the 36th bit is complete, thus providing non-multiplexed, direct drive to the display.

Outputs change only if the serial data bits differ from the previous time.

Display brightness is determined by control of the output current LED displays.

A 1nF capacitor should be connected to brightness control, pin 19, to prevent possible oscillations.

A block diagram is shown in Figure 3. For the M5450 a DATA ENABLE is used instead of the 35th output. The DATA ENABLE input is a metal option for the M5450.

The output current is typically 20 times greater than the current into pin 19, which is set by an external variable resistor. There is an internal limiting resistor of 400W nominal value.

Figure 4 shows the input data format. A start bit of logical "1" precedes the 35 bits of data. At the 36th clock a LOAD signal is generated synchronously with the high state of the clock, which loads the 35 bits of the shift registers into the latches.

At the low state of the clock a RESET signal is generated which clears all the shift registers for the next set of data. The shift registers are static master-slave configurations. There is no clear for the master portion of the first shift register, thus allowing continuous operation.

There must be a complete set of 36 clocks or the shift registers will not clear.

When power is first applied to the chip an internal power ON reset signal is generated which resets all registers and all latches. The START bit and the first clock return the chip to its normal operation.

Bit 1 is the first bit following the start bit and it will appear on Pin 18. A logical "1" at the input will turn on the appropriate LED.

Figure 5 shows the timing relationship between Data, Clock and DATA ENABLE.

A max clock frequency of 0.5MHz is assumed. For applications where a lesser number of outputs are used, it is possible to either increase the current per output or operate the part at higher than 1V V_{OUT}.

The following equation can be used for calculations.

T_j = [(V_{OUT}) (I_{LED}) (No. of segments) + (V_{DD} × 7mA)] (124°C/W) + T_{amb}

where :

T_j = junction temperature (150°C max)

V_{OUT} = the voltage at the LED driver outputs

I_{LED} = the LED current

124°C/W = thermal coefficient of the package

T_{amb} = ambient temperature

The above equation was used to plot Figure 6, Figure 7 and Figure 8.

Table 2. Static Electrical Characteristics
(T_{amb} within operating range, V_{DD} = 4.75V to 13.2V, V_{SS} = 0V, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		4.75		13.2	V
I_{DD}	Supply Current	V_{DD} = 13.2V			7	mA
V_I	Input Voltage Logical "0" Level	± 10µA Input Bias	- 0.3		0.8	V
	Logical "1" Level	$4.75 \leq V_{DD} \leq 5.25$	2.2		V_{DD}	V
		V_{DD} > 5.25	V_{DD} - 2		V_{DD}	V
I_B	Brightness Input Current (note 2)		0		0.75	mA
V_B	Brightness Input Voltage (pin 19)	Input Current = 750µA, T_{amb} = 25°C	3		4.3	V
$V_{O(off)}$	Off State Out. Voltage				13.2	V
I_O	Out. Sink Current (note 3)					
	Segment OFF	V_O = 3V			10	µA
	Segment ON	V_O = 1V (note 4)				
		Brightness In. = 0µA	0		10	µA
		Brightness In. = 100µ	2	27	4	mA
		Brightness In. = 750µA	12	15	25	mA
f_{clock}	Input Clock Frequency		0		0.5	MHz
I_O	Output Matching (note 1)				± 20	%

Note: 1. Output matching is calculated as the percent variation from $I_{MAX} + I_{MIN}/2$.
2. With a fixed resistor on the brightness input some variation in brightness will occur from one device to another.
3. Absolute maximum for each output should be limited to 40mA.
4. The V_O voltage should be regulated by the user. See Figure 7 and Figure 8 for allowable VO versus IO operation.

Figure 4. Input Data Format

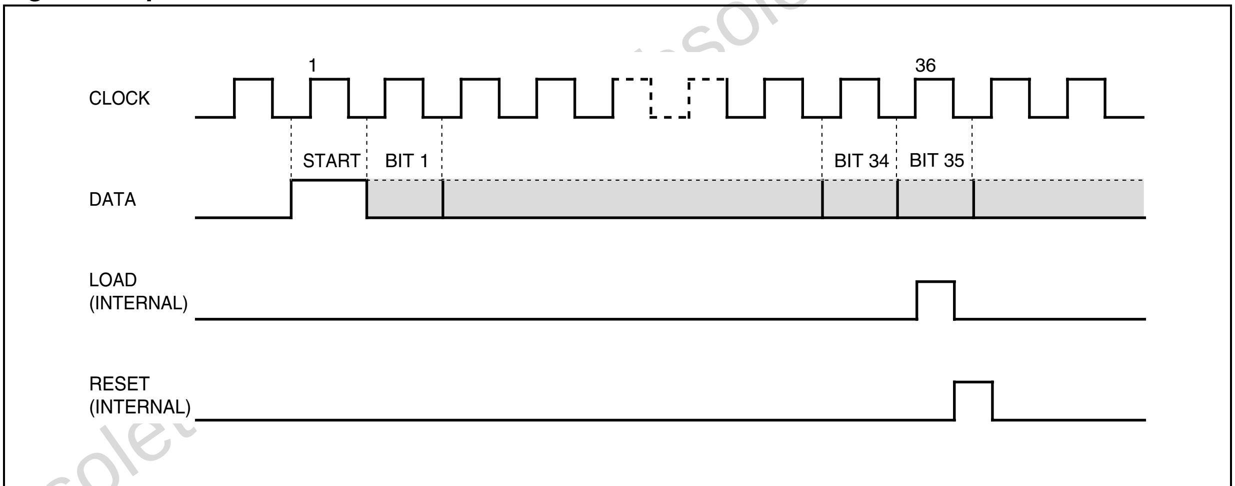


Figure 5.

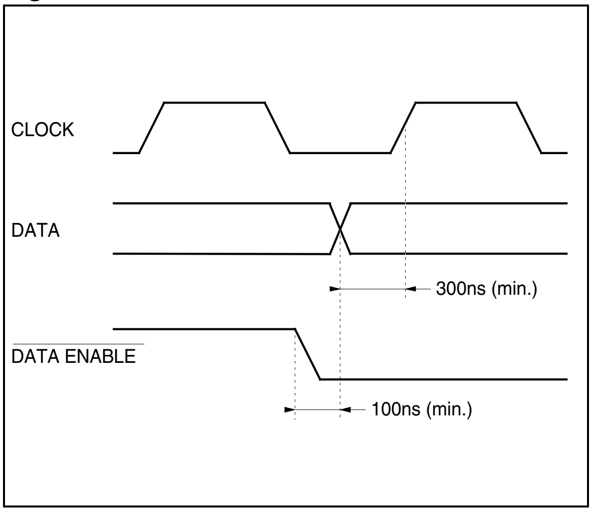


Figure 6.

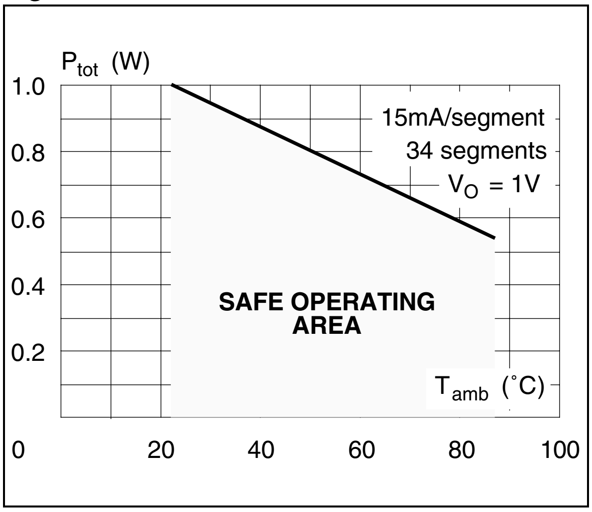


Figure 7.

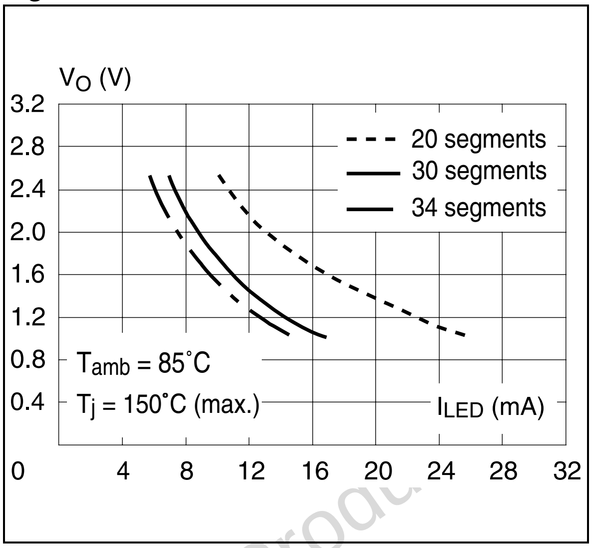
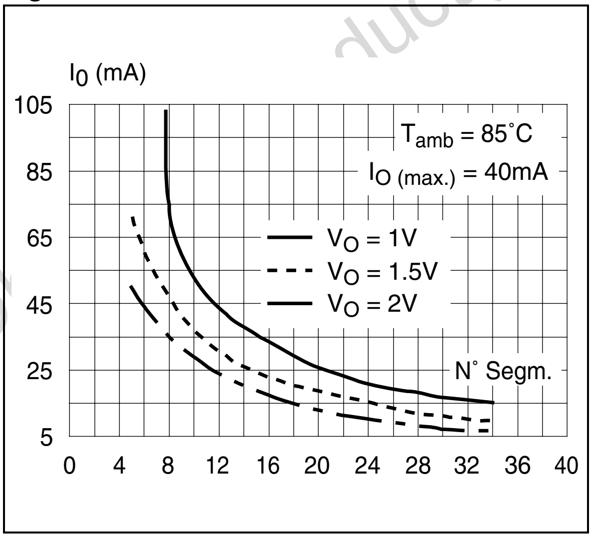


Figure 8.



TYPICAL APPLICATIONS

Figure 9. Basic Electronically Tuned Radio Or Tv System

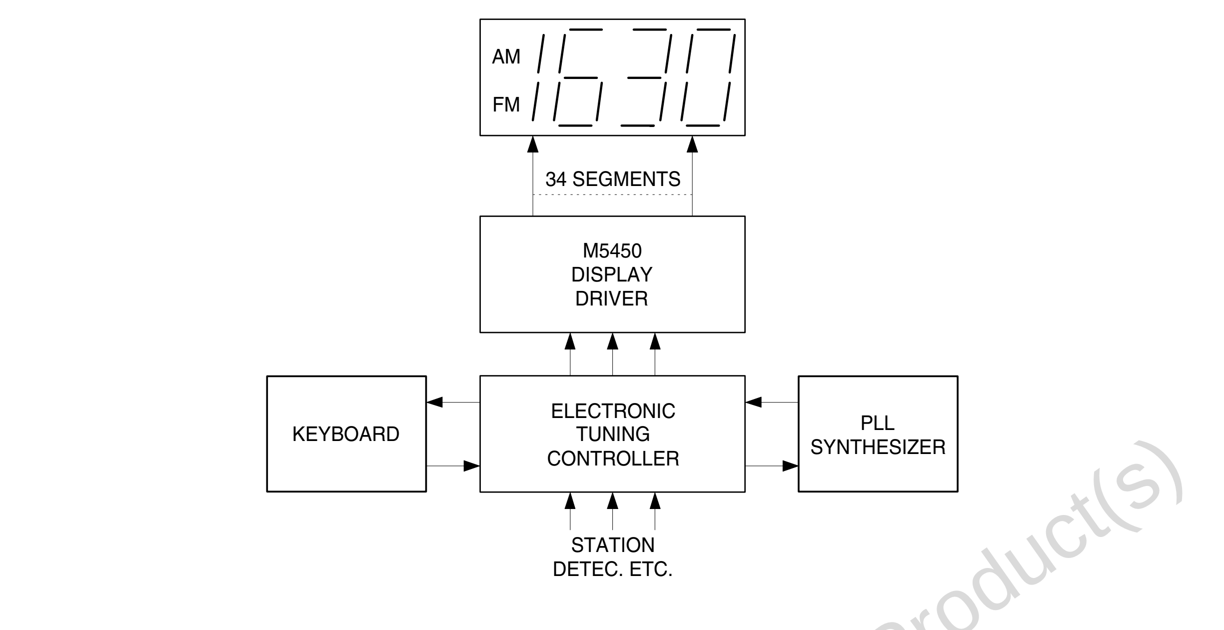
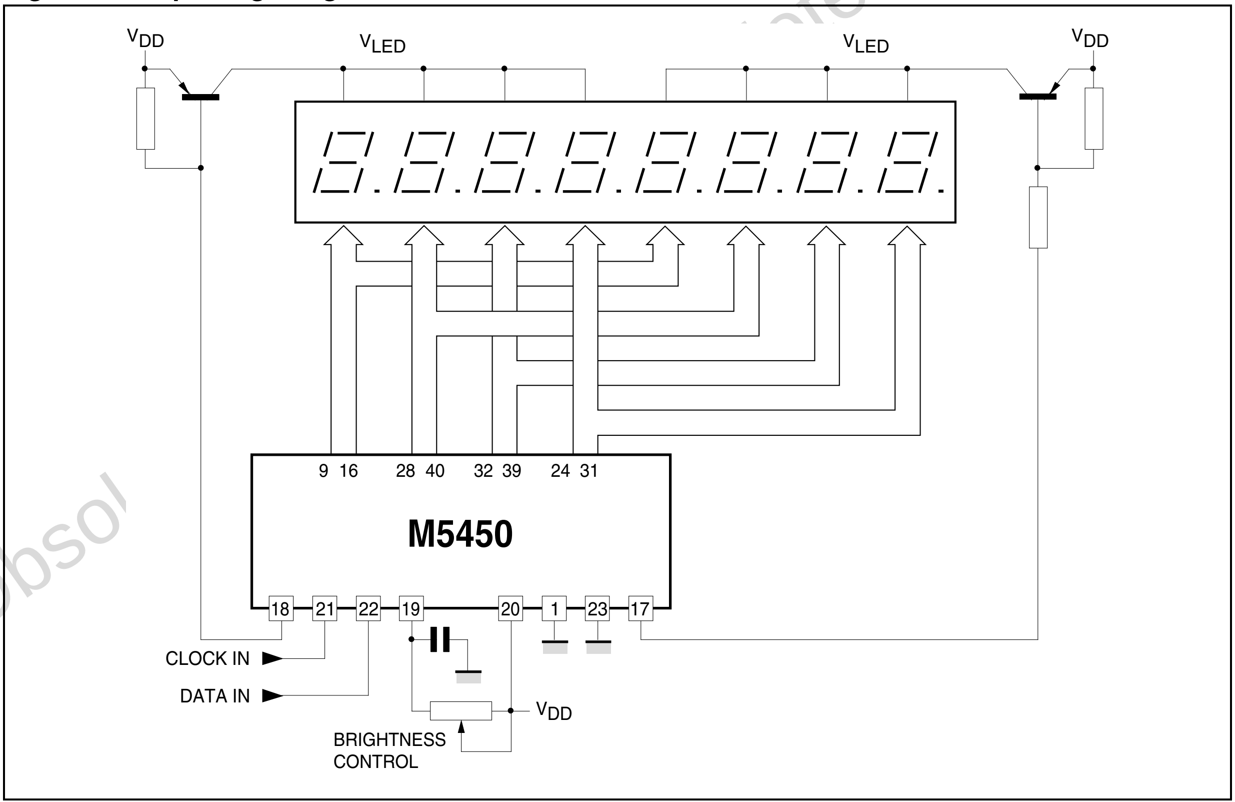


Figure 10. Duplexing 8 Digits With One M5450

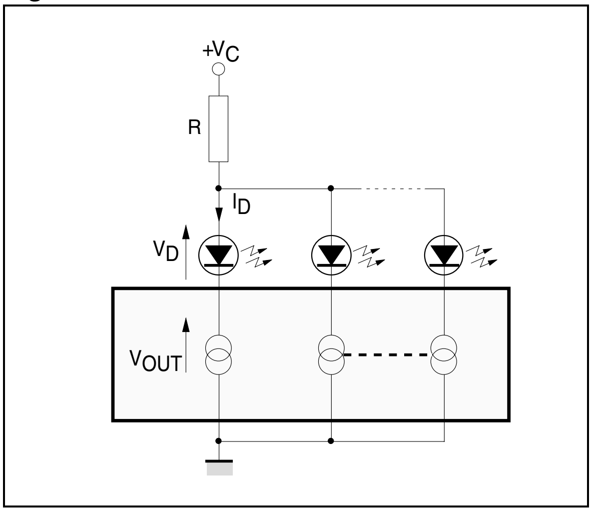


POWER DISSIPATION OF THE IC

The power dissipation of the IC can be limited using different configurations.

Figure 11- In the application R must be chosen taking into account the worst operating conditions.

Figure 11.



R is determined by the maximum number of segments activated

$$R = \frac{V_C - V_{DMAX} - V_{OMIN}}{N_{MAX} I_D}$$

The worst case condition for the device is when roughly half of the maximum number of segments are activated.

It must be checked that the total power dissipation does not exceed the absolute maximum ratings of the device.

In critical cases more resistors can be used in conjunction with groups of segments.

In this case the current variation in the single resistor is reduced and P_{tot} limited.

Figure 12 - In this configuration the drop on the serial connected diodes is quite stable if the diodes are properly chosen.

The total power dissipation of the IC depends, in a first approximation, only on the number of segments activated.

Figure 12.

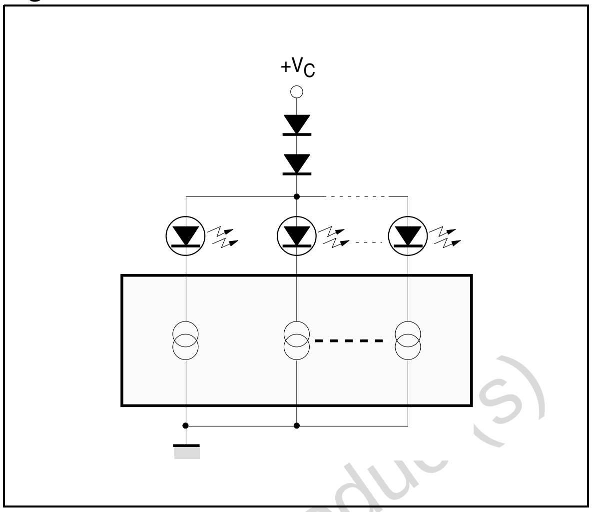
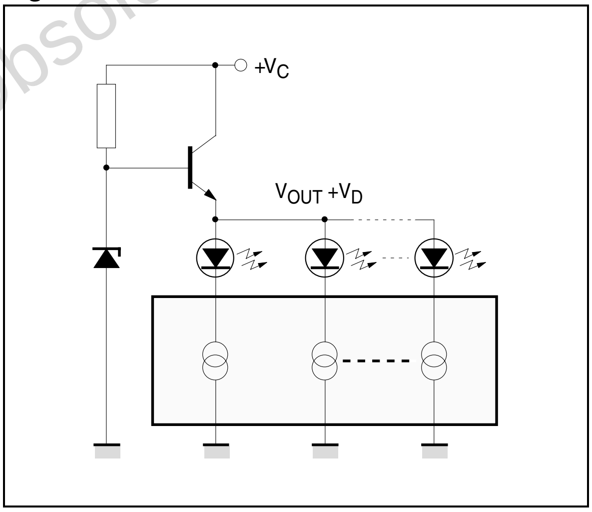


Figure 13 - In this configuration $V_{OUT} + V_D$ is constant. The total power dissipation of the IC depends only on the number of segments activated.

Figure 13.



PART NUMBERING

Table 3. Order Codes

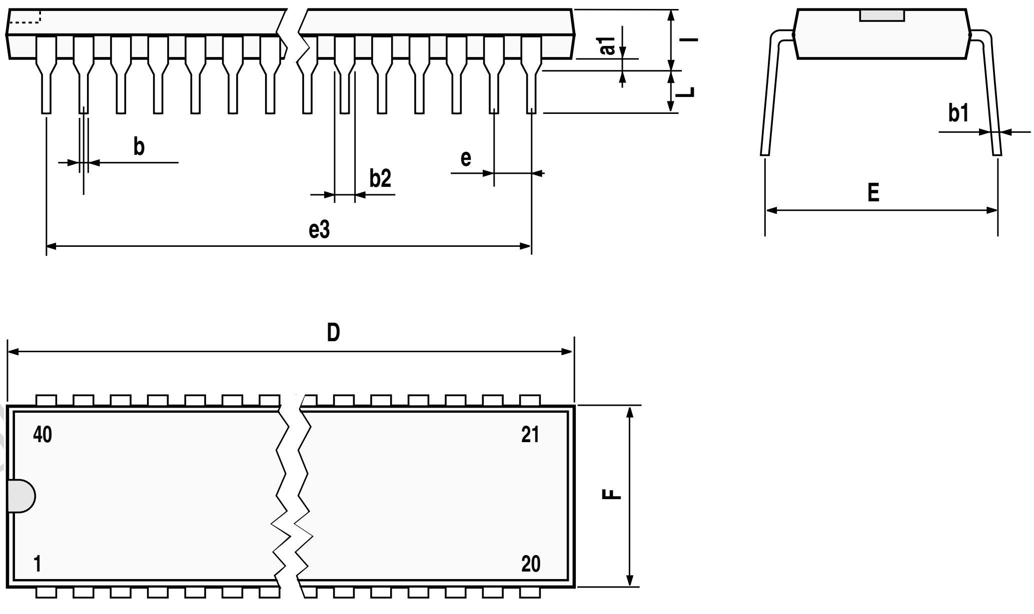
Part Number	Package	Temperature Range
M5450B7/M5451B7	PDIP40	-25 to 85 °C
M5451Q	PLCC44	-25 to 85 °C

PACKAGE MECHANICAL

Table 4. PDIP40 - Mechanical Data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
a1		0.63			0.025	
b		0.45			0.018	
b1	0.23		0.31	0.009		0.012
b2		1.27			0.050	
D			52.58			2.070
E	15.2		16.68	0.598		0.657
e		2.54			0.100	
e3		48.26			1.900	
F			14.1			0.555
i		4.445			0.175	
L		3.3			0.130	

Figure 14. PDIP40 - Package Dimensions

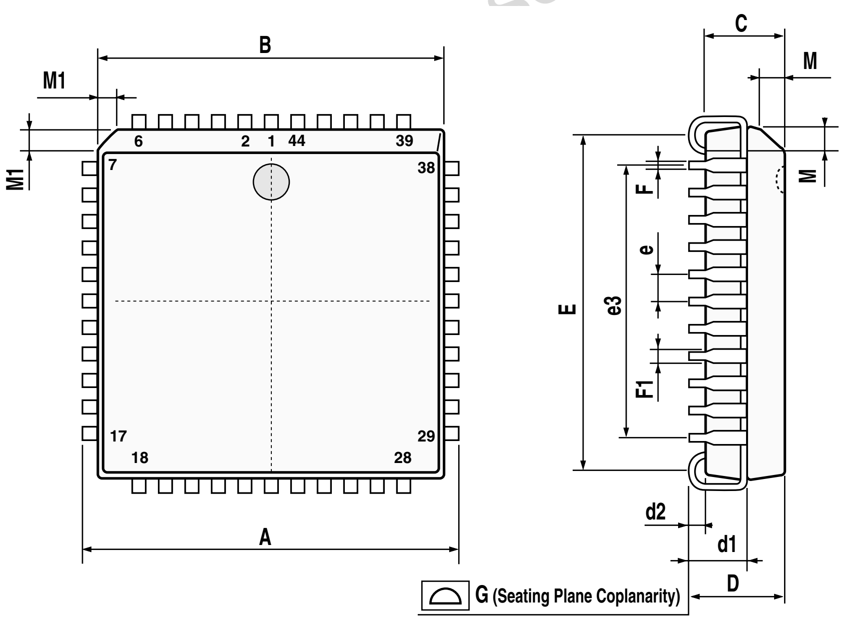


Note: Drawing is not to scale

Table 5. PLCC44 - Mechanical Data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A	17.4		17.65	0.685		0.695
B	16.51		16.65	0.650		0.656
C	3.65		3.7	0.144		0.146
D	4.2		4.57	0.165		0.180
d1	2.59		2.74	0.102		0.108
d2		0.68			0.027	
E	14.99		16	0.590		0.630
e		1.27			0.050	
e3		12.7			0.500	
F		0.46			0.018	
F1		0.71			0.028	
G			0.101			0.004
M		1.16			0.046	
M1		1.14			0.045	

Figure 15. PLCC44 - Package Dimensions



Note: Drawing is not to scale.

REVISION HISTORY

Table 6. Revision History

Date	Revision	Description of Changes
September-1993	1	First Issue
14-Mar-2004	2	Stylesheet update. No content change.