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M5481

LED DISPLAY DRIVER

FEATURES SUMMARY

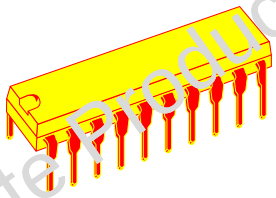
- 2 DIGIT LED DRIVER (14 segments)
- CURRENT GENERATOR OUTPUTS (no registor required)
- CONTINUOUS BRIGHTNESS CONTROL
- SERIAL DATA INPUT
- DATA ENABLE
- WIDE SUPPLY VOLTAGE OPERATION
- TLL COMPATIBILITY
- APPLICATION EXAMPLES
- MICROPROCESSOR DISPLAYS
- INDUSTRIAL CONTROL INDICATOR
- RELAY DRIVER
- INSTRUMENTATION READOUTS

DESCRIPTION

The M5481 is a monolithic MOS integrated circuit produced with a N-channel silicon gate technology. It uses the M5450 die packaged in a 20-pin plastic package copper frame, making it ideal for a 1-digit display. A single pin controls the LED display brightness by setting a reference current through a variable resistor connected either to V_{DD} or to a separate supply of 13.2V maximum.

The M5481 is a pin-to-pin replacement of the NS MM 5481.

Figure 1. Package



PDIP20
(Plastic package)

Figure 2. Pin Connections

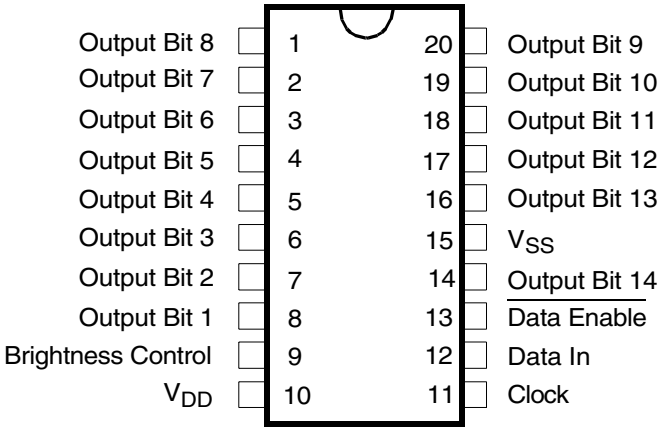


Figure 3. Block Diagram

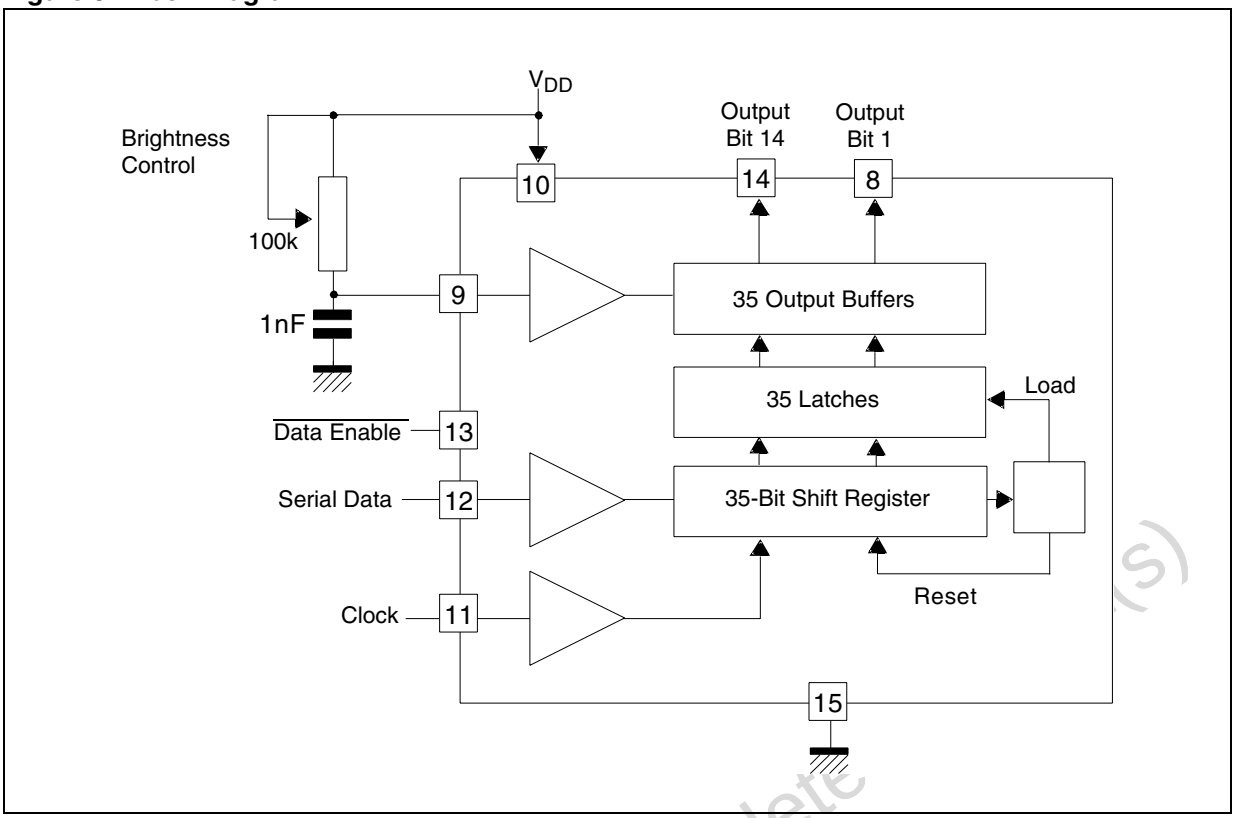


Table 1. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	– 0.3 to 15	V
V_I	Input Voltage	– 0.3 to 15	V
$V_{O(off)}$	Off State Output Voltage	15	V
I_O	Output Sink Current	40	mA
P_{TOT}	Total Package Power Dissipation at 25°C	1.5	W
	Total Package Power Dissipation at 85°C	800	mW
T_j	Junction Temperature	150	°C
T_{OP}	Operating Temperature Range	– 25 to 85	°C
T_{STG}	Storage Temperature Range	– 65 to 150	°C

Note: Stresses exceeding those listed under “Absolute Maximum Ratings” may cause permanent damage to the device and affect its reliability.

Table 2. Static Electrical Characteristics
(T_{amb} within operating range, V_{DD} = 4.75V to 13.2V, V_{SS} = 0V, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		4.5		13.2	V
I_{DD}	Supply Current	V_{DD} = 13.2V			7	mA
V_I	Input Voltage Logical "0" Level	± 10µA Input Bias	- 0.3		0.8	V
	Logical "1" Level	4.75 ≤ V_{DD} ≤ 5.25	2.2		V_{DD}	V
		V_{DD} > 5.25	V_{DD} - 2		V_{DD}	V
I_B	Brightness Input Current (note 2)		0		0.75	mA
V_B	Brightness Input Voltage (pin 9)	Input Current = 750µA, T_{amb} = 25°C	3		4.3	V
$V_{O(off)}$	Off State Out. Voltage				13.2	V
I_O	Out. Sink Current (note 3)					
	Segment OFF	V_O = 3V			10	µA
	Segment ON	V_O = 1V (note 4)				
		Brightness In. = 0µA	0		10	µA
		Brightness In. = 100µA	2	2,7	4	mA
		Brightness In. = 750µA	12	15	25	mA
f_{clock}	Input Clock Frequency		0		0.5	MHz
I_O	Output Matching (note 1)				± 20	%

Note: 1. Output matching is calculated as the percent variation from $I_{MAX} + I_{MIN}/2$.
2. With a fixed resistor on the brightness input some variation in brightness will occur from one device to another.
3. Absolute maximum for each output should be limited to 40mA.
4. The V_O voltage should be regulated by the user.

FUNCTIONAL DESCRIPTION

The M5481 uses the M5450 die which is packaged to operate 2-digit alphanumeric displays with minimal interface with the display and the data source.

Serial data transfer from the data source to the display driver is accomplished with 2 signals, serial data and clock. using a format of a leading “1” followed by the 35 data bits allows data transfer without an additional load signal.

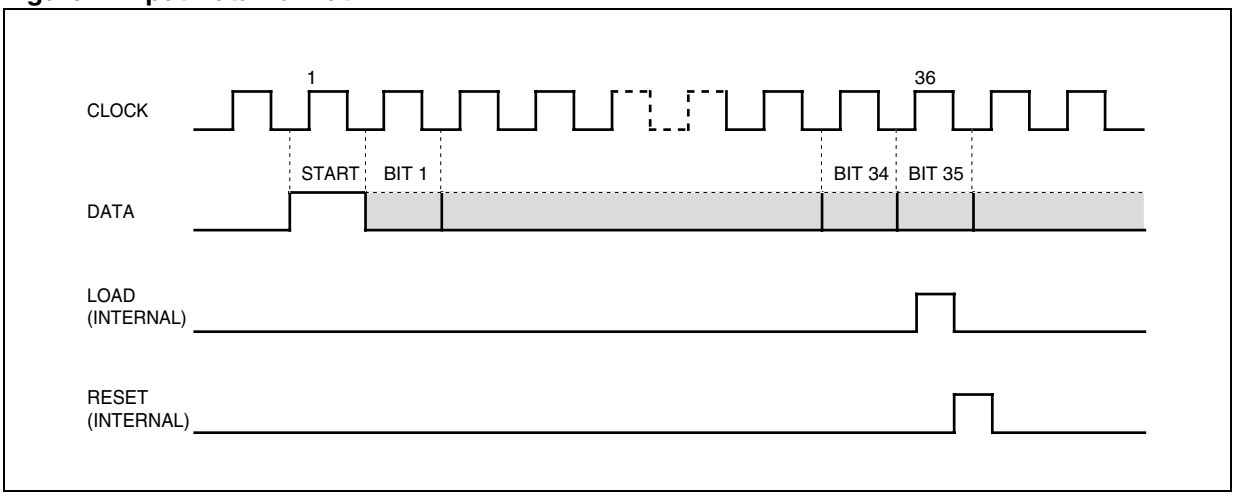
The 35 data bits are latched after the 36th bit is complete, thus providing non-multiplexed, direct drive to the display. Outputs change only if the serial data bits differ from the previous time. Display brightness is determined by control of the output current for LED displays. A 1nF capacitor should be connected to brightness control (pin 9) to prevent possible oscillations.

A block diagram is shown on Figure 3. The output current is typically 20 times greater than the current into pin 9, which is set by an external variable resistor.

The latter is an internal limiting resistor of 400Ω nominal value.

Figure 4 shows the input data format. A start bit of logical “1” precedes the 35 bits of data. At the 36th clock a LOAD is generated synchronously with the high state of the clock, which loads the 35 bits of the shift registers into the latches.

Figure 4. Input Data Format



At the low state of the clock a RESET signal is generated which clears all the shift registers for the next set of data. The shift registers are static master slave configurations. There is no clear for the master portion of the first shift register, thus allowing continuous operation.

There must be a complete set of 36 clocks or the shift registers will not clear.

When power is first applied to the chip an internal power ON reset signal is generated which resets all registers and all latches. The START bit and the first clock reset the chip to its normal operation.

Figure 5 shows the timing relationships between Data, Clock and DATA ENABLE.

A maximum clock frequency of 0.5MHz is assumed.

Table 3 shows the Output Data Format for the M5481. Because it uses only 14 of the possible outputs, 21 of the bits (including bit 35 which was already unused in the M5450) are “Don’t Cares” .

For applications where a lesser number of outputs are used it is possible to either increase the current per output or operate the part at higher than 1V V_{out}.

The following equation can be used for calculations.

$T_j = [(V_{out}) (I_{LED}) (\text{No. of segments}) + V_{DD} \times 7mA] \times (80°C/W) + T_{amb}$

where:

T_j = junction temperature (150°Cmax)

V_{out} = voltage at the LED driver outputs

I_{LED} = LED current

80°C/W = thermal coefficient of the package

T_{amb} = ambiant temperature

Figure 5.

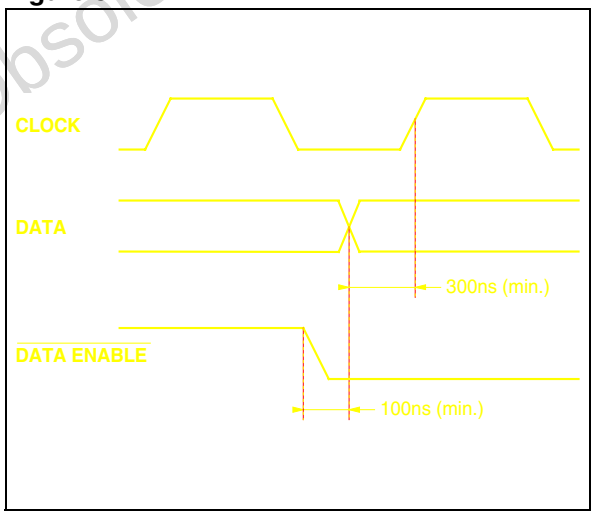


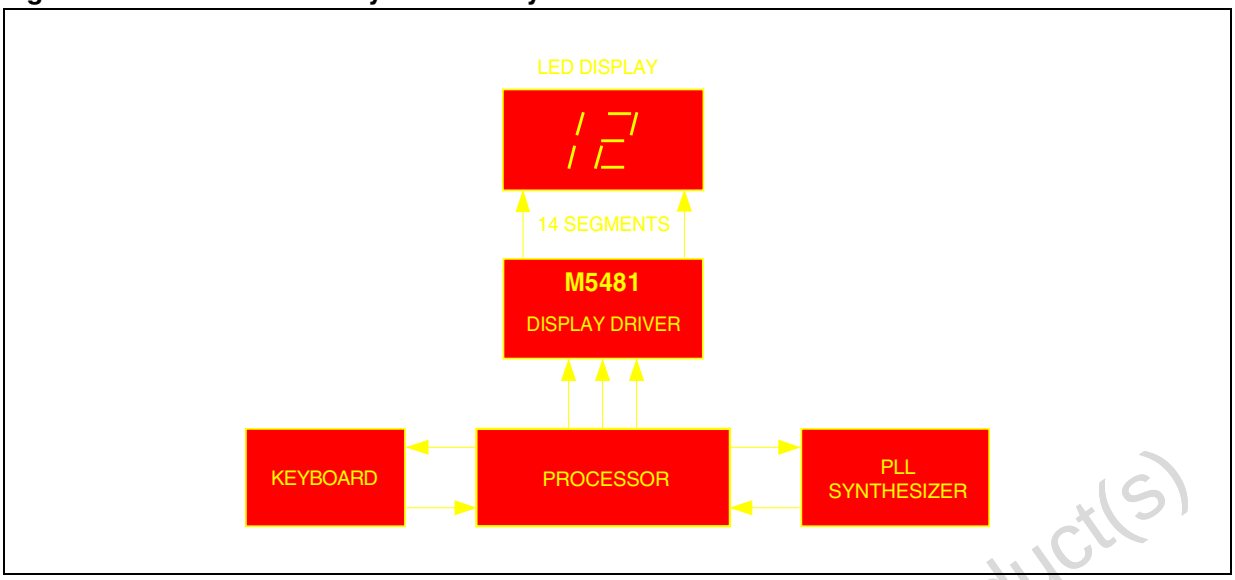
Table 3. Serial Data Bus / Outputs Correspondance

5451	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	START
5481	X	X	X	X	X	14	13	X	X	X	X	12	11	10	9	X	X	X	START

5450	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	START
5481	X	8	7	6	5	X	X	X	X	4	3	2	1	X	X	X	X	START

TYPICAL APPLICATION

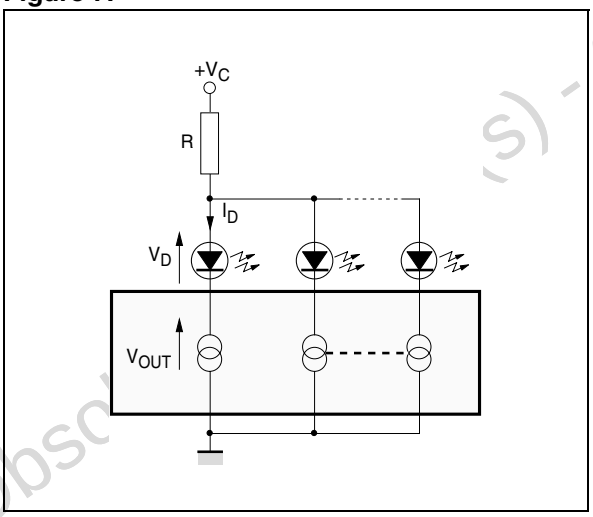
Figure 6. BASIC electronically tuned TV system



POWER DISSIPATION OF THE IC

The power dissipation of the IC can be limited using different configurations.

Figure 7.



In this application R must be chosen taking into account the worst operating conditions.

R is determined by the maximum number of segments activated.

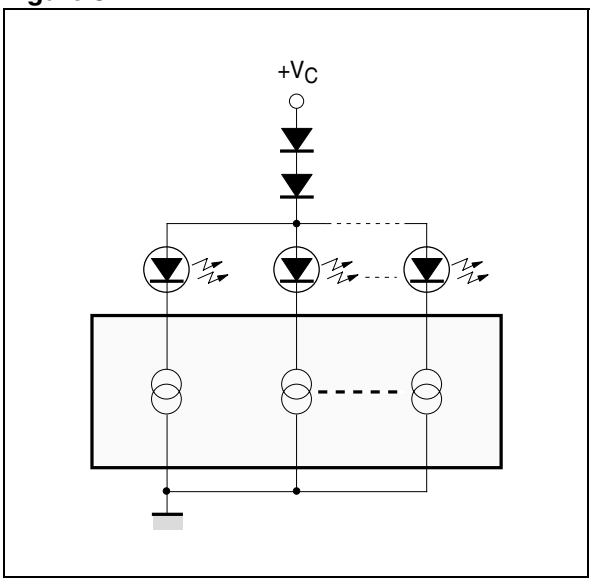
$$R = \frac{V_C - V_{DMAX} - V_{OMIN}}{N_{MAX} L_D}$$

The worst case condition for the device is when roughly half of the maximum number of segments are activated.

It must be checked that the total power dissipation does not exceed the absolute maximum ratings of the device.

In critical cases more resistors can be used in conjunction with groups of segments.In this case the current variation in the single resistor is reduced and P_{tot} limited.

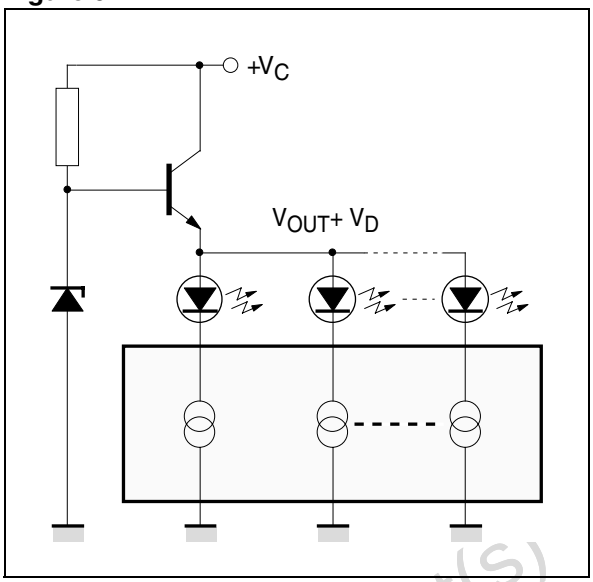
Figure 8.



In this configuration the drop on the serial connected diodes is quite stable if the diodes are properly chosen.

The total power dissipation of the IC depends only, in first approximation, on the number of segments activated.

Figure 9.



In this configuration $V_{OUT}+V_D$ is constant. the total power dissipation of the IC depends only on the number of segments activated.

PART NUMBERING

Table 4. Order Codes

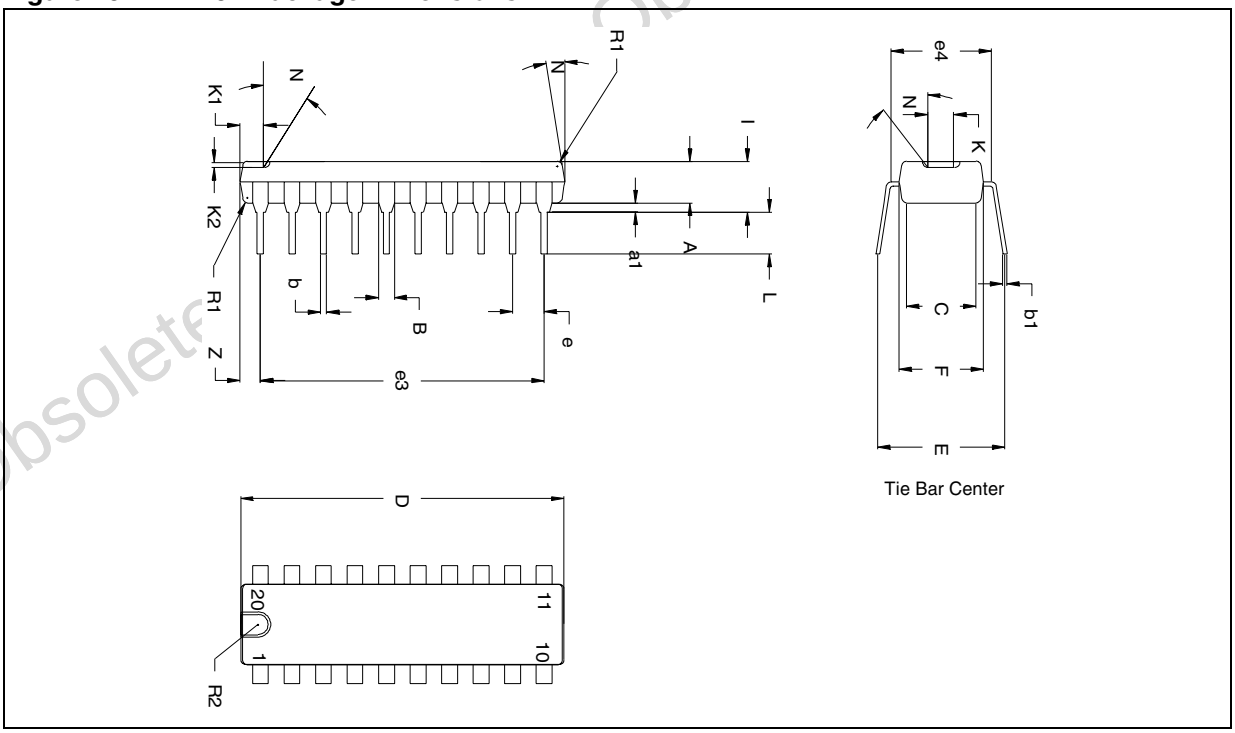
Part Number	Package	Temperature Range
M5481 B7	PDIP	-25 to 85 °C

PACKAGE MECHANICAL

Table 5. PDIP20 - Mechanical Data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A	3.25	3.30	3.35	0.128	0.130	0.132
a1		0.508			0.020	
B	1.39		1.65	0.055		0.065
b	0.381	0.457	0.533	0.015	0.018	0.021
b1	0.20	0.254	0.30	0.008	0.010	0.012
C	5.20	5.33	5.46	0.205	0.210	0.215
D	24.9	25.15	25.4	0.980	0.990	1.000
E	7.8	8.5	9.1	0.307	0.335	0.358
e	2.29	2.54	2.79	0.090	0.100	0.110
e3	22.60	22.86	23.11	0.890	0.900	0.910
e4	7.36	7.62	7.87	0.290	0.300	0.310
F	6.22	6.35	6.50	0.245	0.250	0.255
I	3.42	3.68	3.93	0.135	0.145	0.155
L	3.17	3.30	3.42	0.125	0.130	0.135
N		7d			7d	
R1		0.152			0.006	
R2		0.762			0.030	
K		1.524			0.060	
K1		0.762			0.030	
K2		0.762			0.030	
Z		1.27	1.34		0.050	0.053

Figure 10. PDIP20 - Package Dimensions



Note: Drawing is not to scale

REVISION HISTORY

Table 6. Revision History

Date	Revision	Description of Changes
October-2000	1	First Issue
14-Apr-2004	2	Stylesheet update. No content change.