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About This Book

The primary objective of this reference manual is to define the functionality of the MCF548x processors for use by software and hardware developers.

The information in this book is subject to change without notice, as described in the disclaimers on the title page of this book. As with any technical documentation, it is the readers' responsibility to be sure they are using the most recent version of the documentation.

To locate any published errata or updates for this document, refer to the world-wide web at http://www.freescale.com/coldfire.

Audience

This manual is intended for system software and hardware developers and applications programmers who want to develop products for the MCF548x. It is assumed that the reader understands operating systems, microprocessor system design, basic principles of software and hardware, and basic details of the ColdFire architecture.

Organization

Following is a summary and a brief description of the major sections of this manual:

- Chapter 1, "Overview," includes general descriptions of the modules and features incorporated in the MCF548x, focussing in particular on new features.
- Chapter 2, "Signal Descriptions," provides an alphabetical listing of MCF548x signals, including which are inputs or outputs, how they are multiplexed, and the state of each signal at reset.
- Part I, "Processor Core," is intended for system designers who need to understand the operation of the MCF548x ColdFire core and its enhanced multiply/accumulate (EMAC) execution unit. It describes the programming and exception models, Harvard memory implementation, and debug module. Part 1 contains the following chapters:
  - Chapter 3, "ColdFire Core," provides an overview of the microprocessor core of the MCF548x. The chapter begins with a description of enhancements from the V3 ColdFire core, and then fully describes the V4e programming model as it is implemented on the MCF548x. It also includes a full description of exception handling, data formats, an instruction set summary, and a table of instruction timings.
  - Chapter 4, "Enhanced Multiply-Accumulate Unit (EMAC)," describes the MCF548x enhanced multiply/accumulate unit, which executes integer multiply, multiply-accumulate, and miscellaneous register instructions. The EMAC is integrated into the operand execution pipeline (OEP).
  - Chapter 5, "Memory Management Unit (MMU)," describes describes the ColdFire virtual memory management unit (MMU), which provides virtual-to-physical address translation and memory access control.
  - Chapter 6, "Floating-Point Unit (FPU)," describes instructions implemented in the floating-point unit (FPU) designed for use with the ColdFire family of microprocessors.

- Chapter 7, “Local Memory,” describes the MCF548x implementation of the ColdFire V4e local memory specification.
- Chapter 8, “Debug Support,” describes the Revision C enhanced hardware debug support in the MCF548x. This revision of the ColdFire debug architecture encompasses earlier revisions.

- Part II, “System Integration Unit,” describes the system integration unit, which provides overall control of the bus and serves as the interface between the ColdFire core processor complex and internal peripheral devices. It includes a general description of the SIU and individual chapters that describe components of the SIU, such as the interrupt controller, general purpose timers, slice timers, and GPIOs. Part II contains the following chapters:
  - Chapter 9, “System Integration Unit (SIU),” describes the SIU programming model, bus arbitration, and system-protection functions for the MCF548x.
  - Chapter 10, “Internal Clocks and Bus Architecture,” describes the clocking and internal buses of the MCF548*x* and discusses the main functional blocks controlling the XL bus and the XL bus arbiter.
  - Chapter 11, “General Purpose Timers (GPT),” describes the functionality of the four general purpose timers, GPT0–GPT3.
  - Chapter 12, “Slice Timers (SLT),” describes the two slice timers, shorter term periodic interrupts, used in the MCF548x.
  - Chapter 13, “Interrupt Controller,” describes operation of the interrupt controller portion of the SIU. Includes descriptions of the registers in the interrupt controller memory map and the interrupt priority scheme.
  - Chapter 14, “Edge Port Module (EPORT),” describes EPORT module functionality.
  - Chapter 15, “GPIO,” describes the operation and programming model of the parallel port pin assignment, direction-control, and data registers.
- Part III, “On-Chip Integration,” describes the on-chip integration for the MCF548x device. It includes descriptions of the system SRAM, FlexBus interface, SDRAM controller, PCI, and SEC cryptography accelerator. Part III contains the following chapters:
  - Chapter 16, “32-Kbyte System SRAM,” describes the MCF548x on-chip system SRAM implementation. It covers general operations, configuration, and initialization.
  - Chapter 17, “FlexBus,” describes data transfer operations, error conditions, and reset operations. It describes transfers initiated by the MCF548x and by an external master, and includes detailed timing diagrams showing the interaction of signals in supported bus operations.
  - Chapter 18, “SDRAM Controller (SDRAMC),” describes configuration and operation of the synchronous DRAM controller component of the SIU. It includes a description of signals involved in DRAM operations, including chip select signals and their address, mask, and control registers.
  - Chapter 19, “PCI Bus Controller,” details the operation of the PCI bus controller for the MCF548x.
  - Chapter 20, “PCI Bus Arbiter Module,” describes the MCF548x PCI bus arbiter module, including timing for request and grant handshaking, the arbitration process, and the register in the PCI bus arbiter programing model.

  - Chapter 21, “FlexCAN,” describes the MCF548 implementation of the controller area network (CAN) protocol. This chapter describes FlexCAN module operation and provides a programming model.
  - Chapter 22, “Integrated Security Engine (SEC),” provides an overview of the MCF548x security encryption controller.
  - Chapter 23, “IEEE 1149.1 Test Access Port (JTAG),” describes configuration and operation of the MCF548x JTAG test implementation. It describes the use of JTAG instructions and provides information on how to disable JTAG functionality.
- Part IV, “Communications Subsystem,” contains chapters that discuss the operation and configuration of the communications I/O subsystem including the MCF548x multichannel DMA, communications timer, PSC, FEC, DSPI, and USB2, and I^2C.
  - Chapter 24, “Multichannel DMA,” provides an overview of the multichannel DMA controller module including the operation of the external DMA request signals.
  - Chapter 26, “Comm Timer Module (CTM),” contains a detailed description of the communications timer module, which functions as a baud clock generator or as a DMA task initiator.
  - Chapter 27, “Programmable Serial Controller (PSC),” provides an overview of asynchronous, synchronous, and IrDA 1.1 compliant receiver/transmitter serial communications of the MCF548x.
  - Chapter 28, “DMA Serial Peripheral Interface (DSPI),” describes the use of the DMA serial peripheral interface (DSPI) implemented on the MCF548x processor, including details of the DSPI data transfers. The chapter concludes with timing diagrams and the DSPI features that support Tx and Rx FIFO queue management.
  - Chapter 29, “I2C Interface,” describes the MCF548x I^2C module, including I^2C protocol, clock synchronization, and the registers in the I^2C programing model. It also provides programming examples.
  - Chapter 30, “USB 2.0 Device Controller,” provides an overview of the USB 2.0 device controller module used in the MCF548x.
  - Chapter 31, “Fast Ethernet Controller (FEC),” provides a feature-set overview, a functional block diagram, and transceiver connection information for both MII (Media Independent Interface) and 7-wire serial interfaces. It also provides describes operation and the programming model.
- Part V, “Mechanical,” provides a pinout and both electrical and functional descriptions of the MCF548x signals. It also describes how these signals interact to support the variety of bus operations shown in timing diagrams.
  - Chapter 32, “Mechanical Data,” provides a functional pin listing and package diagram for the MCF548x.

Suggested Reading

This section lists additional reading that provides background for the information in this manual as well as general information about the ColdFire architecture.