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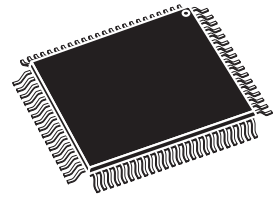
M58BW016DB M58BW016DT M58BW016FT M58BW016FB

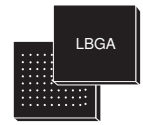
16 Mbit (512 Kbit x 32, boot block, burst)
3 V supply Flash memories

Features

- Supply voltage
  - V_{DD} = 2.7 V to 3.6 V for program, erase and read
  - V_{DDQ} = V_{DDQIN} = 2.4 V to 3.6 V for I/O buffers
  - V_{PP} = 12 V for fast program (optional)
- High performance
  - Access times: 70, 80 ns
  - 56 MHz effective zero wait-state burst read
  - Synchronous burst read
  - Asynchronous page read
- Hardware block protection
  - $\overline{WP}$ pin for write protect of the 2 outermost parameter blocks and all main blocks
  - $\overline{RP}$ pin for write protect of all blocks
- Optimized for FDI drivers
  - Fast program / erase suspend latency time < 6 µs
  - Common Flash interface
- Memory blocks
  - 8 parameters blocks (top or bottom)
  - 31 main blocks
- Low power consumption
  - 5 µA typical deep power-down
  - 60 µA typical standby for M58BW016DT/B
    150 µA typical standby for M58BW016FT/B
  - Automatic standby after asynchronous read
- Electronic signature
  - Manufacturer code: 20h
  - Top device code: 8836h
  - Bottom device code: 8835h
- 100 K write/erase cycling + 20 years data retention (minimum)
- High reliability level with over 1 M write/erase cycling sustained



PQFP80 (T)



LBGA80 10 × 12 mm

- RoHS packages available

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1 Description

The M58BW016DT, M58BW016DB, M58BW016FT and M58BW016FB are 16-Mbit non-volatile Flash memories that can be erased electrically at the block level and programmed in-system on a double-word basis using a 2.7 V to 3.6 V V_{DD} supply for the circuit and a V_{DDQ} supply down to 2.4 V for the input and output buffers. Optionally a 12 V V_{PP} supply can be used to provide fast program and erase for a limited time and number of program/erase cycles.

The devices support asynchronous (latch controlled and page read) and synchronous bus operations. The synchronous burst read interface allows a high data transfer rate controlled by the burst clock, K, signal. It is capable of bursting fixed or unlimited lengths of data. The burst type, latency and length can be configured and can be easily adapted to a large variety of system clock frequencies and microprocessors. All writes are asynchronous. On power-up the memory defaults to read mode with an asynchronous bus.

The devices have a boot block architecture with an array of 8 parameter blocks of 64 Kbits each and 31 main blocks of 512 Kbits each. In the M58BW016DT and M58BW016FT the parameter blocks are located at the top of the address space whereas in the M58BW016DB and M58BW016FB, they are located at the bottom.

Program and erase commands are written to the command interface of the memory. An on-chip program/erase controller simplifies the process of programming or erasing the memory by taking care of all of the special operations that are required to update the memory contents. The end of a program or erase operation can be detected and any error conditions identified in the status register. The command set required to control the memory is consistent with JEDEC standards.

Erase can be suspended in order to perform either read or program in any other block and then resumed. Program can be suspended to read data in any other block and then resumed. Each block can be programmed and erased over 100,000 cycles.

All blocks are protected during power-up.

The M58BW016DT, M58BW016DB, M58BW016FT and M58BW016FB feature two different levels of block protection to avoid unwanted program/erase operations:

- The $\overline{WP}$ pin offers an hardware protection on two of the parameter blocks and all of the main blocks
- All program or erase operations are blocked when Reset, $\overline{RP}$, is held Low. A reset/power-down mode is entered when the $\overline{RP}$ input is Low. In this mode the power consumption is lower than in the normal standby mode, the device is write protected and both the status and the burst configuration registers are cleared. A recovery time is required when the $\overline{RP}$ input goes High.

The memory is offered in a PQFP80 (14 x 20 mm) and LBGA80 (10 × 12 mm) package.

The memories are supplied with all the bits erased (set to '1').

In the present document, M58BW016DT, M58BW016DB, M58BW016FT and M58BW016FB will be referred to as M58BW016 unless otherwise specified.

Figure 1. Logic diagram

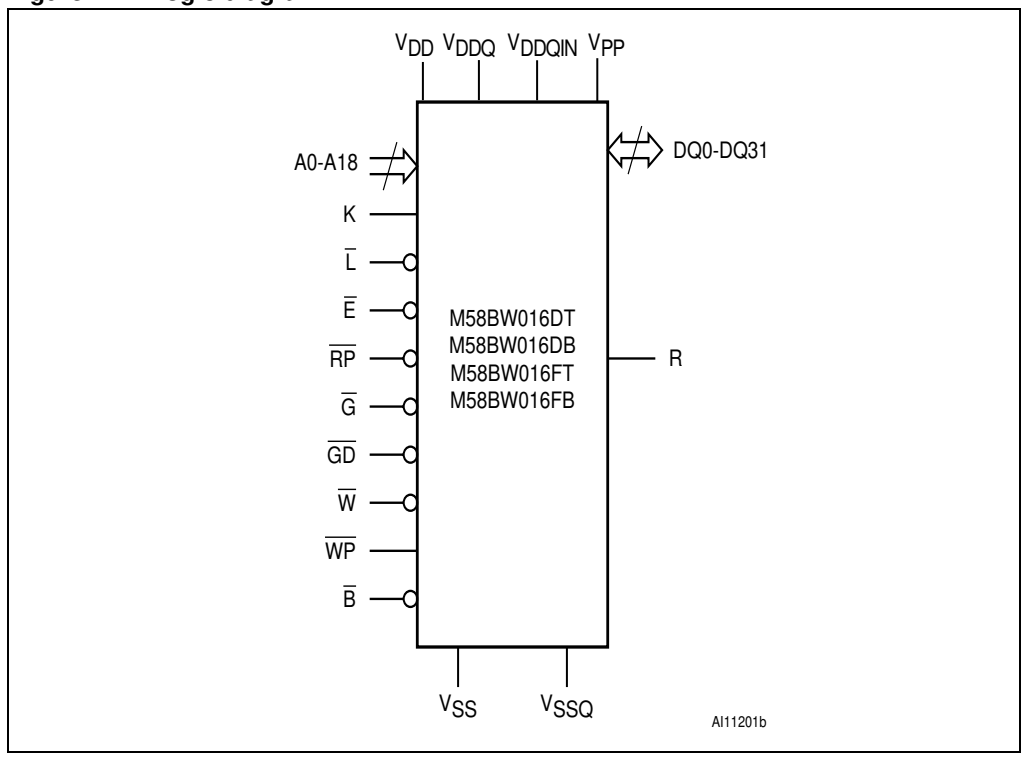


Table 1. Signal names

Signal	Description	Direction
A0-A18	Address inputs	Inputs
DQ0-DQ7	Data input/output, command input	I/O
DQ8-DQ15	Data input/output, Burst Configuration Register	I/O
DQ16-DQ31	Data input/output	I/O
$\overline{B}$	Burst Address Advance	Input
$\overline{E}$	Chip Enable	Input
$\overline{G}$	Output Enable	Input
K	Burst Clock	Input
$\overline{L}$	Latch Enable	Input
R	Valid Data Ready (open drain output)	Output
$\overline{RP}$	Reset/Power-down	Input
$\overline{W}$	Write Enable	Input
$\overline{GD}$	Output Disable	Input
$\overline{WP}$	Write Protect	Input
V_{DD}	Supply voltage	Supply
V_{DDQ}	Power supply for output buffers	Supply
V_{DDQIN}	Power supply for input buffers only	Supply
V_{PP}	Optional supply voltage for fast program and fast erase operations	Supply
V_{SS}	Ground	–
V_{SSQ}	Input/output ground	–
NC	Not connected internally	–
DU	Don't use as internally connected	–

Figure 2. PQFP connections (top view through package)

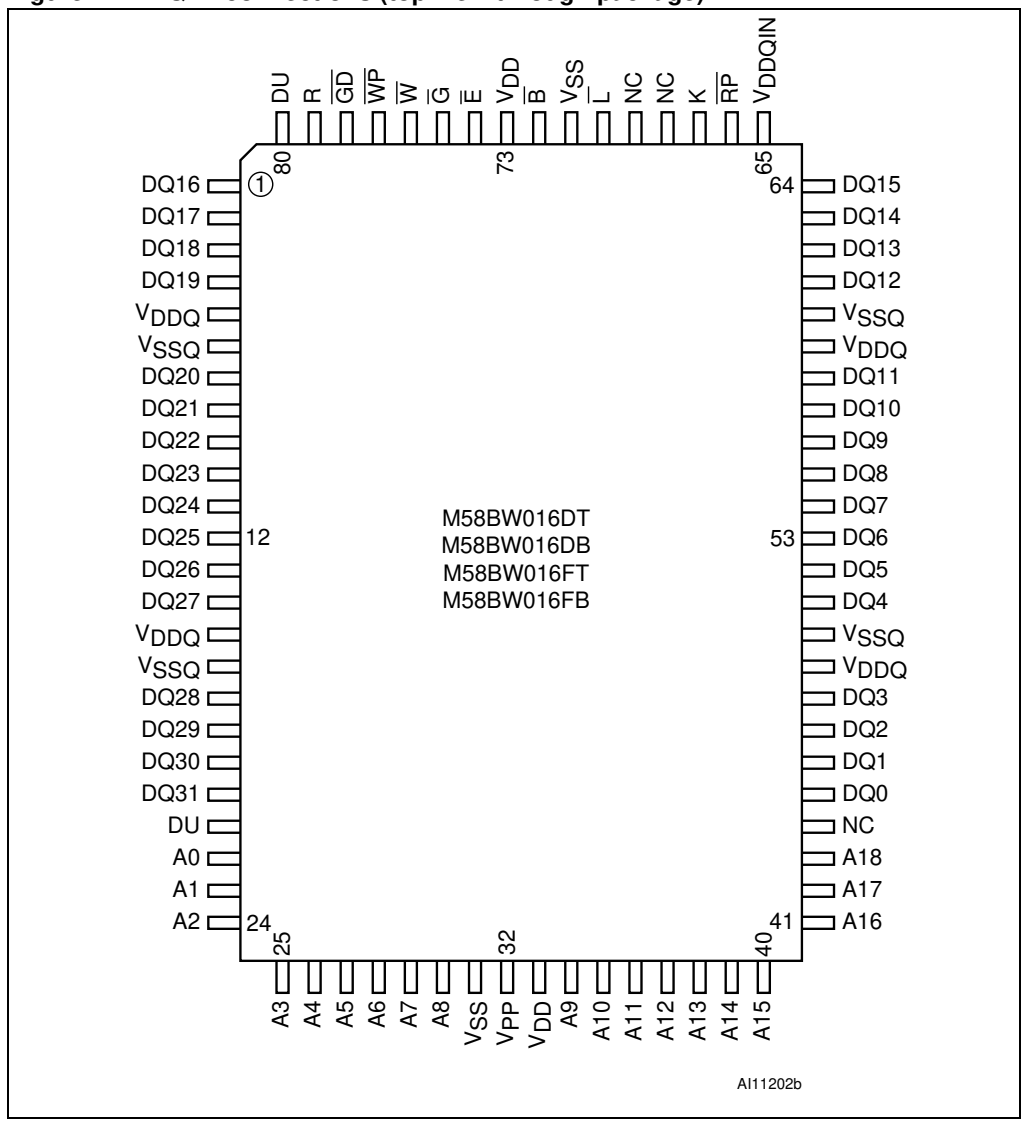
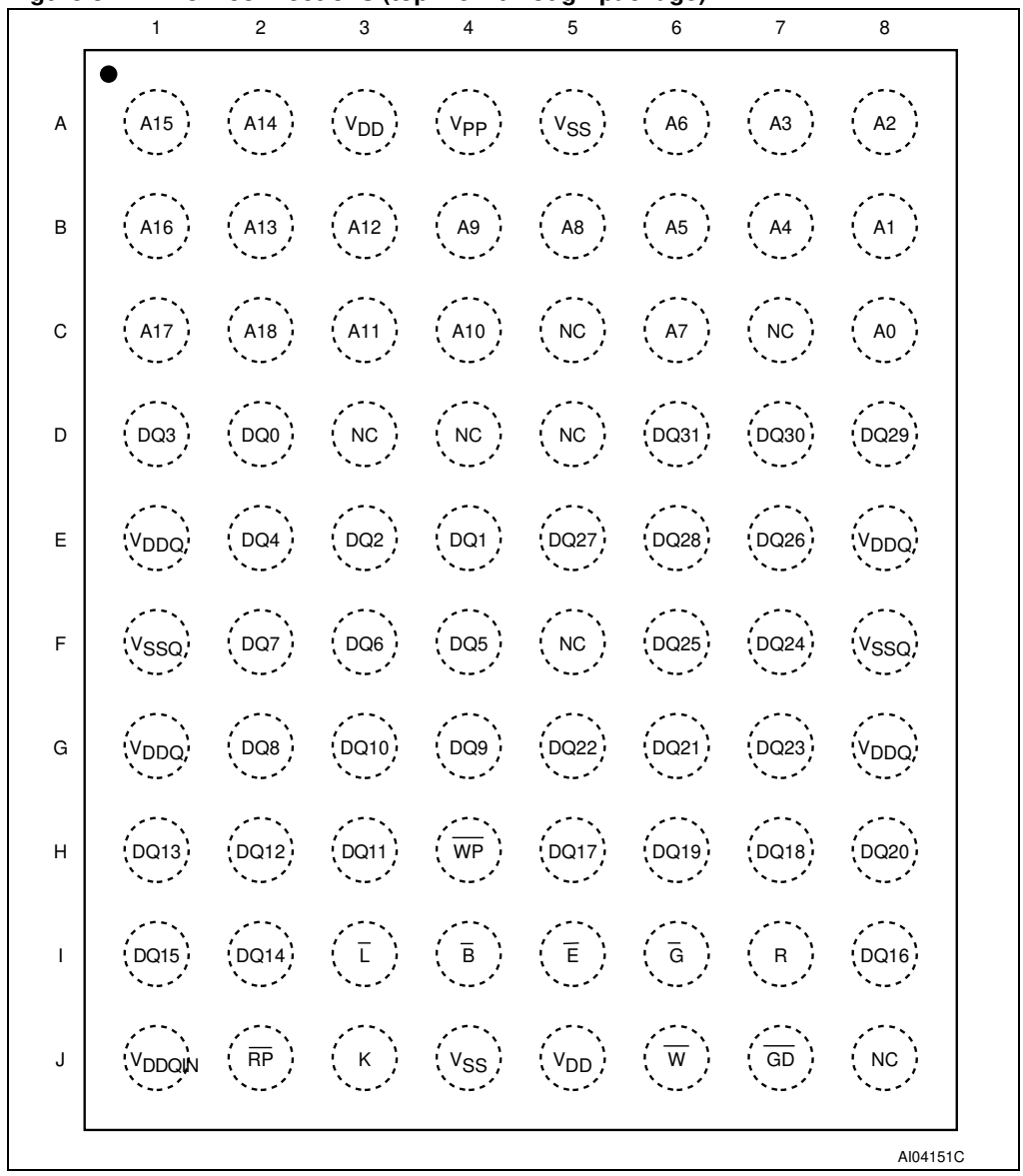


Figure 3. LBGA connections (top view through package)



1.1 Block protection

The M58BW016 feature two different levels of block protection.

- **Write protect pin, $\overline{WP}$ -** When $\overline{WP}$ is Low, V_{IL}, all the lockable parameter blocks (two upper (top) or lower (bottom)) and all the main blocks are protected. When $\overline{WP}$ is High (V_{IH}) all the lockable parameter blocks and all the main blocks are unprotected
- **Reset/power-down pin, $\overline{RP}$ -** If the device is held in reset mode ($\overline{RP}$ at V_{IL}), no program or erase operations can be performed on any block.

After a device reset the first two kinds of block protection ($\overline{WP}$, $\overline{RP}$) can be combined to give a flexible block protection.

Table 2. M58BW016DT and M58BW016FT top boot block addresses

#	Size (Kbit)	Address range
38	64	7F800h-7FFFFh
37	64	7F000h-7F7FFh
36	64	7E800h-7EFFFh
35	64	7E000h-7E7FFh
34	64	7D800h-7DFFFh
33	64	7D000h-7D7FFh
32	64	7C800h-7CFFFh
31	64	7C000h-7C7FFh
30	512	78000h-7BFFFh
29	512	74000h-77FFFh
28	512	70000h-73FFFh
27	512	6C000h-6FFFFh
26	512	68000h-6BFFFh
25	512	64000h-67FFFh
24	512	60000h-63FFFh
23	512	5C000h-5FFFFh
22	512	58000h-5BFFFh
21	512	54000h-57FFFh
20	512	50000h-53FFFh
19	512	4C000h-4FFFFh
18	512	48000h-4BFFFh
17	512	44000h-47FFFh
16	512	40000h-43FFFh
15	512	3C000h-3FFFFh
14	512	38000h-3BFFFh
13	512	34000h-37FFFh
12	512	30000h-33FFFh
11	512	2C000h-2FFFFh
10	512	28000h-2BFFFh
9	512	24000h-27FFFh
8	512	20000h-23FFFh
7	512	1C000h-1FFFFh
6	512	18000h-1BFFFh
5	512	14000h-17FFFh
4	512	10000h-13FFFh
3	512	0C000h-0FFFFh
2	512	08000h-0BFFFh
1	512	04000h-07FFFh
0	512	00000h-03FFFh

Table 3. M58BW016DB and M58BW016FB bottom boot block addresses

#	Size (Kbit)	Address range
38	512	7C000h-7FFFFh
37	512	78000h-7BFFFh
36	512	74000h-77FFFh
35	512	70000h-73FFFh
34	512	6C000h-6FFFFh
33	512	68000h-6BFFFh
32	512	64000h-67FFFh
31	512	60000h-63FFFh
30	512	5C000h-5FFFFh
29	512	58000h-5BFFFh
28	512	54000h-57FFFh
27	512	50000h-53FFFh
26	512	4C000h-4FFFFh
25	512	48000h-4BFFFh
24	512	44000h-47FFFh
23	512	40000h-43FFFh
22	512	3C000h-3FFFFh
21	512	38000h-3BFFFh
20	512	34000h-37FFFh
19	512	30000h-33FFFh
18	512	2C000h-2FFFFh
17	512	28000h-2BFFFh
16	512	24000h-27FFFh
15	512	20000h-23FFFh
14	512	1C000h-1FFFFh
13	512	18000h-1BFFFh
12	512	14000h-17FFFh
11	512	10000h-13FFFh
10	512	0C000h-0FFFFh
9	512	08000h-0BFFFh
8	512	04000h-07FFFh
7	64	03800h-03FFFh
6	64	03000h-037FFh
5	64	02800h-02FFFh
4	64	02000h-027FFh
3	64	01800h-01FFFh
2	64	01000h-017FFh
1	64	00800h-00FFFh
0	64	00000h-007FFh

2 Signal descriptions

See *Figure 1: Logic diagram*, and *Table 1: Signal names* for a brief overview of the signals connected to this device.

2.1 Address inputs (A0-A18)

The address inputs are used to select the cells to access in the memory array during bus operations either to read or to program data. During bus write operations they control the commands sent to the command interface of the program/erase controller. Chip Enable must be Low when selecting the addresses.

The address inputs are latched on the rising edge of Latch Enable $\overline{L}$ or Burst Clock K, whichever occurs first, in a read operation.The address inputs are latched on the rising edge of Chip Enable, Write Enable or Latch Enable, whichever occurs first in a write operation. The address latch is transparent when Latch Enable is Low, V_{IL}. The address is internally latched in an erase or program operation.

2.2 Data inputs/outputs (DQ0-DQ31)

The data inputs/outputs output the data stored at the selected address during a bus read operation, or are used to input the data during a program operation. During bus write operations they represent the commands sent to the command interface of the program/erase controller. When used to input data or write commands they are latched on the rising edge of Write Enable or Chip Enable, whichever occurs first.

When Chip Enable and Output Enable are both Low, V_{IL}, and Output Disable is at V_{IH}, the data bus outputs data from the memory array, the electronic signature, the CFI information or the contents of the status register. The data bus is high impedance when the device is deselected with Chip Enable at V_{IH}, Output Enable at V_{IH}, Output Disable at V_{IL} or Reset/Power-down at V_{IL}. The status register content is output on DQ0-DQ7 and DQ8-DQ31 are at V_{IL}.

2.3 Chip Enable ($\overline{E}$)

The Chip Enable, $\overline{E}$, input activates the memory control logic, input buffers, decoders and sense amplifiers. Chip Enable, $\overline{E}$, at V_{IH} deselects the memory and reduces the power consumption to the standby level.

2.4 Output Enable ($\overline{G}$)

The Output Enable, $\overline{G}$, gates the outputs through the data output buffers during a read operation, when Output Disable $\overline{GD}$ is at V_{IH}. When Output Enable $\overline{G}$ is at V_{IH}, the outputs are high impedance independently of Output Disable.

2.5 Output Disable ($\overline{GD}$)

The Output Disable, $\overline{GD}$, deactivates the data output buffers. When Output Disable, $\overline{GD}$, is at V_{IH}, the outputs are driven by the Output Enable. When Output Disable, $\overline{GD}$, is at V_{IL}, the outputs are high impedance independently of Output Enable. The Output Disable pin must be connected to an external pull-up resistor as there is no internal pull-up resistor to drive the pin.

2.6 Write Enable ($\overline{W}$)

The Write Enable, $\overline{W}$, input controls writing to the command interface, Address inputs and Data latches. Both addresses and data can be latched on the rising edge of Write Enable (also see Latch Enable, $\overline{L}$).

2.7 Reset/Power-down ($\overline{RP}$)

The Reset/Power-down, $\overline{RP}$, is used to apply a hardware reset to the memory. A hardware reset is achieved by holding Reset/Power-down Low, V_{IL}, for at least t_{PLPH}. Writing is inhibited to protect data, the command interface and the program/erase controller are reset. The status register information is cleared and power consumption is reduced to deep power-down level. The device acts as deselected, that is the data outputs are high impedance.

After Reset/Power-down goes High, V_{IH}, the memory will be ready for bus read operations after a delay of t_{PHEL} or bus write operations after t_{PHWL}.

If Reset/Power-down goes Low, V_{IL}, during a Block Erase, or a Program the operation is aborted, in a time of t_{PLRH} maximum, and data is altered and may be corrupted.

During power-up power should be applied simultaneously to V_{DD} and $V_{DDQ(IN)}$ with $\overline{RP}$ held at V_{IL}. When the supplies are stable $\overline{RP}$ is taken to V_{IH}. Output Enable, $\overline{G}$, Chip Enable, $\overline{E}$, and Write Enable, $\overline{W}$, should be held at V_{IH} during power-up.

In an application, it is recommended to associate reset/power-down pin, $\overline{RP}$, with the reset signal of the microprocessor. Otherwise, if a reset operation occurs while the memory is performing an erase or program operation, the memory may output the status register information instead of being initialized to the default asynchronous random read.

See *Table 22: Reset, power-down and power-up AC characteristics* and *Figure 17: Reset, power-down and power-up AC waveforms - control pins low*, for more details.

2.8 Latch Enable ($\overline{L}$)

The bus interface can be configured to latch the address inputs on the rising edge of Latch Enable, $\overline{L}$, for asynchronous latch enable controlled read or write or synchronous burst read operations. In synchronous burst read operations the address is latched on the active edge of the Clock when Latch Enable is Low, V_{IL}. Once latched, the addresses may change without affecting the address used by the memory. When Latch Enable is Low, V_{IL}, the latch is transparent. Latch Enable, $\overline{L}$, can remain at V_{IL} for asynchronous random read and write operations.

2.9 Burst Clock (K)

The Burst Clock, K, is used to synchronize the memory with the external bus during synchronous burst read operations. Bus signals are latched on the active edge of the Clock. The Clock can be configured to have an active rising or falling edge. In synchronous burst read mode the address is latched on the first active clock edge when Latch Enable is Low, V_{IL}, or on the rising edge of Latch Enable, whichever occurs first.

During asynchronous bus operations the Clock is not used.

2.10 Burst Address Advance ($\overline{B}$)

The Burst Address Advance, $\overline{B}$, controls the advancing of the address by the internal address counter during synchronous burst read operations.

Burst Address Advance, $\overline{B}$, is only sampled on the active clock edge of the Clock when the X-latency time has expired. If Burst Address Advance is Low, V_{IL}, the internal address counter advances. If Burst Address Advance is High, V_{IH}, the internal address counter does not change; the same data remains on the data inputs/outputs and Burst Address Advance is not sampled until the Y-latency expires.

The Burst Address Advance, $\overline{B}$, may be tied to V_{IL}.

2.11 Valid Data Ready (R)

The Valid Data Ready output, R, is an open drain output that can be used, during synchronous burst read operations, to identify if the memory is ready to output data or not. The Valid Data Ready output can be configured to be active on the clock edge of the invalid data read cycle or one cycle before. Valid Data Ready, at V_{IH}, indicates that new data is or will be available. When Valid Data Ready is Low, V_{IL}, the previous data outputs remain active.

In all asynchronous operations, Valid Data Ready is high impedance. It may be tied to other components with the same Valid Data Ready signal to create a unique system Ready signal. The Valid Data Ready output has an internal pull-up resistor of around 1 MΩ powered from V_{DDQ}, designers should use an external pull-up resistor of the correct value to meet the external timing requirements for Valid Data Ready going to V_{IH}.

2.12 Write Protect ($\overline{WP}$)

The Write Protect, $\overline{WP}$, provides protection against program or erase operations. When Write Protect, $\overline{WP}$, is at V_{IL} the first two (in the bottom configuration) or last two (in the top configuration) parameter blocks and all main blocks are locked. When Write Protect $\overline{WP}$ is at V_{IH} all the blocks can be programmed or erased, if no other protection is used.

2.13 Supply voltage (V_{DD})

The supply voltage, V_{DD}, is the core power supply. All internal circuits draw their current from the V_{DD} pin, including the program/erase controller.

2.14 Output supply voltage (V_{DDQ})

The output supply voltage, V_{DDQ}, is the output buffer power supply for all operations (read, program and erase) used for DQ0-DQ31 when used as outputs.

2.15 Input supply voltage (V_{DDQIN})

The input supply voltage, V_{DDIN}, is the power supply for all input signal. Input signals are: K, $\overline{B}$, $\overline{L}$, $\overline{W}$, $\overline{GD}$, $\overline{G}$, $\overline{E}$, A0-A18 and DQ0-DQ31, when used as inputs.

2.16 Program/erase supply voltage (V_{PP})

The program/erase supply voltage, V_{PP}, is used for program and erase operations. The memory normally executes program and erase operations at V_{PP1} voltage levels. In a manufacturing environment, programming may be speeded up by applying a higher voltage level, V_{PPH}, to the V_{PP} pin.

The voltage level V_{PPH} may be applied for a total of 80 hours over a maximum of 1000 cycles. Stressing the device beyond these limits could damage the device.

2.17 Ground (V_{SS} and V_{SSQ})

The ground V_{SS} is the reference for the internal supply voltage V_{DD}. The ground V_{SSQ} is the reference for the output and input supplies V_{DDQ}, and V_{DDQIN}. It is essential to connect V_{SS} and V_{SSQ} together.

Note: A 0.1 µF capacitor should be connected between the supply voltages, V_{DD}, V_{DDQ} and V_{DDIN} and the grounds, V_{SS} and V_{SSQ} to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during all operations of the parts, see Table 15: DC characteristics, for maximum current supply requirements.

2.18 Don't use (DU)

This pin should not be used as it is internally connected. Its voltage level can be between V_{SS} and V_{DDQ} or leave it unconnected.

2.19 Not connected (NC)

This pin is not physically connected to the device.

3 Bus operations

Each bus operation that controls the memory is described in this section, see *Table 4*, *Table 5* and *Table 6* Bus operations, for a summary. The bus operation is selected through the burst configuration register; the bits in this register are described at the end of this section.

On power-up or after a hardware reset the memory defaults to asynchronous bus read and asynchronous bus write, no other bus operation can be performed until the burst control register has been configured.

The electronic signature, CFI or status register will be read in asynchronous mode regardless of the burst control register settings.

Typically glitches of less than 5 ns on Chip Enable or Write Enable are ignored by the memory and do not affect bus operations.

3.1 Asynchronous bus operations

For asynchronous bus operations refer to *Table 4* together with the following text.

3.1.1 Asynchronous bus read

Asynchronous bus read operations read from the memory cells, or specific registers (electronic signature, status register, CFI and burst configuration register) in the command interface. A valid bus operation involves setting the desired address on the address inputs, applying a Low signal, V_{IL}, to Chip Enable and Output Enable and keeping Write Enable and Output Disable High, V_{IH}. The data inputs/outputs will output the value, see *Figure 8: Asynchronous bus read AC waveforms*, and *Table 16: Asynchronous bus read AC characteristics*, for details of when the output becomes valid.

Asynchronous read is the default read mode which the device enters on power-up or on return from reset/power-down.

3.1.2 Asynchronous latch controlled bus read

Asynchronous latch controlled bus read operations read from the memory cells or specific registers in the command interface. The address is latched in the memory before the value is output on the data bus, allowing the address to change during the cycle without affecting the address that the memory uses.

A valid bus operation involves setting the desired address on the address inputs, setting Chip Enable and Latch Enable Low, V_{IL} and keeping Write Enable High, V_{IH}; the address is latched on the rising edge of Latch Enable. Once latched, the address inputs can change. Set Output Enable Low, V_{IL}, to read the data on the data inputs/outputs; see *Figure 9: Asynchronous latch controlled bus read AC waveforms*, and *Table 17: Asynchronous latch controlled bus read AC characteristics*, for details on when the output becomes valid.

Note that, since the Latch Enable input is transparent when set Low, V_{IL}, asynchronous bus read operations can be performed when the memory is configured for asynchronous latch enable bus operations by holding Latch Enable Low, V_{IL} throughout the bus operation.

3.1.3 Asynchronous page read

Asynchronous page read operations are used to read from several addresses within the same memory page. Each memory page is 4 double-words and is addressed by the address inputs A0 and A1.

Data is read internally and stored in the page buffer. Valid bus operations are the same as asynchronous bus read operations but with different timings. The first read operation within the page has identical timings, subsequent reads within the same page have much shorter access times. If the page changes then the normal, longer timings apply again. Page read does not support latched controlled read.

See *Figure 10: Asynchronous page read AC waveforms*, and *Table 18: Asynchronous page read AC characteristics*, for details on when the outputs become valid.

3.1.4 Asynchronous bus write

Asynchronous bus write operations write to the command interface to send commands to the memory or to latch addresses and input data to program. Bus write operations are asynchronous, the clock, K, is don't care during bus write operations.

A valid asynchronous bus write operation begins by setting the desired address on the address inputs, and setting Chip Enable, Write Enable and Latch Enable Low, V_{IL}, and Output Enable High, V_{IH}, or Output Disable Low, V_{IL}. The address inputs are latched by the command interface on the rising edge of Chip Enable or Write Enable, whichever occurs first. Commands and input data are latched on the rising edge of Chip Enable, $\overline{E}$, or Write Enable, $\overline{W}$, whichever occurs first. Output Enable must remain High, and Output Disable Low, during the whole asynchronous bus write operation.

See *Figure 11: Asynchronous write AC waveforms*, and *Table 19: Asynchronous write and latch controlled write AC characteristics*, for details of the timing requirements.

3.1.5 Asynchronous latch controlled bus write

Asynchronous latch controlled bus write operations write to the command interface to send commands to the memory or to latch addresses and input data to program. Bus write operations are asynchronous, the clock, K, is don't care during bus write operations.

A valid asynchronous latch controlled bus write operation begins by setting the desired address on the address inputs and pulsing Latch Enable Low, V_{IL}. The address inputs are latched by the command interface on the rising edge of Latch Enable, Write Enable or Chip Enable, whichever occurs first. Commands and input data are latched on the rising edge of Chip Enable, $\overline{E}$, or Write Enable, $\overline{W}$, whichever occurs first. Output Enable must remain High, and Output Disable Low, during the whole asynchronous bus write operation.

See *Figure 12: Asynchronous latch controlled write AC waveforms*, and *Table 19: Asynchronous write and latch controlled write AC characteristics*, for details of the timing requirements.

3.1.6 Output Disable

The data outputs are high impedance when the Output Enable, $\overline{G}$, is at V_{IH} or Output Disable, $\overline{GD}$, is at V_{IL}.

3.1.7 Standby mode

When Chip Enable is High, V_{IH}, and the Program/Erase controller is idle, the memory enters Standby mode, the power consumption is reduced to the standby level and the Data inputs/outputs pins are placed in the high impedance state regardless of Output Enable, Write Enable or Output Disable inputs.

3.1.8 Automatic low power mode

If there is no change in the state of the bus for a short period of time during asynchronous bus read operations the memory enters auto low power mode where the internal supply current is reduced to the auto-standby supply current. The data inputs/outputs will still output data if a bus read operation is in progress.

Automatic low power is only available in asynchronous read modes.

3.1.9 Power-down mode

The memory is in power-down when Reset/Power-down, $\overline{RP}$, is at V_{IL}. The power consumption is reduced to the power-down level and the outputs are high impedance, independent of the Chip Enable, $\overline{E}$, Output Enable, $\overline{G}$, Output Disable, $\overline{GD}$, or Write Enable, $\overline{W}$, inputs.

3.1.10 Electronic signature

Two codes identifying the manufacturer and the device can be read from the memory allowing programming equipment or applications to automatically match their interface to the characteristics of the memory. The electronic signature is output by giving the Read Electronic Signature command. The manufacturer code is output when all the address inputs are at V_{IL}. The device code is output when A1 is at V_{IH} and all the other address pins are at V_{IL} (see *Table 5: Asynchronous read electronic signature operation*). Issue a Read Memory Array command to return to read mode.

Table 4. Asynchronous bus operations(1)

Bus operation	Step	$\overline{E}$	$\overline{G}$	$\overline{GD}$	$\overline{W}$	$\overline{RP}$	$\overline{L}$	A0-A18	DQ0-DQ31
Asynchronous bus read		V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IH}	V_{IL}	Address	Data output
Asynchronous latch controlled bus read	Address Latch	V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	Address	High-Z
	Read	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IH}	V_{IH}	X	Data output
Asynchronous page read		V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IH}	X	Address	Data output
Asynchronous bus write		V_{IL}	V_{IH}	X	V_{IL}	V_{IH}	V_{IL}	Address	Data input
Asynchronous latch controlled bus write	Address Latch	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IH}	V_{IL}	Address	High-Z
	Write	V_{IL}	V_{IH}	X	V_{IL}	V_{IH}	V_{IH}	X	Data input
Output Enable, $\overline{G}$		V_{IL}	V_{IH}	V_{IH}	V_{IH}	V_{IH}	X	X	High-Z
Output Disable, $\overline{GD}$		V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	X	High-Z
Standby		V_{IH}	X	X	X	V_{IH}	X	X	High-Z
Reset/power-down		X	X	X	X	V_{IL}	X	X	High-Z

1. X = don't care.

Table 5. Asynchronous read electronic signature operation

Code	Device	$\overline{E}$	$\overline{G}$	$\overline{GD}$	$\overline{W}$	A18-A0	DQ31-DQ0
Manufacturer	All	V_{IL}	V_{IL}	V_{IH}	V_{IH}	00000h	00000020h
Device	M58BW016DT M58BW016FT	V_{IL}	V_{IL}	V_{IH}	V_{IH}	00001h	00008836h
	M58BW016DB M58BW016FB	V_{IL}	V_{IL}	V_{IH}	V_{IH}	00001h	00008835h
Burst configuration register		V_{IL}	V_{IL}	V_{IH}	V_{IH}	00005h	BCR(1)

1. BCR = Burst configuration register.

3.2 Synchronous bus operations

For synchronous bus operations refer to *Table 6* together with the following text.

3.2.1 Synchronous burst read

Synchronous burst read operations are used to read from the memory at specific times synchronized to an external reference clock.

In the M58BW016FT and M58BW016FB only, once the memory is configured in burst mode, it is mandatory to have an active clock signal since the switching of the output buffer data bus is synchronized to the active edge of the clock. In the absence of clock, no data is output.

Caution: The M58BW016DT and M58BW016DB are not concerned by the paragraph above.

The burst type, length and latency can be configured. The different configurations for synchronous burst read operations are described in *Section 3.3: Burst configuration register*. Refer to *Figure 4* and *Figure 5* for examples of synchronous burst operations.

In continuous burst read, one burst read operation can access the entire memory sequentially by keeping the Burst Address Advance $\overline{B}$ at V_{IL} for the appropriate number of clock cycles. At the end of the memory address space the burst read restarts from the beginning at address 000000h.

A valid synchronous burst read operation begins when the Burst Clock is active and Chip Enable and Latch Enable are Low, V_{IL}. The burst start address is latched and loaded into the internal burst address counter on the valid Burst Clock K edge (rising or falling depending on the value of M6) or on the rising edge of Latch Enable, whichever occurs first.

After an initial memory latency time, the memory outputs data each clock cycle (or two clock cycles depending on the value of M9). The Burst Address Advance $\overline{B}$ input controls the memory burst output. The second burst output is on the next clock valid edge after the Burst Address Advance $\overline{B}$ has been pulled Low.

Valid Data Ready, R, monitors if the memory burst boundary is exceeded and the burst controller of the microprocessor needs to insert wait states. When Valid Data Ready is Low on the active clock edge, no new data is available and the memory does not increment the internal address counter at the active clock edge even if Burst Address Advance, $\overline{B}$, is Low.

Valid Data Ready may be configured (by bit M8 of burst configuration register) to be valid immediately at the valid clock edge or one data cycle before the valid clock edge.

Synchronous burst read will be suspended if Burst Address Advance, $\overline{B}$, goes High, V_{IH}.

If Output Enable is at V_{IL} and Output Disable is at V_{IH}, the last data is still valid.

If Output Enable, $\overline{G}$, is at V_{IH} or Output Disable, $\overline{GD}$, is at V_{IL}, but the Burst Address Advance, $\overline{B}$, is at V_{IL} the internal Burst Address counter is incremented at each Burst Clock K valid edge.

The synchronous burst read timing diagrams and AC characteristics are described in the AC and DC parameters section. See *Figure 13*, *Figure 14*, *Figure 15* and *Figure 16*, and *Table 20*.

3.2.2 Synchronous burst read suspend

During a synchronous burst read operation it is possible to suspend the operation, freeing the data bus for other higher priority devices.

A valid synchronous burst read operation is suspended when both Output Enable and Burst Address Advance are High, V_{IH}. The Burst Address Advance going High, V_{IH}, stops the burst counter and the Output Enable going High, V_{IH}, inhibits the data outputs. The synchronous burst read operation can be resumed by setting Output Enable Low.

Table 6. Synchronous burst read bus operations(1)(2)

Bus operation	Step	$\overline{E}$	$\overline{G}$	$\overline{GD}$	$\overline{RP}$	K(3)	$\overline{L}$	$\overline{B}$	A0-A18 DQ0-DQ31
Synchronous burst read	Address Latch	V_{IL}	V_{IH}	X	V_{IH}	T	V_{IL}	X	Address input
	Read	V_{IL}	V_{IL}	V_{IH}	V_{IH}	T	V_{IH}	V_{IL}	Data output
	Read Suspend	V_{IL}	V_{IH}	X	V_{IH}	X	V_{IH}	V_{IH}	High-Z
	Read Resume	V_{IL}	V_{IL}	V_{IH}	V_{IH}	T	V_{IH}	V_{IL}	Data output
	Burst Address Advance	V_{IL}	V_{IH}	X	V_{IH}	T	V_{IH}	V_{IL}	High-Z
	Read Abort, $\overline{E}$	V_{IH}	X	X	V_{IH}	X	X	X	High-Z
	Read Abort, $\overline{RP}$	X	X	X	V_{IL}	X	X	X	High-Z

1. X = don't care, V_{IL} or V_{IH}.
2. M15 = 0, bit M15 is in the burst configuration register.
3. T = transition, see M6 in the burst configuration register for details on the active edge of K.

3.3 Burst configuration register

The burst configuration register is used to configure the type of bus access that the memory will perform.

The burst configuration register is set through the command interface and will retain its information until it is re-configured, the device is reset, or the device goes into reset/power-down mode. The burst configuration register bits are described in *Table 7*. They specify the selection of the burst length, burst type, burst X and Y latencies and the read operation. Refer to *Figure 4* and *Figure 5* for examples of synchronous burst configurations.

3.3.1 Read select bit (M15)

The read select bit, M15, is used to switch between asynchronous and synchronous bus read operations. When the read select bit is set to '1', bus read operations are asynchronous; when the read select bit is set to '0', bus read operations are synchronous.

On reset or power-up the read select bit is set to'1' for asynchronous accesses.

3.3.2 X-Latency bits (M14-M11)

The X-Latency bits are used during synchronous bus read operations to set the number of clock cycles between the address being latched and the first data becoming available. For correct operation the X-Latency bits can only assume the values in *Table 7: Burst configuration register*. The X-Latency bits should also be selected in conjunction with *Table 8: Burst type definition* to ensure valid settings.

3.3.3 Y-Latency bit (M9)

The Y-Latency bit is used during synchronous bus read operations to set the number of clock cycles between consecutive reads. The Y-Latency value depends on both the X-Latency value and the setting in M9.

When the Y-Latency is '1' the data changes each clock cycle; when the Y-Latency is '2' the data changes every second clock cycle. See *Table 7: Burst configuration register*, and *Table 8: Burst type definition* for valid combinations of the Y-Latency, the X-Latency and the clock frequency.

3.3.4 Valid data ready bit (M8)

The valid data ready bit controls the timing of the valid data ready output pin, R. When the valid data ready bit is '0' the valid data ready output pin is driven Low for the active clock edge when invalid data is output on the bus. When the valid data ready bit is '1' the valid data ready output pin is driven Low one clock cycle prior to invalid data being output on the bus.

3.3.5 Burst type bit (M7)

The burst type bit is used to configure the sequence of addresses read as sequential or interleaved. When the burst type bit is '0' the memory outputs from interleaved addresses; when the burst type bit is '1' the memory outputs from sequential addresses. See *Table 8: Burst type definition*, for the sequence of addresses output from a given starting address in each mode.

3.3.6 Valid clock edge bit (M6)

The valid clock edge bit, M6, is used to configure the active edge of the Clock, K, during synchronous burst read operations. When the valid clock edge bit is ’0’ the falling edge of the clock is the active edge; when the valid clock edge bit is ’1’ the rising edge of the clock is active.

3.3.7 Wrap burst bit (M3)

The burst reads can be confined inside the 4 or 8 double-word boundary (wrap) or overcome the boundary (no wrap). The wrap burst bit is used to select between wrap and no wrap. When the wrap burst bit is set to ‘0’ the burst read wraps; when it is set to ‘1’ the burst read does not wrap.

3.3.8 Burst length bit (M2-M0)

The burst length bits set the maximum number of double-words that can be output during a synchronous burst read operation before the address wraps. Burst lengths of 4 or 8 are available for both the sequential and interleaved burst types, and a continuous burst is available for the sequential type.

Table 7: Burst configuration register gives the valid combinations of the burst length bits that the memory accepts; *Table 8: Burst type definition*, gives the sequence of addresses output from a given starting address for each length.

If either a continuous or a no wrap burst read has been initiated the device will output data synchronously. Depending on the starting address, the device activates the valid data ready output to indicate that a delay is necessary before the data is output. If the starting address is aligned to an 8 double-word boundary, the continuous burst mode will run without activating the valid data ready output. If the starting address is not aligned to an 8 double-word boundary, valid data ready is activated to indicate that the device needs an internal delay to read the successive words in the array.

M10, M5 and M4 are reserved for future use.

Table 7. Burst configuration register

Bit	Description	Value	Description
M15	Read select	0	Synchronous burst read
		1	Asynchronous read (default at power-on)
M14		0	Reserved (default value)
M13-M11	X-Latency(1)	000	Reserved (default value)
		001	Reserved
		010	4, 4-1-1-1(2)
		011	5(3), 5-1-1-1, 5-2-2-2
		100	6(3), 6-1-1-1, 6-2-2-2
		101	7(3), 7-1-1-1, 7-2-2-2
		110	8(3), 8-1-1-1, 8-2-2-2
		111	Reserved
M10		0	Reserved (default value)
M9	Y-Latency(4)	0	One burst clock cycle (default value)
		1	Two burst clock cycles
M8	Valid data ready	0	R valid Low during valid burst clock edge (default value)
		1	R valid Low 1 data cycle before valid burst clock edge
M7	Burst type	0	Interleaved (default value)
		1	Sequential
M6	Valid clock edge	0	Falling burst clock edge (default value)
		1	Rising burst clock edge
M5-M4		00	Reserved (default value)
		01	Reserved
		10	Reserved
		11	Reserved
M3	Wrapping	0	Wrap (default value)
		1	No wrap
M2-M0	Burst length	000	Reserved (default value)
		001	4 double-words
		010	8 double-words
		011	Reserved
		100	Reserved
		101	Reserved
		110	Reserved
		111	Continuous

1. X latencies can be calculated as: $(t_{AVQV} - t_{LLKH} + t_{QVKH}) + t_{SYSTEM\ MARGIN} < (X - 1)\ t_K$. (X is an integer number from 4 to 8, t_K is the clock period and $t_{SYSTEM\ MARGIN}$ is the time margin required for the calculation).
2. This feature is available for the M58BW016F version up to the full operative frequency of 56 MHz, and for the M58BW016D version only if the operative frequency is below 45 MHz.
3. The M58BW016F version has a maximum operative frequency of 66 MHz, fully factory tested.
4. Y latencies can be calculated as: $t_{KHQV} + t_{SYSTEM\ MARGIN} + t_{QVKH} < Y\ t_K$.