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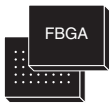
M58LR128KT M58LR128KB
M58LR256KT M58LR256KB

128 or 256 Mbit (x16, multiple bank, multilevel interface, burst) 1.8 V supply flash memories

Features

- Supply voltage
  - V_{DD} = 1.7 V to 2.0 V for program, erase and read
  - V_{DDQ} = 1.7 V to 2.0 V for I/O buffers
  - V_{PP} = 9 V for fast program
- Synchronous/asynchronous read
  - Synchronous burst read mode: 54 MHz, 66 MHz
  - Asynchronous page read mode
  - Random access: 70 ns, 85 ns
- Synchronous burst read suspend
- Programming time
  - 2.5 μs typical word program time using Buffer Enhanced Factory Program command
- Memory organization
  - Multiple bank memory array: 8 Mbit banks for the M58LR128KT/B 16 Mbit banks for the M58LR256KT/B
  - Parameter blocks (top or bottom location)
- Dual operations
  - Program/erase in one bank while read in others
  - No delay between read and write operations
- Block locking
  - All blocks locked at power-up
  - Any combination of blocks can be locked with zero latency
  - $\overline{WP}$ for block lock-down
  - Absolute write protection with $V_{PP} = V_{SS}$



VFBGA56 (ZB) 7.7 x 9 mm
VFBGA79 (ZC) 9 x 11 mm
TFBGA88 (ZQ) 8 x 10 mm

- Security
  - 64 bit unique device number
  - 2112 bit user programmable OTP cells
- Common flash interface (CFI)
- 100,000 program/erase cycles per block
- Electronic signature
  - Manufacturer code: 20h
  - Top device codes: M58LR128KT: 88C4h M58LR256KT: 880Dh
  - Bottom device codes M58LR128KB: 88C5h M58LR256KB: 880Eh
- The M58LR128KT/B is available in the ECOPACK-compliant VFBGA56 package.
- The M58LR256KT/B is available in the ECOPACK-compliant VFBGA79 and TFBGA88 packages.

Contents

List of tables

List of figures

1 Description

The M58LR128KT/B and M58LR256KT/B are 128 Mbit (8 Mbit x16) and 256 Mbit (16 Mbit x 16) non-volatile Flash memories, respectively. They can be erased electrically at block level and programmed in-system on a word-by-word basis using a 1.7 V to 2.0 V V_{DD} supply for the circuitry and a 1.7 V to 2.0 V V_{DDQ} supply for the input/output pins. An optional 9 V V_{PP} power supply is provided to accelerate factory programming.

The devices feature an asymmetrical block architecture:

- The M58LR128KT/B have an array of 131 blocks, and are divided into 8 Mbit banks. There are 15 banks each containing 8 main blocks of 64 Kwords, and one parameter bank containing 4 parameter blocks of 16 Kwords and 7 main blocks of 64 Kwords.
- The M58LR256KT/B have an array of 259 blocks, and are divided into 16 Mbit banks. There are 15 banks each containing 16 main blocks of 64 Kwords, and one parameter bank containing 4 parameter blocks of 16 Kwords and 15 main blocks of 64 Kwords.

The multiple bank architecture allows dual operations. While programming or erasing in one bank, read operations are possible in other banks. Only one bank at a time is allowed to be in program or erase mode. It is possible to perform burst reads that cross bank boundaries. The bank architecture is summarized in *Table 2*, and the memory map is shown in *Figure 4*. The parameter blocks are located at the top of the memory address space for the M58LR128KT and M58LR256KT, and at the bottom for the M58LR128KB and M58LR256KB.

Each block can be erased separately. Erase can be suspended to perform a program or read operation in any other block, and then resumed. Program can be suspended to read data at any memory location except for the one being programmed, and then resumed. Each block can be programmed and erased over 100 000 cycles using the supply voltage V_{DD}. There is a buffer enhanced factory programming command available to speed up programming.

Program and erase commands are written to the command interface of the memory. An internal Program/Erase Controller manages the timings necessary for program and erase operations. The end of a program or erase operation can be detected and any error conditions identified in the Status Register. The command set required to control the memory is consistent with JEDEC standards.

The device supports synchronous burst read and asynchronous read from all blocks of the memory array; at power-up the device is configured for asynchronous read. In synchronous burst read mode, data is output on each clock cycle at frequencies of up to 66 MHz. The synchronous burst read operation can be suspended and resumed.

The device features an automatic standby mode. When the bus is inactive during asynchronous read operations, the device automatically switches to automatic standby mode. In this condition the power consumption is reduced to the standby value and the outputs are still driven.

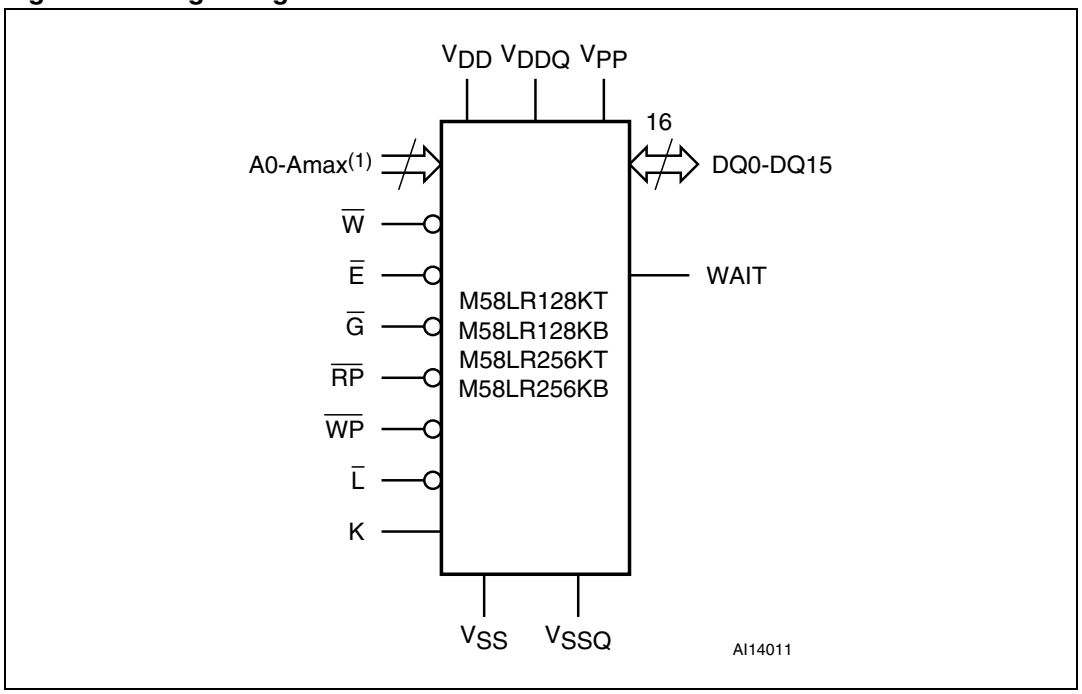
The M58LRxxxKT/B features an instant, individual block locking scheme that allows any block to be locked or unlocked with no latency, enabling instant code and data protection. All blocks have three levels of protection. They can be locked and locked-down individually preventing any accidental programming or erasure. There is an additional hardware protection against program and erase. When $V_{PP} \leq V_{PPLK}$ all blocks are protected against program or erase. All blocks are locked at power-up.

The device includes 17 Protection Registers and 2 Protection Register locks, one for the first Protection Register and the other for the 16 one-time-programmable (OTP) Protection Registers of 128 bits each. The first Protection Register is divided into two segments: a 64 bit segment containing a unique device number written by Numonyx, and a 64 bit segment OTP by the user. The user programmable segment can be permanently protected. *Figure 6*, shows the Protection Register memory map.

The M58LR128KT/B is offered in a VFBGA56 7.7 x 9 mm, 0.75 mm package, and the M58LR256KT/B is offered in a VFBGA79 9 x 11mm, 0.75 mm package and TFGBA88 8 x 10mm, 0.8 mm package.

All devices are supplied with all the bits erased (set to '1').

Figure 1. Logic diagram



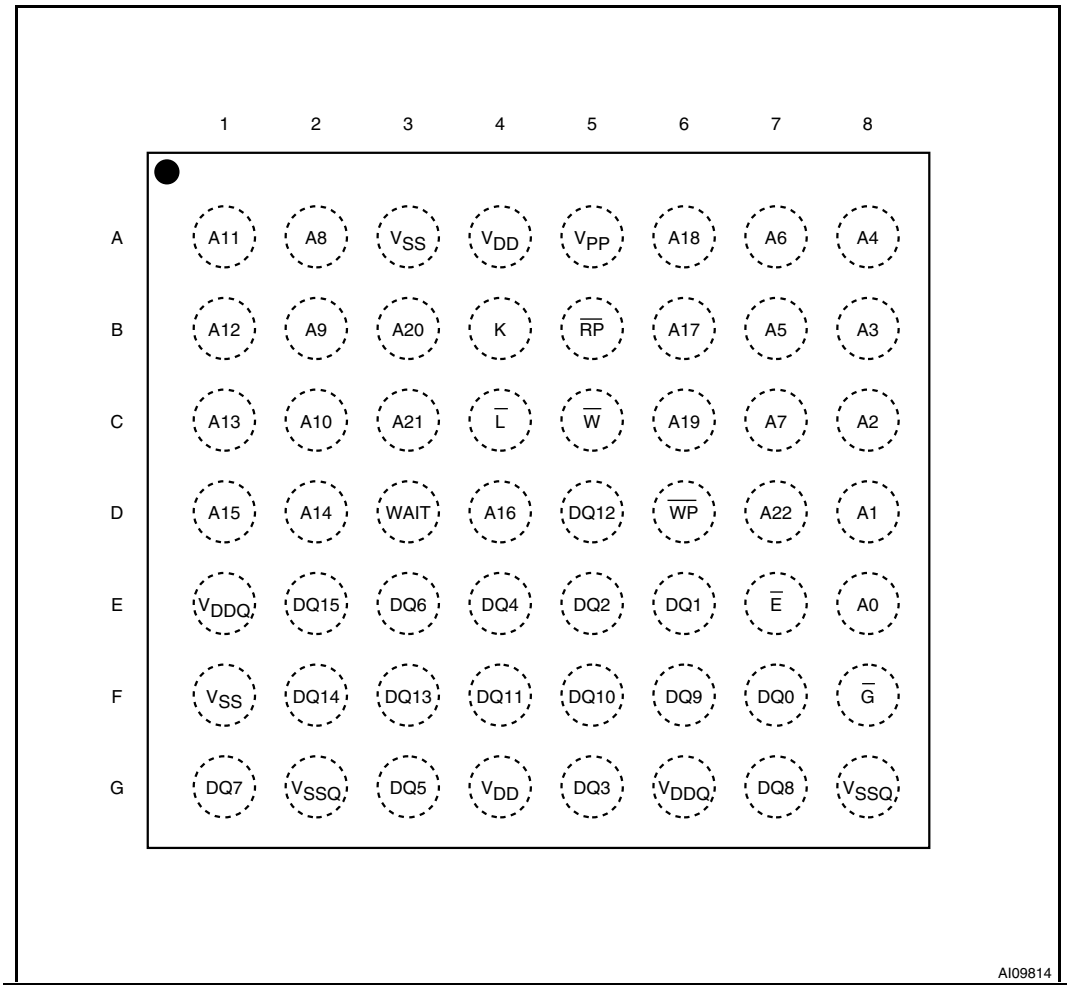
1. Amax is equal to A22 in the M58LR128KT/B and, to A23 in the M58LR256KT/B.

Table 1. Signal names

Signal name	Function	Direction
A0-Amax(1)	Address inputs	Inputs
DQ0-DQ15	Data input/outputs, command inputs	I/O
$\overline{E}$	Chip Enable	Input
$\overline{G}$	Output Enable	Input
$\overline{W}$	Write Enable	Input
$\overline{RP}$	Reset	Input
$\overline{WP}$	Write Protect	Input
K	Clock	Input
$\overline{L}$	Latch Enable	Input
WAIT	Wait	Output
V_{DD}	Supply voltage	
V_{DDQ}	Supply voltage for input/output buffers	
V_{PP}	Optional supply voltage for fast program & erase	
V_{SS}	Ground	
V_{SSQ}	Ground input/output supply	

1. Amax is equal to A22 in the M58LR128KT/B and, to A23 in the M58LR256KT/B.

Figure 2. VFBGA56 package connections (top view through package)



1. This package is available only for the M58LR128KT/B devices.

Figure 3. TFBGA88 connections (top view through package)

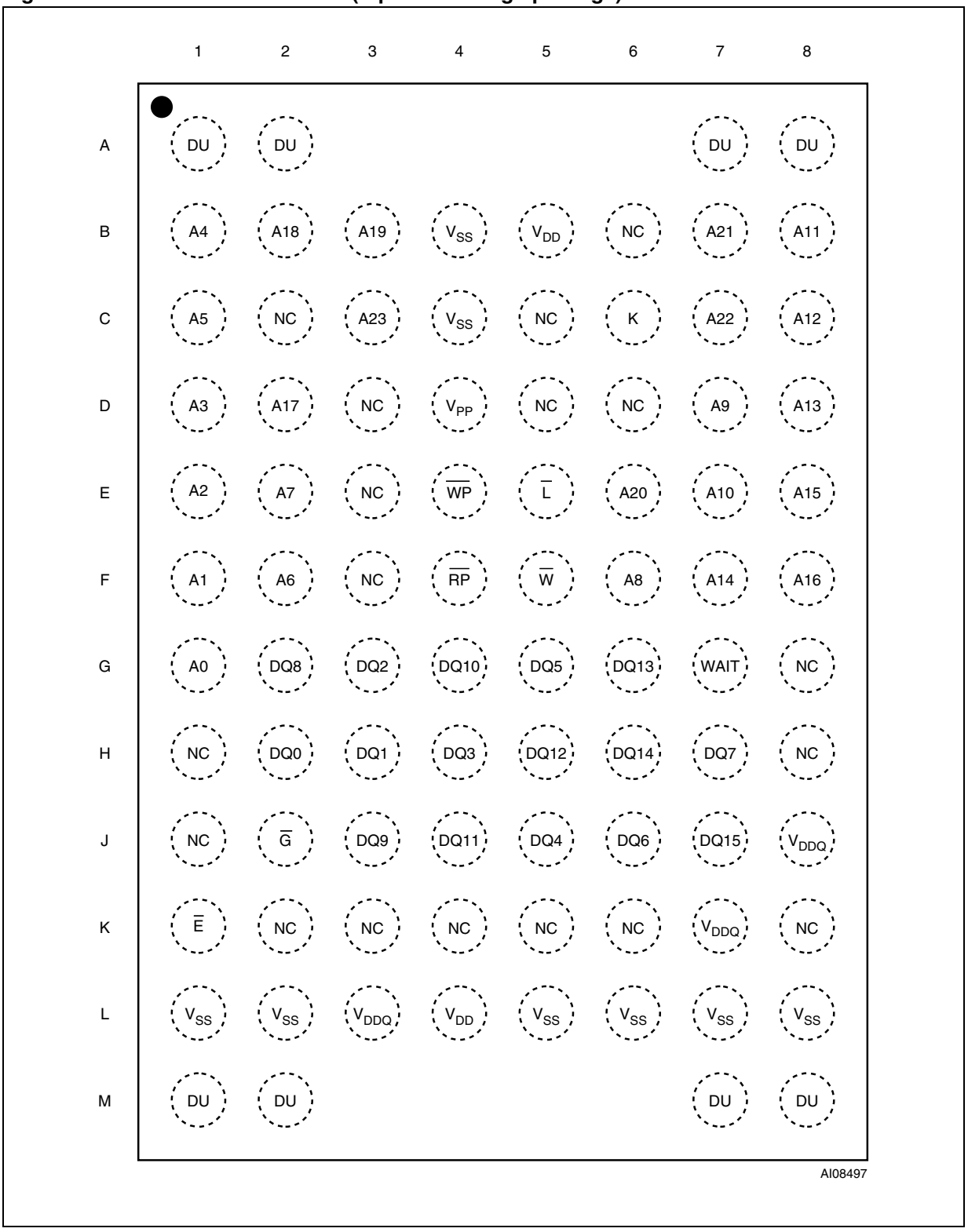


Figure 1: 7x9 Active-Ball Matrix for 256-Mbit Density in VF BGA Package

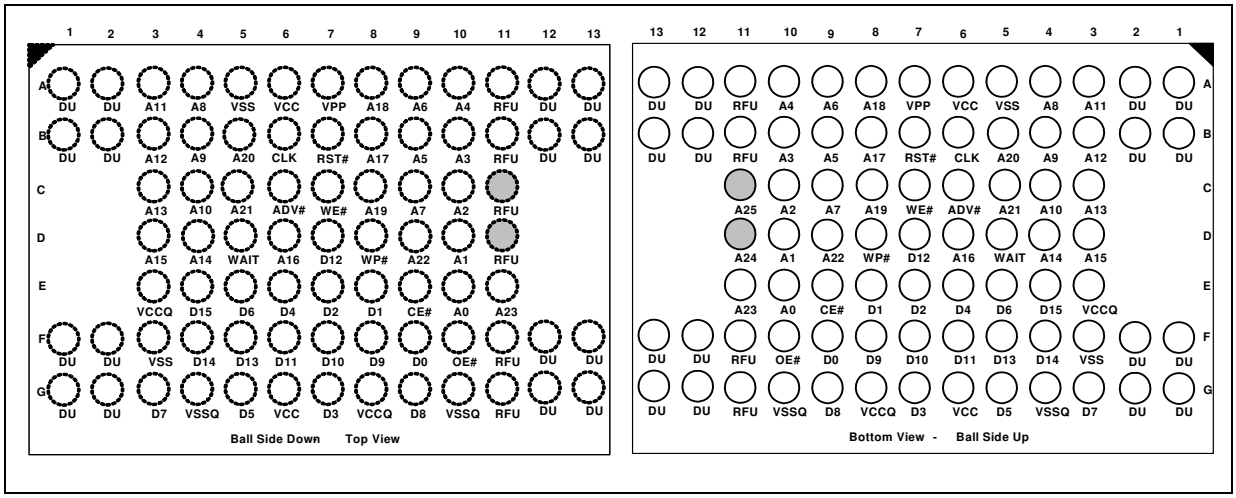


Table 2. M58LR128KT/B bank architecture

Number	Bank size	Parameter blocks	Main blocks
Parameter Bank	8 Mbits	4 blocks of 16 Kwords	7 blocks of 64 Kwords
Bank 1	8 Mbits	-	8 blocks of 64 Kwords
Bank 2	8 Mbits	-	8 blocks of 64 Kwords
Bank 3	8 Mbits	-	8 blocks of 64 Kwords
⋮	⋮	⋮	⋮
Bank 14	8 Mbits	-	8 blocks of 64 Kwords
Bank 15	8 Mbits	-	8 blocks of 64 Kwords

Figure 4. M58LR128KT/B memory map

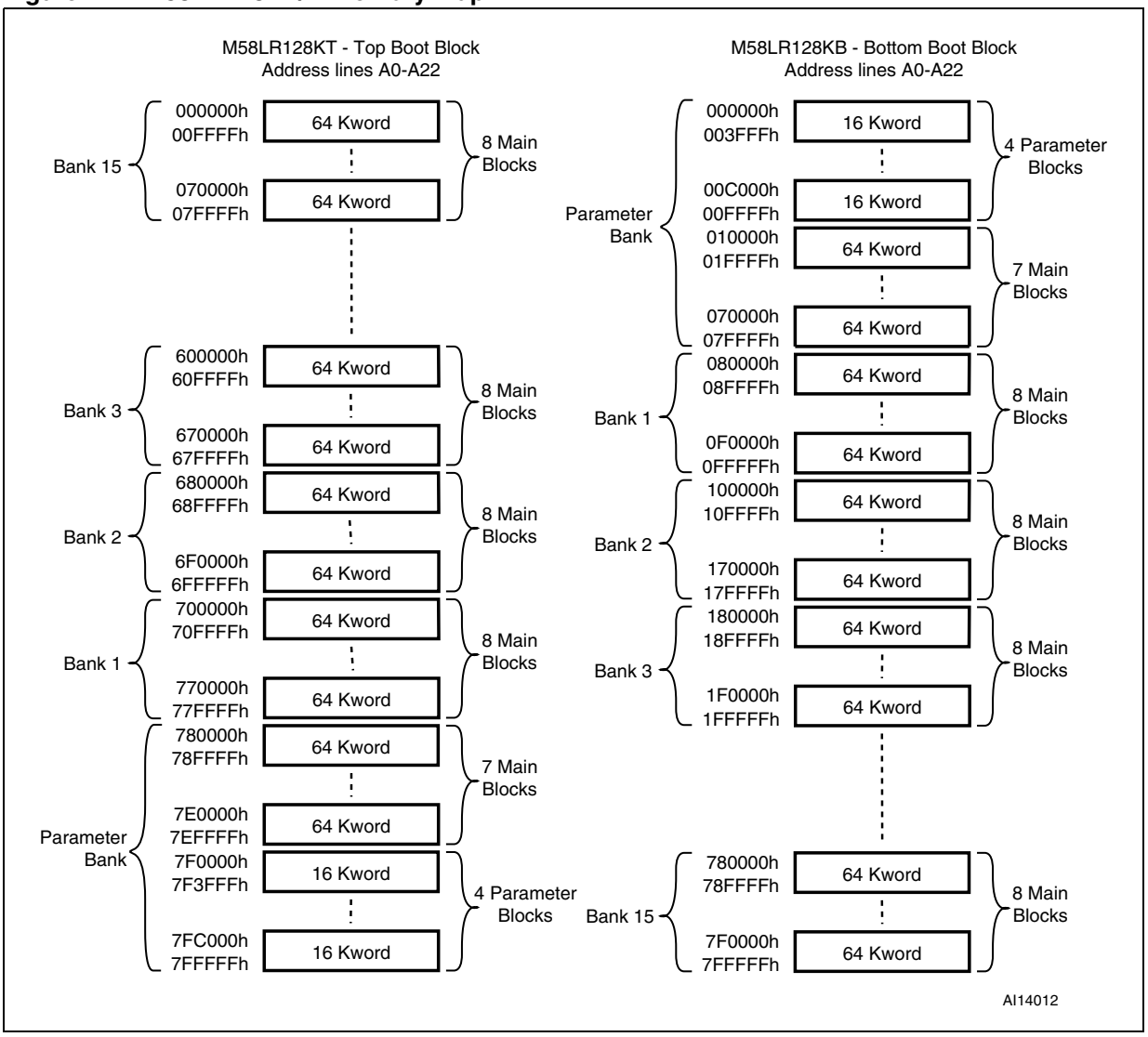
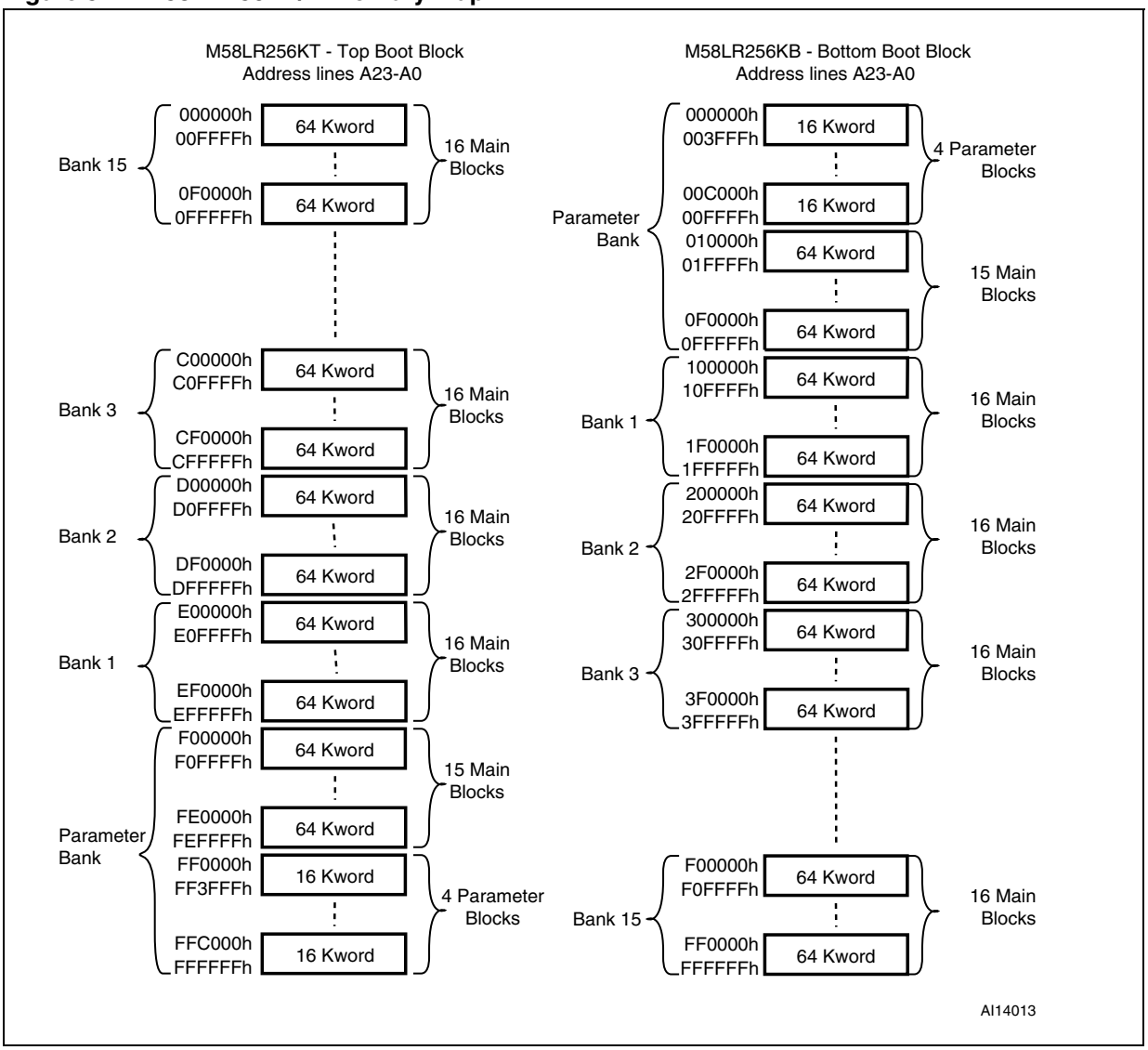


Table 3. M58LR256KT/B bank architecture

Number	Bank size	Parameter blocks	Main blocks
Parameter bank	16 Mbits	4 blocks of 16 Kwords	15 blocks of 64 Kwords
Bank 1	16 Mbits	-	16 blocks of 64 Kwords
Bank 2	16 Mbits	-	16 blocks of 64 Kwords
Bank 3	16 Mbits	-	16 blocks of 64 Kwords
⋮	⋮	⋮	⋮
Bank 14	16 Mbits	-	16 blocks of 64 Kwords
Bank 15	16 Mbits	-	16 blocks of 64 Kwords

Figure 5. M58LR256KT/B memory map



2 Signal descriptions

See *Figure 1: Logic diagram* and *Table 1: Signal names* for a brief overview of the signals connected to this device.

2.1 Address inputs (A0-Amax)

Amax is the highest order address input. It is equal to A22 in the M58LR128KT/B and, to A23 in the M58LR256KT/B. The address inputs select the cells in the memory array to access during bus read operations. During bus write operations they control the commands sent to the command interface of the Program/Erase Controller.

2.2 Data inputs/outputs (DQ0-DQ15)

The data I/O output the data stored at the selected address during a bus read operation or input a command or the data to be programmed during a bus write operation.

2.3 Chip Enable ($\overline{E}$)

The Chip Enable input activates the memory control logic, input buffers, decoders and sense amplifiers. When Chip Enable is at V_{IL} and Reset is at V_{IH} the device is in active mode. When Chip Enable is at V_{IH} the memory is deselected, the outputs are high impedance and the power consumption is reduced to the standby level.

2.4 Output Enable ($\overline{G}$)

The Output Enable input controls data outputs during the bus read operation of the memory.

2.5 Write Enable ($\overline{W}$)

The Write Enable input controls the bus write operation of the memory's command interface. The data and address inputs are latched on the rising edge of Chip Enable or Write Enable, whichever occurs first.

2.6 Write Protect ($\overline{WP}$)

Write Protect is an input that gives an additional hardware protection for each block. When Write Protect is at V_{IL}, the lock-down is enabled and the protection status of the locked-down blocks cannot be changed. When Write Protect is at V_{IH}, the lock-down is disabled and the locked-down blocks can be locked or unlocked. (refer to *Table 17: Lock status*).

2.7 Reset ($\overline{RP}$)

The Reset input provides a hardware reset of the memory. When Reset is at V_{IL}, the memory is in reset mode: the outputs are high impedance and the current consumption is reduced to the Reset supply current I_{DD2}. Refer to *Table 22: DC characteristics - currents* for the value of I_{DD2}. After Reset all blocks are in the locked state and the Configuration Register is reset. When Reset is at V_{IH}, the device is in normal operation. Exiting reset mode the device enters asynchronous read mode, and a negative transition of Chip Enable or Latch Enable is required to ensure valid data outputs.

2.8 Latch Enable ($\overline{L}$)

Latch Enable latches the address bits on its rising edge. The address latch is transparent when Latch Enable is at V_{IL} and it is inhibited when Latch Enable is at V_{IH}.

2.9 Clock (K)

The Clock input synchronizes the memory to the microcontroller during synchronous read operations; the address is latched on a Clock edge (rising or falling, according to the configuration settings) when Latch Enable is at V_{IL}. Clock is ignored during asynchronous read and in write operations.

2.10 Wait (WAIT)

Wait is an output signal used during synchronous read to indicate whether the data on the output bus are valid. This output is high impedance when Chip Enable is at V_{IH}, Output Enable is at V_{IH} or Reset is at V_{IL}. It can be configured to be active during the wait cycle or one clock cycle in advance.

2.11 V_{DD} supply voltage

V_{DD} provides the power supply to the internal core of the memory device. It is the main power supply for all operations (read, program and erase).

2.12 V_{DDQ} supply voltage

V_{DDQ} provides the power supply to the I/O pins and enables all outputs to be powered independently from V_{DD}. V_{DDQ} can be tied to V_{DD} or can use a separate supply.

2.13 V_{PP} program supply voltage

V_{PP} is both a control input and a power supply pin. The two functions are selected by the voltage range applied to the pin.

If V_{PP} is kept in a low voltage range (0V to V_{DDQ}) V_{PP} is seen as a control input. In this case a voltage lower than V_{PPLK} provides absolute protection against program or erase, while V_{PP} in the V_{PP1} range enables these functions (see Tables *22* and *23*, DC characteristics for the relevant values). V_{PP} is only sampled at the beginning of a program or erase. A change in its value after the operation has started does not have any effect and program or erase operations continue.

If V_{PP} is in the range of V_{PPH} it acts as a power supply pin. In this condition V_{PP} must be stable until the program/erase algorithm is completed.

2.14 V_{SS} ground

V_{SS} ground is the reference for the core supply. It must be connected to the system ground.

2.15 V_{SSQ} ground

V_{SSQ} ground is the reference for the input/output circuitry driven by V_{DDQ}. V_{SSQ} must be connected to V_{SS}

Note: Each device in a system should have V_{DD}, V_{DDQ} and V_{PP} decoupled with a 0.1 µF ceramic capacitor close to the pin (high frequency, inherently low inductance capacitors should be as close as possible to the package). See Figure 10: AC measurement load circuit. The PCB track widths should be sufficient to carry the required V_{PP} program and erase currents.

3 Bus operations

There are six standard bus operations that control the device. These are bus read, bus write, address latch, output disable, standby and reset. See *Table 4: Bus operations* for a summary.

Typically glitches of less than 5 ns on Chip Enable or Write Enable are ignored by the memory and do not affect bus write operations.

3.1 Bus read

Bus read operations are used to output the contents of the memory array, the electronic signature, the Status Register and the Common Flash interface. Both Chip Enable and Output Enable must be at V_{IL} to perform a read operation. The Chip Enable input should be used to enable the device, and Output Enable should be used to gate data onto the output. The data read depends on the previous command written to the memory (see command interface section). See Figures *11*, *12* and *13* read AC waveforms, and Tables *24* and *25* read AC characteristics for details of when the output becomes valid.

3.2 Bus write

Bus write operations write commands to the memory or latch input data to be programmed. A bus write operation is initiated when Chip Enable and Write Enable are at V_{IL} with Output Enable at V_{IH}. Commands, input data and addresses are latched on the rising edge of Write Enable or Chip Enable, whichever occurs first. The addresses must be latched prior to the write operation by toggling Latch Enable (when Chip Enable is at V_{IL}). The Latch Enable must be tied to V_{IH} during the bus write operation.

See Figures *17* and *18*, write AC waveforms, and Tables *26* and *27*, write AC characteristics for details of the timing requirements.

3.3 Address Latch

Address latch operations input valid addresses. Both Chip enable and Latch Enable must be at V_{IL} during address latch operations. The addresses are latched on the rising edge of Latch Enable.

3.4 Output disable

The outputs are high impedance when the Output Enable is at V_{IH}.

3.5 Standby

Standby disables most of the internal circuitry allowing a substantial reduction of the current consumption. The memory is in standby when Chip Enable and Reset are at V_{IH}. The power consumption is reduced to the standby level I_{DD3} and the outputs are set to high impedance, independently from the Output Enable or Write Enable inputs. If Chip Enable switches to V_{IH} during a program or erase operation, the device enters standby mode when finished.

3.6 Reset

During reset mode the memory is deselected and the outputs are high impedance. The memory is in reset mode when Reset is at V_{IL}. The power consumption is reduced to the reset level, independently from the Chip Enable, Output Enable or Write Enable inputs. If Reset is pulled to V_{SS} during a program or erase, this operation is aborted and the memory content is no longer valid.

Table 4. Bus operations(1)

Operation	$\overline{E}$	$\overline{G}$	$\overline{W}$	$\overline{L}$	$\overline{RP}$	WAIT(2)	DQ15-DQ0
Bus read	V_{IL}	V_{IL}	V_{IH}	V_{IL}(3)	V_{IH}		Data output
Bus write	V_{IL}	V_{IH}	V_{IL}	V_{IL}(3)	V_{IH}		Data input
Address latch	V_{IL}	X	V_{IH}	V_{IL}	V_{IH}		Data output or Hi-Z(4)
Output disable	V_{IL}	V_{IH}	V_{IH}	X	V_{IH}	Hi-Z	Hi-Z
Standby	V_{IH}	X	X	X	V_{IH}	Hi-Z	Hi-Z
Reset	X	X	X	X	V_{IL}	Hi-Z	Hi-Z

1. X = ‘don't care’
2. WAIT signal polarity is configured using the Set Configuration Register command.
3. $\overline{L}$ can be tied to V_{IH} if the valid address has been previously latched.
4. Depends on $\overline{G}$.

4 Command interface

All bus write operations to the memory are interpreted by the command interface. Commands consist of one or more sequential bus write operations. An internal Program/Erase Controller manages all timings and verifies the correct execution of the program and erase commands. The Program/Erase Controller provides a Status Register whose output may be read at any time to monitor the progress or the result of the operation.

The command interface is reset to read mode when power is first applied, when exiting from Reset or whenever V_{DD} is lower than V_{LKO}. Command sequences must be followed exactly. Any invalid combination of commands are ignored.

Refer to *Table 5: Command codes*, *Table 6: Standard commands*, *Table 7: Factory commands* and *Appendix D: Command interface state tables* for a summary of the command interface.

Table 5. Command codes

Hex Code	Command
01h	Block Lock Confirm
03h	Set Configuration Register Confirm
10h	Alternative Program Setup
20h	Block Erase Setup
2Fh	Block Lock-Down Confirm
40h	Program Setup
50h	Clear Status Register
60h	Block Lock Setup, Block Unlock Setup, Block Lock Down Setup and Set Configuration Register Setup
70h	Read Status Register
80h	Buffer Enhanced Factory Program Setup
90h	Read Electronic Signature
98h	Read CFI Query
B0h	Program/Erase Suspend
BCh	Blank Check Setup
C0h	Protection Register Program
CBh	Blank Check Confirm
D0h	Program/Erase Resume, Block Erase Confirm, Block Unlock Confirm, Buffer Program or Buffer Enhanced Factory Program Confirm
E8h	Buffer Program
FFh	Read Array

4.1 Read Array command

The Read Array command returns the addressed bank to read array mode.

One bus write cycle is required to issue the Read Array command. Once a bank is in read array mode, subsequent read operations outputs the data from the memory array.

A Read Array command can be issued to any banks while programming or erasing in another bank.

If the Read Array command is issued to a bank currently executing a program or erase operation, the bank returns to read array mode but the program or erase operation continues, however the data output from the bank is not guaranteed until the program or erase operation has finished. The read modes of other banks are not affected.

4.2 Read Status Register command

The device contains a Status Register that monitors program or erase operations.

The Read Status Register command reads the contents of the Status Register for the addressed bank.

One bus write cycle is required to issue the Read Status Register command. Once a bank is in read Status Register mode, subsequent read operations output the contents of the Status Register.

The Status Register data is latched on the falling edge of the Chip Enable or Output Enable signals. Either Chip Enable or Output Enable must be toggled to update the Status Register data.

The Read Status Register command can be issued at any time, even during program or erase operations. The Read Status Register command only changes the read mode of the addressed bank. The read modes of other banks are not affected. only asynchronous read and single synchronous read operations should be used to read the Status Register. A Read Array command is required to return the bank to read array mode.

See *Table 10* for the description of the Status Register bits.

4.3 Read Electronic Signature command

The Read Electronic Signature command reads the manufacturer and device codes, the lock status of the addressed bank, the Protection Register, and the Configuration Register.

One bus write cycle is required to issue the Read Electronic Signature command. Once a bank is in read electronic signature mode, subsequent read operations in the same bank output the manufacturer code, the device code, the lock status of the addressed bank, the Protection Register, or the Configuration Register (see *Table 9*).

The Read Electronic Signature command can be issued at any time, even during program or erase operations, except during Protection Register Program operations. Dual operations between the parameter bank and the electronic signature location are not allowed (see *Table 16: Dual operation limitations* for details).

If a Read Electronic Signature command is issued to a bank that is executing a program or erase operation, the bank goes into read electronic signature mode. Subsequent bus read cycles output the electronic signature data and the Program/Erase Controller continue to program or erase in the background.

The Read Electronic Signature command only changes the read mode of the addressed bank. The read modes of other banks are not affected. Only asynchronous read and single synchronous read operations should be used to read the electronic signature. A Read Array command is required to return the bank to read array mode.

4.4 Read CFI Query command

The Read CFI Query command reads data from the common Flash interface (CFI).

One bus write cycle is required to issue the Read CFI Query command. Once a bank is in read CFI query mode, subsequent bus read operations in the same bank read from the common Flash interface.

The Read CFI Query command can be issued at any time, even during program or erase operations.

If a Read CFI Query command is issued to a bank that is executing a program or erase operation the bank gos into read CFI query mode. Subsequent bus read cycles output the CFI data and the Program/Erase Controller continues to program or erase in the background.

The Read CFI Query command only changes the read mode of the addressed bank. The read modes of other banks are not affected. Only asynchronous read and single synchronous read operations should be used to read from the CFI. A Read Array command is required to return the bank to read array mode. Dual operations between the parameter bank and the CFI memory space are not allowed (see *Table 16: Dual operation limitations* for details).

See *Appendix B: Common Flash interface* and Tables *45*, *46*, *47*, *48*, *49*, *50*, *51*, *52*, *53* and *54* for details on the information contained in the common Flash interface memory area.