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# M58LT128HST
# M58LT128HSB

## 128 Mbit (8 Mb ×16, multiple bank, multilevel interface, burst) 1.8 V supply, secure Flash memories

## Features

- Supply voltage
  - $V_{DD}$ = 1.7 V to 2.0 V for Program, Erase and Read
  - $V_{DDQ}$ = 2.7 V to 3.6 V for I/O buffers
  - $V_{PP}$ = 9 V for fast program
- Synchronous/Asynchronous Read
  - Synchronous Burst Read mode: 52 MHz
  - Asynchronous Page Read mode
  - Random access: 85 ns
- Synchronous Burst Read Suspend
- Programming time
  - 2.5 µs typical word program time using Buffer Enhanced Factory Program command
- Memory organization
  - Multiple bank memory array: 8-Mbit banks
  - Parameter blocks (top or bottom location)
- Dual operations
  - program/erase in one bank while read in others
  - No delay between Read and Write operations
- Block protection
  - All blocks protected at power-up
  - Any combination of blocks can be protected with zero latency
  - Absolute write protection with $V_{PP} = V_{SS}$
- Security
  - Software security features
  - 64-bit unique device number
  - 2112-bit user programmable OTP Cells
- Common flash interface (CFI)
- 100 000 program/erase cycles per block


TBGA64 (ZA)
10 × 13 mm

- Electronic signature
  - Manufacturer code: 20h
  - Top device codes: M58LT128HST: 88D6h
  - Bottom device codes M58LT128HSB: 88D7h
- TBGA64 package
  - ECOPACK® available

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# 1 Description

The M58LT128HST/B are 128 Mbit (8 Mbit x 16) non-volatile secure Flash memories. They may be erased electrically at block level and programmed in system on a word-by-word basis using a 1.7 V to 2.0 V $V_{DD}$ supply for the circuitry and a 2.7 V to 3.6 V $V_{DDQ}$ supply for the Input/Output pins. An optional 9 V $V_{PP}$ power supply is provided to accelerate factory programming.

The devices feature an asymmetrical block architecture, with an array of 131 blocks, divided into 8 Mbit banks. There are 15 banks each containing 8 main blocks of 64 Kwords, and one parameter bank containing 4 parameter blocks of 16 Kwords and 7 main blocks of 64 Kwords.

The multiple bank architecture allows dual operations, while programming or erasing in one bank, Read operations are possible in other banks. Only one bank at a time is allowed to be in Program or Erase mode. It is possible to perform burst reads that cross bank boundaries. The bank architecture is summarized in *Table 2*, and the memory map is shown in *Figure 3*. The parameter blocks are located at the top of the memory address space for the M58LT128HST, and at the bottom for the M58LT128HSB.

Each block can be erased separately. Erase can be suspended to perform a program or read operation in any other block, and then resumed. Program can be suspended to read data at any memory location except for the one being programmed, and then resumed. Each block can be programmed and erased over 100,000 cycles using the supply voltage $V_{DD}$. There is a buffer-enhanced factory programming command available to accelerate programming.

Program And Erase Commands Are Written To The command interface of the memory. An internal Program/Erase Controller manages the timings necessary for program and erase operations. The end of a program or erase operation can be detected and any error conditions identified in the Status Register. The command set required to control the memory is consistent with JEDEC standards.

The device supports Synchronous Burst Read and Asynchronous Read from all blocks of the memory array; at power-up the device is configured for Asynchronous Read. In Synchronous Burst Read mode, data is output on each clock cycle at frequencies of up to 52 MHz. The Synchronous Burst Read operation can be suspended and resumed.

The device features an Automatic Standby mode. When the bus is inactive during Asynchronous Read operations, the device automatically switches to the Automatic Standby mode. In this condition the power consumption is reduced to the standby value and the outputs are still driven.

The M58LT128HST/B features an instant, individual block protection scheme that allows any block to be protected or unprotected with no latency, enabling instant code and data protection. They can be protected individually preventing any accidental programming or erasure. There is an additional hardware protection against program and erase. When $V_{PP} \leq V_{PPLK}$ all blocks are protected against program or erase. All blocks are protected at power-up.

The device includes 17 Protection Registers and 2 Protection Register locks, one for the first Protection Register and the other for the 16 one-time-programmable (OTP) Protection Registers of 128 bits each. The first Protection Register is divided into two segments: a 64 bit segment containing a unique device number written by Numonyx, and a 64 bit segment OTP by the user. The user programmable segment can be permanently protected. *Figure 4*, shows the Protection Register memory map.

The M58LT128HST/B also has a full set of software security features that are not described in this datasheet, but are documented in a dedicated application note. For further information, please contact Numonyx.

The M58LT128HST/B are offered in a TBGA64, 10 × 13 mm, 1 mm pitch package. They are supplied with all the bits erased (set to '1').

**Figure 1. Logic diagram**

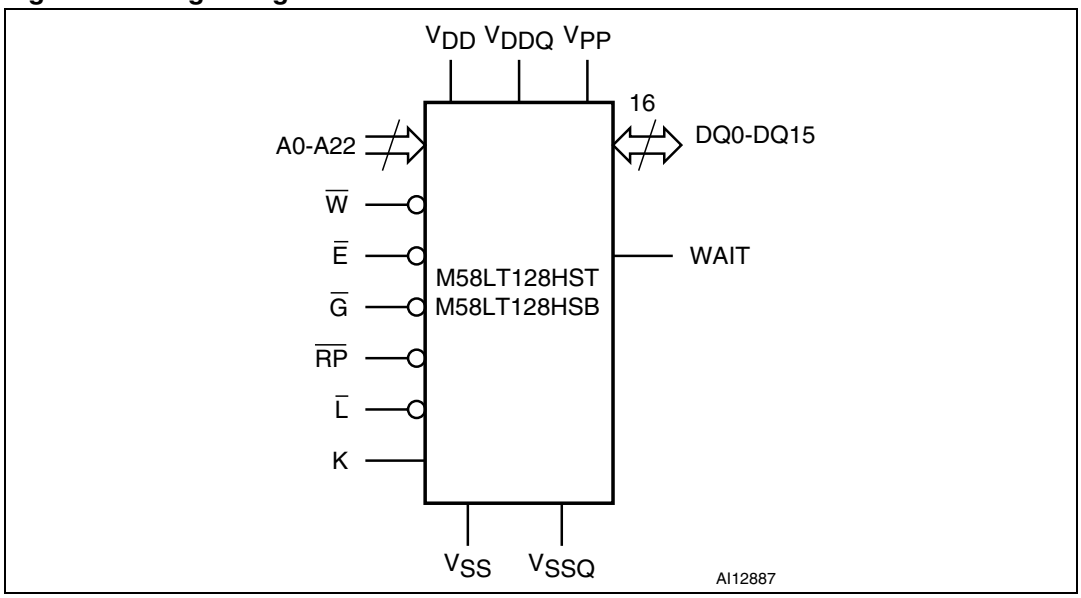



**Table 1. Signal names**

| Signal name | Function | Direction |
|---|---|---|
| A0-A22 | Address inputs | Inputs |
| DQ0-DQ15 | Data input/outputs, command inputs | I/O |
| $\overline{E}$ | Chip Enable | Input |
| $\overline{G}$ | Output Enable | Input |
| $\overline{W}$ | Write Enable | Input |
| $\overline{RP}$ | Reset | Input |
| K | Clock | Input |
| $\overline{L}$ | Latch Enable | Input |
| WAIT | Wait | Output |
| $V_{DD}$ | Supply voltage | Input |
| $V_{DDQ}$ | Supply voltage for input/output buffers | Input |
| $V_{PP}$ | Optional supply voltage for fast program & erase | Input |
| $V_{SS}$ | Ground | |
| $V_{SSQ}$ | Ground input/output supply | Input |
| NC | Not Connected Internally | |
| DU | Do Not Use | |

**Figure 2. TBGA64 package connections (top view through package)**

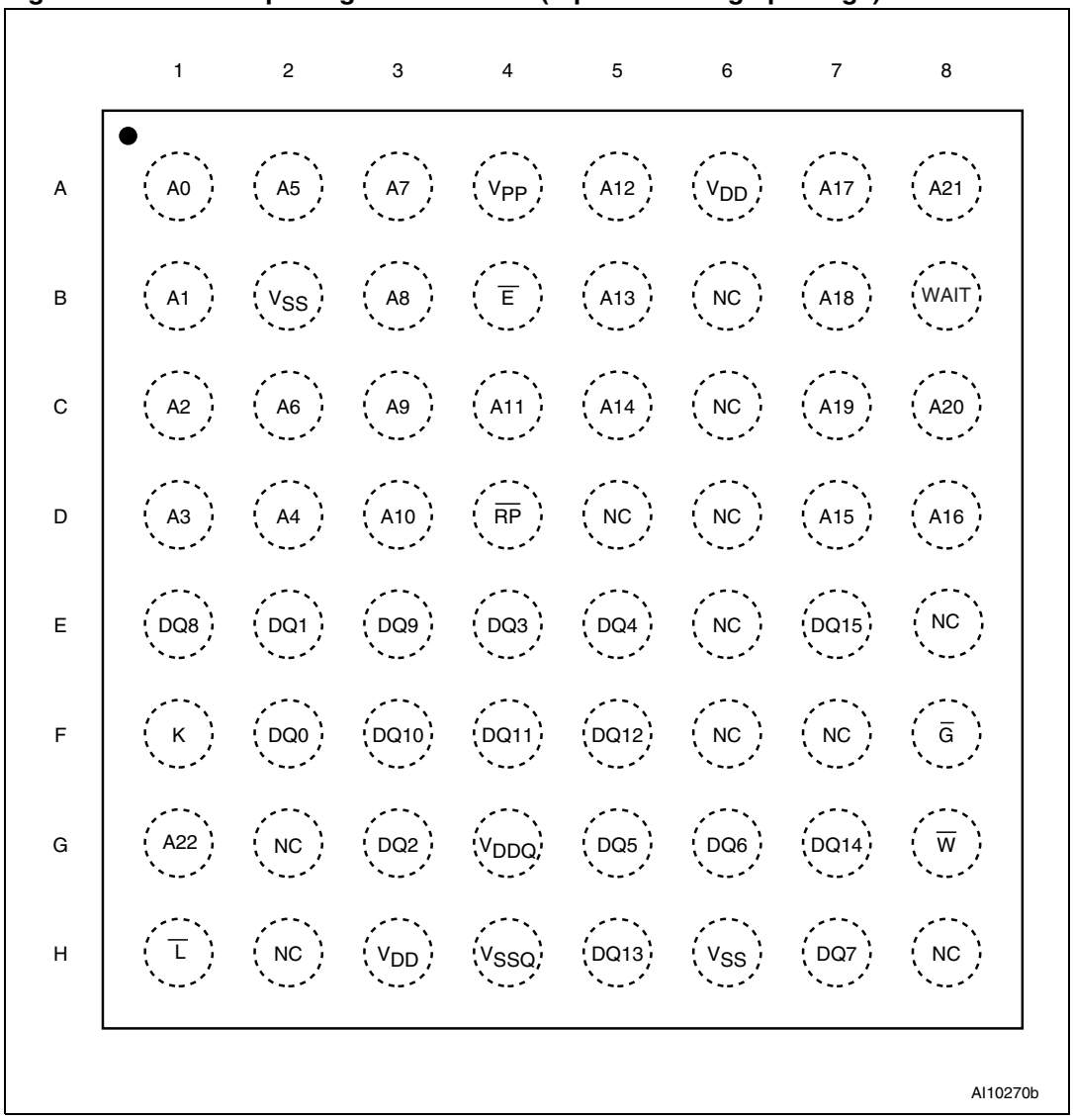
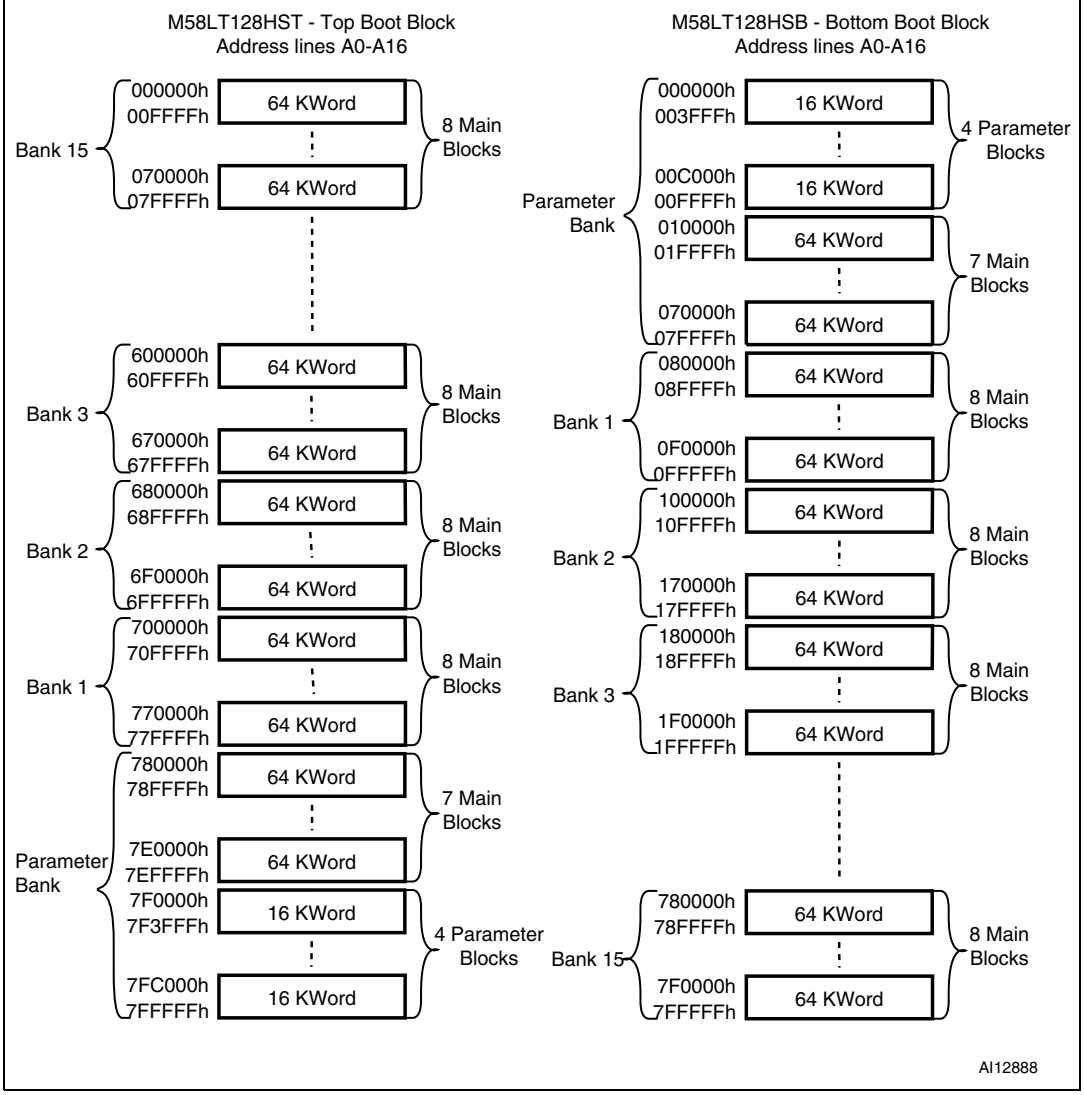


**Table 2. Bank architecture**

| Number | Bank size | Parameter blocks | Main blocks |
|---|---|---|---|
| Parameter bank | 8 Mbits | 4 blocks of 16 Kwords | 7 blocks of 64 Kwords |
| Bank 1 | 8 Mbits | - | 8 blocks of 64 Kwords |
| Bank 2 | 8 Mbits | - | 8 blocks of 64 Kwords |
| Bank 3 | 8 Mbits | - | 8 blocks of 64 Kwords |
| ⋮ | ⋮ | ⋮ | ⋮ |
| Bank 14 | 8 Mbits | - | 8 blocks of 64 Kwords |
| Bank 15 | 8 Mbits | - | 8 blocks of 64 Kwords |

**Figure 3. Memory map**



# 2 Signal descriptions

See *Figure 1: Logic diagram* and *Table 1: Signal names*, for a brief overview of the signals connected to this device.

## 2.1 Address inputs (A0-A22)

The Address Inputs select the cells in the memory array to access during Bus Read operations. During Bus Write operations they control the commands sent to the command interface of the Program/Erase Controller.

## 2.2 Data inputs/outputs (DQ0-DQ15)

The Data I/O output the data stored at the selected address during a Bus Read operation or input a command or the data to be programmed during a Bus Write operation.

## 2.3 Chip Enable ($\overline{E}$)

The Chip Enable input activates the memory control logic, input buffers, decoders and sense amplifiers. When Chip Enable is at $V_{IL}$ and Reset is at $V_{IH}$ the device is in active mode. When Chip Enable is at $V_{IH}$ the memory is deselected, the outputs are high impedance and the power consumption is reduced to the standby level.

## 2.4 Output Enable ($\overline{G}$)

The Output Enable input controls data outputs during the Bus Read operation of the memory.

## 2.5 Write Enable ($\overline{W}$)

The Write Enable input controls the Bus Write operation of the memory's Command Interface. The data and address inputs are latched on the rising edge of Chip Enable or Write Enable whichever occurs first.

## 2.6 Reset ($\overline{RP}$)

The Reset input provides a hardware reset of the memory. When Reset is at $V_{IL}$, the memory is in reset mode: the outputs are high impedance and the current consumption is reduced to the Reset Supply Current $I_{DD2}$. Refer to *Table 20: DC characteristics - currents*, for the value of $I_{DD2}$. After Reset, all blocks are in the protected state and the Configuration Register is reset. When Reset is at $V_{IH}$, the device is in normal operation. When exiting Reset mode the device enters Asynchronous Read mode, but a negative transition of Chip Enable or Latch Enable is required to ensure valid data outputs.

## 2.7 Latch Enable ($\overline{L}$)

Latch Enable latches the address bits on its rising edge. The address latch is transparent when Latch Enable is at $V_{IL}$ and it is inhibited when Latch Enable is at $V_{IH}$.

## 2.8 Clock (K)

The Clock input synchronizes the memory to the microcontroller during Synchronous Read operations; the address is latched on a Clock edge (rising or falling, according to the configuration settings) when Latch Enable is at $V_{IL}$. Clock is ignored during Asynchronous Read and in Write operations.

## 2.9 Wait (WAIT)

Wait is an output signal used during synchronous read to indicate whether the data on the output bus are valid. This output is high impedance when Chip Enable is at $V_{IH}$, Output Enable is at $V_{IH}$ or Reset is at $V_{IL}$. It can be configured to be active during the wait cycle or one clock cycle in advance.

## 2.10 $V_{DD}$ supply voltage

$V_{DD}$ provides the power supply to the internal core of the memory device. It is the main power supply for all operations (Read, Program, and Erase).

## 2.11 $V_{DDQ}$ supply voltage

$V_{DDQ}$ provides the power supply to the I/O pins and enables all outputs to be powered independently from $V_{DD}$.

## 2.12 $V_{PP}$ program supply voltage

$V_{PP}$ is both a control input and a power supply pin. The two functions are selected by the voltage range applied to the pin.

If $V_{PP}$ is kept in a low voltage range (0V to $V_{DDQ}$) $V_{PP}$ is seen as a control input. In this case a voltage lower than $V_{PPLK}$ gives absolute protection against program or erase, while $V_{PP}$ in the $V_{PP1}$ range enables these functions (see Tables *20* and *21*, DC Characteristics for the relevant values). $V_{PP}$ is only sampled at the beginning of a program or erase; a change in its value after the operation has started does not have any effect and program or erase operations continue.

If $V_{PP}$ is in the range of $V_{PPH}$ it acts as a power supply pin. In this condition $V_{PP}$ must be stable until the Program/Erase algorithm is completed.

## 2.13 $V_{SS}$ ground

$V_{SS}$ ground is the reference for the core supply. It must be connected to the system ground.

## 2.14 $V_{SSQ}$ ground

$V_{SSQ}$ ground is the reference for the input/output circuitry driven by $V_{DDQ}$. $V_{SSQ}$ must be connected to $V_{SS}$

*Note: Each device in a system should have $V_{DD}$, $V_{DDQ}$ and $V_{PP}$ decoupled with a 0.1µF ceramic capacitor close to the pin (high-frequency, inherently low inductance capacitors should be as close as possible to the package). See Figure 8: AC measurement load circuit. The PCB track widths should be sufficient to carry the required $V_{PP}$ program and erase currents.*

# 3 Bus operations

There are six standard bus operations that control the device. These are Bus Read, Bus Write, Address Latch, Output Disable, Standby and Reset. See *Table 3: Bus operations*, for a summary.

Typically glitches of less than 5 ns on Chip Enable or Write Enable are ignored by the memory and do not affect Bus Write operations.

## 3.1 Bus Read

Bus Read operations are used to output the contents of the Memory Array, the Electronic Signature, the Status Register and the Common Flash Interface. Both Chip Enable and Output Enable must be at $V_{IL}$ to perform a Read operation. The Chip Enable input is used to enable the device. Output Enable is used to gate data onto the output. The data read depends on the previous command written to the memory (see Command Interface section). See Figures *9*, *10* and *11* Read AC Waveforms, and Tables *22* and *23* Read AC Characteristics, for details of when the output becomes valid.

## 3.2 Bus Write

Bus Write operations write commands to the memory or latch input data to be programmed. A Bus Write operation is initiated when Chip Enable and Write Enable are at $V_{IL}$ with Output Enable at $V_{IH}$. Commands, input data and addresses are latched on the rising edge of Write Enable or Chip Enable, whichever occurs first. The addresses must be latched prior to the write operation by toggling Latch Enable (when Chip Enable is at $V_{IL}$). The Latch Enable must be tied to $V_{IH}$ during the Bus Write operation.

See Figures *15* and *16*, Write AC waveforms, and Tables *24* and *25*, Write AC characteristics, for details of the timing requirements.

## 3.3 Address Latch

Address Latch operations input valid addresses. Both Chip Enable and Latch Enable must be at $V_{IL}$ during Address Latch operations. The addresses are latched on the rising edge of Latch Enable.

## 3.4 Output Disable

The outputs are high impedance when the Output Enable is at $V_{IH}$.

## 3.5 Standby

Standby disables most of the internal circuitry, allowing a substantial reduction of the current consumption. The memory is in Standby when Chip Enable and Reset are at $V_{IH}$. The power consumption is reduced to the standby level $I_{DD3}$ and the outputs are set to high impedance, independently from the Output Enable or Write Enable inputs. If Chip Enable switches to $V_{IH}$ during a Program or Erase operation, the device enters Standby mode when finished.

## 3.6 Reset

During Reset mode the memory is deselected and the outputs are high impedance. The memory is in Reset mode when Reset is at $V_{IL}$. The power consumption is reduced to the Reset level, independently from the Chip Enable, Output Enable, or Write Enable inputs. If Reset is pulled to $V_{SS}$ during a Program or Erase, this operation is aborted and the memory content is no longer valid.

**Table 3. Bus operations(1)**

| Operation | $\overline{E}$ | $\overline{G}$ | $\overline{W}$ | $\overline{L}$ | $\overline{RP}$ | WAIT(2) | DQ15-DQ0 |
|---|---|---|---|---|---|---|---|
| Bus Read | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | $V_{IL}$(3) | $V_{IH}$ | | Data Output |
| Bus Write | $V_{IL}$ | $V_{IH}$ | $V_{IL}$ | $V_{IL}$(3) | $V_{IH}$ | | Data Input |
| Address Latch | $V_{IL}$ | X | $V_{IH}$ | $V_{IL}$ | $V_{IH}$ | | Data Output or Hi-Z(4) |
| Output Disable | $V_{IL}$ | $V_{IH}$ | $V_{IH}$ | X | $V_{IH}$ | Hi-Z | Hi-Z |
| Standby | $V_{IH}$ | X | X | X | $V_{IH}$ | Hi-Z | Hi-Z |
| Reset | X | X | X | X | $V_{IL}$ | Hi-Z | Hi-Z |

1. X = 'Don't care'.
2. WAIT signal polarity is configured using the Set Configuration Register command.
3. $\overline{L}$ can be tied to $V_{IH}$ if the valid address has been previously latched.
4. Depends on $\overline{G}$.

# 4 Command interface

All Bus Write operations to the memory are interpreted by the Command Interface. Commands consist of one or more sequential Bus Write operations. An internal Program/Erase Controller handles all timings and verifies the correct execution of the program and erase commands. The Program/Erase Controller provides a Status Register whose output may be read at any time to monitor the progress or the result of the operation.

When exiting from Reset or whenever $V_{DD}$ is lower than $V_{LKO}$, the Command Interface is reset to Read mode when power is first applied. Command sequences must be followed exactly. Any invalid combination of commands is ignored.

Refer to *Table 4: Command codes*, *Table 5: Standard commands*, *Table 6: Factory commands*, and *Appendix D: Command Interface state tables* for a summary of the Command Interface.

**Table 4. Command codes**

| Hex Code | Command |
|---|---|
| 01h | Block Protect Confirm |
| 03h | Set Configuration Register Confirm |
| 10h | Alternative Program Setup |
| 20h | Block Erase Setup |
| 40h | Program Setup |
| 50h | Clear Status Register |
| 60h | Block Protect Setup, Block Unprotect Setup and Set Configuration Register Setup |
| 70h | Read Status Register |
| 80h | Buffer Enhanced Factory Program Setup |
| 90h | Read Electronic Signature |
| 98h | Read CFI Query |
| B0h | Program/Erase Suspend |
| BCh | Blank Check Setup |
| C0h | Protection Register Program |
| CBh | Blank Check Confirm |
| D0h | Program/Erase Resume, Block Erase Confirm, Block Unprotect Confirm, Buffer Program or Buffer Enhanced Factory Program Confirm |
| E8h | Buffer Program |
| FFh | Read Array |

## 4.1 Read Array command

The Read Array command returns the addressed bank to Read Array mode.

One Bus Write cycle is required to issue the Read Array command. Once a bank is in Read Array mode, subsequent read operations outputs the data from the memory array.

A Read Array command can be issued to any banks while programming or erasing in another bank. If the Read Array command is issued to a bank currently executing a program or erase operation, the bank returns to Read Array mode, but the Program or Erase operation continues. However, the data output from the bank is not guaranteed until the Program or Erase operation is finished. The Read modes of other banks are not affected.

## 4.2 Read Status Register command

The device contains a Status Register that is used to monitor program or erase operations.

The Read Status Register command is used to read the contents of the Status Register for the addressed bank.

One Bus Write cycle is required to issue the Read Status Register command. Once a bank is in Read Status Register mode, subsequent Read operations output the contents of the Status Register.

The Status Register data is latched on the falling edge of the Chip Enable or Output Enable signals. Either Chip Enable or Output Enable must be toggled to update the Status Register data

The Read Status Register command can be issued at any time, even during Program or Erase operations. The Read Status Register command only changes the Read mode of the addressed bank. The Read modes of other banks are not affected. Only Asynchronous Read and Single Synchronous Read operations should be used to read the Status Register. A Read Array command is required to return the bank to Read Array mode.

See *Table 9* for the description of the Status Register Bits.

## 4.3 Read Electronic Signature command

The Read Electronic Signature command is used to read the manufacturer and device codes, the protection status of the addressed bank, the Protection Register, and the Configuration Register.

One Bus Write cycle is required to issue the Read Electronic Signature command. Once a bank is in Read Electronic Signature mode, subsequent Read operations in the same bank output the manufacturer code, the device code, the protection status of the addressed bank, the Protection Register, or the Configuration Register (see *Table 8*).

The Read Electronic Signature command can be issued at any time, even during Program or Erase operations, except during Protection Register Program operations. Dual operations between the parameter bank and the electronic signature location are not allowed (see *Table 15: Dual operation limitations* for details).

If a Read Electronic Signature command is issued to a bank that is executing a Program or Erase operation the bank go into Read Electronic Signature mode. Subsequent Bus Read cycles output the Electronic Signature data and the Program/Erase Controller continues to program or erase in the background.

The Read Electronic Signature command only changes the Read mode of the addressed bank. The Read modes of other banks are not affected. Only Asynchronous Read and Single Synchronous Read operations should be used to read the Electronic Signature. A Read Array command is required to return the bank to Read Array mode.

## 4.4 Read CFI Query command

The Read CFI Query command is used to read data from the Common Flash Interface (CFI).

One Bus Write cycle is required to issue the Read CFI Query command. Once a bank is in Read CFI Query mode, subsequent Bus Read operations in the same bank read from the Common Flash Interface. The Read CFI Query command can be issued at any time, even during Program or Erase operations.

If a Read CFI Query command is issued to a bank that is executing a Program or Erase operation the bank goes into Read CFI Query mode. Subsequent Bus Read cycles output the CFI data and the Program/Erase controller continues to Program or Erase in the background.

The Read CFI Query command only changes the Read mode of the addressed bank. The Read modes of other banks are not affected. Only Asynchronous Read and Single Synchronous Read operations should be used to read from the CFI. A Read Array command is required to return the bank to Read Array mode. Dual operations between the Parameter Bank and the CFI memory space are not allowed (see *Table 15: Dual operation limitations* for details).

See *Appendix B: Common Flash Interface*, Tables *31*, *32*, *33*, *34*, *35*, *36*, *37*, *38*, *39* and *40* for details on the information contained in the Common Flash Interface memory area.

## 4.5 Clear Status Register command

The Clear Status Register command can be used to reset (set to ‘0’) all error bits (SR1, 3, 4 and 5) in the Status Register.

One Bus Write cycle is required to issue the Clear Status Register command. The Clear Status Register command does not affect the Read mode of the bank.

The error bits in the Status Register do not automatically return to ‘0’ when a new command is issued. The error bits in the Status Register should be cleared before attempting a new Program or Erase command.

## 4.6 Block Erase command

The Block Erase command is used to erase a block. It sets all the bits within the selected block to ’1’. All previous data in the block is lost.

If the block is protected then the erase operation aborts, the data in the block is not changed, and the Status Register outputs the error.

The following two Bus Write cycles are required to issue the command:

- The first bus cycle sets up the Block Erase command.
- The second latches the block address and starts the Program/Erase Controller.

If the second bus cycle is not the Block Erase Confirm code, Status Register bits SR4 and SR5 are set and the command is aborted.

Once the command is issued, the bank enters Read Status Register mode and any Read operation within the addressed bank outputs the contents of the Status Register. A Read Array command is required to return the bank to Read Array mode.

During Block Erase operations the bank containing the block being erased only accepts the Read Array, Read Status Register, Read Electronic Signature, Read CFI Query, and the Program/Erase Suspend command; all other commands are ignored.

The Block Erase operation aborts if Reset, $\overline{RP}$, goes to $V_{IL}$. As data integrity cannot be guaranteed when the Block Erase operation is aborted, the block must be erased again.

Refer to *Chapter 8: Dual operations and multiple bank architecture* for detailed information about simultaneous operations allowed in banks not being erased.

Typical erase times are given in *Table 16: Program/erase times and endurance cycles*.

See *Appendix C*, *Figure 23: Block Erase flowchart and pseudo code* for a suggested flowchart for using the Block Erase command.

## 4.7 Blank Check command

The Blank Check command is used to check whether a block has been completely erased. Only one block at a time can be checked. To use the Blank Check command, $V_{PP}$ must be equal to $V_{PPH}$. If $V_{PP}$ is not equal to $V_{PPH}$, the device ignores the command and no error is shown in the Status Register.

The following two bus cycles are required to issue the Blank Check command:

- The first bus cycle writes the Blank Check command (BCh) to any address in the block to be checked.
- The second bus cycle writes the Blank Check Confirm command (CBh) to any address in the block to be checked and starts the Blank Check operation.

If the second bus cycle is not Blank Check Confirm, Status Register bits SR4 and SR5 are set to '1' and the command aborts.

Once the command is issued the addressed bank automatically enters the Status Register mode and further reads the Status Register contents within the bank output.

The only operation permitted during Blank Check is Read Status Register. Dual operations are not supported while a Blank Check operation is in progress. Blank Check operations cannot be suspended and are not allowed while the device is in Program/Erase Suspend.

The SR7 Status Register bit indicates the status of the Blank Check operation in progress: SR7 = '0' means that the Blank Check operation is still ongoing, and SR7 = '1' means that the operation is complete.

The SR5 Status Register bit goes High (SR5 = '1') to indicate if the Blank Check operation has failed.

At the end of the operation the bank remains in the Read Status Register mode until another command is written to the Command Interface.

See *Appendix C*, *Figure 20: Blank Check flowchart and pseudo code* for a suggested flowchart for using the Blank Check command.

Typical Blank Check times are given in *Table 16: Program/erase times and endurance cycles*.

## 4.8 Program command

The Program command is used to program a single word to the memory array.

If the block being programmed is protected, then the Program operation aborts, the data in the block is not changed, and the Status Register outputs the error.

The following two Bus Write cycles are required to issue the Program Command:

- The first bus cycle sets up the Program command.
- The second latches the address and data to be programmed and starts the Program/Erase Controller.

Once the programming has started, Read operations in the bank being programmed output the Status Register content.

During a Program operation, the bank containing the word being programmed only accepts the Read Array, Read Status Register, Read Electronic Signature, Read CFI Query and the Program/Erase Suspend commands; all other commands are ignored. A Read Array command is required to return the bank to Read Array mode.

Refer to *Chapter 8: Dual operations and multiple bank architecture* for detailed information about simultaneous operations allowed in banks not being programmed.

Typical Program times are given in *Table 16: Program/erase times and endurance cycles*.

The Program operation aborts if Reset, $\overline{RP}$, goes to $V_{IL}$. As data integrity cannot be guaranteed when the Program operation is aborted, the word must be reprogrammed.

See *Appendix C*, *Figure 19: Program flowchart and pseudo code* for the flowchart for using the Program command.

## 4.9 Buffer Program command

The Buffer Program Command makes use of the device's 32-word Write Buffer to accelerate programming. Up to 32 words can be loaded into the Write Buffer, which can dramatically reduce in-system programming time compared to the standard non-buffered Program command.

Four successive steps are required to issue the Buffer Program command:

1. The first Bus Write cycle sets up the Buffer Program command. The setup code can be addressed to any location within the targeted block.

After the first Bus Write cycle, Read operations in the bank output the contents of the Status Register. Status Register bit SR7 should be read to check that the buffer is available (SR7 = '1'). If the buffer is not available (SR7 = '0'), re-issue the Buffer Program command to update the Status Register contents.

2. The second Bus Write cycle sets up the number of words to be programmed. Value "n" is written to the same block address, where n+1 is the number of words to be programmed.
3. Use n+1 Bus Write cycles to load the address and data for each word into the Write Buffer. Addresses must lie within the range from the start address to the start address + n, where the start address is the location of the first data to be programmed. Optimum performance is obtained when the start address corresponds to a 32-word boundary.
4. The final Bus Write cycle confirms the Buffer Program command and starts the program operation.

All the addresses used in the Buffer Program operation must lie within the same block.

Invalid address combinations or an incorrect sequence of Bus Write cycles sets an error in the Status Register and aborts the operation without affecting the data in the memory array.

If the block being programmed is protected an error is set in the Status Register, and the operation aborts without affecting the data in the memory array.

During Buffer Program operations the bank being programmed only accepts the Read Array, Read Status Register, Read Electronic Signature, Read CFI Query, and the Program/Erase Suspend command; all other commands are ignored.

Refer to *Chapter 8: Dual operations and multiple bank architecture* for detailed information about simultaneous operations allowed in banks not being programmed.

See *Appendix C*, *Figure 21: Buffer Program flowchart and pseudo code* for a suggested flowchart on using the Buffer Program command.

## 4.10 Buffer Enhanced Factory Program command

The Buffer Enhanced Factory Program command has been specially developed to accelerate programming in manufacturing environments where the programming time is critical. It is used to program one or more Write Buffer(s) of 32 words to a block. Once the device enters Buffer Enhanced Factory Program mode, the Write Buffer can be reloaded any number of times as long as the address remains within the same block. Only one block can be programmed at a time.

If the block being programmed is protected, then the Program operation aborts, the data in the block is not changed and the Status Register outputs the error.

The use of the Buffer Enhanced Factory Program command requires the following operating conditions:

- $V_{PP}$ must be set to $V_{PPH}$
- $V_{DD}$ must be within operating range
- Ambient temperature $T_A$ must be 30°C ± 10°C
- The targeted block must be unprotected
- The start address must be aligned with the start of a 32-word buffer boundary
- The address must remain the Start Address throughout programming.

Dual operations are not supported during the Buffer Enhanced Factory Program operation and the command cannot be suspended.

The Buffer Enhanced Factory Program Command consists of three phases: the Setup Phase, the Program and Verify Phase, and the Exit Phase. Refer to *Table 6: Factory commands* for detailed information.

### 4.10.1 Setup phase

The Buffer Enhanced Factory Program command requires the following two Bus Write cycles to initiate the command.

- The first Bus Write cycle sets up the Buffer Enhanced Factory Program command.
- The second Bus Write cycle confirms the command.

After the Confirm command is issued, Read operations output the contents of the Status Register. The read Status Register command must not be issued, othewise it is interpreted as data to program.

The Status Register Program/Erase Controller bit SR7 should be read to check that the Program/Erase Controller is ready to proceed to the next phase.

If an error is detected, SR4 goes high (set to ‘1’) and the Buffer Enhanced Factory Program operation is terminated. See *Chapter 5: Status Register* for details on the error.

### 4.10.2 Program and verify phase

The program and verify phase requires 32 cycles to program the 32 words to the Write Buffer. The data is stored sequentially, starting at the first address of the Write Buffer, until the Write Buffer is full (32 words). To program less than 32 words, the remaining words should be programmed with FFFFh.

The following three successive steps are required to issue and execute the program and verify phase of the command.

1. Use one Bus Write operation to latch the Start Address and the first word to be programmed. The Status Register Bank Write status bit SR0 should be read to check that the Program/Erase Controller is ready for the next word.
2. Each subsequent word to be programmed is latched with a new Bus Write operation. The address must remain the start address as the Program/Erase Controller increments the address location. If any address is given that is not in the same block as the start address, the program and verify phase terminates. Status Register bit SR0 should be read between each Bus Write cycle to check that the Program/Erase Controller is ready for the next word.
3. Once the Write Buffer is full, the data is programmed sequentially to the memory array. After the Program operation, the device automatically verifies the data and reprograms, if necessary.

The program and verify phase can be repeated, without re-issuing the command, to program additional 32 word locations as long as the address remains in the same block.

4. Finally, after all words, or the entire block has been programmed, write one Bus Write operation to any address outside the block containing the start address, to terminate program and verify phase.

Status Register bit SR0 must be checked to determine whether the Program operation is finished. The Status Register may be checked for errors at any time but it must be checked after the entire block has been programmed.

### 4.10.3 Exit phase

Status Register Program/Erase Controller bit SR7 set to ‘1’ indicates that the device has exited the Buffer Enhanced Factory Program operation and returned to Read Status Register mode. A full Status Register check should be done to ensure that the block has been successfully programmed. See Section *Table 5: Status Register* for more details.

For optimum performance the Buffer Enhanced Factory Program command should be limited to a maximum of 100 program/erase cycles per block. If this limit is exceeded, the internal algorithm continues to work properly but some degradation in performance is possible. Typical program times are given in *Table 16*.

See *Appendix C*, *Figure 27: Buffer Enhanced Factory Program flowchart and pseudo code* for a suggested flowchart on using the Buffer Enhanced Factory Program command.