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M58LW032C

32 Mbit (2Mb x16, Uniform Block, Burst)
3V Supply Flash Memory

FEATURES SUMMARY

- WIDE x16 DATA BUS for HIGH BANDWIDTH
- SUPPLY VOLTAGE
 - $V_{DD} = 2.7$ to $3.6V$ core supply voltage for Program, Erase and Read operations
 - $V_{DDQ} = 1.8$ to V_{DD} for I/O Buffers
- SYNCHRONOUS/ASYNCHRONOUS READ
 - Synchronous Burst Read
 - Asynchronous Random Read
 - Asynchronous Address Latch Controlled Read
 - Page Read
- ACCESS TIME
 - Synchronous Burst Read up to 56MHz
 - Asynchronous Page Mode Read 90/25ns, 110/25ns
 - Random Read 90ns, 110ns
- PROGRAMMING TIME
 - 16 Word Write Buffer
 - 12 μ s Word effective programming time
- 32 UNIFORM 64 KWord MEMORY BLOCKS
- ENHANCED SECURITY
 - Block Protection/ Unprotection
 - Smart Protection: irreversible block locking system
 - V_{PEN} signal for Program Erase Enable
 - 128 bit Protection Register with 64 bit Unique Code in OTP area
- PROGRAM and ERASE SUSPEND
- COMMON FLASH INTERFACE
- 100,000 PROGRAM/ERASE CYCLES per BLOCK
- ELECTRONIC SIGNATURE
 - Manufacturer Code: 0020h
 - Device Code M58LW032C: 8822h
- PACKAGES
 - Compliant with Lead-Free Soldering Processes
 - Lead-Free Versions

Figure 1. Packages

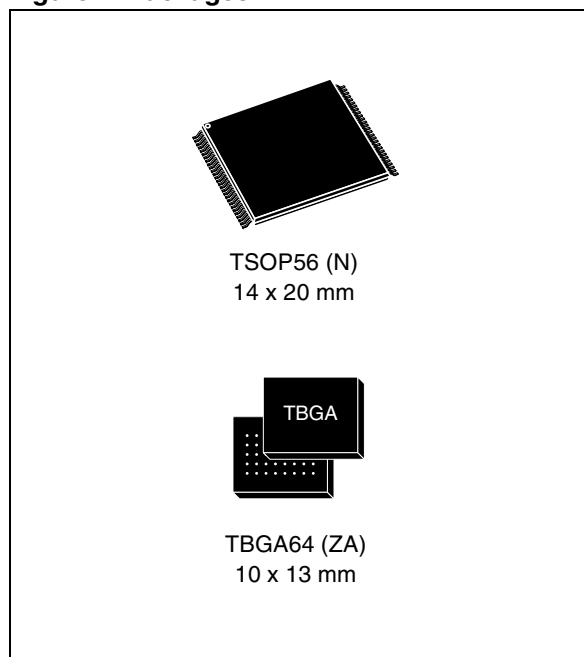


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SUMMARY DESCRIPTION

M58LW032C is a 32 Mbit (2Mb x16) non-volatile memory that can be read, erased and reprogrammed. These operations can be performed using a single low voltage (2.7V to 3.6V) core supply. On power-up the memory defaults to Read mode with an asynchronous bus where it can be read in the same way as a non-burst Flash memory.

The memory is divided into 32 blocks of 1Mbit that can be erased independently so it is possible to preserve valid data while old data is erased. Program and Erase commands are written to the Command Interface of the memory. An on-chip Program/Erase Controller simplifies the process of programming or erasing the memory by taking care of all of the special operations that are required to update the memory contents. The end of a Program or Erase operation can be detected and any error conditions identified in the Status Register. The command set required to control the memory is consistent with JEDEC standards.

The device supports synchronous burst read and asynchronous read from all blocks of the memory array; at power-up the device is configured for asynchronous read. In asynchronous mode an Address Latch input can be used to latch addresses in Latch Controlled mode. In synchronous burst mode, data is output on each clock cycle at frequencies of up to 56MHz.

The Write Buffer allows the microprocessor to program from 1 to 16 Words in parallel, both speeding up the programming and freeing up the microprocessor to perform other work. A Word Program command is available to program a single Word.

Erase can be suspended in order to perform either Read or Program in any other block and then resumed. Program can be suspended to Read data in any other block and then resumed. Each block can be programmed and erased over 100,000 cycles.

The M58LW032C has several security features to increase data protection.

- Block Protection, where each block can be individually protected against program or erase operations. All blocks are protected during power-up. The protection of the blocks

is non-volatile; after power-up the protection status of each block is restored to the state when power was last removed.

- Program Erase Enable input V_{PEN} , program or erase operations are not possible when the Program Erase Enable input V_{PEN} is low.
- Smart Protection, which allows protected blocks to be permanently locked. This feature is not described in the datasheet for security reasons. Please contact STMicroelectronics for further details.
- 128 bit Protection Register, divided into two 64 bit segments: the first contains a unique device number written by ST, the second is user programmable. The user programmable segment can be protected.

The Reset/Power-Down pin is used to apply a Hardware Reset to the memory and to set the device in power-down mode.

The device features an Auto Low Power mode. If the bus becomes inactive during Asynchronous Read operations, the device automatically enters Auto Low Power mode. In this mode the power consumption is reduced to the Auto Low Power supply current.

The STS signal is an open drain output that can be used to identify the Program/Erase Controller status. It can be configured in two modes: Ready/Busy mode where a static signal indicates the status of the P/E.C, and Status mode where a pulsing signal indicates the end of a Program or Block Erase operation. In Status mode it can be used as a system interrupt signal, useful for saving CPU time.

The memory is available in TSOP56 (14 x 20 mm) and TBGA64 (10 x 13mm, 1mm pitch) packages.

In addition to the standard version, the packages are also available in Lead-free version, in compliance with JEDEC Std J-STD-020B, the ST ECO-PACK 7191395 Specification, and the RoHS (Restriction of Hazardous Substances) directive.

All packages are compliant with Lead-free soldering processes.

Figure 2. Logic Diagram

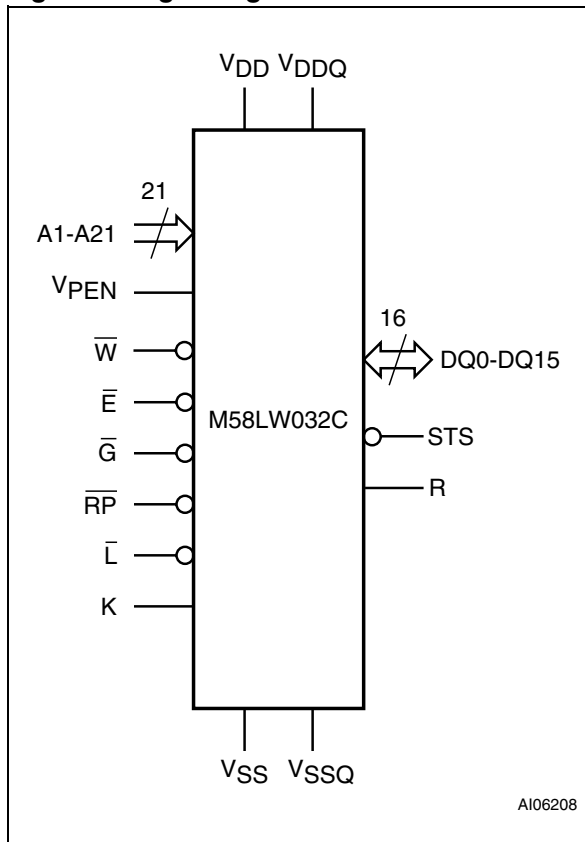
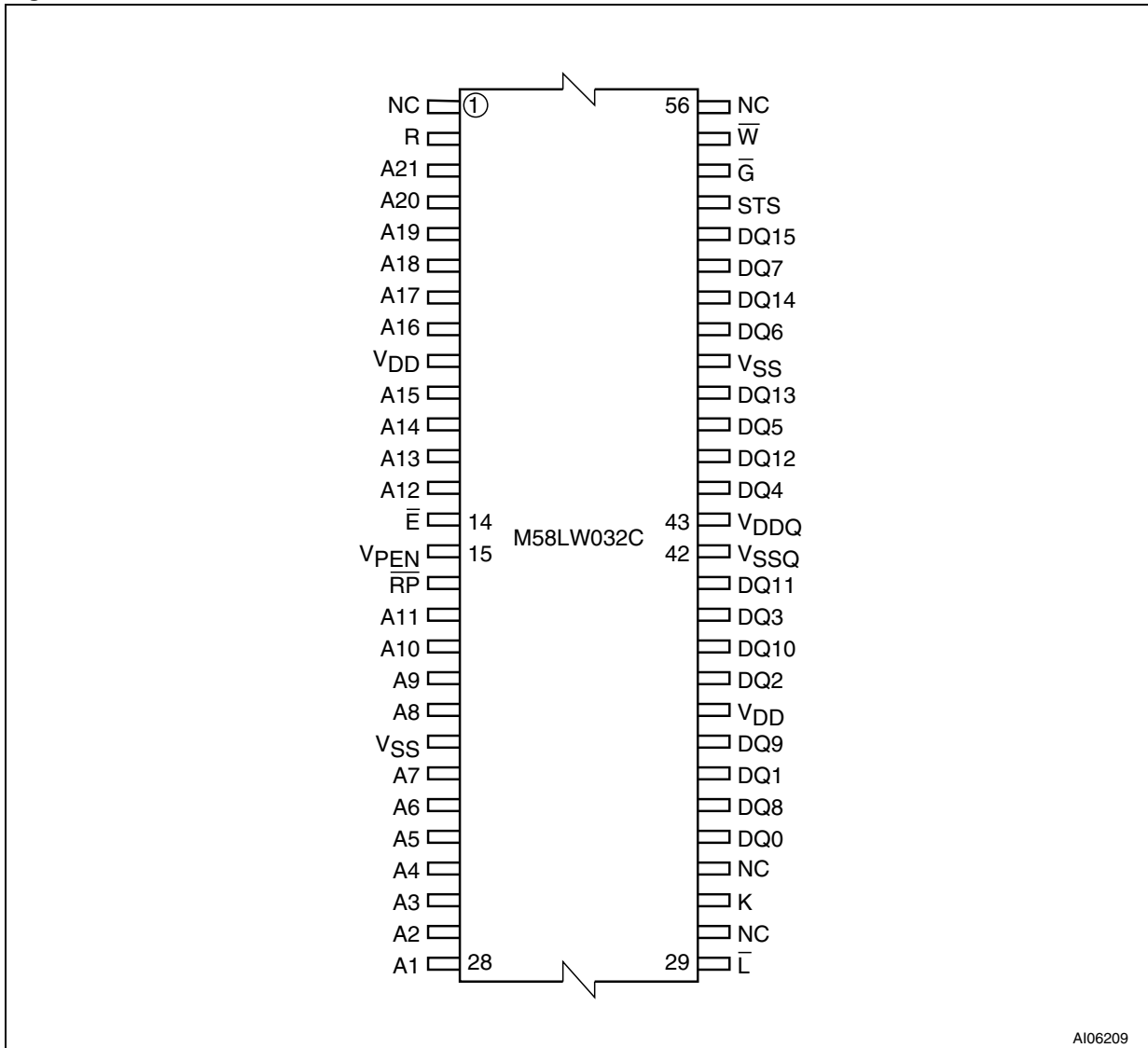


Table 1. Signal Names

A1-A21	Address inputs
DQ0-DQ15	Data Inputs/Outputs
\bar{E}	Chip Enable
\bar{G}	Output Enable
K	Clock
\bar{L}	Latch Enable
R	Valid Data Ready
STS	Status/(Ready/Busy)
\bar{RP}	Reset/Power-Down
VPEN	Program/Erase Enable
\bar{W}	Write Enable
VDD	Supply Voltage
VDDQ	Input/Output Supply Voltage
VSS	Ground
VSSQ	Input/Output Ground
NC	Not Connected Internally

Figure 3. TSOP56 Connections



AI06209

Figure 4. TBGA64 Connections (Top view through package)

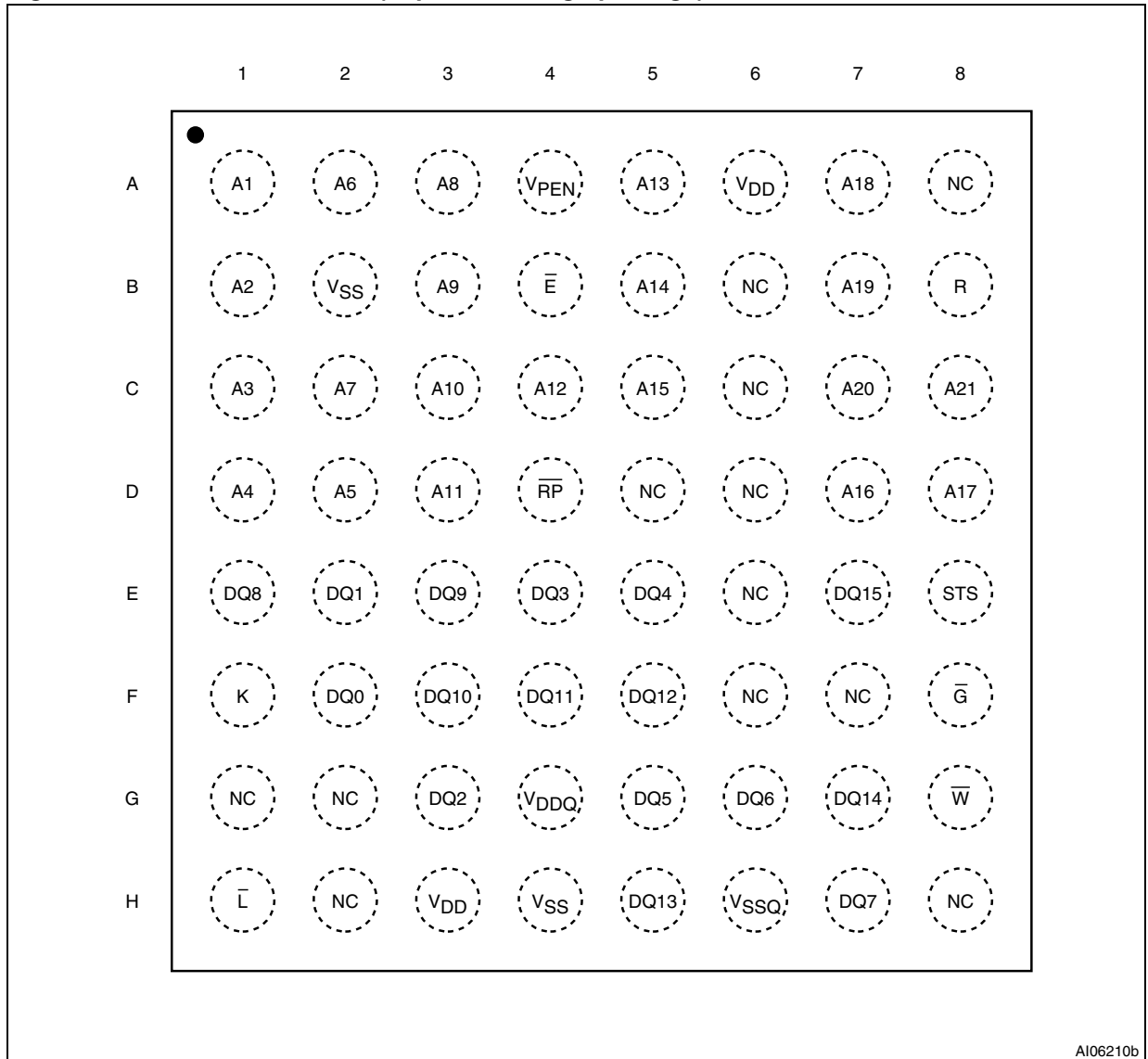
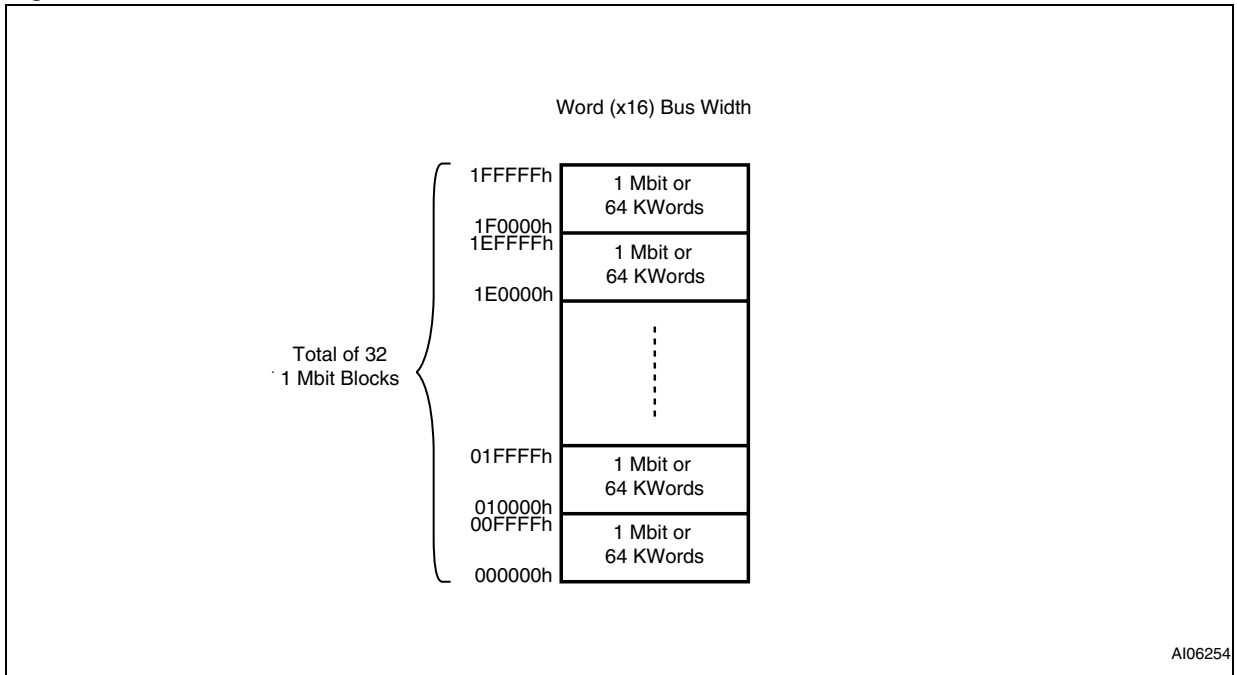


Figure 5. Block Addresses



Note: Also see [APPENDIX A., Table 25.](#) for a full listing of the Block Addresses.

SIGNAL DESCRIPTIONS

See [Figure 2., Logic Diagram](#), and [Table 1., Signal Names](#), for a brief overview of the signals connected to this device.

Address Inputs (A1-A21). The Address Inputs are used to select the cells to access in the memory array during Bus Read operations either to read or to program data to. During Bus Write operations they control the commands sent to the Command Interface of the internal state machine. Chip Enable and Latch Enable must be low when selecting the addresses.

The address inputs are latched on the rising edge of Chip Enable, Write Enable or Latch Enable, whichever occurs first in a Write operation. The address latch is transparent when Latch Enable is low, V_{IL} . The address is internally latched in an Erase or Program operation.

Data Inputs/Outputs (DQ0-DQ15). The Data Inputs/Outputs output the data stored at the selected address during a Bus Read operation, or are used to input the data during a program operation. During Bus Write operations they represent the commands sent to the Command Interface of the internal state machine. When used to input data or Write commands they are latched on the rising edge of Write Enable or Chip Enable, whichever occurs first.

When Chip Enable and Output Enable are both low, V_{IL} , the data bus outputs data from the memory array, the Electronic Signature, the Block Protection status, the CFI Information or the contents of the Status Register. The data bus is high impedance when the chip is deselected, Output Enable is high, V_{IH} , or the Reset/Power-Down signal is low, V_{IL} . When the Program/Erase Controller is active the Ready/Busy status is given on DQ7.

Chip Enable (\bar{E}). The Chip Enable, \bar{E} , input activates the memory control logic, input buffers, decoders and sense amplifiers. Chip Enable, \bar{E} , at V_{IH} deselected the memory and reduces the power consumption to the Standby level, I_{DD1} .

Output Enable (\bar{G}). The Output Enable, \bar{G} , gates the outputs through the data output buffers during a read operation. When Output Enable, \bar{G} , is at V_{IH} the outputs are high impedance. Output Enable, \bar{G} , can be used to inhibit the data output during a burst read operation.

Write Enable (\bar{W}). The Write Enable input, \bar{W} , controls writing to the Command Interface, Input Address and Data latches. Both addresses and data can be latched on the rising edge of Write Enable (also see Latch Enable, L).

Reset/Power-Down (RP). The Reset/Power-Down pin can be used to apply a Hardware Reset to the memory.

A Hardware Reset is achieved by holding Reset/Power-Down Low, V_{IL} , for at least t_{PLPH} . When Reset/Power-Down is Low, V_{IL} , the Status Register information is cleared and the power consumption is reduced to power-down level. The device is deselected and outputs are high impedance. If Reset/Power-Down goes low, V_{IL} , during a Block Erase, a Write to Buffer and Program or a Block Protect/Unprotect the operation is aborted and the data may be corrupted. In this case the Ready/Busy pin stays low, V_{IL} , for a maximum timing of $t_{PLPH} + t_{PHRH}$, until the completion of the Reset/Power-Down pulse.

After Reset/Power-Down goes High, V_{IH} , the memory will be ready for Bus Read and Bus Write operations after t_{PHQV} . Note that Ready/Busy does not fall during a reset, see Ready/Busy Output section.

In an application, it is recommended to associate Reset/Power-Down pin, RP, with the reset signal of the microprocessor. Otherwise, if a reset operation occurs while the memory is performing an Erase or Program operation, the memory may output the Status Register information instead of being initialized to the default Asynchronous Random Read.

Latch Enable (\bar{L}). The Bus Interface is configured to latch the Address Inputs on the rising edge of Latch Enable, L. In synchronous bus operations the address is latched on the active edge of the Clock when Latch Enable is Low, V_{IL} or on the rising of Latch Enable, whichever occurs first. Once latched, the addresses may change without affecting the address used by the memory. When Latch Enable is Low, V_{IL} , the latch is transparent.

Clock (K). The Clock, K, is used to synchronize the memory with the external bus during Synchronous Bus Read operations. The Clock can be configured to have an active rising or falling edge. Bus signals are latched on the active edge of the Clock during synchronous bus operations. In Synchronous Burst Read mode the address is latched on the first active clock edge when Latch Enable is low, V_{IL} , or on the rising edge of Latch Enable, whichever occurs first.

During asynchronous bus operations the Clock is not used.

Valid Data Ready (R). The Valid Data Ready output, R, is an open drain output that can be used to identify if the memory is ready to output data or not. The Valid Data Ready output is only active during Synchronous Burst Read operations when the Burst Length is set to Continuous. The Valid Data Ready output can be configured to be active on the clock edge of the invalid data read cycle or one cycle before. Valid Data Ready Low, V_{OL} , in-

icates that the data is not, or will not be valid. Valid Data Ready in a high-impedance state indicates that valid data is or will be available.

Unless Synchronous Burst Read has been selected, Valid Data Ready is high-impedance. It may be tied to other components with the same Valid Data Ready signal to create a unique System Ready signal.

The Valid Data Ready, R, output has an internal pull-up resistor of approximately 1 M Ω powered from V_{DDQ}, designers should use an external pull-up resistor of the correct value to meet the external timing requirements for Valid Data Ready rising. Refer to [Figure 19](#).

Status/(Ready/Busy) (STS). The STS signal is an open drain output that can be used to identify the Program/Erase Controller status. It can be configured in two modes:

- Ready/Busy - the pin is Low, V_{OL}, during Program and Erase operations and high impedance when the memory is ready for any Read, Program or Erase operation.
- Status - the pin gives a pulsing signal to indicate the end of a Program or Block Erase operation.

After power-up or reset the STS pin is configured in Ready/Busy mode. The pin can be configured for Status mode using the Configure STS command.

When the Program/Erase Controller is idle, or suspended, STS can float High through a pull-up resistor. The use of an open-drain output allows the STS pins from several memories to be connected to a single pull-up resistor (a Low will indicate that one, or more, of the memories is busy).

STS is not Low during a reset unless the reset was applied when the Program/Erase controller was active. Ready/Busy can rise before Reset/Power-Down rises.

Program/Erase Enable (V_{PEN}). The Program/Erase Enable input, V_{PEN}, is used to protect all blocks, preventing Program and Erase operations from affecting their data.

Program/Erase Enable must be kept High during all Program/Erase Controller operations, otherwise the operations is not guaranteed to succeed and data may become corrupt.

V_{DD} Supply Voltage. V_{DD} provides the power supply to the internal core of the memory device. It is the main power supply for all operations (Read, Program and Erase).

V_{DDQ} Supply Voltage. V_{DDQ} provides the power supply to the I/O pins and enables all Outputs to be powered independently from V_{DD}. V_{DDQ} can be tied to V_{DD} or can use a separate supply.

It is recommended to power-up and power-down V_{DD} and V_{DDQ} together to avoid any condition that would result in data corruption.

V_{SS} Ground. Ground, V_{SS}, is the reference for the core power supply. It must be connected to the system ground.

V_{SSQ} Ground. V_{SSQ} ground is the reference for the input/output circuitry driven by V_{DDQ}. V_{SSQ} must be connected to V_{SS}.

Note: Each device in a system should have V_{DD} and V_{DDQ} decoupled with a 0.1 μ F ceramic capacitor close to the pin (high frequency, inherently low inductance capacitors should be as close as possible to the package). See [Figure 10., AC Measurement Load Circuit.](#)

BUS OPERATIONS

There are six standard bus operations that control the device. These are Address Latch, Bus Read, Bus Write, Output Disable, Power-Down and Standby. See [Table 2., Bus Operations](#), for a summary.

Typically glitches of less than 5ns on Chip Enable or Write Enable are ignored by the memory and do not affect Bus Write operations.

Address Latch. Address latch operations input valid addresses.

A valid bus operation involves setting the desired address on the Address Inputs, setting Chip Enable and Latch Enable Low, V_{IL} and keeping Write Enable High, V_{IH} ; the address is latched on the rising edge of Address Latch.

Bus Read. Bus Read operations are used to output the contents of the Memory Array, the Electronic Signature, the Status Register, the Common Flash Interface and the Block Protection Status.

A valid bus operation involves setting the desired address on the Address Inputs, applying a Low signal, V_{IL} , to Chip Enable, Output Enable and Latch Enable and keeping Write Enable High, V_{IH} . The data read depends on the previous command written to the memory (see Command Interface section). See [Figures 11, 12, 13, 18 and 19 Read AC Waveforms](#), and [Tables 15, 16, 17 and 20 Read AC Characteristics](#), for details of when the output becomes valid.

Bus Write. Bus Write operations write Commands to the memory or latch addresses and input data to be programmed.

A valid Bus Write operation begins by setting the desired address on the Address Inputs and setting Latch Enable Low, V_{IL} . The Address Inputs are latched by the Command Interface on the rising edge of Chip Enable or Write Enable, whichever occurs first. The Data Inputs/Outputs are latched by the Command Interface on the rising edge of Chip Enable or Write Enable, whichever occurs first. Output Enable must remain High, V_{IH} , during the Bus Write operation.

See [Figures 14, 15, 16 and 17, Write AC Waveforms](#), and [Tables 18 and 19, Write AC Characteristics](#), for details of the timing requirements.

Output Disable. The Data Inputs/Outputs are high impedance when the Output Enable is at V_{IH} .

Power-Down. The memory is in Power-Down mode when Reset/Power-Down, \overline{RP} , is Low. The power consumption is reduced to the Power-Down level, I_{DD2} , and the outputs are high impedance, independent of Chip Enable, Output Enable or Write Enable.

Standby. Standby disables most of the internal circuitry, allowing a substantial reduction of the current consumption. The memory is in standby when Chip Enable is at V_{IH} . The power consumption is reduced to the standby level I_{DD1} and the outputs are set to high impedance, independently from the Output Enable or Write Enable inputs.

If Chip Enable switches to V_{IH} during a program or erase operation, the device enters Standby mode when finished.

Table 2. Bus Operations

Operation	\overline{E}	\overline{G}	\overline{W}	\overline{RP}	\overline{L}	A1-A21	DQ0-DQ15
Address Latch	V_{IL}	X	V_{IH}	V_{IH}	V_{IL}	Address	Data Output or Hi-Z ⁽²⁾
Bus Read	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	Address	Data Output
Bus Write	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	Address	Data Input
Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{IH}	X	X	High Z
Power-Down	X	X	X	V_{IL}	X	X	High Z
Standby	V_{IH}	X	X	V_{IH}	X	X	High Z

Note: 1. X = Don't Care V_{IL} or V_{IH} .

2. Depends on \overline{G}

READ MODES

Read operations can be performed in two different ways depending on the settings in the Configuration Register. If the clock signal is 'don't care' for the data output, the read operation is asynchronous; if the data output is synchronized with clock, the read operation is synchronous.

The read mode and format of the data output are determined by the Configuration Register. (See Configuration Register section for details).

On Power-up or after a Hardware Reset the memory defaults to Asynchronous Read mode.

Asynchronous Read Modes

In Asynchronous Read operations the clock signal is 'don't care'. The device outputs the data corresponding to the address latched, that is the memory array, Status Register, Common Flash Interface, Electronic Signature or Block Protection Status depending on the command issued. CR15 in the Configuration Register must be set to '1' for asynchronous operations.

During Asynchronous Read operations, if the bus is inactive for a time equivalent to t_{AVQV} , the device automatically enters Auto Low Power mode. In this mode the internal supply current is reduced to the Auto Low Power supply current, I_{DP5} . The Data Inputs/Outputs will still output data if a Bus Read operation is in progress.

Automatic Low Power is only available in Asynchronous Read modes.

Asynchronous Read operations can be performed in three different ways, Asynchronous Latch Controlled Read, Asynchronous Random Read and Asynchronous Page Read.

Asynchronous Latch Controlled Read.

In Asynchronous Latch Controlled Read operations read the address is latched in the memory before the value is output on the data bus, allowing the address to change during the cycle without affecting the address that the memory uses.

A valid bus operation involves setting the desired address on the Address Inputs, setting Chip Enable and Latch Enable Low, V_{IL} and keeping Write Enable High, V_{IH} ; the address is latched on the rising edge of Address Latch. Once latched, the Address Inputs can change. Set Output Enable Low, V_{IL} , to read the data on the Data Inputs/Outputs; see [Figure 12., Asynchronous Latch Controlled Bus Read AC Waveforms](#), and [Table 16., Asynchronous Latch Controlled Bus Read AC Characteristics](#), for details on when the output becomes valid.

See [Figure 12., Asynchronous Latch Controlled Bus Read AC Waveforms](#), and [Table 16., Asynchronous Latch Controlled Bus Read AC Characteristics](#), for details.

Asynchronous Random Read. As the Latch Enable input is transparent when set Low, V_{IL} , Asynchronous Random Read operations can be performed by holding Latch Enable Low, V_{IL} throughout the bus operation.

See [Figure 11., Asynchronous Bus Read AC Waveforms](#), and [Table 15., Asynchronous Bus Read AC Characteristics.](#), for details.

Asynchronous Page Read. In Asynchronous Page Read mode a Page of data is internally read and stored in a Page Buffer. Each memory page is 4 Words and has the same A3-A22, only A1 and A2 may change.

The first read operation within the Page has the normal access time (t_{AVQV}), subsequent reads within the same Page have much shorter access times (t_{AVQV1}). If the Page changes then the normal, longer timings apply again.

See [Figure 13., Asynchronous Page Read AC Waveforms](#), and [Table 17., Asynchronous Page Read AC Characteristics](#), for details.

Synchronous Read Modes

In Synchronous Read mode the data output is synchronized with the clock. CR15 in the Configuration Register must be set to '0' for synchronous operations.

Synchronous Burst Read. In Synchronous Burst Read mode the data is output in bursts synchronized with the clock. It is possible to perform burst reads across bank boundaries.

Synchronous Burst Read mode can only be used to read the memory array. For other read operations, such as Read Status Register, Read CFI, Read Electronic Signature and Block Protection Status, Single Synchronous Read or Asynchronous Read must be used.

In Synchronous Burst Read mode the flow of the data output depends on parameters that are configured in the Configuration Register.

A valid Synchronous Burst Read operation begins when the address is set on the Address Inputs, Write Enable is High, V_{IH} , and Chip Enable and Latch Enable are Low, V_{IL} , during the active edge of the Clock. The address is latched on the first active clock edge when Latch Enable is low, or on the rising edge of Latch Enable, whichever occurs first. The data becomes available for output after the X-latency specified in the Burst Control Register has expired. The output buffers are activated by setting Output Enable Low, V_{IL} . See [Figures 6 and 7](#) for examples of Synchronous Burst Read operations.

The number of Words to be output during a Synchronous Burst Read operation can be configured as 4 Words, 8 Words or Continuous (Burst Length

bits CR2-CR0). In Synchronous Continuous Burst Read mode one Burst Read operation can access the entire memory sequentially. If the starting address is not associated with a page (4 Word) boundary the Valid Data Ready, R, output goes Low, V_{IL} , to indicate that the data will not be ready in time and additional wait-states are required. The Valid Data Ready output timing (bit CR8) can be changed in the Configuration Register.

The order of the data output can be modified through the Burst Type bit in the Configuration

Register. The burst sequence can be sequential or interleaved.

See [Table 20.](#), [Synchronous Burst Read AC Characteristics](#), and [Figure 18](#) and [Figure 19](#), Synchronous Burst Read AC Waveform for details.

Single Synchronous Read. Single Synchronous Read operations are similar to Synchronous Burst Read operations except that only the first data output after the X latency is valid. Single Synchronous Reads are used to read the Status Register, CFI, Electronic Signature and Block Protection Status.

CONFIGURATION REGISTER

The Configuration Register is used to configure the type of bus access that the memory will perform. The Configuration Register bits are described in [Table 3](#). They specify the selection of the burst length, burst type, burst X and Y latencies and the Read operation. See [Figures 6 and 7](#) for examples of Synchronous Burst Read configurations.

The Configuration Register is set through the Command Interface and will retain its information until it is re-configured, the device is reset, or the device goes into Reset/Power-Down mode. The Configuration Register is read using the Read Electronic Signature Command at address 05h.

Read Select Bit (CR15). The Read Select bit, CR15, is used to switch between asynchronous and synchronous Bus Read operations. When the Read Select bit is set to '1', Bus Read operations are asynchronous; when the Read Select bit is set to '0', Bus Read operations are synchronous.

On reset or power-up the Read Select bit is set to '1' for asynchronous access.

X-Latency Bits (CR13-CR11). The X-Latency bits are used during Synchronous Bus Read operations to set the number of clock cycles between the address being latched and the first data becoming available. For correct operation the X-Latency bits can only assume the values in [Table 3](#), [Configuration Register](#).

Internal Clock Divider Bit (CR10). The Internal Clock Divider Bit is used to divide the internal clock by two. When CR10 is set to '1' the internal clock is divided by two, which effectively means that the X and Y-Latency values are multiplied by two, that is the number of clock cycles between the address being latched and the first data becoming available will be twice the value set in CR13-CR11, and the number of clock cycles between consecutive reads will be twice the value set in CR9. For example 8-1-1-1 will become 16-2-2-2. When CR10 is set to '0' the internal clock runs normally and the X and Y-Latency values are those set in CR13-CR11 and CR9.

Y-Latency Bit (CR9). The Y-Latency bit is used during Synchronous Bus Read operations to set

the number of clock cycles between consecutive reads. The Y-Latency value depends on both the X-Latency value and the setting in CR9.

When the Y-Latency is 1 the data changes each clock cycle; when the Y-Latency is 2 the data changes every second clock cycle. See [Table 3](#), [Configuration Register](#), for valid combinations of the Y-Latency, the X-Latency and the Clock frequency.

Valid Data Ready Bit (CR8). The Valid Data Ready bit controls the timing of the Valid Data Ready output pin, R. When the Valid Data Ready bit is '0' the Valid Data Ready output pin is driven Low for the active clock edge when invalid data is output on the bus. When the Valid Data Ready bit is '1' the Valid Data Ready output pin is driven Low one clock cycle prior to invalid data being output on the bus.

Burst Type Bit (CR7). The Burst Type bit is used to configure the sequence of addresses read as sequential or interleaved. When the Burst Type bit is '0' the memory outputs from interleaved addresses; when the Burst Type bit is '1' the memory outputs from sequential addresses. See [Table 4](#), [Burst Type Definition](#), for the sequence of addresses output from a given starting address in each mode.

Valid Clock Edge Bit (CR6). The Valid Clock Edge bit, CR6, is used to configure the active edge of the Clock, K, during Synchronous Burst Read operations. When the Valid Clock Edge bit is '0' the falling edge of the Clock is the active edge; when the Valid Clock Edge bit is '1' the rising edge of the Clock is active.

Burst Length Bit (CR2-CR0). The Burst Length bits set the maximum number of Words that can be output during a Synchronous Burst Read operation.

[Table 3](#), [Configuration Register](#), gives the valid combinations of the Burst Length bits that the memory accepts; [Table 4](#), [Burst Type Definition](#), give the sequence of addresses output from a given starting address for each length.

CR5 CR4 and CR3 are reserved for future use.

Table 3. Configuration Register

Address Bit	Mnemonic	Bit Name	Reset Value	Value	Description
16	CR15	Read Select	1	0	Synchronous Burst Read
				1	Asynchronous Bus Read (default at power-up)
15	CR14	Reserved			
14 to 12	CR13-CR11	X-Latency ⁽²⁾	XXX	001	Reserved
				010	X-Latency = 4, 4-1-1-1 (use only with Y-Latency = 1) ⁽¹⁾
				011	X-Latency = 5, 5-1-1-1, 5-2-2-2
				100	X-Latency = 6, 6-1-1-1, 6-2-2-2
				101	X-Latency = 7, 7-1-1-1, 7-2-2-2
				110	X-Latency = 8, 8-1-1-1, 8-2-2-2
11	CR10	Internal Clock Divider	X	0	X and Y-Latencies remains as set in CR13-CR11 and CR9
				1	Divides internal clock, X and Y-Latencies multiplied by 2
10	CR9	Y-Latency ⁽³⁾	X	0	Y-Latency = 1
				1	Y-Latency = 2
9	CR8	Valid Data Ready	X	0	R valid Low during valid Clock edge
				1	R valid Low one cycle before valid Clock edge
8	CR7	Burst Type	X	0	Interleaved
				1	Sequential
7	CR6	Valid Clock Edge	X	0	Falling Clock edge
				1	Rising Clock edge
6 to 4	CR5-CR3	Reserved			
3 to 1	CR2-CR0	Burst Length	XXX	001	4 Words
				010	8 Words
				111	Continuous

Note: 1. 4 - 2 - 2 - 2 (represents X-Y-Y-Y) is not allowed.

2. X latencies can be calculated as: $(t_{AVQV} - t_{LLKH} + t_{QVKH}) + t_{SYSTEM\ MARGIN} < (X - 1) t_k$. (X is an integer number from 4 to 8 and t_k is the clock period).

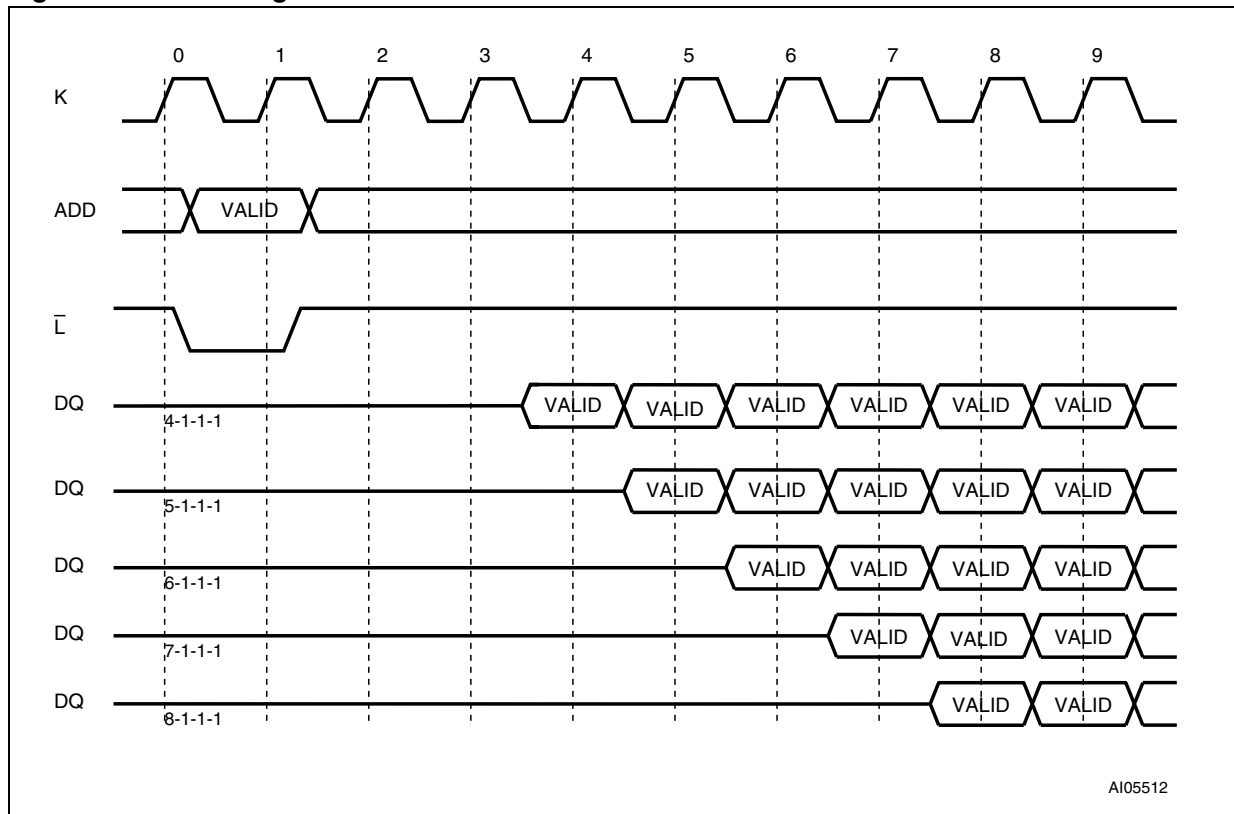
3. Y latencies can be calculated as: $t_{KHQV} + t_{SYSTEM\ MARGIN} + t_{QVKH} < Y t_k$.

4. $t_{SYSTEM\ MARGIN}$ is the time margin required for the calculation.

Table 4. Burst Type Definition

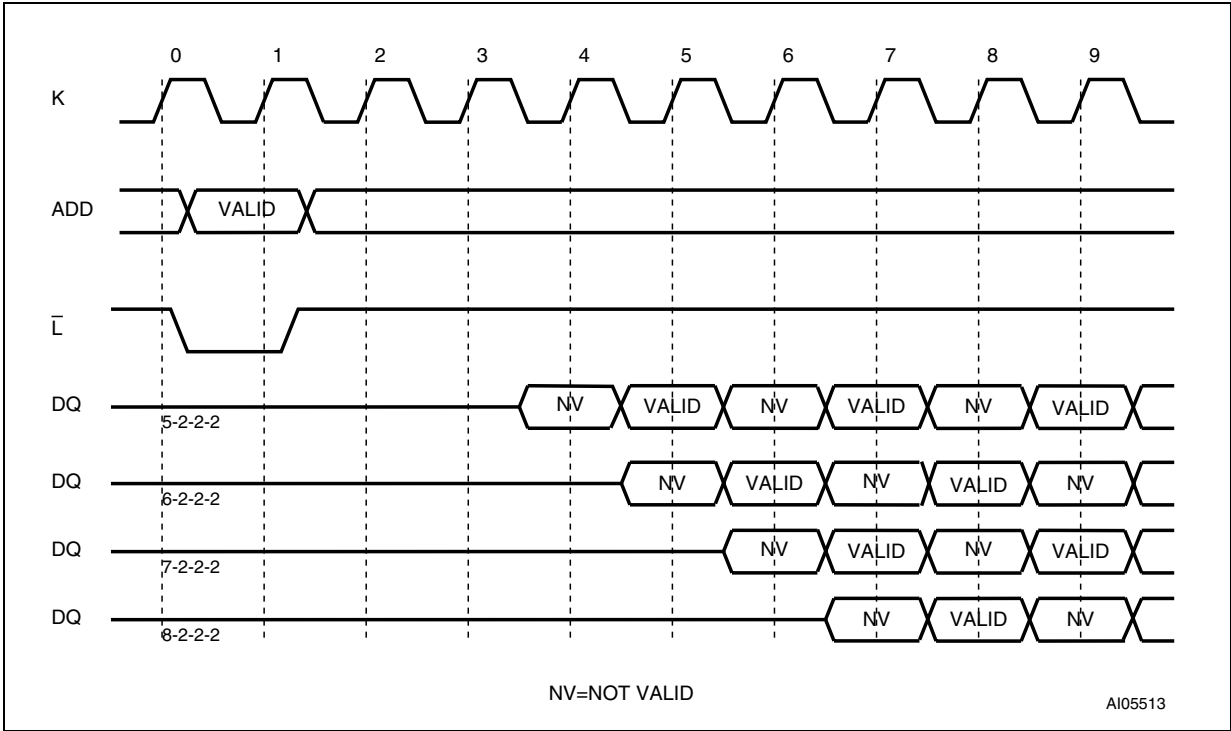
Starting Address	x4 Sequential	x4 Interleaved	x8 Sequential	x8 Interleaved	Continuous
0	0-1-2-3	0-1-2-3	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7-8-9-10..
1	1-2-3-0	1-0-3-2	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6	1-2-3-4-5-6-7-8-9-10-11..
2	2-3-0-1	2-3-0-1	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5	2-3-4-5-6-7-8-9-10-11-12..
3	3-0-1-2	3-2-1-0	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4	3-4-5-6-7-8-9-10-11-12-13..
4	-	-	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3	4-5-6-7-8-9-10-11-2-13-14..
5	-	-	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2	5-6-7-8-9-10-11-12-13-14..
6	-	-	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1	6-7-8-9-10-11-12-13-14-15..
7	-	-	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0	7-8-9-10-11-12-13-14-15-16..
8	-	-	-	-	8-9-10-11-12-13-14-15-16-17..

Figure 6. Burst Configuration X-1-1-1



AI05512

Figure 7. Burst Configuration X-2-2-2



COMMAND INTERFACE

All Bus Write operations to the memory are interpreted by the Command Interface. Commands consist of one or more sequential Bus Write operations. The Commands are summarized in [Table 5., Commands](#). Refer to [Table 5.](#) in conjunction with the text descriptions below.

After power-up or a Reset operation the memory enters Read mode.

Synchronous Read operations and Latch Controlled Bus Read operations can only be used to read the memory array. The Electronic Signature, CFI or Status Register will be read in asynchronous mode or single synchronous burst mode. Once the memory returns to Read Memory Array mode the bus will resume the setting in the Configuration Register automatically.

Read Memory Array Command. The Read Memory Array command returns the memory to Read mode. One Bus Write cycle is required to issue the Read Memory Array command and return the memory to Read mode. Once the command is issued the memory remains in Read mode until another command is issued. From Read mode Bus Read commands will access the memory array.

While the Program/Erase Controller is executing a Program, Erase, Block Protect, Blocks Unprotect or Protection Register Program operation the memory will not accept the Read Memory Array command until the operation completes.

Read Electronic Signature Command. The Read Electronic Signature command is used to read the Manufacturer Code, the Device Code, the Block Protection Status, the Configuration Register and the Protection Register. One Bus Write cycle is required to issue the Read Electronic Signature command. Once the command is issued subsequent Bus Read operations read the Manufacturer Code, the Device Code, the Block Protection Status, the Configuration Register or the Protection Register until another command is issued. Refer to [Table 7., Read Electronic Signature](#), [Table 8., Read Protection Register](#), and [Figure 8., Protection Register Memory Map](#), for information on the addresses.

Read Query Command. The Read Query Command is used to read data from the Common Flash Interface (CFI) Memory Area. One Bus Write cycle is required to issue the Read Query Command. Once the command is issued subsequent Bus Read operations read from the Common Flash Interface Memory Area. See [APPENDIX B.](#), Tables [26](#), [27](#), [28](#), [29](#), [30](#) and [31](#) for details on the information contained in the Common Flash Interface (CFI) memory area.

Read Status Register Command. The Read Status Register command is used to read the Status

Register. One Bus Write cycle is required to issue the Read Status Register command. Once the command is issued subsequent Bus Read operations read the Status Register until another command is issued.

The Status Register information is present on the output data bus (DQ1-DQ7) when both Chip Enable and Output Enable are low, V_{IL} .

See the section on the Status Register and [Table 10.](#) for details on the definitions of the Status Register bits

Clear Status Register Command. The Clear Status Register command can be used to reset bits SR1, SR3, SR4 and SR5 in the Status Register to '0'. One Bus Write is required to issue the Clear Status Register command.

The bits in the Status Register are sticky and do not automatically return to '0' when a new Write to Buffer and Program, Erase, Block Protect, Block Unprotect or Protection Register Program command is issued. If any error occurs then it is essential to clear any error bits in the Status Register by issuing the Clear Status Register command before attempting a new Program, Erase or Resume command.

Block Erase Command. The Block Erase command can be used to erase a block. It sets all of the bits in the block to '1'. All previous data in the block is lost. If the block is protected then the Erase operation will abort, the data in the block will not be changed and the Status Register will output the error.

Two Bus Write operations are required to issue the command; the second Bus Write cycle latches the block address in the internal state machine and starts the Program/Erase Controller. Once the command is issued subsequent Bus Read operations read the Status Register. See the section on the Status Register for details on the definitions of the Status Register bits.

During the Erase operation the memory will only accept the Read Status Register command and the Program/Erase Suspend command. All other commands will be ignored. Typical Erase times are given in [Table 9.](#)

See [APPENDIX C.](#), [Figure 25., Erase Flowchart and Pseudo Code](#), for a suggested flowchart on using the Block Erase command.

Word Program Command. The Word Program command is used to program a single word in the memory array. Two Bus Write operations are required to issue the command; the first write cycle sets up the Word Program command, the second write cycle latches the address and data to be pro-

grammed in the internal state machine and starts the Program/Erase Controller.

If the block being programmed is protected an error will be set in the Status Register and the operation will abort without affecting the data in the memory array. The block must be unprotected using the Blocks Unprotect command.

Write to Buffer and Program Command. The Write to Buffer and Program command is used to program the memory array.

Up to 16 Words can be loaded into the Write Buffer and programmed into the memory. Each Write Buffer has the same A5-A21 addresses.

Four successive steps are required to issue the command.

1. One Bus Write operation is required to set up the Write to Buffer and Program Command. Issue the set up command with the selected memory Block Address where the program operation should occur (any address in the block where the values will be programmed can be used). Any Bus Read operations will start to output the Status Register after the 1st cycle.
2. Use one Bus Write operation to write the same block address along with the value N on the Data Inputs/Output, where N+1 is the number of Words to be programmed.
3. Use N+1 Bus Write operations to load the address and data for each Word into the Write Buffer. See the constraints on the address combinations listed below. The addresses must have the same A5-A21.
4. Finally, use one Bus Write operation to issue the final cycle to confirm the command and start the Program operation.

Invalid address combinations or failing to follow the correct sequence of Bus Write cycles will set an error in the Status Register and abort the operation without affecting the data in the memory array. The Status Register should be cleared before re-issuing the command.

If the block being programmed is protected an error will be set in the Status Register and the operation will abort without affecting the data in the memory array. The block must be unprotected using the Blocks Unprotect command.

See [APPENDIX C., Figure 23., Write to Buffer and Program Flowchart and Pseudo Code](#), for a suggested flowchart on using the Write to Buffer and Program command.

Program/Erase Suspend Command. The Program/Erase Suspend command is used to pause a Word Program, Write to Buffer and Program or Erase operation. The command will only be accepted during a Program or an Erase operation. It

can be issued at any time during an Erase operation but will only be accepted during a Word Program or Write to Buffer and Program command if the Program/Erase Controller is running.

One Bus Write cycle is required to issue the Program/Erase Suspend command and pause the Program/Erase Controller. Once the command is issued it is necessary to poll the Program/Erase Controller Status bit (SR7) to find out when the Program/Erase Controller has paused; no other commands will be accepted until the Program/Erase Controller has paused. After the Program/Erase Controller has paused, the memory will continue to output the Status Register until another command is issued.

During the polling period between issuing the Program/Erase Suspend command and the Program/Erase Controller pausing it is possible for the operation to complete. Once the Program/Erase Controller Status bit (SR7) indicates that the Program/Erase Controller is no longer active, the Program Suspend Status bit (SR2) or the Erase Suspend Status bit (SR6) can be used to determine if the operation has completed or is suspended. For timing on the delay between issuing the Program/Erase Suspend command and the Program/Erase Controller pausing see [Table 9](#).

During Program/Erase Suspend the Read Memory Array, Read Status Register, Read Electronic Signature, Read Query and Program/Erase Resume commands will be accepted by the Command Interface. Additionally, if the suspended operation was Erase then the Write to Buffer and Program, and the Program Suspend commands will also be accepted. When a program operation is completed inside a Block Erase Suspend the Read Memory Array command must be issued to reset the device in Read mode, then the Erase Resume command can be issued to complete the whole sequence. Only the blocks not being erased may be read or programmed correctly.

See [APPENDIX C., Figure 24., Program Suspend & Resume Flowchart and Pseudo Code](#), and [Figure 26., Erase Suspend & Resume Flowchart and Pseudo Code](#), for suggested flowcharts on using the Program/Erase Suspend command.

Program/Erase Resume Command. The Program/Erase Resume command can be used to restart the Program/Erase Controller after a Program/Erase Suspend operation has paused it. One Bus Write cycle is required to issue the Program/Erase Resume command. Once the command is issued subsequent Bus Read operations read the Status Register.

Set Configuration Register Command. The Set Configuration Register command is used to write a new value to the Burst Configuration Control Register which defines the burst length, type,

X and Y latencies, Synchronous/Asynchronous Read mode and the valid Clock edge configuration.

Two Bus Write cycles are required to issue the Set Configuration Register command. Once the command is issued the memory returns to Read mode as if a Read Memory Array command had been issued.

The value for the Configuration Register is presented on A1-A16. CR0 is on A1, CR1 on A2, etc.; the other address bits are ignored.

Block Protect Command. The Block Protect command is used to protect a block and prevent Program or Erase operations from changing the data in it. Two Bus Write cycles are required to issue the Block Protect command; the second Bus Write cycle latches the block address in the internal state machine and starts the Program/Erase Controller. Once the command is issued subsequent Bus Read operations read the Status Register. See the section on the Status Register for details on the definitions of the Status Register bits.

During the Block Protect operation the memory will only accept the Read Status Register command. All other commands will be ignored. Typical Block Protection times are given in [Table 9](#).

The Block Protection bits are non-volatile, once set they remain set through reset and power-down/power-up. They are cleared by a Blocks Unprotect command.

See [APPENDIX C., Figure 27., Block Protect Flowchart and Pseudo Code](#), for a suggested flowchart on using the Block Protect command.

Blocks Unprotect Command. The Blocks Unprotect command is used to unprotect all of the blocks. Two Bus Write cycles are required to issue the Blocks Unprotect command; the second Bus Write cycle starts the Program/Erase Controller. Once the command is issued subsequent Bus Read operations read the Status Register. See the section on the Status Register for details on the definitions of the Status Register bits.

During the Block Unprotect operation the memory will only accept the Read Status Register command. All other commands will be ignored. Typical Block Protection times are given in [Table 9](#).

See [APPENDIX C., Figure 28., Blocks Unprotect Flowchart and Pseudo Code](#), for a suggested flowchart on using the Block Unprotect command.

Protection Register Program Command. The Protection Register Program command is used to Program the 64 bit user segment of the Protection Register. The segment is programmed 16 bits at a

time. Two write cycles are required to issue the Protection Register Program command.

- The first bus cycle sets up the Protection Register Program command.
- The second latches the Address and the Data to be written to the Protection Register and starts the Program/Erase Controller.

Read operations output the Status Register content after the programming has started.

The user-programmable segment can be locked by programming bit 1 of the Protection Register Lock location to '0' (see [Table 8](#)). Bit 0 of the Protection Register Lock location locks the factory programmed segment and is programmed to '0' in the factory. The locking of the Protection Register is not reversible, once the lock bits are programmed no further changes can be made to the values stored in the Protection Register, see [Figure 8., Protection Register Memory Map](#). Attempting to program a previously protected Protection Register will result in a Status Register error.

The Protection Register Program cannot be suspended. See [APPENDIX C., Figure 29., Protection Register Program Flowchart and Pseudo Code](#), for the flowchart for using the Protection Register Program command.

Configure STS Command.

The Configure STS command is used to configure the Status/(Ready/Busy) pin. After power-up or reset the STS pin is configured in Ready/Busy mode. The pin can be configured in Status mode using the Configure STS command (refer to Status/(Ready/Busy) section for more details).

Two write cycles are required to issue the Configure STS command.

- The first bus cycle sets up the Configure STS command.
- The second specifies one of the four possible configurations (refer to [Table 6., Configuration Codes](#)):
 - Ready/Busy mode
 - Pulse on Erase complete mode
 - Pulse on Program complete mode
 - Pulse on Erase or Program complete mode

The device will not accept the Configure STS command while the Program/Erase controller is busy or during Program/Erase Suspend. When STS pin is pulsing it remains Low for a typical time of 250ns. Any invalid Configuration Code will set an error in the Status Register.

Table 5. Commands

Command	Cycles	Bus Operations											
		1st Cycle			2nd Cycle			Subsequent			Final		
		Op.	Addr.	Data	Op.	Addr.	Data	Op.	Addr.	Data	Op.	Addr.	Data
Read Memory Array	≥ 2	Write	X	FFh	Read	RA	RD						
Read Electronic Signature	≥ 2	Write	X	90h	Read	IDA ⁽³⁾	IDD ⁽³⁾						
Read Status Register	2	Write	X	70h	Read	X	SRD						
Read Query	≥ 2	Write	X	98h	Read	QA ⁽⁴⁾	QD ⁽⁴⁾						
Clear Status Register	1	Write	X	50h									
Block Erase	2	Write	X	20h	Write	BA	D0						
Word Program	2	Write	X	40h 10h	Write	PA	PD						
Write to Buffer and Program	4 + N	Write	BA	E8h	Write	BA	N	Write	PA	PD	Write	X	D0h
Program/Erase Suspend	1	Write	X	B0h									
Program/Erase Resume	1	Write	X	D0h									
Set Configuration Register	2	Write	X	60h	Write	BCR	03h						
Block Protect	2	Write	X	60h	Write	BA	01h						
Blocks Unprotect	2	Write	X	60h	Write	X	D0h						
Protection Register Program	2	Write	X	C0h	Write	PRA	PRD						
Configure STS command	2	Write	X	B8h	Write	X	CC						

Note: 1. X Don't Care; RA Read Address, RD Read Data, IDA Identifier Address, IDD Identifier Data, SRD Status Register Data, PA Program Address; PD Program Data, QA Query Address, QD Query Data, BA Any address in the Block, BCR Configuration Register value, CC Configuration Code.

2. Base Address, refer to [Figure 8.](#) and [Table 8.](#) for more information.

3. For Identifier addresses and data refer to [Table 7.](#), [Read Electronic Signature.](#)

4. For Query Address and Data refer to [APPENDIX B., COMMON FLASH INTERFACE - CFI.](#)

Table 6. Configuration Codes

Configuration Code	DQ1	DQ2	Mode	STS Pin	Description
00h	0	0	Ready/Busy	V _{OL} during P/E operations Hi-Z when the memory is ready	The STS pin is Low during Program and Erase operations and high impedance when the memory is ready for any Read, Program or Erase operation.
01h	0	1	Pulse on Erase complete	Pulse Low then High when operation completed ⁽²⁾	Supplies a system interrupt pulse at the end of a Block Erase operation.
02h	1	0	Pulse on Program complete		Supplies a system interrupt pulse at the end of a Program operation.
03h	1	1	Pulse on Erase or Program complete		Supplies a system interrupt pulse at the end of a Block Erase or Program operation.

Note: 1. DQ2-DQ7 are reserved

2. When STS pin is pulsing it remains Low for a typical time of 250ns.

Table 7. Read Electronic Signature

Code	Address (A21-A1)	Data (DQ15-DQ0)
Manufacturer Code	000000h	0020h
Device Code	000001h	8822h
Block Protection Status	SBA+02h	0000h (Block Unprotected) 0001h (Block Protected)
Configuration Register	000005h	BCR
Protection Register	000080h ⁽²⁾	PRD

Note: 1. SBA is the Start Base Address of each block, BCR is Configuration Register data, PRD is Protection Register Data.
 2. Base Address, refer to [Figure 8.](#) and [Table 8.](#) for more information.

Table 8. Read Protection Register

Word	Use	A8	A7	A6	A5	A4	A3	A2	A1
Lock	Factory, User	1	0	0	0	0	0	0	0
0	Factory (Unique ID)	1	0	0	0	0	0	0	1
1	Factory (Unique ID)	1	0	0	0	0	0	1	0
2	Factory (Unique ID)	1	0	0	0	0	0	1	1
3	Factory (Unique ID)	1	0	0	0	0	1	0	0
4	User	1	0	0	0	0	1	0	1
5	User	1	0	0	0	0	1	1	0
6	User	1	0	0	0	0	1	1	1
7	User	1	0	0	0	1	0	0	0

Figure 8. Protection Register Memory Map

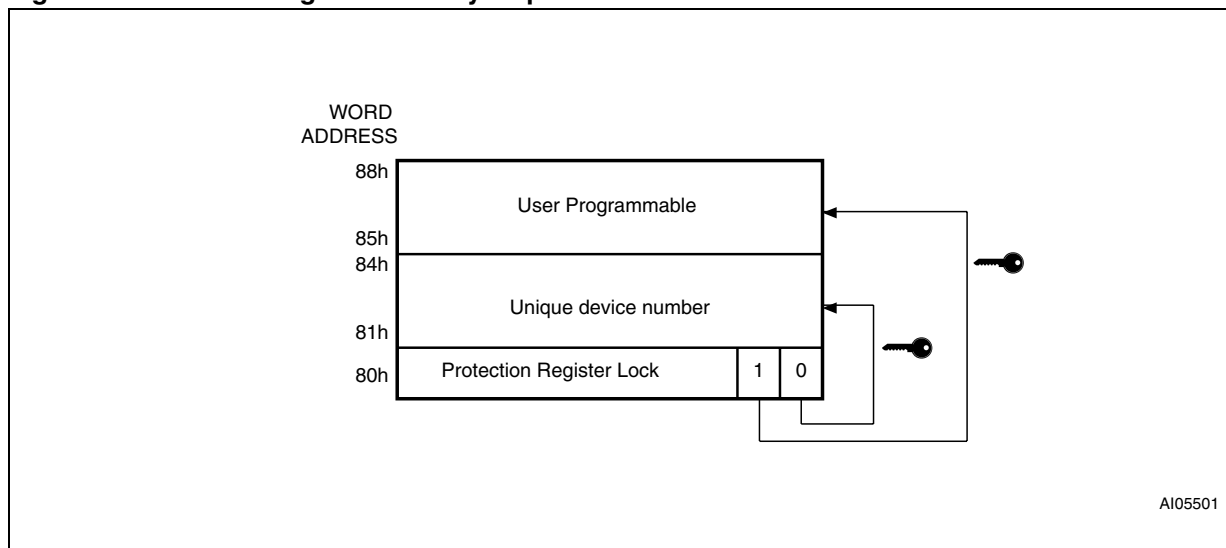


Table 9. Program, Erase Times and Program Erase Endurance Cycles

Parameters	M58LW032C			Unit
	Min	Typ ^(1,2)	Max ⁽²⁾	
Block (1Mb) Erase		1.2	4.8 ⁽⁴⁾	s
Chip Program (Write to Buffer)		24	72 ⁽⁴⁾	s
Chip Erase Time		37	110 ⁽⁴⁾	s
Program Write Buffer		192 ⁽³⁾	576 ⁽⁴⁾	μs
Word/Byte Program Time (Word/Byte Program command)		16	48 ⁽⁴⁾	μs
Program Suspend Latency Time		1	20 ⁽⁵⁾	μs
Erase Suspend Latency Time		1	25 ⁽⁵⁾	μs
Block Protect Time		18	30 ⁽⁵⁾	μs
Blocks Unprotect Time		0.75	1.2 ⁽⁵⁾	s
Program/Erase Cycles (per block)	100,000			cycles
Data Retention	20			years

Note: 1. Typical values measured at room temperature and nominal voltages.

2. Sampled, but not 100% tested.

3. Effective byte programming time 6μs, effective word programming time 12μs.

4. Maximum value measured at worst case conditions for both temperature and V_{DD} after 100,000 program/erase cycles.

5. Maximum value measured at worst case conditions for both temperature and V_{DD}.