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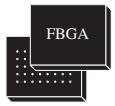
M58WR016KU M58WR016KL M58WR032KU M58WR032KL M58WR064KU M58WR064KL

16-, 32- and 64-Mbit (x 16, mux I/O, multiple bank, burst) 1.8 V supply flash memories

Features

- Supply voltage
  - V_{DD} = 1.7 V to 2 V for program, erase and read
  - V_{DDQ} = 1.7 V to 2 V for I/O buffers
  - V_{PP} = 9 V for fast program
- Multiplexed address/data
- Synchronous/asynchronous read
  - Synchronous burst read mode: 66 MHz
  - Random access: 70 ns
- Synchronous burst read suspend
- Programming time
  - 10 µs by word typical for factory program
  - Double/quadruple word program option
  - Enhanced factory program options
- Memory blocks
  - Multiple bank memory array: 4-Mbit banks
  - Parameter blocks (top or bottom location)
- Dual operations
  - Program erase in one bank while read in others
  - No delay between read and write operations
- Block locking
  - All blocks locked at power up
  - Any combination of blocks can be locked
  - $\overline{WP}$ for block lock-down
- Security
  - 128-bit user programmable OTP cells
  - 64-bit unique device number
- Common flash interface (CFI)
- 100,000 program/erase cycles per block



VFBGA44 (ZA)
7.5 x 5 mm

- Electronic signature
  - Manufacturer code: 20h
  - Top device code,
    M58WR016KU: 8823h
    M58WR032KU: 8828h
    M58WR064KU: 88C0h
  - Bottom device code,
    M58WR016KL: 8824h
    M58WR032KL: 8829h
    M58WR064KL: 88C1h
- RoHS compliant packages available

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1 Description

The M58WR016KU/L, M58WR032KU/L and M58WR064KU/L are 16-Mbit (1 Mbit x 16), 32- Mbit (2 Mbits x 16) and 64-Mbit (4 Mbits x 16) non-volatile flash memories, respectively. In the rest of the document, they will be referred to as M58WRxxxKU/L unless otherwise specified.

The M58WRxxxKU/L may be erased electrically at block level and programmed in-system on a word-by-word basis using a 1.7 V to 2 V V_{DD} supply for the circuitry and a 1.7 V to 2 V V_{DDQ} supply for the input/output pins. An optional 9 V V_{PP} power supply is provided to speed up customer programming.

The first 16 address lines are multiplexed with the data input/output signals on the multiplexed address/data bus ADQ0-ADQ15. The remaining address lines, A16-Amax, are the most significant bit addresses.

The device features an asymmetrical block architecture:

- the M58WR016KU/L have an array of 39 blocks, and are divided into 4-Mbit banks. There are 3 banks each containing 8 main blocks of 32 Kwords, and one parameter bank containing 8 parameter blocks of 4 Kwords and 7 main blocks of 32 Kwords.
- the M58WR032KU/L have an array of 71 blocks, and are divided into 4-Mbit banks. There are 7 banks each containing 8 main blocks of 32 Kwords, and one parameter bank containing 8 parameter blocks of 4 Kwords and 7 main blocks of 32 Kwords.
- the M58WR064KU/L have an array of 135 blocks, and are divided into 4-Mbit banks. There are 15 banks each containing 8 main blocks of 32 Kwords, and one parameter bank containing 8 parameter blocks of 4 Kwords and 7 main blocks of 32 Kwords.

The multiple bank architecture allows dual operations; while programming or erasing in one bank, read operations are possible in other banks. Only one bank at a time is allowed to be in program or erase mode. It is possible to perform burst reads that cross bank boundaries. The bank architectures are summarized in Tables *2*, *3* and *4*, and the memory maps are shown in Figures *3*, *4* and *5*. The parameter blocks are located at the top of the memory address space for the M58WR016KU, M58WR032KU and M58WR064KU, and at the bottom for the M58WR016KL, M58WR032KL and M58WR064KL.

Each block can be erased separately. Erase can be suspended to perform program in any other block, and then resumed. Program can be suspended to read data in any other block and then resumed. Each block can be programmed and erased over 100,000 cycles using the supply voltage V_{DD}. There are two enhanced factory programming commands available to speed up programming.

Program and erase commands are written to the command interface of the memory. An internal program/erase controller takes care of the timings necessary for program and erase operations. The end of a program or erase operation can be detected and any error conditions identified in the status register. The command set required to control the memory is consistent with JEDEC standards.

The device supports synchronous burst read and asynchronous read from all blocks of the memory array; at power-up the device is configured for asynchronous read. In synchronous burst mode, data is output on each clock cycle at frequencies of up to 66 MHz. The synchronous burst read operation can be suspended and resumed.

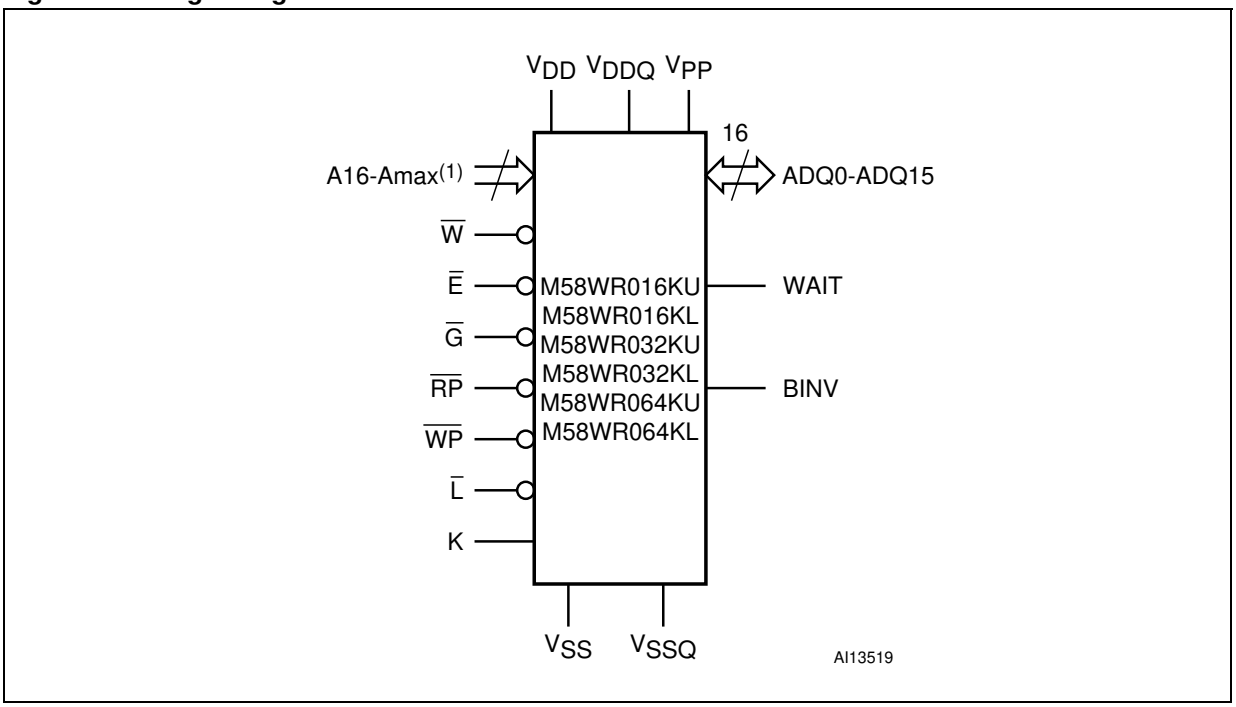
The device features an automatic standby mode. When the bus is inactive during asynchronous read operations, the device automatically switches to automatic standby mode. In this condition the power consumption is reduced to the standby value I_{DD4} and the outputs are still driven.

The M58WRxxxKU/L features an instant, individual block locking scheme that allows any block to be locked or unlocked with no latency, enabling instant code and data protection. All blocks have three levels of protection. They can be locked and locked down individually, preventing any accidental programming or erasure. There is additional hardware protection against program and erase. When $V_{PP} \leq V_{PPLK}$ all blocks are protected against program or erase. All blocks are locked at power- up.

The device includes a protection register to increase the protection of a system's design. The protection register is divided into two segments: a 64 bit segment containing a unique device number written by Numonyx, and a 128 bit segment one-time-programmable (OTP) by the user. The user programmable segment can be permanently protected. *Figure 6: Protection register memory map* shows the protection register memory map.

The memory is available in a VFBGA44 7.5 x 5 mm, 10 x 4 active ball array, 0.5 mm pitch package, and is supplied with all the bits erased (set to '1').

Figure 1. Logic diagram



1. Amax is equal to A19 in the M58WR016KU/L, to A20 in the M58WR032KU/L, and to A21 in the M58WR064KU/L.

Table 1. Signal names

Name	Description	Direction
A16-Amax(1)	Address inputs	Inputs
ADQ0-ADQ15	Data input/outputs or address inputs, command inputs	I/O
$\overline{E}$	Chip Enable	Input
$\overline{G}$	Output Enable	Input
$\overline{W}$	Write Enable	Input
$\overline{RP}$	Reset/Power-down	Input
$\overline{WP}$	Write Protect	Input
K	Clock	Input
$\overline{L}$	Latch Enable	Input
WAIT	Wait	Output
BINV	Bus invert	I/O
V_{DD}	Supply voltage	
V_{DDQ}	Supply voltage for input/output buffers	
V_{PP}	Optional supply voltage for fast program and erase	
V_{SS}	Ground	
V_{SSQ}	Ground input/output supply	
NC	Not connected internally	

1. Amax is equal to A19 in the M58WR016KU/L, to A20 in the M58WR032KU/L, and to A21 in the M58WR064KU/L.

Figure 2. VFBGA44 connections (top view through package)

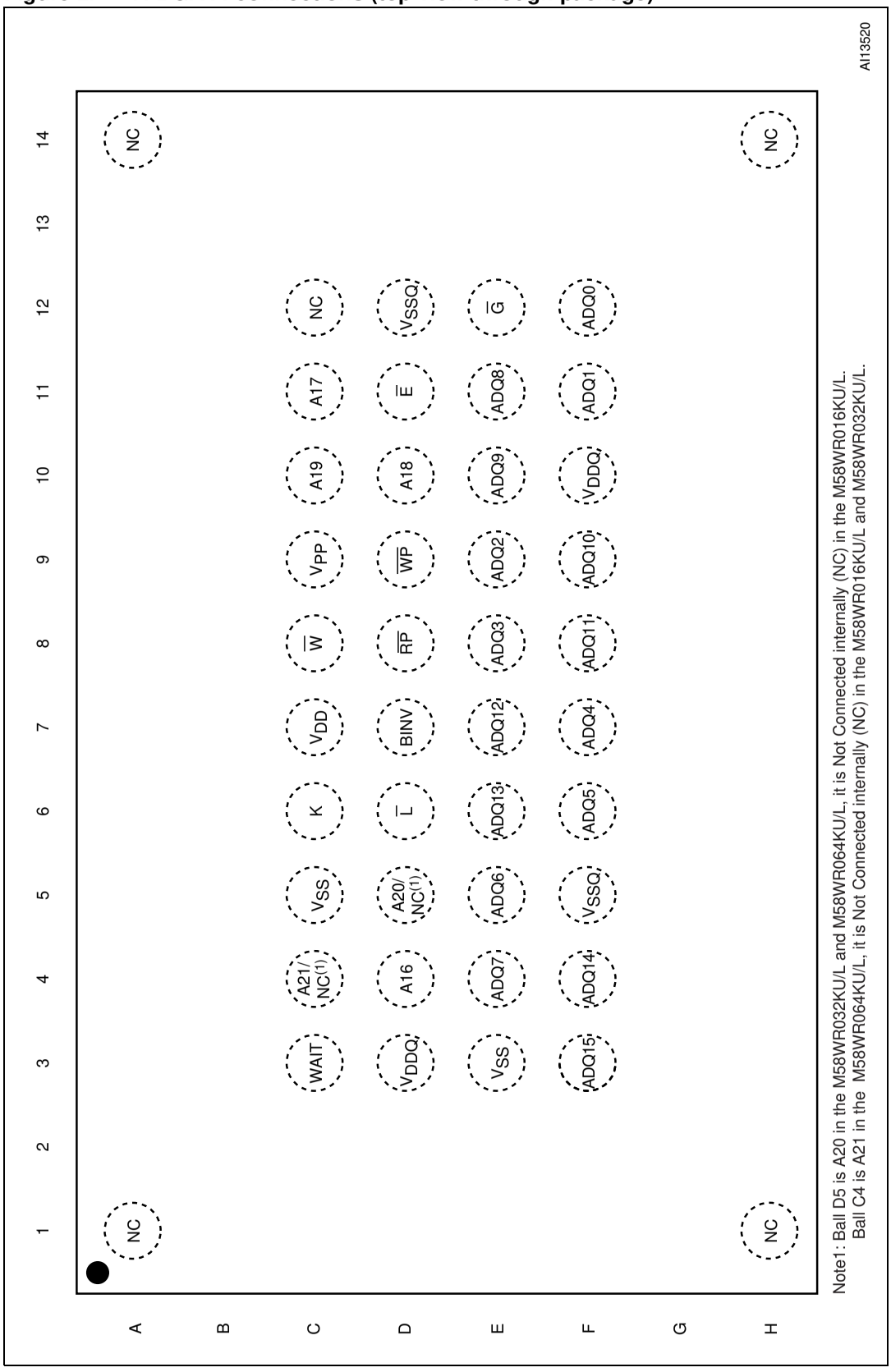


Table 2. M58WR016KU/L bank architecture

Number	Bank size	Parameter blocks	Main Blocks
Parameter bank	4 Mbits	8 blocks of 4 Kwords	7 blocks of 32 Kwords
Bank 1	4 Mbits	-	8 blocks of 32 Kwords
Bank 2	4 Mbits	-	8 blocks of 32 Kwords
Bank 3	4 Mbits	-	8 blocks of 32 Kwords

Table 3. M58WR032KU/L bank architecture

Number	Bank size	Parameter blocks	Main blocks
Parameter bank	4 Mbits	8 blocks of 4 Kwords	7 blocks of 32 Kwords
Bank 1	4 Mbits	-	8 blocks of 32 Kwords
Bank 2	4 Mbits	-	8 blocks of 32 Kwords
Bank 3	4 Mbits	-	8 blocks of 32 Kwords
⋮	⋮	⋮	⋮
Bank 6	4 Mbits	-	8 blocks of 32 Kwords
Bank 7	4 Mbits	-	8 blocks of 32 Kwords

Table 4. M58WR064KU/L bank architecture

Number	Bank size	Parameter blocks	Main blocks
Parameter bank	4 Mbits	8 blocks of 4 Kwords	7 blocks of 32 Kwords
Bank 1	4 Mbits	-	8 blocks of 32 Kwords
Bank 2	4 Mbits	-	8 blocks of 32 Kwords
Bank 3	4 Mbits	-	8 blocks of 32 Kwords
⋮	⋮	⋮	⋮
Bank 14	4 Mbits	-	8 blocks of 32 Kwords
Bank 15	4 Mbits	-	8 blocks of 32 Kwords

Figure 3. M58WR016KU/L memory map

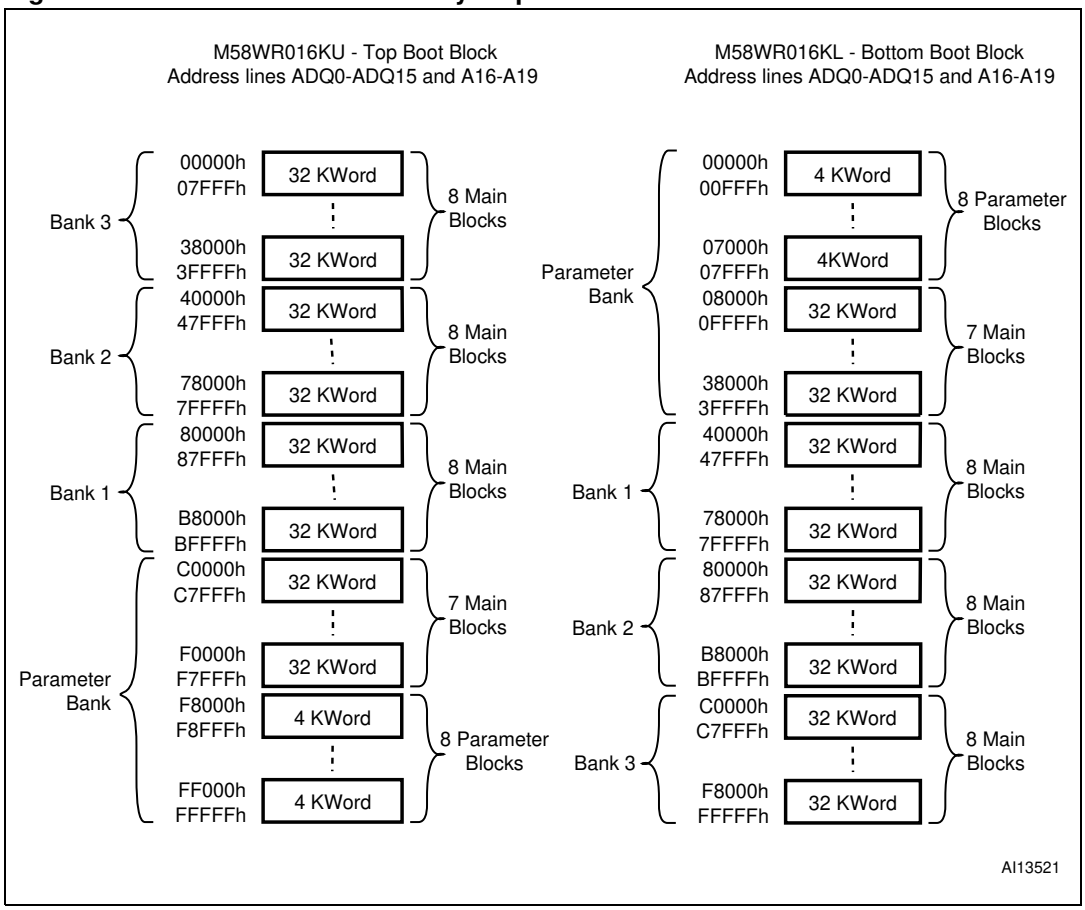


Figure 4. M58WR032KU/L memory map

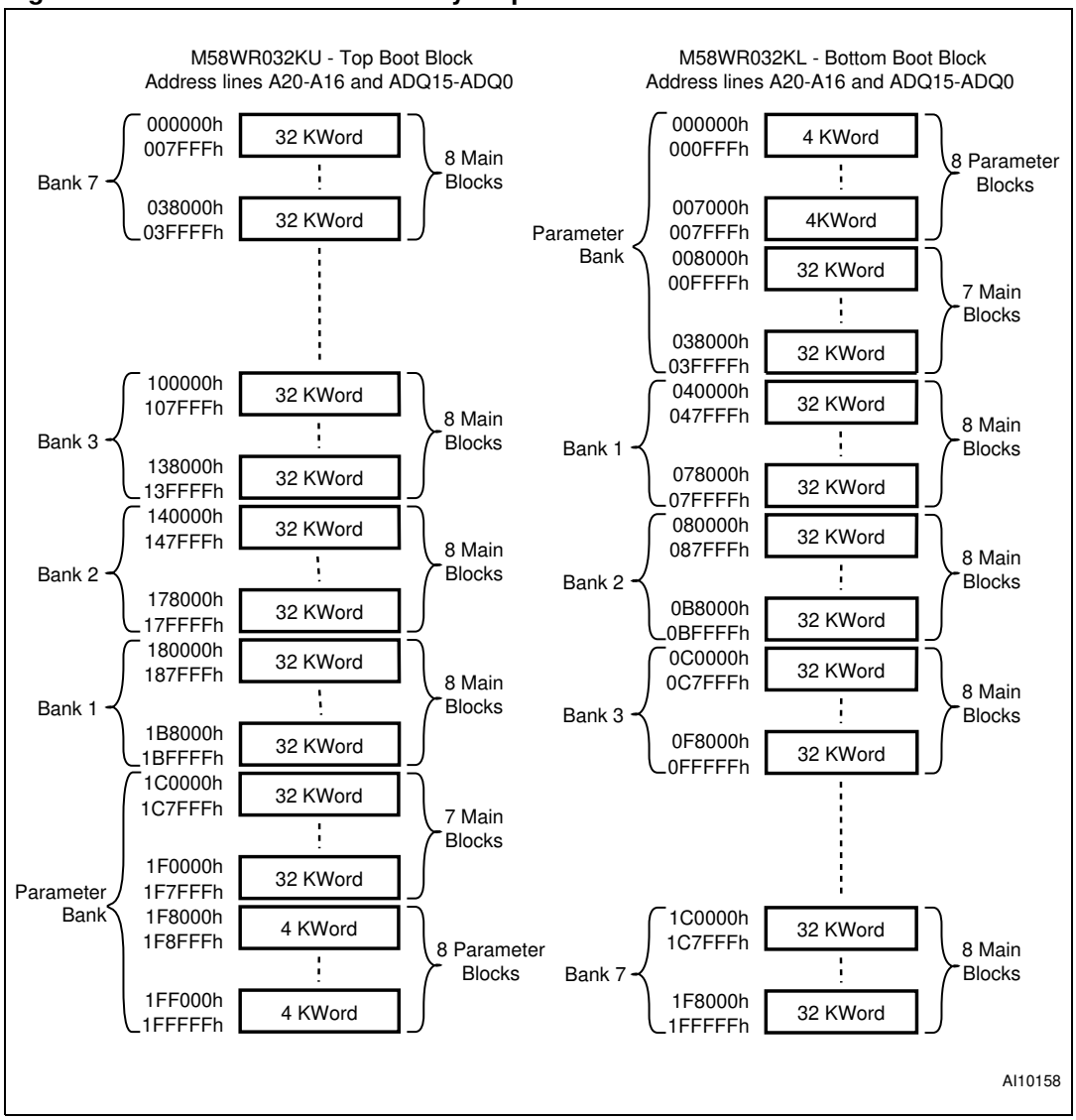
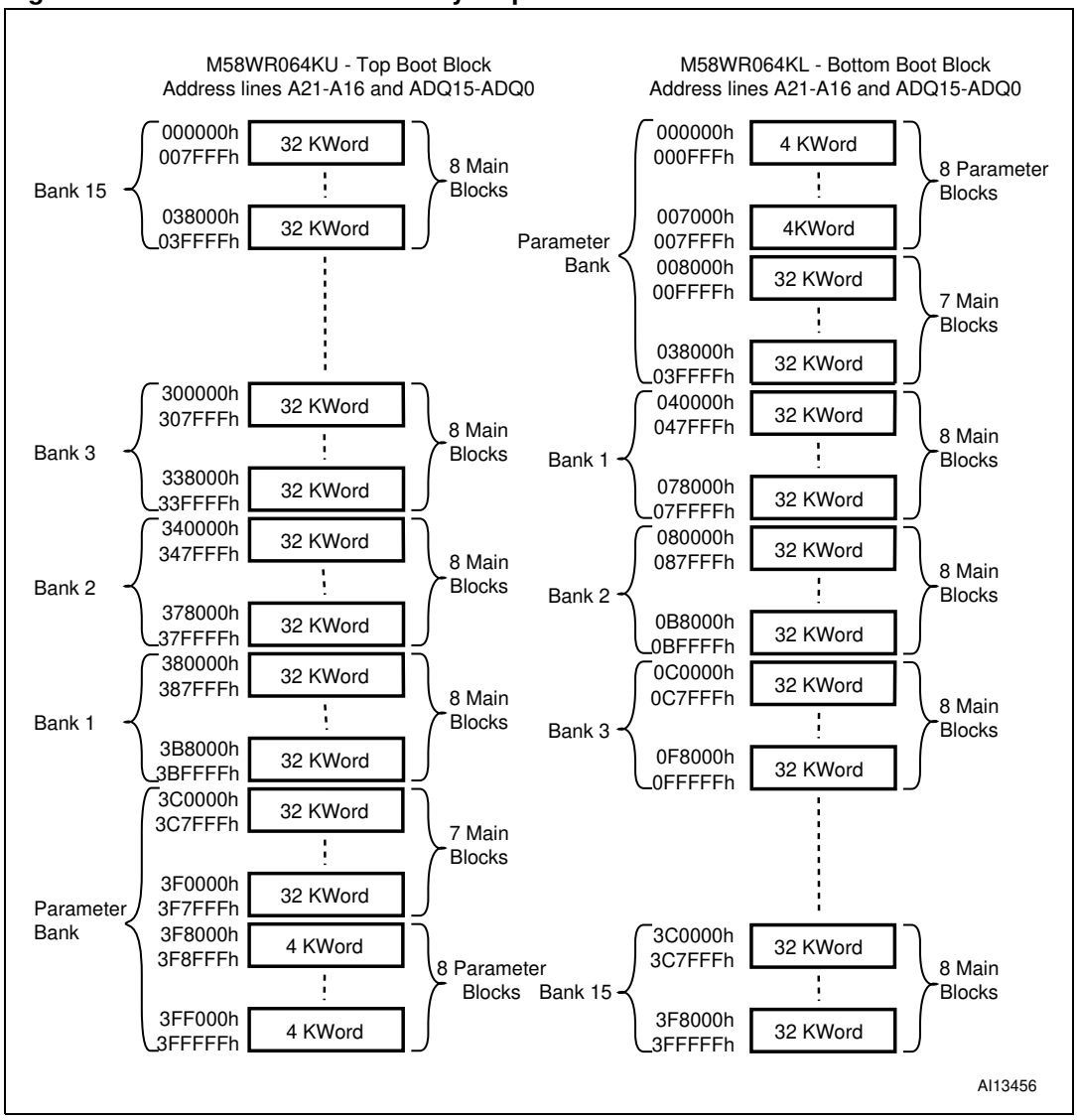


Figure 5. M58WR064KU/L memory map



2 Signal descriptions

See *Figure 1: Logic diagram* and *Table 1: Signal names* for a brief overview of the signals connected to this device.

2.1 Address inputs (ADQ0-ADQ15, A16-Amax)

Amax is equal to A19 in the M58WR016KU/L, to A20 in the M58WR032KU/L, and to A21 in the M58WR064KU/L.

The address inputs select the cells in the memory array to access during bus read operations. During bus write operations they control the commands sent to the command interface of the program/erase controller.

2.2 Data input/output (ADQ0-ADQ15)

The data I/O outputs the data stored at the selected address during a bus read operation or inputs a command or the data to be programmed during a bus write operation.

2.3 Chip Enable ($\overline{E}$)

The Chip Enable input activates the memory control logic, input buffers, decoders and sense amplifiers. When Chip Enable is at V_{IL} and Reset is at V_{IH} the device is in active mode. When Chip Enable is at V_{IH} the memory is deselected, the outputs are high impedance and the power consumption is reduced to the standby level.

2.4 Output Enable ($\overline{G}$)

The Output Enable controls data outputs during the bus read operation of the memory.

2.5 Write Enable ($\overline{W}$)

The Write Enable controls the bus write operation of the memory's command interface. The data is latched on the rising edge of Chip Enable or Write Enable, whichever occurs first.

2.6 Write Protect ($\overline{WP}$)

Write Protect is an input that gives an additional hardware protection for each block. When Write Protect is at V_{IL}, the lock-down is enabled and the protection status of the locked-down blocks cannot be changed. When Write Protect is at V_{IH}, the lock-down is disabled and the locked-down blocks can be locked or unlocked. (refer to *Table 17: Lock status*).

2.7 Reset/Power-down ($\overline{RP}$)

The Reset/Power-down input provides a hardware reset of the memory, and/or power-down functions, depending on the settings in the configuration register. When Reset/Power-Down is at V_{IL}, the memory is in reset mode: the outputs are high impedance and the current consumption is reduced to the standby supply current I_{DD3}, or to the reset/power-down supply current I_{DD2} if the power-down function is enabled. Refer to *Table 22: DC characteristics - currents* for the value of I_{DD2} and I_{DD3}.

After reset all blocks are in the locked state and the bits of the configuration register are reset except for power-down bit CR5. When Reset/Power-down is at V_{IH}, the device is in normal operation. Upon exiting reset mode the device enters asynchronous read mode, but a negative transition of Chip Enable or Latch Enable is required to ensure valid data outputs.

2.8 Latch Enable ($\overline{L}$)

Latch Enable latches the ADQ0-ADQ15 and A16-Amax address bits on its rising edge. The address latch is transparent when Latch Enable is at V_{IL} and it is inhibited when Latch Enable is at V_{IH}.

2.9 Clock (K)

The clock input synchronizes the memory to the microcontroller during synchronous read operations; the address is latched on a Clock edge (rising or falling, according to the configuration settings) when Latch Enable is at V_{IL}. Clock is ‘don't care ‘during asynchronous read and in write operations.

2.10 Wait (WAIT)

Wait is an output signal used during synchronous read to indicate whether the data on the output bus are valid. This output is high impedance when Chip Enable is at V_{IH} or Reset is at V_{IL}. It can be configured to be active during the wait cycle or one clock cycle in advance. The WAIT signal is forced deasserted when Output Enable is at V_{IH}.

2.11 Bus Invert (BINV)

Bus Invert is an input/output signal that reduces the amount of power required to switch the external address/data bus. Power is saved by inverting the data on ADQ0-ADQ15 each time the inversion results in a reduced number of pin transitions. Data is inverted when BINV is at V_{IH} (for example, if the data is AAAAh and BINV is at V_{IH}, AAAAh becomes 5555h). BINV is high impedance when Chip Enable or Output Enable is at V_{IH} or when Reset/Power-down is at V_{IL}.

2.12 V_{DD} supply voltage

V_{DD} provides the power supply to the internal core of the memory device. It is the main power supply for all operations (read, program and erase).

2.13 V_{DDQ} supply voltage

V_{DDQ} provides the power supply to the I/O pins and enables all outputs to be powered independently from V_{DD}. V_{DDQ} can be tied to V_{DD} or can use a separate supply.

2.14 V_{PP} program supply voltage

V_{PP} is both a control input and a power supply pin. The two functions are selected by the voltage range applied to the pin.

If V_{PP} is kept in a low voltage range (0 V to V_{DDQ}) V_{PP} is seen as a control input. In this case a voltage lower than V_{PPLK} gives an absolute protection against program or erase, while V_{PP} in the V_{PP1} range enables these functions (see Tables *22* and *23*, DC characteristics for the relevant values). V_{PP} is only sampled at the beginning of a program or erase; a change in its value after the operation has started does not have any effect and program or erase operations continue.

If V_{PP} is in the range of V_{PPH} it acts as a power supply pin. In this condition V_{PP} must be stable until the program/erase algorithm is completed.

2.15 V_{SS} ground

V_{SS} ground is the reference for the core supply and must be connected to the system ground.

2.16 V_{SSQ} ground

V_{SSQ} ground is the reference for the input/output circuitry driven by V_{DDQ}. V_{SSQ} must be connected to V_{SS}.

Note: Each device in a system should have V_{DD}, V_{DDQ} and V_{PP} decoupled with a 0.1 µF ceramic capacitor close to the pin (high-frequency, inherently-low inductance capacitors should be as close as possible to the package). See Figure 10: AC measurement load circuit. The PCB track widths should be sufficient to carry the required V_{PP} program and erase currents.

3 Bus operations

There are six standard bus operations that control the device. These are bus read, bus write, address latch, output disable, standby and reset. See *Table 5: Bus operations* for a summary.

Typically glitches of less than 5 ns on Chip Enable or Write Enable are ignored by the memory and do not affect bus write operations.

3.1 Bus read

Bus read operations output the contents of the memory array, the electronic signature, the status register and the common flash interface. Both Chip Enable and Output Enable must be at V_{IL} to perform a read operation. The Chip Enable input should be used to enable the device, and Output Enable should be used to gate data onto the output. The data read depends on the previous command written to the memory (see *Section 4: Command interface*). See Figures *11*, *12* and *13* read AC waveforms, and Tables *24* and *25* read AC characteristics for details of when the output becomes valid.

3.2 Bus write

Bus write operations write commands to the memory or latch input data to be programmed. A bus write operation is initiated when Chip Enable and Write Enable are at V_{IL} with Output Enable at V_{IH}. Commands and input data are latched on the rising edge of Write Enable or Chip Enable, whichever occurs first. The addresses must also be latched prior to the write operation by toggling Latch Enable (when Chip Enable is at V_{IL}). The Latch Enable must be tied to V_{IH} during the bus write operation.

See Figures *16* and *17*, write AC waveforms, and Tables *26* and *27*, write AC characteristics for details of the timing requirements.

3.3 Address latch

Address latch operations input valid addresses. Both Chip enable and Latch Enable must be at V_{IL} during address latch operations. The addresses are latched on the rising edge of Latch Enable.

3.4 Output disable

The outputs are high impedance when the Output Enable is at V_{IH}.

3.5 Standby

Standby disables most of the internal circuitry allowing a substantial reduction of the current consumption. The memory is in standby when Chip Enable and Reset are at V_{IH}. The power consumption is reduced to the standby level and the outputs are set to high impedance, independently from the Output Enable or Write Enable inputs. If Chip Enable switches to V_{IH} during a program or erase operation, the device enters standby mode when finished.

3.6 Reset/Power-down

During reset mode the memory is deselected and the outputs are high impedance. The memory is in reset mode when Reset/Power-down is at V_{IL}. The power consumption is reduced to the standby level, or to the reset/power-down level if the power-down function is enabled, independent of the Chip Enable, Output Enable or Write Enable inputs. If Reset/Power-Down is pulled to V_{SS} during a program or erase, this operation is aborted and the memory content is no longer valid.

Table 5. Bus operations

Operation	$\overline{E}$	$\overline{G}$	$\overline{W}$	$\overline{L}$	$\overline{RP}$	WAIT(1)	ADQ15-ADQ0
Bus read	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IH}		Data output
Bus write	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IH}		Data input
Address latch	V_{IL}	V_{IH}	x	V_{IL}	V_{IH}		Address input
Output disable	V_{IL}	V_{IH}	V_{IH}	V_{IH}	V_{IH}		Hi-Z
Standby	V_{IH}	X(2)	X	X	V_{IH}	Hi-Z	Hi-Z
Reset/power-down	X	X	X	X	V_{IL}	Hi-Z	Hi-Z

1. WAIT signal polarity is configured using the Set Configuration Register command.
2. X = ‘don't care’

4 Command interface

All bus write operations to the memory are interpreted by the command interface. Commands consist of one or more sequential bus write operations. An internal program/erase controller manages all timings and verifies the correct execution of the program and erase commands. The program/erase controller provides a status register whose output may be read at any time to monitor the progress or the result of the operation.

The command interface is reset to read mode when power is first applied, when exiting from reset or whenever V_{DD} is lower than V_{LKO}. Command sequences must be followed exactly. Any invalid combination of commands are ignored.

Refer to *Table 6: Command codes*, and *Appendix D*, Tables *47*, *48*, *49* and *50*, command interface states - modify and lock tables for a summary of the command interface.

The command interface is split into two types of commands: standard commands and factory program commands. The following sections explain in detail how to perform each command.

Table 6. Command codes

Hex Code	Command
01h	Block Lock Confirm
03h	Set Configuration Register Confirm
10h	Alternative Program Setup
20h	Block Erase Setup
2Fh	Block Lock-Down Confirm
30h	Enhanced Factory Program Setup
35h	Double Word Program Setup
40h	Program Setup
50h	Clear Status Register
56h	Quadruple Word Program Setup
60h	Block Lock Setup, Block Unlock Setup, Block Lock Down Setup and Set Configuration Register Setup
70h	Read Status Register
75h	Quadruple Enhanced Factory Program Setup
90h	Read Electronic Signature
98h	Read CFI Query
B0h	Program/Erase Suspend
C0h	Protection Register Program
D0h	Program/Erase Resume, Block Erase Confirm, Block Unlock Confirm or Enhanced Factory Program Confirm
FFh	Read Array

5 Command interface - standard commands

The following commands are the basic commands used to read, write to, and configure the device. Refer to *Table 7: Standard commands* in conjunction with the following text descriptions.

5.1 Read Array command

The Read Array command returns the addressed bank to read array mode. One bus write cycle is required to issue the Read Array command and return the addressed bank to read array mode. Subsequent read operations read the addressed location and output the data. A Read Array command can be issued in one bank while programming or erasing in another bank. However, if a Read Array command is issued to a bank currently executing a program or erase operation the command is executed but the output data is not guaranteed.

5.2 Read Status Register command

The status register indicates when a program or erase operation is complete and the success or failure of operation itself. Issue a Read Status Register command to read the status register content. The Read Status Register command can be issued at any time, even during program or erase operations.

The following read operations output the content of the status register of the addressed bank. The status register is latched on the falling edge of $\overline{E}$ or $\overline{G}$ signals, and can be read until $\overline{E}$ or $\overline{G}$ returns to V_{IH}. Either $\overline{E}$ or $\overline{G}$ must be toggled to update the latched data. See *Table 10* for the description of the status register bits. This mode supports asynchronous or single synchronous reads only.

5.3 Read Electronic Signature command

The Read Electronic Signature command reads the manufacturer and device codes, the block locking status, the protection register, and the configuration register.

The Read Electronic Signature command consists of one write cycle to an address within one of the banks. A subsequent read operation in the same bank outputs the manufacturer code, the device code, the protection status of the blocks in the targeted bank, the protection register, or the configuration register (see *Table 8*).

The Read Electronic Signature command can be issued at any time, even during program or erase operations, except during protection register program operations. Dual operations between the parameter bank and the electronic signature location are not allowed (see *Table 16: Dual operation limitations* for details).

If a Read Electronic Signature command is issued in a bank that is executing a program or erase operation the bank goes into read electronic signature mode, subsequent bus read cycles output the electronic signature data, and the program/erase controller continues to program or erase in the background. This mode only supports asynchronous or single synchronous reads only; it does not support synchronous burst reads.

5.4 Read CFI Query command

The Read CFI Query command reads data from the common flash interface (CFI). The Read CFI Query command consists of one bus write cycle to an address within one of the banks. Once the command is issued subsequent bus read operations in the same bank read from the common flash interface.

If a Read CFI Query command is issued in a bank that is executing a program or erase operation, the bank goes into read CFI query mode, subsequent bus read cycles output the CFI data, and the program/erase controller continues to program or erase in the background. This mode only supports asynchronous or single synchronous reads; it does not support synchronous burst reads.

The status of the other banks is not affected by the command (see *Table 14*). After issuing a Read CFI Query command, a Read Array command should be issued to the addressed bank to return the bank to read array mode. Dual operations between the parameter bank and the CFI memory space are not allowed (see *Table 16: Dual operation limitations*).

See *Appendix B: Common flash interface*, Tables *37*, *38*, *39*, *40*, *41*, *42*, *43*, *44*, *45* and *46* for details on the information contained in the common flash interface memory area.

5.5 Clear Status Register command

The Clear Status Register command reset (set to ‘0’) error bits SR1, SR3, SR4 and SR5 in the status register. One bus write cycle is required to issue the Clear Status Register command. After the Clear Status Register command the bank returns to read mode.

The error bits in the status register do not automatically return to ‘0’ when a new command is issued. The error bits in the status register should be cleared before attempting a new program or erase command.

5.6 Block Erase command

The Block Erase command erases a block by setting all the bits within the selected block to '1'. All previous data in the block is lost. If the block is protected then the erase operation aborts, the data in the block does not change, and the status register outputs the error. The Block Erase command can be issued at any moment regardless of whether the block has been programmed or not.

Two bus write cycles are required to issue the command.

- The first bus cycle sets up the erase command.
- The second latches the block address in the program/erase controller and starts it.

If the second bus cycle is not Write Erase Confirm (D0h), status register bits SR4 and SR5 are set and the command aborts. Erase aborts if Reset turns to V_{IL}. As data integrity cannot be guaranteed when the erase operation aborts, the block must be erased again.

Once the Block Erase command is issued the device outputs the status register data when any address within the bank is read. At the end of the operation the bank remains in read status register mode until a Read Array, Read CFI Query or Read Electronic Signature command is issued.

During erase operations the bank containing the block being erased only accepts the Read Array, Read Status Register, Read Electronic Signature, Read CFI Query and the Program/Erase Suspend commands: all other commands are ignored. Refer to *Section 10: Dual operations and multiple bank architecture* for detailed information about simultaneous operations allowed in banks not being erased. Typical erase times are given in *Table 18: Program and erase times and endurance cycles*.

See *Appendix C*, *Figure 24: Block erase flowchart and pseudocode* for a suggested flowchart for using the Block Erase command.

5.7 Program command

The memory array can be programmed word-by-word. Only one word in one bank can be programmed at any one time. If the block is protected then the program operation aborts, the data in the block does not changed, and the status register outputs the error.

Two bus write cycles are required to issue the Program command.

- The first bus cycle sets up the Program command.
- The second latches the address and the data to be written and starts the program/erase controller.

After programming has started, read operations in the bank being programmed output the status register content.

During program operations the bank being programmed only accepts the Read Array, Read Status Register, Read Electronic Signature, Read CFI Query and the Program/Erase Suspend commands. Refer to *Section 10: Dual operations and multiple bank architecture* for detailed information about simultaneous operations allowed in banks not being programmed. Typical program times are given in *Table 18: Program and erase times and endurance cycles*.

Programming aborts if Reset goes to V_{IL}. As data integrity cannot be guaranteed when the program operation is aborted, the memory location must be reprogrammed.