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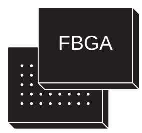
# M58WR064ET
# M58WR064EB

## 64 Mbit (4Mb x 16, Multiple Bank, Burst) 1.8V Supply Flash Memory

### FEATURES SUMMARY

- SUPPLY VOLTAGE
  - $V_{DD}$ = 1.65V to 2.2V for Program, Erase and Read
  - $V_{DDQ}$ = 1.65V to 3.3V for I/O Buffers
  - $V_{PP}$ = 12V for fast Program (optional)
- SYNCHRONOUS / ASYNCHRONOUS READ
  - Synchronous Burst Read mode: 54MHz
  - Asynchronous/ Synchronous Page Read mode
  - Random Access: 70, 80, 100 ns
- PROGRAMMING TIME
  - 8µs by Word typical for Fast Factory Program
  - Double/Quadruple Word Program option
  - Enhanced Factory Program options
- MEMORY BLOCKS
  - Multiple Bank Memory Array: 4 Mbit Banks
  - Parameter Blocks (Top or Bottom location)
- DUAL OPERATIONS
  - Program Erase in one Bank while Read in others
  - No delay between Read and Write operations
- BLOCK LOCKING
  - All blocks locked at Power up
  - Any combination of blocks can be locked
  - $\overline{WP}$ for Block Lock-Down
- SECURITY
  - 128 bit user programmable OTP cells
  - 64 bit unique device number
  - One parameter block permanently lockable
- COMMON FLASH INTERFACE (CFI)
- 100,000 PROGRAM/ERASE CYCLES per BLOCK

**Figure 1. Package**




VFBGA56 (ZB)
7.7 x 9 mm

- ELECTRONIC SIGNATURE
  - Manufacturer Code: 20h
  - Top Device Code, M58WR064ET: 8810h
  - Bottom Device Code, M58WR064EB: 8811h

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## SUMMARY DESCRIPTION

The M58WR064E is a 64 Mbit (4Mbit x16) non-volatile Flash memory that may be erased electrically at block level and programmed in-system on a Word-by-Word basis using a 1.65V to 2.2V $V_{DD}$ supply for the circuitry and a 1.65V to 3.3V $V_{DDQ}$ supply for the Input/Output pins. An optional 12V $V_{PP}$ power supply is provided to speed up customer programming.

The device features an asymmetrical block architecture. M58WR064E has an array of 135 blocks, and is divided into 4 Mbit banks. There are 15 banks each containing 8 main blocks of 32 KWords, and one parameter bank containing 8 parameter blocks of 4 KWords and 7 main blocks of 32 KWords. The Multiple Bank Architecture allows Dual Operations, while programming or erasing in one bank, Read operations are possible in other banks. Only one bank at a time is allowed to be in Program or Erase mode. It is possible to perform burst reads that cross bank boundaries. The bank architecture is summarized in Table 2, and the memory maps are shown in Figure 4. The Parameter Blocks are located at the top of the memory address space for the M58WR064ET, and at the bottom for the M58WR064EB.

Each block can be erased separately. Erase can be suspended, in order to perform program in any other block, and then resumed. Program can be suspended to read data in any other block and then resumed. Each block can be programmed and erased over 100,000 cycles using the supply voltage $V_{DD}$. There are two Enhanced Factory programming commands available to speed up programming.

Program and Erase commands are written to the Command Interface of the memory. An internal Program/Erase Controller takes care of the timings necessary for program and erase operations. The end of a program or erase operation can be detected and any error conditions identified in the Status Register. The command set required to control the memory is consistent with JEDEC standards.

The device supports synchronous burst read and asynchronous read from all blocks of the memory array; at power-up the device is configured for asynchronous read. In synchronous burst mode, data is output on each clock cycle at frequencies of up to 54MHz.

The device features an Automatic Standby mode. When the bus is inactive during Asynchronous Read operations, the device automatically switches to the Automatic Standby mode. In this condition the power consumption is reduced to the standby value $I_{DD4}$ and the outputs are still driven.

The M58WR064E features an instant, individual block locking scheme that allows any block to be locked or unlocked with no latency, enabling instant code and data protection. All blocks have three levels of protection. They can be locked and locked-down individually preventing any accidental programming or erasure. There is an additional hardware protection against program and erase. When $V_{PP} \leq V_{PPLK}$ all blocks are protected against program or erase. All blocks are locked at Power-Up.

The device includes a Protection Register and a Security Block to increase the protection of a system's design. The Protection Register is divided into two segments: a 64 bit segment containing a unique device number written by ST, and a 128 bit segment One-Time-Programmable (OTP) by the user. The user programmable segment can be permanently protected. The Security Block, parameter block 0, can be permanently protected by the user. Figure 5, shows the Security Block and Protection Register Memory Map.

The memory is offered in a VFBGA56, 7.7 x 9 mm 0.75 mm ball pitch package and is supplied with all the bits erased (set to '1').

**Figure 2. Logic Diagram**

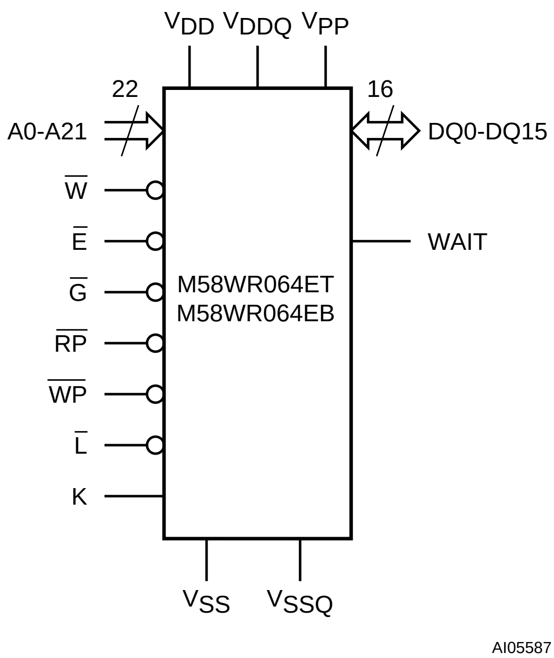



**Table 1. Signal Names**

| | |
|---|---|
| A0-A21 | Address Inputs |
| DQ0-DQ15 | Data Input/Outputs, Command Inputs |
| $\overline{E}$ | Chip Enable |
| $\overline{G}$ | Output Enable |
| $\overline{W}$ | Write Enable |
| $\overline{RP}$ | Reset |
| $\overline{WP}$ | Write Protect |
| K | Clock |
| $\overline{L}$ | Latch Enable |
| WAIT | Wait |
| $V_{DD}$ | Supply Voltage |
| $V_{DDQ}$ | Supply Voltage for Input/Output Buffers |
| $V_{PP}$ | Optional Supply Voltage for Fast Program & Erase |
| $V_{SS}$ | Ground |
| $V_{SSQ}$ | Ground Input/Output Supply |
| NC | Not Connected Internally |

**Figure 3. VFBGA Connections (Top view through package)**

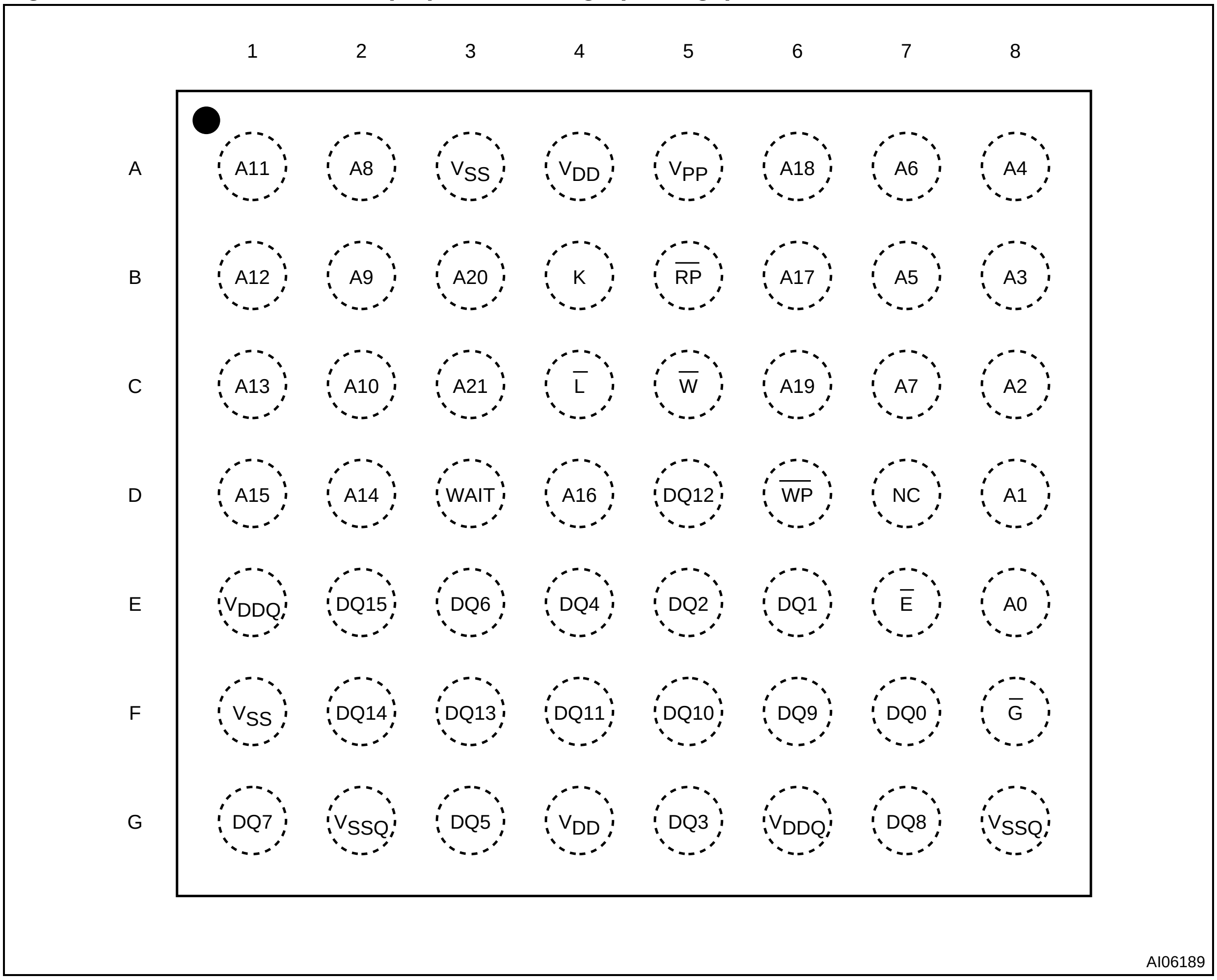
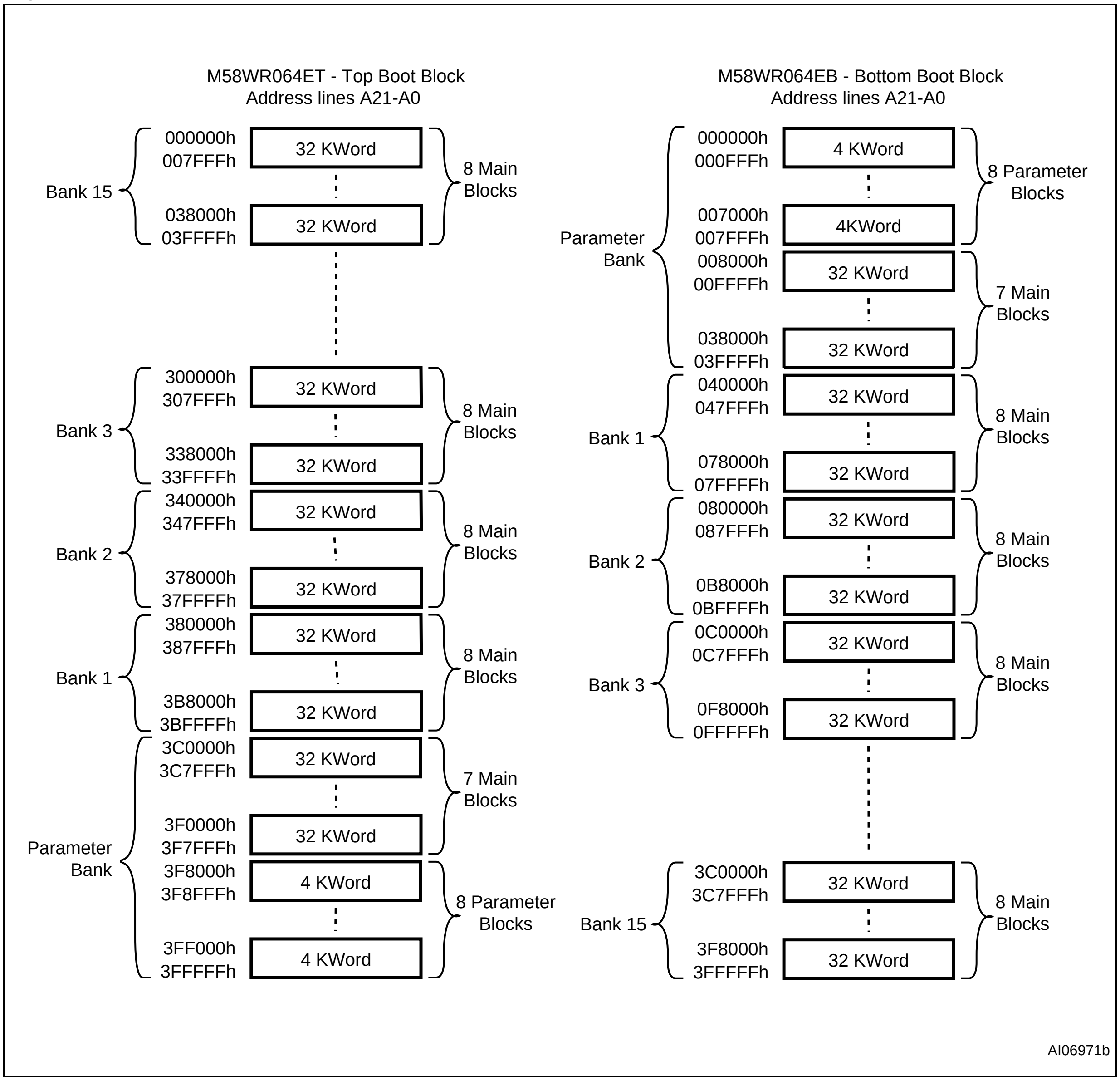



**Table 2. Bank Architecture**

| Number | Bank Size | Parameter Blocks | Main Blocks |
|---|---|---|---|
| Parameter Bank | 4 Mbits | 8 blocks of 4 KWords | 7 blocks of 32 KWords |
| Bank 1 | 4 Mbits | - | 8 blocks of 32 KWords |
| Bank 2 | 4 Mbits | - | 8 blocks of 32 KWords |
| Bank 3 | 4 Mbits | - | 8 blocks of 32 KWords |
| ⋮ | ⋮ | ⋮ | ⋮ |
| Bank 14 | 4 Mbits | - | 8 blocks of 32 KWords |
| Bank 15 | 4 Mbits | - | 8 blocks of 32 KWords |

**Figure 4. Memory Map**



## SIGNAL DESCRIPTIONS

See Figure 2 Logic Diagram and Table 1,Signal Names, for a brief overview of the signals connected to this device.

**Address Inputs (A0-A21).** The Address Inputs select the cells in the memory array to access during Bus Read operations. During Bus Write operations they control the commands sent to the Command Interface of the internal state machine.

**Data Input/Output (DQ0-DQ15).** The Data I/O outputs the data stored at the selected address during a Bus Read operation or inputs a command or the data to be programmed during a Bus Write operation.

**Chip Enable ($\overline{E}$).** The Chip Enable input activates the memory control logic, input buffers, decoders and sense amplifiers. When Chip Enable is at $V_{IL}$and Reset is at $V_{IH}$ the device is in active mode. When Chip Enable is at $V_{IH}$ the memory is deselected, the outputs are high impedance and the power consumption is reduced to the stand-by level.

**Output Enable ($\overline{G}$).** The Output Enable controls data outputs during the Bus Read operation of the memory.

**Write Enable ($\overline{W}$).** The Write Enable controls the Bus Write operation of the memory's Command Interface. The data and address inputs are latched on the rising edge of Chip Enable or Write Enable whichever occurs first.

**Write Protect ($\overline{WP}$).** Write Protect is an input that gives an additional hardware protection for each block. When Write Protect is at $V_{IL}$, the Lock-Down is enabled and the protection status of the Locked-Down blocks cannot be changed. When Write Protect is at $V_{IH}$, the Lock-Down is disabled and the Locked-Down blocks can be locked or unlocked. (refer to Table 13, Lock Status).

**Reset ($\overline{RP}$).** The Reset input provides a hardware reset of the memory. When Reset is at $V_{IL}$, the memory is in reset mode: the outputs are high impedance and the current consumption is reduced to the Reset Supply Current $I_{DD2}$. Refer to Table 2, DC Characteristics - Currents for the value of $I_{DD2.}$ After Reset all blocks are in the Locked state and the Configuration Register is reset. When Reset is at $V_{IH}$, the device is in normal operation. Exiting reset mode the device enters asynchronous read mode, but a negative transition of Chip Enable or Latch Enable is required to ensure valid data outputs.

The Reset pin can be interfaced with 3V logic without any additional circuitry. It can be tied to $V_{RPH}$ (refer to Table 19, DC Characteristics).

**Latch Enable ($\overline{L}$).** Latch Enable latches the address bits on its rising edge. The address latch is transparent when Latch Enable is at $V_{IL}$ and it is inhibited when Latch Enable is at $V_{IH}$. Latch Enable can be kept Low (also at board level) when the Latch Enable function is not required or supported.

**Clock (K).** The clock input synchronizes the memory to the microcontroller during synchronous read operations; the address is latched on a Clock edge (rising or falling, according to the configuration settings) when Latch Enable is at $V_{IL}$. Clock is don't care during asynchronous read and in write operations.

**Wait (WAIT).** Wait is an output signal used during synchronous read to indicate whether the data on the output bus are valid. This output is high impedance when Chip Enable is at $V_{IH}$ or Reset is at $V_{IL}$. It can be configured to be active during the wait cycle or one clock cycle in advance. The WAIT signal is not gated by Output Enable.

**$V_{DD}$ Supply Voltage .** $V_{DD}$ provides the power supply to the internal core of the memory device. It is the main power supply for all operations (Read, Program and Erase).

**$V_{DDQ}$ Supply Voltage.** $V_{DDQ}$ provides the power supply to the I/O pins and enables all Outputs to be powered independently from $V_{DD}$. $V_{DDQ}$ can be tied to $V_{DD}$ or can use a separate supply.

**$V_{PP}$ Program Supply Voltage.** $V_{PP}$ is both a control input and a power supply pin. The two functions are selected by the voltage range applied to the pin.

If $V_{PP}$ is kept in a low voltage range (0V to $V_{DDQ}$) $V_{PP}$ is seen as a control input. In this case a voltage lower than $V_{PPLK}$ gives an absolute protection against program or erase, while $V_{PP}$ > $V_{PP1}$ enables these functions (see Tables 18 and 19, DC Characteristics for the relevant values). $V_{PP}$ is only sampled at the beginning of a program or erase; a change in its value after the operation has started does not have any effect and program or erase operations continue.

If $V_{PP}$ is in the range of $V_{PPH}$ it acts as a power supply pin. In this condition $V_{PP}$ must be stable until the Program/Erase algorithm is completed.

**$V_{SS}$ Ground.** $V_{SS}$ ground is the reference for the core supply. It must be connected to the system ground.

**$V_{SSQ}$ Ground.** $V_{SSQ}$ ground is the reference for the input/output circuitry driven by $V_{DDQ}$. $V_{SSQ}$ must be connected to $V_{SS}$

**Note: Each device in a system should have $V_{DD}$, $V_{DDQ}$ and $V_{PP}$ decoupled with a 0.1µF ceramic capacitor close to the pin (high frequency, inherently low inductance capacitors should be as close as possible to the pack-**

**age). See Figure 9, AC Measurement Load Circuit. The PCB trace widths should be sufficient to carry the required $V_{PP}$ program and erase currents.**

## BUS OPERATIONS

There are six standard bus operations that control the device. These are Bus Read, Bus Write, Address Latch, Output Disable, Standby and Reset. See Table 3, Bus Operations, for a summary.

Typically glitches of less than 5ns on Chip Enable or Write Enable are ignored by the memory and do not affect Bus Write operations.

**Bus Read.** Bus Read operations are used to output the contents of the Memory Array, the Electronic Signature, the Status Register and the Common Flash Interface. Both Chip Enable and Output Enable must be at $V_{IL}$ in order to perform a read operation. The Chip Enable input should be used to enable the device. Output Enable should be used to gate data onto the output. The data read depends on the previous command written to the memory (see Command Interface section). See Figures 10, 11, 12 and 13 Read AC Waveforms, and Tables 20 and 21 Read AC Characteristics, for details of when the output becomes valid.

**Bus Write.** Bus Write operations write Commands to the memory or latch Input Data to be programmed. A bus write operation is initiated when Chip Enable and Write Enable are at $V_{IL}$ with Output Enable at $V_{IH}$. Commands, Input Data and Addresses are latched on the rising edge of Write Enable or Chip Enable, whichever occurs first. The addresses can also be latched prior to the write operation by toggling Latch Enable. In this case the Latch Enable should be tied to $V_{IH}$ during the bus write operation.

See Figures 15 and 16, Write AC Waveforms, and Tables 22 and 23, Write AC Characteristics, for details of the timing requirements.

**Address Latch.** Address latch operations input valid addresses. Both Chip enable and Latch Enable must be at $V_{IL}$ during address latch operations. The addresses are latched on the rising edge of Latch Enable.

**Output Disable.** The outputs are high impedance when the Output Enable is at $V_{IH}$.

**Standby.** Standby disables most of the internal circuitry allowing a substantial reduction of the current consumption. The memory is in stand-by when Chip Enable and Reset are at $V_{IH}$. The power consumption is reduced to the stand-by level and the outputs are set to high impedance, independently from the Output Enable or Write Enable inputs. If Chip Enable switches to $V_{IH}$ during a program or erase operation, the device enters Standby mode when finished.

**Reset.** During Reset mode the memory is deselected and the outputs are high impedance. The memory is in Reset mode when Reset is at $V_{IL}$. The power consumption is reduced to the Standby level, independently from the Chip Enable, Output Enable or Write Enable inputs. If Reset is pulled to $V_{SS}$ during a Program or Erase operation, this operation is aborted and the memory content is no longer valid.

**Table 3. Bus Operations**

| Operation | $\overline{E}$ | $\overline{G}$ | $\overline{W}$ | $\overline{L}$ | $\overline{RP}$ | WAIT(4) | DQ15-DQ0 |
|---|---|---|---|---|---|---|---|
| Bus Read | $V_{IL}$ | $V_{IL}$ | $V_{IH}$ | $V_{IL}$(2) | $V_{IH}$ | | Data Output |
| Bus Write | $V_{IL}$ | $V_{IH}$ | $V_{IL}$ | $V_{IL}$(2) | $V_{IH}$ | | Data Input |
| Address Latch | $V_{IL}$ | X | $V_{IH}$ | $V_{IL}$ | $V_{IH}$ | | Data Output or Hi-Z (3) |
| Output Disable | $V_{IL}$ | $V_{IH}$ | $V_{IH}$ | X | $V_{IH}$ | | Hi-Z |
| Standby | $V_{IH}$ | X | X | X | $V_{IH}$ | Hi-Z | Hi-Z |
| Reset | X | X | X | X | $V_{IL}$ | Hi-Z | Hi-Z |

Note: 1. X = Don't care.
2. $\overline{L}$ can be tied to $V_{IH}$ if the valid address has been previously latched.
3. Depends on $\overline{G}$.
4. WAIT signal polarity is configured using the Set Configuration Register command.

## COMMAND INTERFACE

All Bus Write operations to the memory are interpreted by the Command Interface. Commands consist of one or more sequential Bus Write operations. An internal Program/Erase Controller handles all timings and verifies the correct execution of the Program and Erase commands. The Program/Erase Controller provides a Status Register whose output may be read at any time to monitor the progress or the result of the operation.

The Command Interface is reset to read mode when power is first applied, when exiting from Reset or whenever $V_{DD}$ is lower than $V_{LKO}$. Command sequences must be followed exactly. Any invalid combination of commands will be ignored.

Refer to Table 4, Command Codes and Appendix D, Tables 40, 41, 42 and 43, Command Interface States - Modify and Lock Tables, for a summary of the Command Interface.

The Command Interface is split into two types of commands: Standard commands and Factory Program commands. The following sections explain in detail how to perform each command.

**Table 4. Command Codes**

| Hex Code | Command |
|---|---|
| 01h | Block Lock Confirm |
| 03h | Set Configuration Register Confirm |
| 10h | Alternative Program Setup |
| 20h | Block Erase Setup |
| 2Fh | Block Lock-Down Confirm |
| 30h | Enhanced Factory Program Setup |
| 35h | Double Word Program Setup |
| 40h | Program Setup |
| 50h | Clear Status Register |
| 56h | Quadruple Word Program Setup |
| 60h | Block Lock Setup, Block Unlock Setup, Block Lock Down Setup and Set Configuration Register Setup |
| 70h | Read Status Register |
| 75h | Quadruple Enhanced Factory Program Setup |
| 80h | Bank Erase Setup |
| 90h | Read Electronic Signature |
| 98h | Read CFI Query |
| B0h | Program/Erase Suspend |
| C0h | Protection Register Program |
| D0h | Program/Erase Resume, Block Erase Confirm, Bank Erase Confirm, Block Unlock Confirm or Enhanced Factory Program Confirm |
| FFh | Read Array |

## COMMAND INTERFACE - STANDARD COMMANDS

The following commands are the basic commands used to read, write to and configure the device. Refer to Table 5, Standard Commands, in conjunction with the following text descriptions.

### Read Array Command

The Read Array command returns the addressed bank to Read Array mode. One Bus Write cycle is required to issue the Read Array command and return the addressed bank to Read Array mode. Subsequent read operations will read the addressed location and output the data. A Read Array command can be issued in one bank while programming or erasing in another bank. However if a Read Array command is issued to a bank currently executing a Program or Erase operation the command will be executed but the output data is not guaranteed.

### Read Status Register Command

The Status Register indicates when a Program or Erase operation is complete and the success or failure of operation itself. Issue a Read Status Register command to read the Status Register content. The Read Status Register command can be issued at any time, even during Program or Erase operations.

The following read operations output the content of the Status Register of the addressed bank. The Status Register is latched on the falling edge of $\overline{E}$ or $\overline{G}$ signals, and can be read until $\overline{E}$ or $\overline{G}$ returns to $V_{IH}$. Either $\overline{E}$ or $\overline{G}$ must be toggled to update the latched data. See Table 8 for the description of the Status Register Bits. This mode supports asynchronous or single synchronous reads only.

### Read Electronic Signature Command

The Read Electronic Signature command reads the Manufacturer and Device Codes, the Block Locking Status, the Protection Register, and the Configuration Register.

The Read Electronic Signature command consists of one write cycle to an address within one of the banks. A subsequent Read operation in the same bank will output the Manufacturer Code, the Device Code, the protection Status of the blocks in the targeted bank, the Protection Register, or the Configuration Register (see Table 6).

If a Read Electronic Signature command is issued in a bank that is executing a Program or Erase operation the bank will go into Read Electronic Signature mode, subsequent Bus Read cycles will output the Electronic Signature data and the Program/Erase controller will continue to program or erase in the background. This mode supports asynchronous or single synchronous reads only, it does not support page mode or synchronous burst reads.

### Read CFI Query Command

The Read CFI Query command is used to read data from the Common Flash Interface (CFI). The Read CFI Query Command consists of one Bus Write cycle, to an address within one of the banks. Once the command is issued subsequent Bus Read operations in the same bank read from the Common Flash Interface.

If a Read CFI Query command is issued in a bank that is executing a Program or Erase operation the bank will go into Read CFI Query mode, subsequent Bus Read cycles will output the CFI data and the Program/Erase controller will continue to Program or Erase in the background. This mode supports asynchronous or single synchronous reads only, it does not support page mode or synchronous burst reads.

The status of the other banks is not affected by the command (see Table 11). After issuing a Read CFI Query command, a Read Array command should be issued to the addressed bank to return the bank to Read Array mode.

See Appendix C, Common Flash Interface, Tables 30, 31, 32, 33, 34, 36, 37, 38 and 39 for details on the information contained in the Common Flash Interface memory area.

### Clear Status Register Command

The Clear Status Register command can be used to reset (set to ‘0’) error bits 1, 3, 4 and 5 in the Status Register. One bus write cycle is required to issue the Clear Status Register command. The Clear Status Register command does not change the Read mode of the bank.

The error bits in the Status Register do not automatically return to ‘0’ when a new command is issued. The error bits in the Status Register should be cleared before attempting a new Program or Erase command.

### Block Erase Command

The Block Erase command can be used to erase a block. It sets all the bits within the selected block to ’1’. All previous data in the block is lost. If the block is protected then the Erase operation will abort, the data in the block will not be changed and the Status Register will output the error. The Block Erase command can be issued at any moment, regardless of whether the block has been programmed or not.

Two Bus Write cycles are required to issue the command.

- The first bus cycle sets up the Erase command.
- The second latches the block address in the internal state machine and starts the Program/ Erase Controller.

If the second bus cycle is not Write Erase Confirm (D0h), Status Register bits 4 and 5 are set and the command aborts. Erase aborts if Reset turns to $V_{IL}$. As data integrity cannot be guaranteed when the Erase operation is aborted, the block must be erased again.

Once the command is issued the device outputs the Status Register data when any address within the bank is read. At the end of the operation the bank will remain in Read Status Register mode until a Read Array, Read CFI Query or Read Electronic Signature command is issued.

During Erase operations the bank containing the block being erased will only accept the Read Array, Read Status Register, Read Electronic Signature, Read CFI Query and the Program/Erase Suspend command, all other commands will be ignored. Refer to Dual Operations section for detailed information about simultaneous operations allowed in banks not being erased. Typical Erase times are given in Table 14, Program, Erase Times and Program/Erase Endurance Cycles.

See Appendix C, Figure 25, Block Erase Flowchart and Pseudo Code, for a suggested flowchart for using the Block Erase command.

**Program Command**

The memory array can be programmed word-by-word. Only one Word in one bank can be programmed at any one time. Two bus write cycles are required to issue the Program Command.

- The first bus cycle sets up the Program command.
- The second latches the Address and the Data to be written and starts the Program/Erase Controller.

After programming has started, read operations in the bank being programmed output the Status Register content.

During Program operations the bank being programmed will only accept the Read Array, Read Status Register, Read Electronic Signature, Read CFI Query and the Program/Erase Suspend command. Refer to Dual Operations section for detailed information about simultaneous operations allowed in banks not being programmed. Typical Program times are given in Table 14, Program, Erase Times and Program/Erase Endurance Cycles.

Programming aborts if Reset goes to $V_{IL}$. As data integrity cannot be guaranteed when the program operation is aborted, the memory location must be reprogrammed.

See Appendix C, Figure 21, Program Flowchart and Pseudo Code, for the flowchart for using the Program command.

**Program/Erase Suspend Command**

The Program/Erase Suspend command is used to pause a Program or Block Erase operation. A Bank Erase operation cannot be suspended.

One bus write cycle is required to issue the Program/Erase command. Once the Program/Erase Controller has paused bits SR7, SR6 and/ or SR2 of the Status Register will be set to ‘1’. The command can be addressed to any bank.

During Program/Erase Suspend the Command Interface will accept the Program/Erase Resume, Read Array (cannot read the erase-suspended block or the program-suspended Word), Read Status Register, Read Electronic Signature and Read CFI Query commands. Additionally, if the suspend operation was Erase then the Clear status Register, Program, Block Lock, Block Lock-Down or Block Unlock commands will also be accepted. The block being erased may be protected by issuing the Block Lock, Block Lock-Down or Protection Register Program commands. Only the blocks not being erased may be read or programmed correctly. When the Program/Erase Resume command is issued the operation will complete. Refer to the Dual Operations section for detailed information about simultaneous operations allowed during Program/Erase Suspend.

During a Program/Erase Suspend, the device can be placed in standby mode by taking Chip Enable to $V_{IH}$. Program/Erase is aborted if Reset turns to $V_{IL}$.

See Appendix C, Figure 24, Program Suspend & Resume Flowchart and Pseudo Code, and Figure 26, Erase Suspend & Resume Flowchart and Pseudo Code for flowcharts for using the Program/ Erase Suspend command.

**Program/Erase Resume Command**

The Program/Erase Resume command can be used to restart the Program/Erase Controller after a Program/Erase Suspend command has paused it. One Bus Write cycle is required to issue the command. The command can be written to any address.

The Program/Erase Resume command does not change the read mode of the banks. If the suspended bank was in Read Status Register, Read Electronic signature or Read CFI Query mode the bank remains in that mode and outputs the corresponding data. If the bank was in Read Array mode subsequent read operations will output invalid data.

If a Program command is issued during a Block Erase Suspend, then the erase cannot be resumed until the programming operation has completed. It is possible to accumulate suspend operations. For example: suspend an erase operation, start a programming operation, suspend the programming operation then read the array. See Appendix C, Figure 24, Program Suspend & Resume Flowchart and Pseudo Code, and Figure 26, Erase Suspend & Resume Flowchart and Pseudo Code for flowcharts for using the Program/Erase Resume command.

### Protection Register Program Command

The Protection Register Program command is used to Program the 128 bit user One-Time-Programmable (OTP) segment of the Protection Register and the Protection Register Lock. The segment is programmed 16 bits at a time. When shipped all bits in the segment are set to ‘1’. The user can only program the bits to ‘0’.

Two write cycles are required to issue the Protection Register Program command.

- The first bus cycle sets up the Protection Register Program command.
- The second latches the Address and the Data to be written to the Protection Register and starts the Program/Erase Controller.

Read operations output the Status Register content after the programming has started.

The segment can be protected by programming bit 1 of the Protection Lock Register. Bit 1 of the Protection Lock Register also protects bit 2 of the Protection Lock Register. Programming bit 2 of the Protection Lock Register will result in a permanent protection of Parameter Block #0 (see Figure 5, Security Block and Protection Register Memory Map). Attempting to program a previously protected Protection Register will result in a Status Register error. The protection of the Protection Register and/or the Security Block is not reversible.

The Protection Register Program cannot be suspended. See Appendix C, Figure 28, Protection Register Program Flowchart and Pseudo Code, for a flowchart for using the Protection Register Program command.

### Set Configuration Register Command

The Set Configuration Register command is used to write a new value to the Burst Configuration Control Register which defines the burst length, type, X latency, Synchronous/Asynchronous Read mode and the valid Clock edge configuration.

Two Bus Write cycles are required to issue the Set Configuration Register command.

- The first cycle writes the setup command and the address corresponding to the Configuration Register content.
- The second cycle writes the Configuration Register data and the confirm command.

The Read mode of the banks is not modified when the Set Configuration Register command is issued.

The value for the Configuration Register is always presented on A0-A15. CR0 is on A0, CR1 on A1, etc.; the other address bits are ignored.

### Block Lock Command

The Block Lock command is used to lock a block and prevent Program or Erase operations from changing the data in it. All blocks are locked at power-up or reset.

Two Bus Write cycles are required to issue the Block Lock command.

- The first bus cycle sets up the Block Lock command.
- The second Bus Write cycle latches the block address.

The lock status can be monitored for each block using the Read Electronic Signature command. Table. 13 shows the Lock Status after issuing a Block Lock command.

The Block Lock bits are volatile, once set they remain set until a hardware reset or power-down/power-up. They are cleared by a Block Unlock command. Refer to the section, Block Locking, for a detailed explanation. See Appendix C, Figure 27, Locking Operations Flowchart and Pseudo Code, for a flowchart for using the Lock command.

### Block Unlock Command

The Block Unlock command is used to unlock a block, allowing the block to be programmed or erased. Two Bus Write cycles are required to issue the Block Unlock command.

- The first bus cycle sets up the Block Unlock command.
- The second Bus Write cycle latches the block address.

The lock status can be monitored for each block using the Read Electronic Signature command. Table 13 shows the protection status after issuing a Block Unlock command. Refer to the section, Block Locking, for a detailed explanation and Appendix C, Figure 27, Locking Operations Flowchart and Pseudo Code, for a flowchart for using the Unlock command.

### Block Lock-Down Command

A locked or unlocked block can be locked-down by issuing the Block Lock-Down command. A locked-down block cannot be programmed or erased, or have its protection status changed when $\overline{WP}$ is low, $V_{IL}$. When $\overline{WP}$ is high, $V_{IH}$, the Lock-Down function is disabled and the locked blocks can be individually unlocked by the Block Unlock command.

Two Bus Write cycles are required to issue the Block Lock-Down command.

- The first bus cycle sets up the Block Lock command.

- The second Bus Write cycle latches the block address.

The lock status can be monitored for each block using the Read Electronic Signature command. Locked-Down blocks revert to the locked (and not locked-down) state when the device is reset on power-down. Table. 13 shows the Lock Status after issuing a Block Lock-Down command. Refer to the section, Block Locking, for a detailed explanation and Appendix C, Figure 27, Locking Operations Flowchart and Pseudo Code, for a flowchart for using the Lock-Down command.

**Table 5. Standard Commands**

| Commands | Cycles | Bus Operations | | | | | |
|---|---|---|---|---|---|---|---|
| | | 1st Cycle | | | 2nd Cycle | | |
| | | Op. | Add | Data | Op. | Add | Data |
| Read Array | 1+ | Write | BKA | FFh | Read | WA | RD |
| Read Status Register | 1+ | Write | BKA | 70h | Read | BKA(2) | SRD |
| Read Electronic Signature | 1+ | Write | BKA | 90h | Read | BKA(2) | ESD |
| Read CFI Query | 1+ | Write | BKA | 98h | Read | BKA(2) | QD |
| Clear Status Register | 1 | Write | BKA | 50h | | | |
| Block Erase | 2 | Write | BKA or BA(3) | 20h | Write | BA | D0h |
| Program | 2 | Write | BKA or WA(3) | 40h or 10h | Write | WA | PD |
| Program/Erase Suspend | 1 | Write | X | B0h | | | |
| Program/Erase Resume | 1 | Write | X | D0h | | | |
| Protection Register Program | 2 | Write | PRA | C0h | Write | PRA | PRD |
| Set Configuration Register | 2 | Write | CRD | 60h | Write | CRD | 03h |
| Block Lock | 2 | Write | BKA or BA(3) | 60h | Write | BA | 01h |
| Block Unlock | 2 | Write | BKA or BA(3) | 60h | Write | BA | D0h |
| Block Lock-Down | 2 | Write | BKA or BA(3) | 60h | Write | BA | 2Fh |

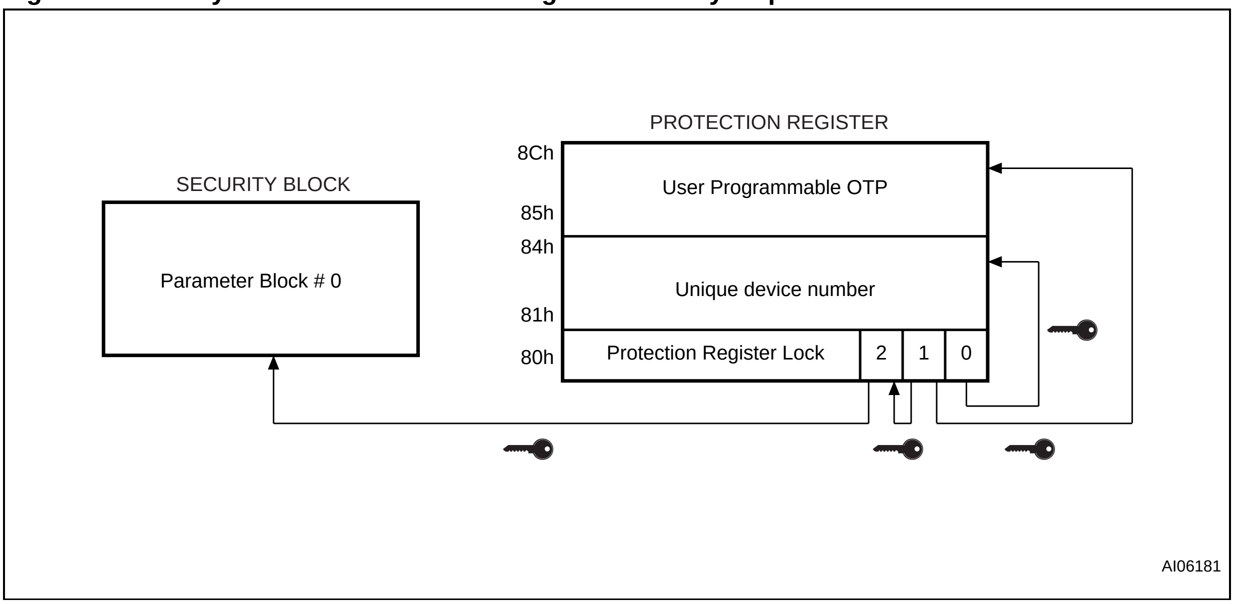
Note: 1. X = Don't Care, WA=Word Address in targeted bank, RD=Read Data, SRD=Status Register Data, ESD=Electronic Signature Data, QD=Query Data, BA=Block Address, BKA= Bank Address, PD=Program Data, PRA=Protection Register Address, PRD=Protection Register Data, CRD=Configuration Register Data.
2. Must be same bank as in the first cycle. The signature addresses are listed in Table 6.
3. Any address within the bank can be used.

**Table 6. Electronic Signature Codes**

| Code | | Address (h) | Data (h) |
|---|---|---|---|
| Manufacturer Code | | Bank Address + 00 | 0020 |
| Device Code | Top | Bank Address + 01 | 8810 |
| | Bottom | Bank Address + 01 | 8811 |
| Block Protection | Lock | Block Address + 02 | 0001 |
| | Unlocked | | 0000 |
| | Locked and Locked-Down | | 0003 |
| | Unlocked and Locked-Down | | 0002 |
| Reserved | | Bank Address + 03 | Reserved |
| Configuration Register | | Bank Address + 05 | CR |
| Protection Register Lock | ST Factory Default | Bank Address + 80 | 0006 |
| | Security Block Permanently Locked | | 0002 |
| | OTP Area Permanently Locked | | 0004 |
| | Security Block and OTP Area Permanently Locked | | 0000 |
| Protection Register | | Bank Address + 81<br>Bank Address + 84 | Unique Device Number |
| | | Bank Address + 85<br>Bank Address + 8C | OTP Area |

Note: CR=Configuration Register.

**Figure 5. Security Block and Protection Register Memory Map**



## COMMAND INTERFACE - FACTORY PROGRAM COMMANDS

The Factory Program commands are used to speed up programming. They require $V_{PP}$ to be at $V_{PPH}$ except for the Bank Erase command which also operates at $V_{PP} = V_{DD}$. Refer to Table 7, Factory Program Commands, in conjunction with the following text descriptions.

The use of Factory Program commands requires certain operating conditions.

- $V_{PP}$ must be set to $V_{PPH}$ (except for Bank Erase command),
- $V_{DD}$ must be within operating range,
- Ambient temperature, $T_A$ must be 25°C ± 5°C,
- The targeted block must be unlocked.

### Bank Erase Command

The Bank Erase command can be used to erase a bank. It sets all the bits within the selected bank to '1'. All previous data in the bank is lost. The Bank Erase command will ignore any protected blocks within the bank. If all blocks in the bank are protected then the Bank Erase operation will abort and the data in the bank will not be changed. The Status Register will not output any error.

Bank Erase operations can be performed at both $V_{PP} = V_{PPH}$ and $V_{PP} = V_{DD}$.

Two Bus Write cycles are required to issue the command.

- The first bus cycle sets up the Bank Erase command.
- The second latches the bank address in the internal state machine and starts the Program/ Erase Controller.

If the second bus cycle is not Write Bank Erase Confirm (D0h), Status Register bits SR4 and SR5 are set and the command aborts. Erase aborts if Reset turns to $V_{IL}$. As data integrity cannot be guaranteed when the Erase operation is aborted, the bank must be erased again.

Once the command is issued the device outputs the Status Register data when any address within the bank is read. At the end of the operation the bank will remain in Read Status Register mode until a Read Array, Read CFI Query or Read Electronic Signature command is issued.

During Bank Erase operations the bank being erased will only accept the Read Array, Read Status Register, Read Electronic Signature and Read CFI Query command, all other commands will be ignored.

For optimum performance, Bank Erase commands should be limited to a maximum of 100 Program/Erase cycles per Block. After 100 Program/ Erase cycles the internal algorithm will still operate properly but some degradation in performance may occur.

Dual operations are not supported during Bank Erase operations and the command cannot be suspended.

Typical Erase times are given in Table 14, Program, Erase Times and Program/Erase Endurance Cycles.

### Double Word Program Command

The Double Word Program command improves the programming throughput by writing a page of two adjacent words in parallel. The two words must differ only for the address A0.

Three bus write cycles are necessary to issue the Double Word Program command.

- The first bus cycle sets up the Double Word Program Command.
- The second bus cycle latches the Address and the Data of the first word to be written.
- The third bus cycle latches the Address and the Data of the second word to be written and starts the Program/Erase Controller.

Read operations in the bank being programmed output the Status Register content after the programming has started.

During Double Word Program operations the bank being programmed will only accept the Read Array, Read Status Register, Read Electronic Signature and Read CFI Query command, all other commands will be ignored. Dual operations are not supported during Double Word Program operations and the command cannot be suspended. Typical Program times are given in Table 14, Program, Erase Times and Program/Erase Endurance Cycles.

Programming aborts if Reset goes to $V_{IL}$. As data integrity cannot be guaranteed when the program operation is aborted, the memory locations must be reprogrammed.

See Appendix C, Figure 22, Double Word Program Flowchart and Pseudo Code, for the flowchart for using the Double Word Program command.

### Quadruple Word Program Command

The Quadruple Word Program command improves the programming throughput by writing a page of four adjacent words in parallel. The four words must differ only for the addresses A0 and A1.

Five bus write cycles are necessary to issue the Quadruple Word Program command.

- The first bus cycle sets up the Double Word Program Command.
- The second bus cycle latches the Address and the Data of the first word to be written.

- The third bus cycle latches the Address and the Data of the second word to be written.
- The fourth bus cycle latches the Address and the Data of the third word to be written.
- The fifth bus cycle latches the Address and the Data of the fourth word to be written and starts the Program/Erase Controller.

Read operations to the bank being programmed output the Status Register content after the programming has started.

Programming aborts if Reset goes to $V_{IL}$. As data integrity cannot be guaranteed when the program operation is aborted, the memory locations must be reprogrammed.

During Quadruple Word Program operations the bank being programmed will only accept the Read Array, Read Status Register, Read Electronic Signature and Read CFI Query command, all other commands will be ignored.

Dual operations are not supported during Quadruple Word Program operations and the command cannot be suspended. Typical Program times are given in Table 14, Program, Erase Times and Program/Erase Endurance Cycles.

See Appendix C, Figure 23, Quadruple Word Program Flowchart and Pseudo Code, for the flowchart for using the Quadruple Word Program command.

### Enhanced Factory Program Command

The Enhanced Factory Program command can be used to program large streams of data within any one block. It greatly reduces the total programming time when a large number of Words are written to a block at any one time.

Dual operations are not supported during the Enhanced Factory Program operation and the command cannot be suspended.

For optimum performance the Enhanced Factory Program commands should be limited to a maximum of 10 program/erase cycles per block. If this limit is exceeded the internal algorithm will continue to work properly but some degradation in performance is possible. Typical Program times are given in Table 14.

The Enhanced Factory Program command has four phases: the Setup Phase, the Program Phase to program the data to the memory, the Verify Phase to check that the data has been correctly programmed and reprogram if necessary and the Exit Phase. Refer to Table 7, Enhanced Factory Program Command and Figure 29, Enhanced Factory Program Flowchart.

**Setup Phase.** The Enhanced Factory Program command requires two Bus Write operations to initiate the command.

- The first bus cycle sets up the Enhanced Factory Program command.
- The second bus cycle confirms the command.

The Status Register P/E.C. Bit 7 should be read to check that the P/E.C. is ready. After the confirm command is issued, read operations output the Status Register data. The read Status Register command must not be issued as it will be interpreted as data to program.

**Program Phase.** The Program Phase requires n+1 cycles, where n is the number of Words (refer to Table 7, Enhanced Factory Program Command and Figure 29, Enhanced Factory Program Flowchart).

Three successive steps are required to issue and execute the Program Phase of the command.

1. Use one Bus Write operation to latch the Start Address and the first Word to be programmed. The Status Register Bank Write Status bit SR0 should be read to check that the P/E.C. is ready for the next Word.
2. Each subsequent Word to be programmed is latched with a new Bus Write operation. The address can either remain the Start Address, in which case the P/E.C. increments the address location or the address can be incremented in which case the P/E.C. jumps to the new address. If any address that is not in the same block as the Start Address is given with data FFFFh, the Program Phase terminates and the Verify Phase begins. The Status Register bit SR0 should be read between each Bus Write cycle to check that the P/E.C. is ready for the next Word.
3. Finally, after all Words have been programmed, write one Bus Write operation with data FFFFh to any address outside the block containing the Start Address, to terminate the programming phase. If the data is not FFFFh, the command is ignored.

The memory is now set to enter the Verify Phase.

**Verify Phase.** The Verify Phase is similar to the Program Phase in that all Words must be resent to the memory for them to be checked against the programmed data. The Program/Erase Controller checks the stream of data with the data that was programmed in the Program Phase and reprograms the memory location if necessary.

Three successive steps are required to execute the Verify Phase of the command.

1. Use one Bus Write operation to latch the Start Address and the first Word, to be verified. The Status Register bit SR0 should be read to check that the Program/Erase Controller is ready for the next Word.

2. Each subsequent Word to be verified is latched with a new Bus Write operation. The Words must be written in the same order as in the Program Phase. The address can remain the Start Address or be incremented. If any address that is not in the same block as the Start Address is given with data FFFFh, the Verify Phase terminates. Status Register bit SR0 should be read to check that the P/E.C. is ready for the next Word.
3. Finally, after all Words have been verified, write one Bus Write operation with data FFFFh to any address outside the block containing the Start Address, to terminate the Verify Phase.

If the Verify Phase is successfully completed the memory remains in Read Status Register mode. If the Program/Erase Controller fails to reprogram a given location, the error will be signaled in the Status Register.

**Exit Phase.** Status Register P/E.C. bit SR7 set to '1' indicates that the device has returned to Read mode. A full Status Register check should be done to ensure that the block has been successfully programmed. See the section on the Status Register for more details.

### Quadruple Enhanced Factory Program Command

The Quadruple Enhanced Factory Program command can be used to program one or more pages of four adjacent Words in parallel. The four Words must differ only for the addresses A0 and A1.

Dual operations are not supported during Quadruple Enhanced Factory Program operations and the command cannot be suspended.

The Quadruple Enhanced Factory Program command has four phases: the Setup Phase, the Load Phase where the data is loaded into the buffer, the combined Program and Verify Phase where the loaded data is programmed to the memory and then automatically checked and reprogrammed if necessary and the Exit Phase. Unlike the Enhanced Factory Program it is not necessary to resubmit the data for the Verify Phase. The Load Phase and the Program and Verify Phase can be repeated to program any number of pages within the block.

**Setup Phase.** The Quadruple Enhanced Factory Program command requires one Bus Write operation to initiate the load phase. After the setup command is issued, read operations output the Status Register data. The Read Status Register command must not be issued as it will be interpreted as data to program.

**Load Phase.** The Load Phase requires 4 cycles to load the data (refer to Table 7, Factory Program Commands and Figure 30, Quadruple Enhanced Factory Program Flowchart). Once the first Word of each Page is written it is impossible to exit the Load phase until all four Words have been written.

Two successive steps are required to issue and execute the Load Phase of the Quadruple Enhanced Factory Program command.

1. Use one Bus Write operation to latch the Start Address and the first Word of the first Page to be programmed. For subsequent Pages the first Word address can remain the Start Address (in which case the next Page is programmed) or can be any address in the same block. If any address with data FFFFh is given that is not in the same block as the Start Address, the device enters the Exit Phase. For the first Load Phase Status Register bit SR7 should be read after the first Word has been issued to check that the command has been accepted (bit SR7 set to '0'). This check is not required for subsequent Load Phases.
2. Each subsequent Word to be programmed is latched with a new Bus Write operation. The address is only checked for the first Word of each Page as the order of the Words to be programmed is fixed.

The memory is now set to enter the Program and Verify Phase.

**Program and Verify Phase.** In the Program and Verify Phase the four Words that were loaded in the Load Phase are programmed in the memory array and then verified by the Program/Erase Controller. If any errors are found the Program/Erase Controller reprograms the location. During this phase the Status Register shows that the Program/Erase Controller is busy, Status Register bit SR7 set to '0', and that the device is not waiting for new data, Status Register bit SR0 set to '1'. When Status Register bit SR0 is set to '0' the Program and Verify phase has terminated.

Once the Verify Phase has successfully completed subsequent pages in the same block can be loaded and programmed. The device returns to the beginning of the Load Phase by issuing one Bus Write operation to latch the Address and the first of the four new Words to be programmed.

**Exit Phase.** Finally, after all the pages have been programmed, write one Bus Write operation with data FFFFh to any address outside the block containing the Start Address, to terminate the Load and Program and Verify Phases.

Status Register bit SR7 set to '1' and bit SR0 set to '0' indicate that the Quadruple Enhanced Factory Program command has terminated. A full Status Register check should be done to ensure that the block has been sucessfully programmed. See the section on the Status Register for more details.

If the Program and Verify Phase has successfully completed the memory returns to Read mode. If the P/E.C. fails to program and reprogram a given location, the error will be signaled in the Status Register.

**Table 7. Factory Program Commands**

| Command | Phase | Cycles | Bus Write Operations | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 1st | | 2nd | | 3rd | | Final -1 | | Final | |
| | | | Add | Data | Add | Data | Add | Data | Add | Data | Add | Data |
| Bank Erase | | 2 | BKA | 80h | BKA | D0h | | | | | | |
| Double Word Program(4) | | 3 | BKA or WA1(8) | 35h | WA1 | PD1 | WA2 | PD2 | | | | |
| Quadruple Word Program(5) | | 5 | BKA or WA1(8) | 56h | WA1 | PD1 | WA2 | PD2 | WA3 | PD3 | WA4 | PD4 |
| Enhanced Factory Program (6) | Setup, Program | 2+ n+1 | BKA or WA1(8) | 30h | BA or WA1(9) | D0h | WA1(2) | PD1 | WAn(3) | PAn | NOT WA1(2) | FFFFh |
| | Verify, Exit | n+1 | WA1(2) | PD1 | WA2(3) | PD2 | WA3(3) | PD3 | WAn(3) | PAn | NOT WA1(2) | FFFFh |
| Quadruple Enhanced Factory Program (5,6) | Setup, first Load | 5 | BKA or WA1(8) | 75h | WA1(2) | PD1 | WA2(7) | PD2 | WA3(7) | PD3 | WA4(7) | PD4 |
| | First Program & Verify | | Automatic | | | | | | | | | |
| | Subsequent Loads | 4 | WA1i (2) | PD1i | WA2i (7) | PD2i | WA3i (7) | PD3i | | | WA4i (7) | PD4i |
| | Subsequent Program & Verify | | Automatic | | | | | | | | | |
| | Exit | 1 | NOT WA1 (2) | FFFFh | | | | | | | | |

Note: 1. WA=Word Address in targeted bank, BKA= Bank Address, PD=Program Data, BA=Block Address.
2. WA1 is the Start Address. NOT WA1 is any address that is not in the same block as WA1.
3. Address can remain Starting Address WA1 or be incremented.
4. Word Addresses 1 and 2 must be consecutive Addresses differing only for A0.
5. Word Addresses 1,2,3 and 4 must be consecutive Addresses differing only for A0 and A1.
6. A Bus Read must be done between each Write cycle where the data is programmed or verified to read the Status Register and check that the memory is ready to accept the next data. n = number of Words, i = number of Pages to be programmed.
7. Address is only checked for the first Word of each Page as the order to program the Words in each page is fixed so subsequent Words in each Page can be written to any address.
8. Any address within the bank can be used.
9. Any address within the block can be used.

## STATUS REGISTER

The Status Register provides information on the current or previous Program or Erase operations. Issue a Read Status Register command to read the contents of the Status Register, refer to Read Status Register Command section for more details. To output the contents, the Status Register is latched and updated on the falling edge of the Chip Enable or Output Enable signals and can be read until Chip Enable or Output Enable returns to $V_{IH}$. The Status Register can only be read using single asynchronous or single synchronous reads. Bus Read operations from any address within the bank, always read the Status Register during Program and Erase operations.

The various bits convey information about the status and any errors of the operation. Bits SR7, SR6, SR2 and SR0 give information on the status of the device and are set and reset by the device. Bits SR5, SR4, SR3 and SR1 give information on errors, they are set by the device but must be reset by issuing a Clear Status Register command or a hardware reset. If an error bit is set to ‘1’ the Status Register should be reset before issuing another command. SR7 to SR1 refer to the status of the device while SR0 refers to the status of the addressed bank.

The bits in the Status Register are summarized in Table 8, Status Register Bits. Refer to Table 8 in conjunction with the following text descriptions.

**Program/Erase Controller Status Bit (SR7).** The Program/Erase Controller Status bit indicates whether the Program/Erase Controller is active or inactive in any bank. When the Program/Erase Controller Status bit is Low (set to ‘0’), the Program/Erase Controller is active; when the bit is High (set to ‘1’), the Program/Erase Controller is inactive, and the device is ready to process a new command.

The Program/Erase Controller Status is Low immediately after a Program/Erase Suspend command is issued until the Program/Erase Controller pauses. After the Program/Erase Controller pauses the bit is High.

During Program, Erase, operations the Program/ Erase Controller Status bit can be polled to find the end of the operation. Other bits in the Status Register should not be tested until the Program/Erase Controller completes the operation and the bit is High.

After the Program/Erase Controller completes its operation the Erase Status, Program Status, $V_{PP}$ Status and Block Lock Status bits should be tested for errors.

**Erase Suspend Status Bit (SR6).** The Erase Suspend Status bit indicates that an Erase operation has been suspended or is going to be suspended in the addressed block. When the Erase Suspend Status bit is High (set to ‘1’), a Program/ Erase Suspend command has been issued and the memory is waiting for a Program/Erase Resume command.

The Erase Suspend Status should only be considered valid when the Program/Erase Controller Status bit is High (Program/Erase Controller inactive). SR7 is set within the Erase Suspend Latency time of the Program/Erase Suspend command being issued therefore the memory may still complete the operation rather than entering the Suspend mode.

When a Program/Erase Resume command is issued the Erase Suspend Status bit returns Low.

**Erase Status Bit (SR5).** The Erase Status bit can be used to identify if the memory has failed to verify that the block or bank has erased correctly. When the Erase Status bit is High (set to ‘1’), the Program/Erase Controller has applied the maximum number of pulses to the block or bank and still failed to verify that it has erased correctly. The Erase Status bit should be read once the Program/ Erase Controller Status bit is High (Program/Erase Controller inactive).

Once set High, the Erase Status bit can only be reset Low by a Clear Status Register command or a hardware reset. If set High it should be reset before a new Program or Erase command is issued, otherwise the new command will appear to fail.

**Program Status Bit (SR4).** The Program Status bit is used to identify a Program failure or an attempt to program a ‘1’ to an already programmed bit when $V_{PP} = V_{PPH}$.

When the Program Status bit is High (set to ‘1’), the Program/Erase Controller has applied the maximum number of pulses to the byte and still failed to verify that it has programmed correctly.

After an attempt to program a '1' to an already programmed bit, the Program Status bit SR4 only goes High (set to '1') if $V_{PP} = V_{PPH}$ (if $V_{PP}$ is different from $V_{PPH}$, SR4 remains Low (set to '0') and the attempt is not shown).

The Program Status bit should be read once the Program/Erase Controller Status bit is High (Program/Erase Controller inactive).

Once set High, the Program Status bit can only be reset Low by a Clear Status Register command or a hardware reset. If set High it should be reset before a new command is issued, otherwise the new command will appear to fail.

**$V_{PP}$ Status Bit (SR3).** The $V_{PP}$ Status bit can be used to identify an invalid voltage on the $V_{PP}$ pin during Program and Erase operations. The $V_{PP}$ pin is only sampled at the beginning of a Program or Erase operation. Indeterminate results can occur if $V_{PP}$ becomes invalid during an operation.

When the $V_{PP}$ Status bit is Low (set to ‘0’), the voltage on the $V_{PP}$ pin was sampled at a valid voltage; when the $V_{PP}$ Status bit is High (set to ‘1’), the $V_{PP}$ pin has a voltage that is below the $V_{PP}$ Lockout Voltage, $V_{PPLK}$, the memory is protected and Program and Erase operations cannot be performed.

Once set High, the $V_{PP}$ Status bit can only be reset Low by a Clear Status Register command or a hardware reset. If set High it should be reset before a new Program or Erase command is issued, otherwise the new command will appear to fail.

**Program Suspend Status Bit (SR2).** The Program Suspend Status bit indicates that a Program operation has been suspended in the addressed block. When the Program Suspend Status bit is High (set to ‘1’), a Program/Erase Suspend command has been issued and the memory is waiting for a Program/Erase Resume command. The Program Suspend Status should only be considered valid when the Program/Erase Controller Status bit is High (Program/Erase Controller inactive). SR2 is set within the Program Suspend Latency time of the Program/Erase Suspend command being issued therefore the memory may still complete the operation rather than entering the Suspend mode.

When a Program/Erase Resume command is issued the Program Suspend Status bit returns Low.

**Block Protection Status Bit (SR1).** The Block Protection Status bit can be used to identify if a Program or Block Erase operation has tried to modify the contents of a locked block.

When the Block Protection Status bit is High (set to ‘1’), a Program or Erase operation has been attempted on a locked block.

Once set High, the Block Protection Status bit can only be reset Low by a Clear Status Register command or a hardware reset. If set High it should be reset before a new command is issued, otherwise the new command will appear to fail.

**Bank Write/Multiple Word Program Status Bit (SR0).** The Bank Write Status bit indicates whether the addressed bank is programming or erasing. In Enhanced Factory Program mode the Multiple Word Program bit shows if a Word has finished programming or verifying depending on the phase. The Bank Write Status bit should only be considered valid when the Program/Erase Controller Status SR7 is Low (set to ‘0’).

When both the Program/Erase Controller Status bit and the Bank Write Status bit are Low (set to ‘0’), the addressed bank is executing a Program or Erase operation. When the Program/Erase Controller Status bit is Low (set to ‘0’) and the Bank Write Status bit is High (set to ‘1’), a Program or Erase operation is being executed in a bank other than the one being addressed.

In Enhanced Factory Program mode if Multiple Word Program Status bit is Low (set to ‘0’), the device is ready for the next Word, if the Multiple Word Program Status bit is High (set to ‘1’) the device is not ready for the next Word.

Note: Refer to Appendix C, Flowcharts and Pseudo Codes, for using the Status Register.

**Table 8. Status Register Bits**

| Bit | Name | Type | Logic Level | Definition | |
|---|---|---|---|---|---|
| SR7 | P/E.C. Status | Status | ’1’ | Ready | |
| | | | ’0’ | Busy | |
| SR6 | Erase Suspend Status | Status | ’1’ | Erase Suspended | |
| | | | ’0’ | Erase In progress or Completed | |
| SR5 | Erase Status | Error | ’1’ | Erase Error | |
| | | | ’0’ | Erase Success | |
| SR4 | Program Status | Error | ’1’ | Program Error | |
| | | | ’0’ | Program Success | |
| SR3 | $V_{PP}$ Status | Error | ’1’ | $V_{PP}$ Invalid, Abort | |
| | | | ’0’ | $V_{PP}$ OK | |
| SR2 | Program Suspend Status | Status | ’1’ | Program Suspended | |
| | | | ’0’ | Program In Progress or Completed | |
| SR1 | Block Protection Status | Error | ’1’ | Program/Erase on protected Block, Abort | |
| | | | ’0’ | No operation to protected blocks | |
| SR0 | Bank Write Status | Status | ’0’ | SR7 = ‘0’ | Program or erase operation in addressed bank |
| | | | | SR7 = ‘1’ | No Program or erase operation in the device |
| | | | ’1’ | SR7 = ‘0’ | Program or erase operation in a bank other than the addressed bank |
| | | | | SR7 = ‘1’ | Not Allowed |
| | Multiple Word Program Status (Enhanced Factory Program mode) | Status | ’1’ | SR7 = ‘0’ | the device is NOT ready for the next word |
| | | | | SR7 = ‘1’ | Not Allowed |
| | | | ’0’ | SR7 = ‘0’ | the device is ready for the next Word |
| | | | | SR7 = ‘1’ | the device is exiting from EFP |

Note: Logic level ’1’ is High, ’0’ is Low.

## CONFIGURATION REGISTER

The Configuration Register is used to configure the type of bus access that the memory will perform. Refer to Read Modes section for details on read operations.

The Configuration Register is set through the Command Interface. After a Reset or Power-Up the device is configured for asynchronous page read (CR15 = 1). The Configuration Register bits are described in Table 9. They specify the selection of the burst length, burst type, burst X latency and the Read operation. Refer to Figures 6 and 7 for examples of synchronous burst configurations.

### Read Select Bit (CR15)

The Read Select bit, CR15, is used to switch between asynchronous and synchronous Bus Read operations. When the Read Select bit is set to ’1’, read operations are asynchronous; when the Read Select bit is set to ’0’, read operations are synchronous. Synchronous Burst Read is supported in both parameter and main blocks and can be performed across banks.

On reset or power-up the Read Select bit is set to’1’ for asynchronous access.

### X-Latency Bits (CR13-CR11)

The X-Latency bits are used during Synchronous Read operations to set the number of clock cycles between the address being latched and the first data becoming available. For correct operation the X-Latency bits can only assume the values in Table 9, Configuration Register.

The correspondence between X-Latency settings and the maximum sustainable frequency must be calculated taking into account some system parameters. Two conditions must be satisfied:

1. Depending on whether $t_{AVK\_CPU}$ or $t_{DELAY}$ is supplied either one of the following two equations must be satisfied:

   $(n + 1)\ t_K \geq t_{ACC} - t_{AVK\_CPU} + t_{QVK\_CPU}$

   $(n + 2)\ t_K \geq t_{ACC} + t_{DELAY} + t_{QVK\_CPU}$

2. and also

   $t_K > t_{KQV} + t_{QVK\_CPU}$

where

n is the chosen X-Latency configuration code

$t_K$ is the clock period

$t_{AVK\_CPU}$ is clock to address valid, $\overline{L}$ Low, or $\overline{E}$ Low, whichever occurs last

$t_{DELAY}$ is address valid, $\overline{L}$ Low, or $\overline{E}$ Low to clock, whichever occurs last

$t_{QVK\_CPU}$ is the data setup time required by the system CPU,

$t_{KQV}$ is the clock to data valid time

$t_{ACC}$ is the random access time of the device.

Refer to Figure 6, X-Latency and Data Output Configuration Example.

### Wait Polarity Bit (CR10)

In synchronous burst mode the Wait signal indicates whether the output data are valid or a WAIT state must be inserted. The Wait Polarity bit is used to set the polarity of the Wait signal. When the Wait Polarity bit is set to ‘0’ the Wait signal is active Low. When the Wait Polarity bit is set to ‘1’ the Wait signal is active High (default).

### Data Output Configuration Bit (CR9)

The Data Output Configuration bit determines whether the output remains valid for one or two clock cycles. When the Data Output Configuration Bit is ’0’ the output data is valid for one clock cycle, when the Data Output Configuration Bit is ’1’ the output data is valid for two clock cycles.

The Data Output Configuration depends on the condition:

- $t_K > t_{KQV} + t_{QVK\_CPU}$

where $t_K$ is the clock period, $t_{QVK\_CPU}$ is the data setup time required by the system CPU and $t_{KQV}$ is the clock to data valid time. If this condition is not satisfied, the Data Output Configuration bit should be set to ‘1’ (two clock cycles). Refer to Figure 6, X-Latency and Data Output Configuration Example.

### Wait Configuration Bit (CR8)

In burst mode the Wait bit controls the timing of the Wait output pin, WAIT. When WAIT is asserted, Data is Not Valid and when WAIT is deasserted, Data is Valid. When the Wait bit is ’0’ the Wait output pin is asserted during the wait state. When the Wait bit is ’1’ (default) the Wait output pin is asserted one clock cycle before the wait state.

### Burst Type Bit (CR7)

The Burst Type bit is used to configure the sequence of addresses read as sequential or interleaved. When the Burst Type bit is ’0’ the memory outputs from interleaved addresses; when the Burst Type bit is ’1’ (default) the memory outputs from sequential addresses. See Tables 10, Burst Type Definition, for the sequence of addresses output from a given starting address in each mode.

### Valid Clock Edge Bit (CR6)

The Valid Clock Edge bit, CR6, is used to configure the active edge of the Clock, K, during Synchronous Burst Read operations. When the Valid Clock Edge bit is ’0’ the falling edge of the Clock is the active edge; when the Valid Clock Edge bit is ’1’ the rising edge of the Clock is active.

### Wrap Burst Bit (CR3)

The burst reads can be confined inside the 4 or 8 Word boundary (wrap) or overcome the boundary