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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
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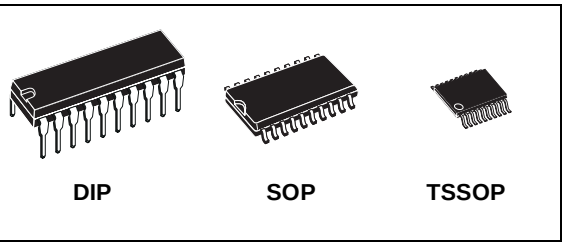
M74HC299

8 BIT PIPO SHIFT REGISTER WITH ASYNCHRONOUS CLEAR

- HIGH SPEED :
  f_{MAX} = 80MHz (TYP.) at V_{CC} = 6V
- LOW POWER DISSIPATION:
  I_{CC} =4μA(MAX.) at T_A=25°C
- HIGH NOISE IMMUNITY:
  $V_{NIH} = V_{NIL}$ = 28 % V_{CC} (MIN.)
- SYMMETRICAL OUTPUT IMPEDANCE:
  $|I_{OH}| = I_{OL}$ = 6mA (MIN) FOR QA' TO QH'
  $|I_{OH}| = I_{OL}$ = 4mA (MIN) FOR QA TO QH
- BALANCED PROPAGATION DELAYS:
  $t_{PLH} \cong t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE:
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 299



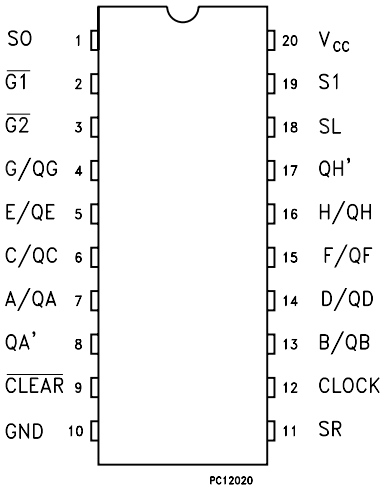
ORDER CODES

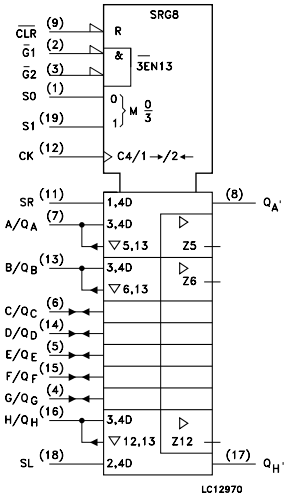
PACKAGE	TUBE	T & R
DIP	M74HC299B1R	
SOP	M74HC299M1R	M74HC299RM13TR
TSSOP		M74HC299TTR

DESCRIPTION

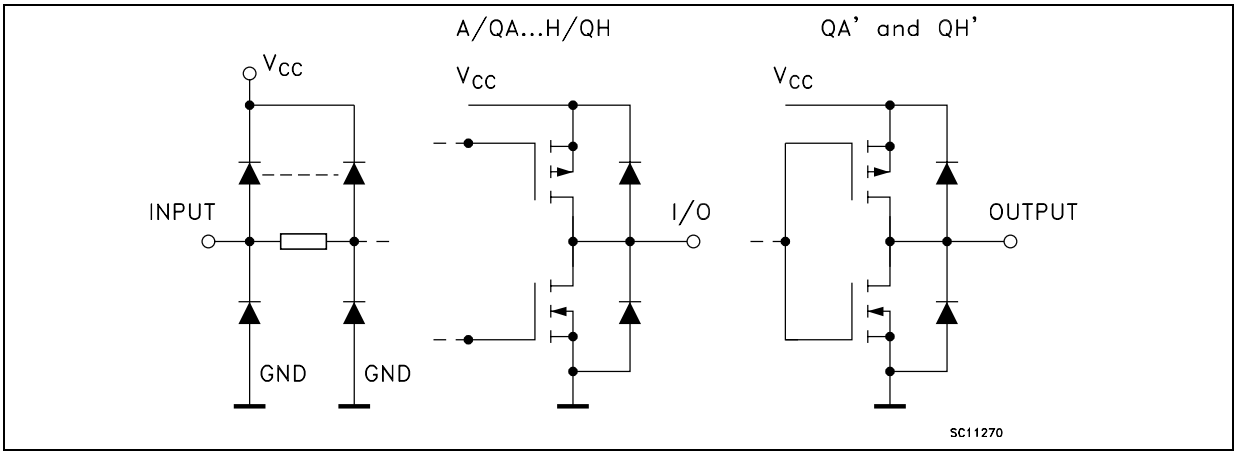
The M74HC299 is an high speed CMOS 8 BIT PIPO SHIFT REGISTER (3-STATE) fabricated with silicon gate C^2MOS technology.
This device has four modes (HOLD, SHIFT LEFT, SHIFT RIGHT and LOAD DATA). Each mode is chosen by two function select inputs ($\overline{S0}$, S1). When one or both enable inputs, ($\overline{G1}$, $\overline{G2}$) are high, the eight input/output terminals are in the high impedance state; however sequential operation or clearing of the register is not affected. Clear function on the M74HC299 is asynchronous to CLOCK.
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

PIN CONNECTION AND IEC LOGIC SYMBOLS





IINPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

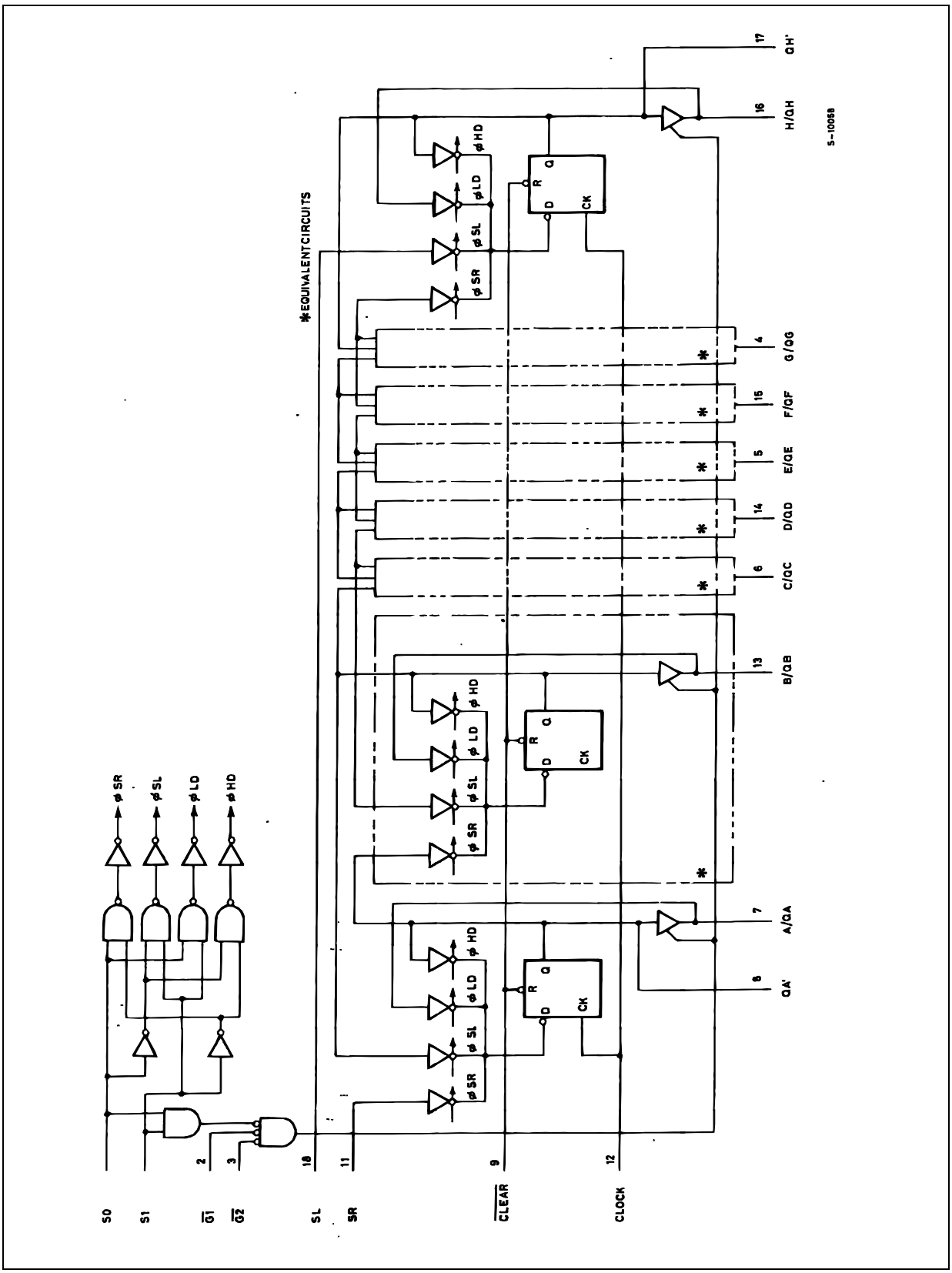
PIN No	SYMBOL	NAME AND FUNCTION
1, 19	$\overline{S0}$, $\overline{S1}$	Mode Select Inputs
2, 3	$\overline{G1}$, $\overline{G2}$	3-State Output Enable Inputs (Active LOW)
7, 13, 6, 14, 5, 15, 4, 16	A/QA to H/QH	Parallel Data Inputs or 3-State Parallel Outputs (Bus Driver)
8, 17	QA' to QH'	Serial Outputs (Standard Output)
9	$\overline{CLEAR}$	Asynchronous Master Reset Input (Active LOW)
11	SR	Serial Data Shift Right Input
12	CLOCK	Clock Input (LOW to HIGH, Edge-triggered)
18	SL	Serial Data Shift Left Input
10	GND	Ground (0V)
20	V_{CC}	Positive Supply Voltage

TRUTH TABLE

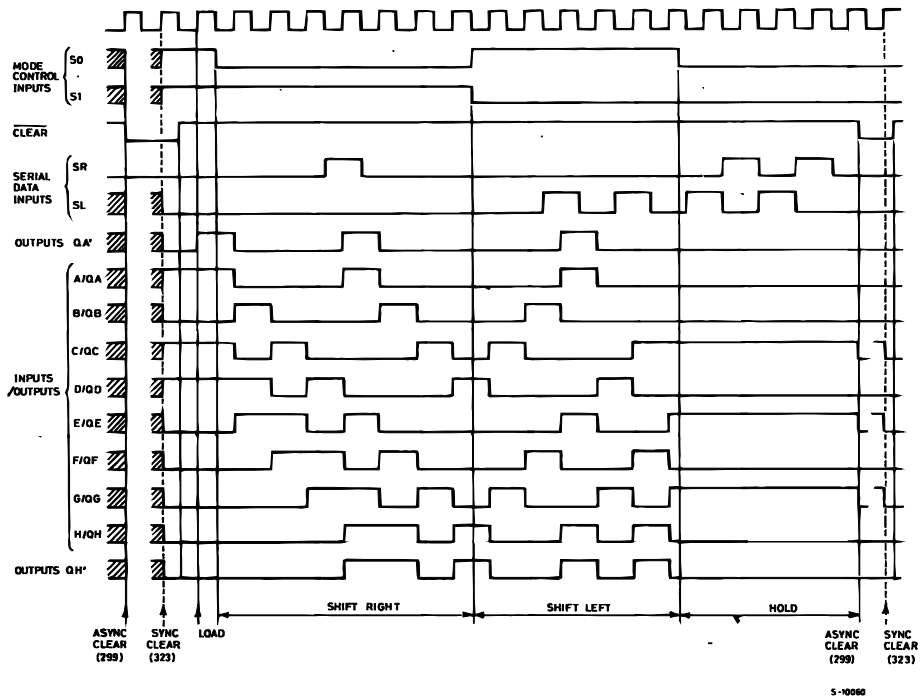
MODE	INPUTS						INPUTS/OUTPUTS				OUTPUTS	
	$\overline{CLEAR}$	FUNCTION SELECTED		OUTPUT CONTROL		CLOCK	SERIAL		A/QA	H/QH	QA'	QH'
		S1	S0	$\overline{G1}$*	$\overline{G2}$*		SL	SR				
Z	L	H	H	X	X	X	X	X	Z	Z	L	L
CLEAR	L	L	X	L	L	X	X	X	L	L	L	L
	L	X	L	L	L	X	X	X	L	L	L	L
HOLD	H	L	L	L	L	X	X	X	QA0	QH0	QA0	QH0
SHIFT RIGHT	H	L	H	L	L	⌐	X	H	H	QGn	H	QGn
	H	L	H	L	L	⌐	X	L	L	QGn	L	QGn
SHIFT LEFT	H	H	L	L	L	⌐	H	X	QBn	H	QBn	H
	H	H	L	L	L	⌐	L	X	QBn	L	QBn	L
LOAD	H	H	H	X	X	⌐	X	X	a	h	a	h

* When one or both output controls are high, the eight input/output terminals are in the high impedance state: however sequential operation or clearing of the register is not affected.
Z : High Impedance
Qn0 : The level of An before the indicated steady state input conditions were established.
Qnn : The level of Qn before the most recent active transition indicated by ⌐ OR ⌐
a, h : The level of the steady state inputs A, H, respectively.
X : Don't Care

LOGIC DIAGRAM



TIMING CHART



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin (QA-QH)	± 35	mA
I_O	DC Output Source Sink Current Per Output Pin (QA'-QH')	± 235	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 70	mA
P_D	Power Dissipation	500(*)	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not t implied
(*) 500mW at 65 °C; derate to 300mW by 10mW/°C from 65°C to 85°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature		-55 to 125	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2.0V	0 to 1000	ns
		V_{CC} = 4.5V	0 to 500	ns
		V_{CC} = 6.0V	0 to 400	ns

DC SPECIFICATIONS

Symbol	Parameter	Test Condition		Value							Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0		1.5			1.5		1.5		V
		4.5		3.15			3.15		3.15		
		6.0		4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0				0.5		0.5		0.5	V
		4.5				1.35		1.35		1.35	
		6.0				1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5	I_O=-20 µA	4.4	4.5		4.4		4.4		
		6.0	I_O=-20 µA	5.9	6.0		5.9		5.9		
	QA to QH	4.5	I_O=-6.0 mA	4.18	4.31		4.13		4.10		
		6.0	I_O=-7.8 mA	5.68	5.8		5.63		5.60		
	QA' to QH'	4.5	I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0	I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	I_O=20 µA		0.0	0.1		0.1		0.1	V
		4.5	I_O=20 µA		0.0	0.1		0.1		0.1	
		6.0	I_O=20 µA		0.0	0.1		0.1		0.1	
	QA to QH	4.5	I_O=6.0 mA		0.17	0.26		0.33		0.40	
		6.0	I_O=7.8 mA		0.18	0.26		0.33		0.40	
	QA' to QH'	4.5	I_O=4.0 mA		0.17	0.26		0.33		0.40	
		6.0	I_O=5.2 mA		0.18	0.26		0.33		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND			± 0.1		± 1		± 1	µA
I_{OZ}	High Impedance Output Leakage Current	6.0	V_I = V_{IH} or V_{IL} V_O = V_{CC} or GND			± 0.5		± 5		± 10	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND			4		40		80	µA

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6ns)

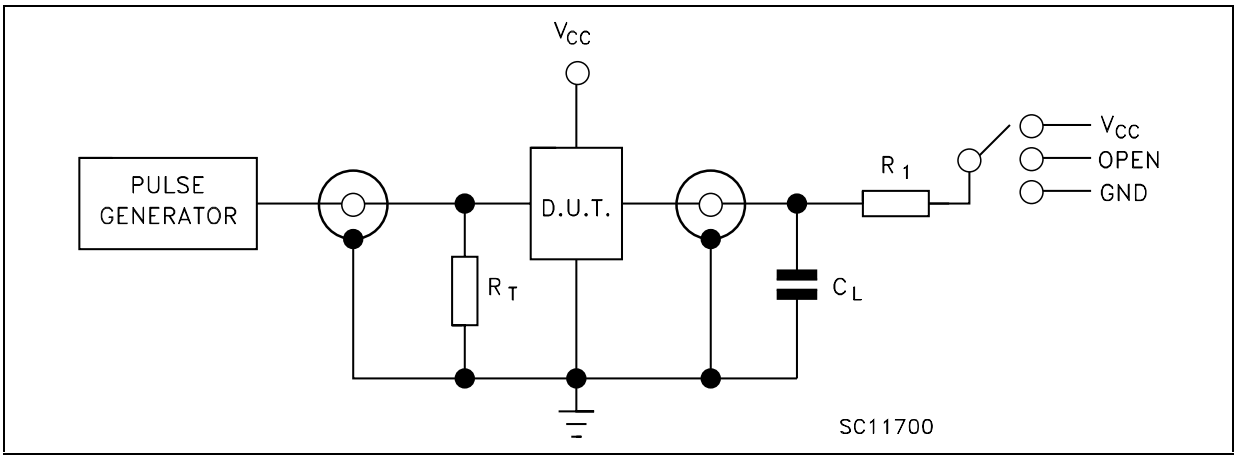
Symbol	Parameter	Test Condition			Value							Unit
		V_{CC} (V)			T_A = 25°C			-40 to 85°C		-55 to 125°C		
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time (QA, QH)	2.0	50			25	60		75		90	ns
		4.5				7	12		15		18	
		6.0				6	10		13		15	
t_{TLH} t_{THL}	Output Transition Time (QA', QH')	2.0	50			30	75		95		110	ns
		4.5				8	15		19		22	
		6.0				7	13		16		19	
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK - QA', QH')	2.0	50			85	170		215		255	ns
		4.5				23	34		43		51	
		6.0				18	29		37		43	
t_{PHL}	Propagation Delay Time (CLEAR - QA', QH')	2.0	50			85	175		220		265	ns
		4.5				24	35		44		53	
		6.0				18	30		37		45	
t_{PLH} t_{PHL}	Propagation Delay Time (CLOCK - QA, QH)	2.0	50			80	160		200		240	ns
		4.5				21	32		40		48	
		6.0				17	27		34		41	
		2.0	150			100	200		250		300	ns
		4.5				26	40		50		60	
		6.0				21	34		43		51	
t_{PZL} t_{PZH}	High Impedance Output Enable Time	2.0	50	R_L = 1 KΩ		60	130		165		195	ns
		4.5				17	26		33		39	
		6.0				13	22		28		33	
		2.0	150	R_L = 1 KΩ		78	170		15		255	ns
		4.5				23	34		43		51	
		6.0				17	29		37		43	
t_{PLZ} t_{PHZ}	High Impedance Output Disable Time	2.0	50	R_L = 1 KΩ		54	150		190		225	ns
		4.5				19	30		38		45	
		6.0				16	26		32		38	
f_{MAX}	Maximum Clock Frequency	2.0	50		6	12		4.8		4		MHz
		4.5			30	58		24		20		
		6.0			35	80		28		24		
$t_{W(L)}$ $t_{W(H)}$	Minimum Pulse Width (CLOCK)	2.0	50				75		95		110	ns
		4.5					15		19		22	
		6.0					13		16		19	
$t_{W(L)}$	Minimum Pulse Width (CLEAR)	2.0	50				75		95		110	ns
		4.5					15		19		22	
		6.0					13		16		19	
t_s	Minimum Set-up Time (S0, S1) (SL, SR, A, H)	2.0	50				100		125		150	ns
		4.5					20		25		30	
		6.0					17		21		26	
t_h	Minimum Hold Time (S0, S1) (SL, SR, A, H)	2.0	50				0		0		0	ns
		4.5					0		0		0	
		6.0					0		0		0	
t_{REM}	Minimum Removal Time (CLEAR)	2.0	50				50		65		75	ns
		4.5					10		13		15	
		6.0					9		11		13	

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Condition		Value							Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
C_{IN}	Input Capacitance	5.0			5	10		10		10	pF
C_{PD}	Power Dissipation Capacitance (note 1)	5.0			170						pF

1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}$

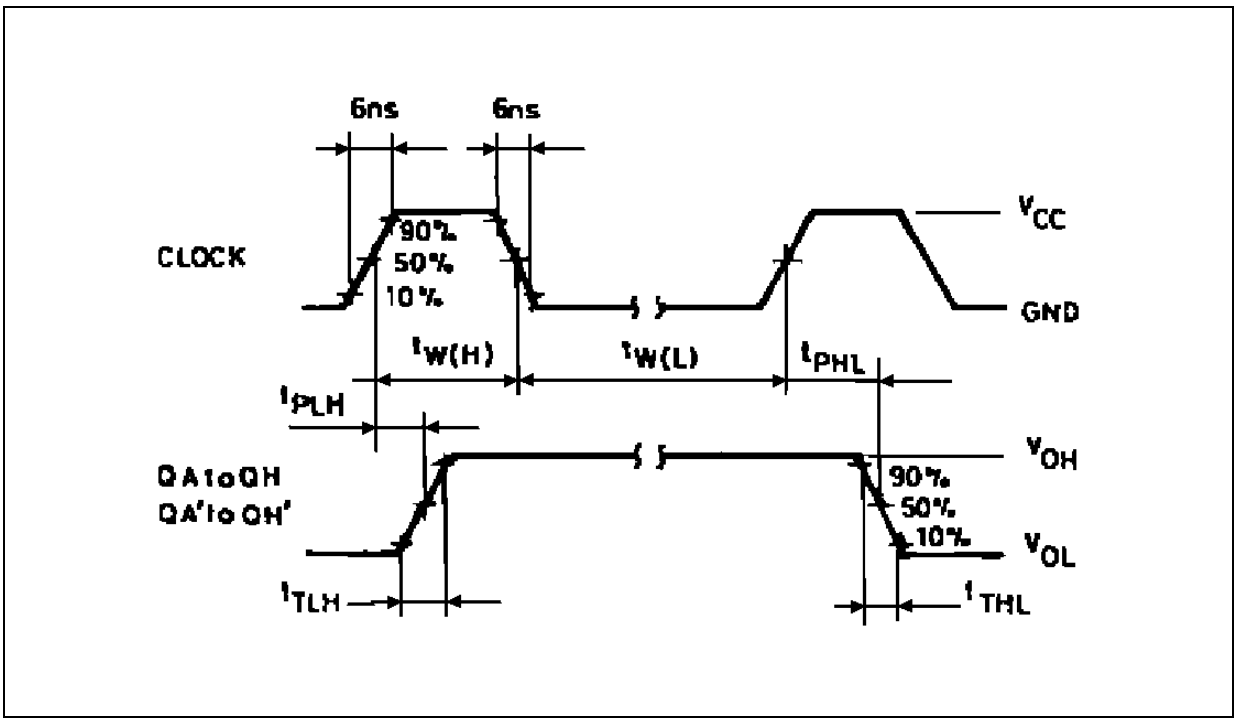
TEST CIRCUIT



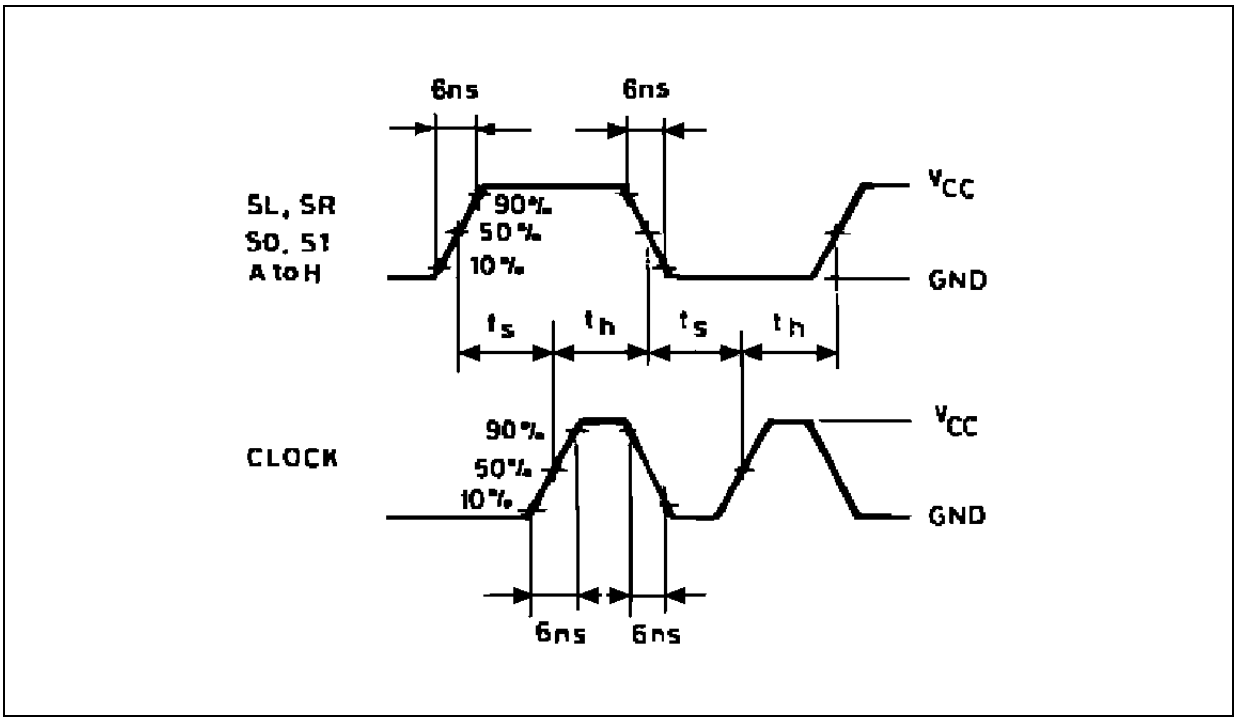
TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	V_{CC}
t_{PZH}, t_{PHZ}	GND

C_L = 50pF/150pF or equivalent (includes jig and probe capacitance)
R_1 = 1KΩ or equivalent
R_T = Z_{OUT} of pulse generator (typically 50Ω)

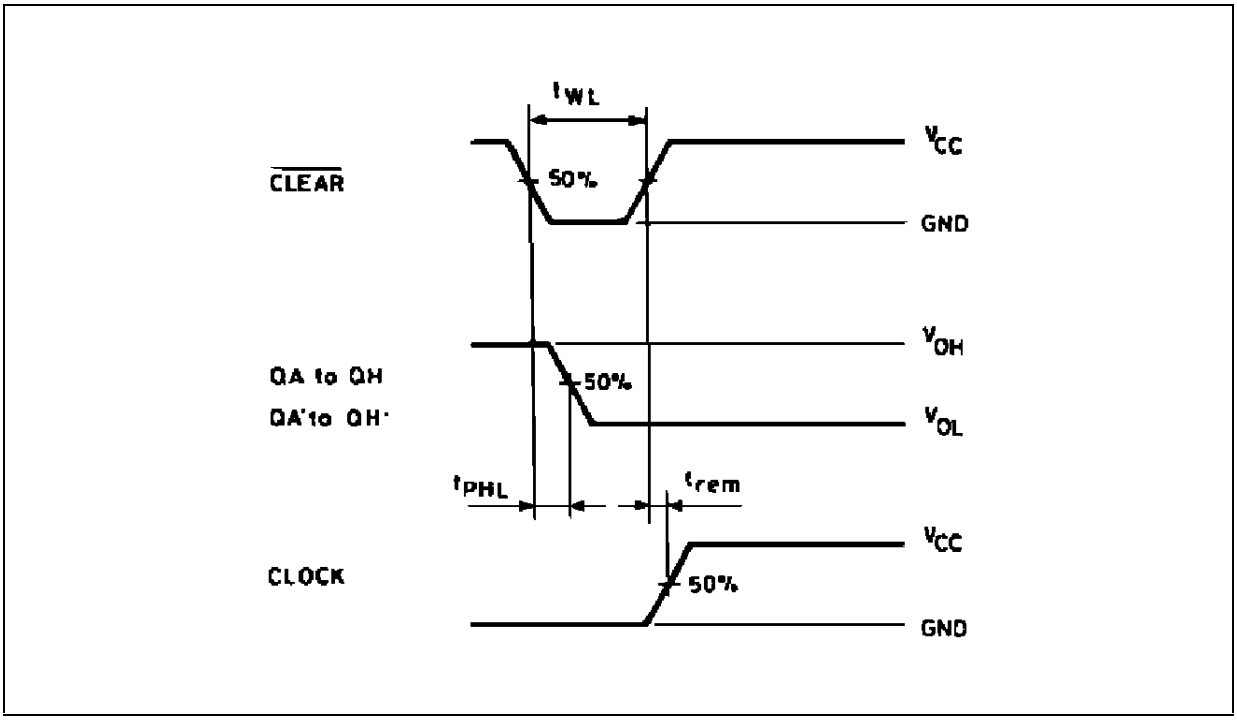
WAVEFORM 1: PROPAGATION DELAY TIMES, MINIMUM PULSE WIDTH (f=1MHz; 50% duty cycle)



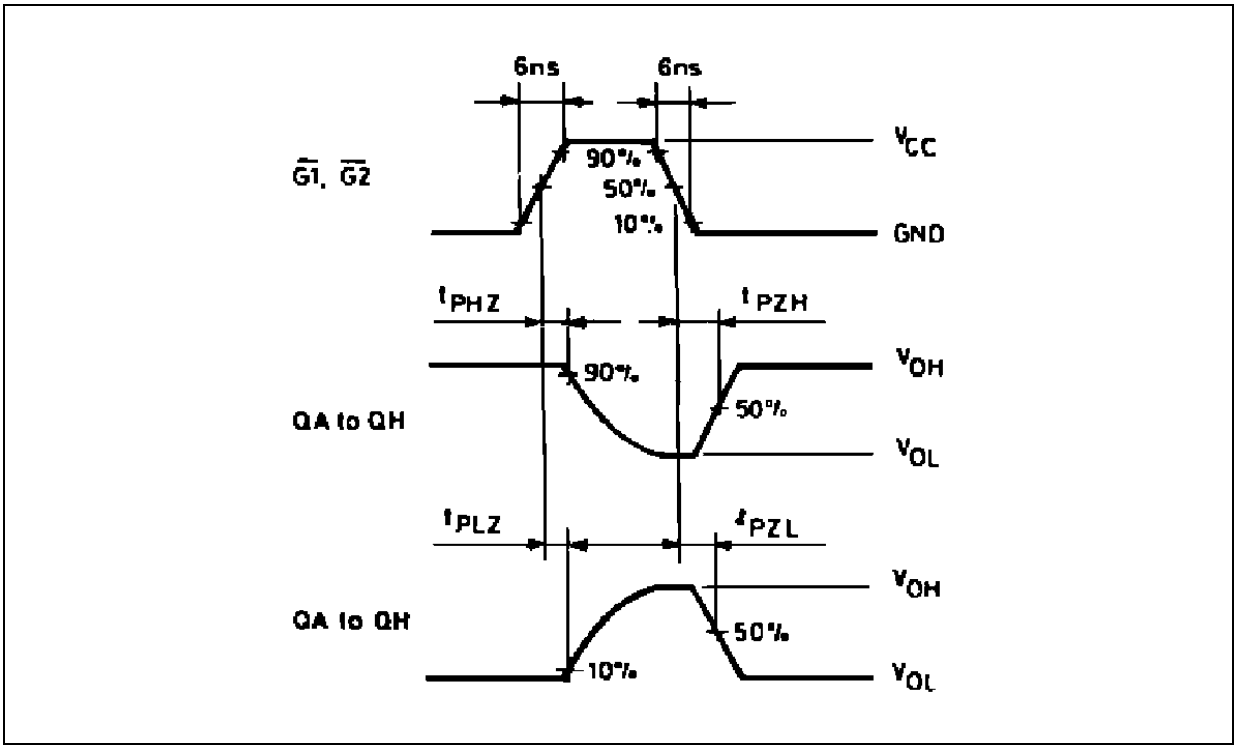
WAVEFORM 2 : SETUP AND HOLD TIMES (f=1MHz; 50% duty cycle)



WAVEFORM 3 :PROPAGATION DELAY AND REMOVAL TIME, MINIMUM PULSE WIDTH
(f=1MHz; 50% duty cycle)

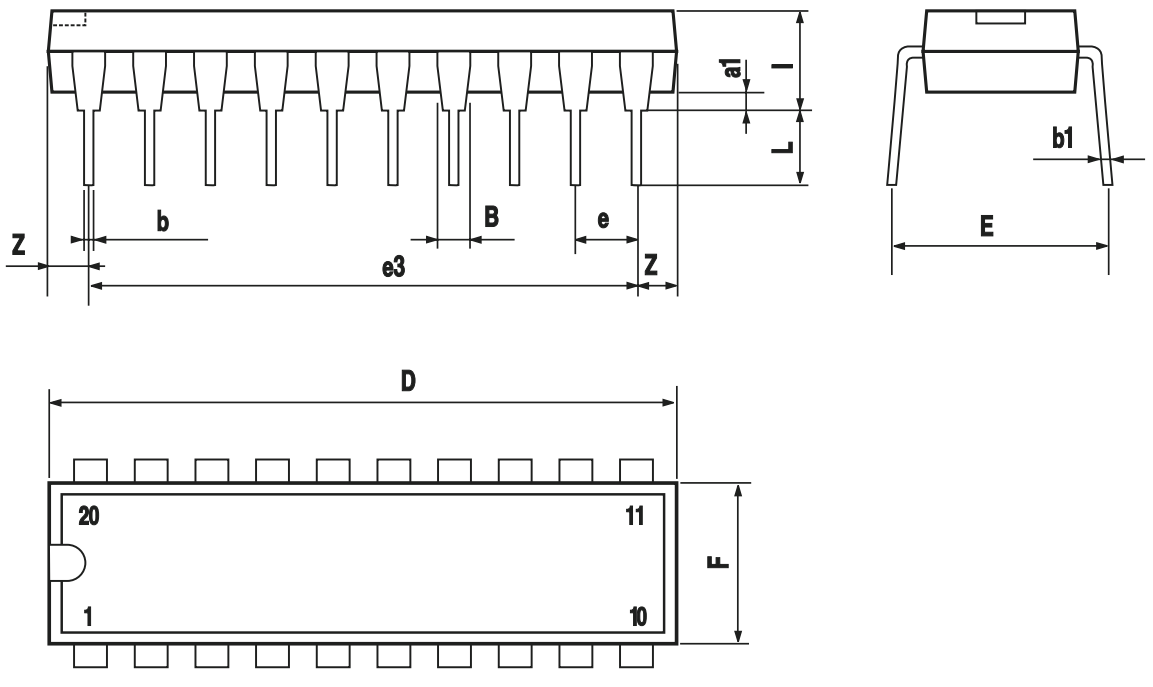


WAVEFORM 4: OUTPUT ENABLE AND DISABLE TIMES (f=1MHz; 50% duty cycle)



Plastic DIP-20 (0.25) MECHANICAL DATA

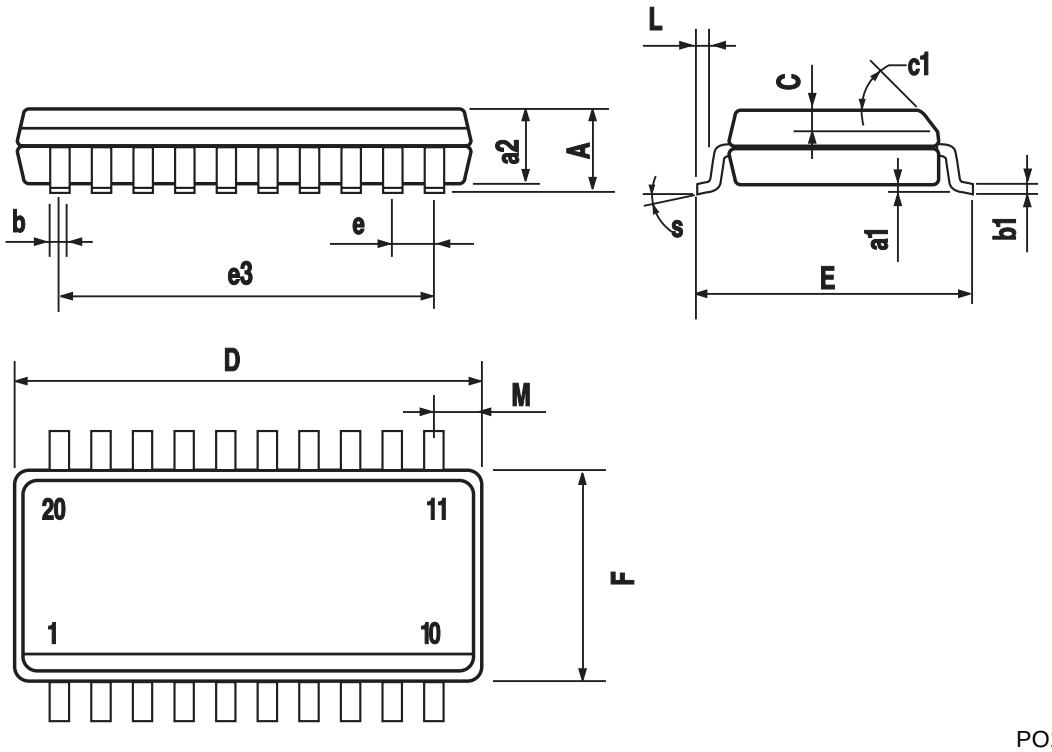
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
a1	0.254			0.010		
B	1.39		1.65	0.055		0.065
b		0.45			0.018	
b1		0.25			0.010	
D			25.4			1.000
E		8.5			0.335	
e		2.54			0.100	
e3		22.86			0.900	
F			7.1			0.280
I			3.93			0.155
L		3.3			0.130	
Z			1.34			0.053



P001J

SO-20 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.1		0.2	0.004		0.008
a2			2.45			0.096
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.012
C		0.5			0.020	
c1	45° (typ.)					
D	12.60		13.00	0.496		0.512
E	10.00		10.65	0.393		0.419
e		1.27			0.050	
e3		11.43			0.450	
F	7.40		7.60	0.291		0.300
L	0.50		1.27	0.020		0.050
M			0.75			0.029
S	8° (max.)					



PO13L

TSSOP20 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	6.4	6.5	6.6	0.252	0.256	0.260
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030