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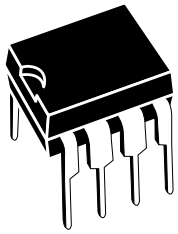
M93S46-W M93S56-W M93S66-W

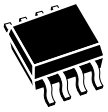
4 Kbit, 2 Kbit and 1 Kbit serial MICROWIRE bus EEPROM with write protection

Datasheet - production data



PDIP8 (BN)

TSSOP8 (DW)
169 mil width



SO8 (MN)
150 mil width

MSv35377V1

Features

- Compatible with MICROWIRE bus serial interface
- Memory array
  - 1 Kbit, 2 Kbit or 4 Kbit of EEPROM
  - Organized by word (16b)
  - Page = 4 words
- Write
  - Byte write within 5 ms
  - Page write within 5 ms
  - Ready/busy signal during programming
- User defined write protected area
- High-speed clock: 2 MHz
- Single supply voltage:
  - 2.5 V to 5.5 V
- Operating temperature range:
- -40 °C up to +85 °C.
- Enhanced ESD protection
- More than 4 million write cycles
- More than 200-year data retention

Packages

- PDIP8 ECOPACK®1
- TSSOP8 ECOPACK®2
- SO8 ECOPACK®2

Contents

List of tables

List of figures

1 Description

The M93S46, M93S56, M93S66 devices are Electrically Erasable PROgrammable Memories (EEPROMs) organized as 64, 128 or 256 words (one word is 16 bits), accessed through the MICROWIRE bus.

The M93S46, M93S56, M93S66 can operate with a supply voltage from 2.5 V to 5.5 V over an ambient temperature range of -40 °C / +85 °C.

Figure 1: Logic diagram

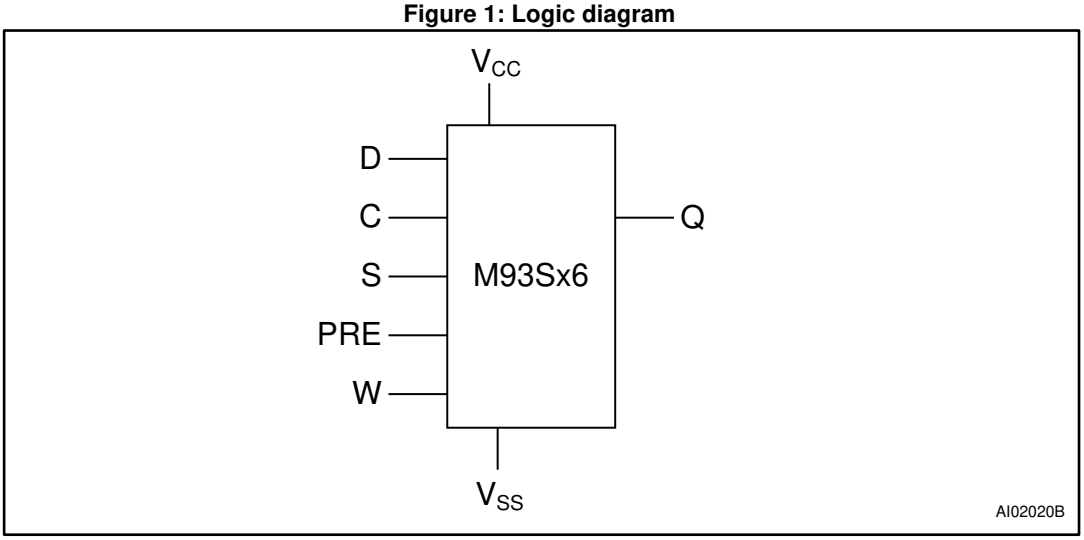
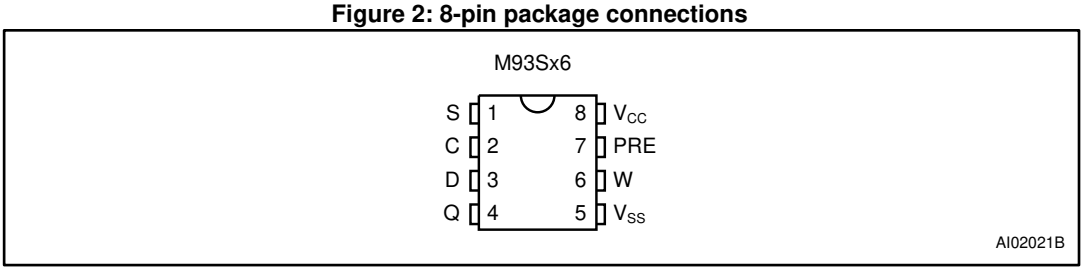


Figure 2: 8-pin package connections



1. See *Section 9: "Package mechanical data"* for package dimensions, and how to identify pin-1.

Table 1: Signal names

Signal name	Function
S	Chip select input
D	Serial data input
Q	Serial data output
C	Serial clock
PRE	Protection register enable
W	Write enable
V_{CC}	Supply voltage
V_{SS}	Ground

2 Signal description

During all operations, V_{CC} must be held stable and within the specified valid range: V_{CC}(min) to V_{CC}(max).

All of the input and output signals can be held high or low (according to voltages of V_{IL}, V_{IH}, V_{OL} or V_{OH}, as specified in *Table 10: "DC Characteristics (M93Sx6-W, device grade 6)"*. These signals are described next.

2.1 Serial data output (Q)

This output signal is used to transfer data serially out of the device. Data is shifted out on the rising edge of Serial Clock (C).

2.2 Serial data input (D)

This input signal is used to transfer data serially into the device. It receives instructions, addresses, and the data to be written. Values are latched on the rising edge of Serial Clock (C).

2.3 Serial clock (C)

This input signal provides the timing of the serial interface. Instructions, addresses, or data present at Serial Data Input (D) are latched on the rising edge of Serial Clock (C). Data on Serial Data Output (Q) changes after the rising edge of Serial Clock (C).

2.4 Chip select (S)

When this input signal is low, the device is deselected and Serial Data Output (Q) is at high impedance. Unless an internal Write cycle is in progress, the device will be in the Standby Power mode. Driving Chip Select (S) high selects the device, placing it in the Active Power mode.

2.5 Protection register (PRE)

The Protection enable (PRE) signal must be driven High before and during the instructions accessing the Protection Register.

2.6 Write protect (W)

This input signal is used to control the memory in write protected mode. When Write Protect (W) is held low, writes to the memory are disabled, but other operations remain enabled. Write Protect (W) must either be driven high or low, but must not be left floating.

2.7 V_{SS} ground

V_{SS} is the reference for the V_{CC} supply voltage.

2.8 Supply voltage (V_{CC})

2.8.1 Operating supply voltage V_{CC}

Prior to selecting the memory and issuing instructions to it, a valid and stable VCC voltage within the specified [V_{CC}(min), V_{CC}(max)] range must be applied (see *Table 5: "Operating conditions (M93Sx6-W)"*). This voltage must remain stable and valid until the end of the

transmission of the instruction and, for a Write instruction, until the completion of the internal write cycle (t_W). In order to secure a stable DC supply voltage, it is recommended to decouple the V_{CC} line with a suitable capacitor (usually of the order of 10 nF to 100 nF) close to the V_{CC}/V_{SS} package pins.

2.8.2 Device reset

In order to prevent inadvertent write operations during power-up, a power-on-reset (POR) circuit is included. At power-up, the device does not respond to any instruction until V_{CC} reaches the internal reset threshold voltage

When V_{CC} passes over the POR threshold, the device is reset and is in the following state:

- in Standby Power mode
- deselected

The device must not be accessed until VCC reaches a valid and stable V_{CC} voltage within the specified [V_{CC}(min), V_{CC}(max)] range defined in *Table 5: "Operating conditions (M93Sx6-W)"*.

2.8.3 Power-up conditions

When the power supply is turned on, V_{CC} must rise continuously from V_{SS} to V_{CC}. During this time, the Chip Select (S) line is not allowed to float but should be driven low. It is therefore recommended to connect the S line to V_{CC} via a suitable pull-down resistor.

2.8.4 Power-down

During power-down (continuous decrease in the V_{CC} supply voltage below the minimum V_{CC} operating voltage defined in *Table 5: "Operating conditions (M93Sx6-W)"*, the device must be:

- deselected (S driven low)
- in Standby Power mode (there should not be any internal write cycle in progress).

3 Operating features

The device is compatible with the MICROWIRE protocol. All instructions, addresses and input data bytes are shifted into the device, most significant bit first. The Serial Data Input (D) is sampled on the first rising edge of the Serial Clock (C) after Chip Select (S) goes high. All output data bytes are shifted out of the device, most significant bit first. The Serial Data Output (Q) is latched on the rising edge of the Serial Clock (C) after the read instruction has been clocked into the device.

The M93Sx6 is accessed by a set of instructions which includes Read, Write, Page Write, Write All and instructions used to set the memory protection. These are summarized in *Table 2: "Instruction set for the M93S46"* and *Table 3: "Instruction set for the M93S66, M93S56"*).

A Read Data from Memory (READ) instruction loads the address of the first word to be read into an internal address counter. The data contained at this address is then clocked out serially. The address counter is automatically incremented after the data is output and, if the Chip Select Input (S) is held High, the M93Sx6 can output a sequential stream of data words. In this way, the memory can be read as a data stream, or continuously as the address counter automatically rolls over to 00h when the highest address is reached.

Writing data is internally self-timed (the external clock signal on Serial Clock (C) may be stopped or left running after the start of a Write cycle) and does not require an erase cycle prior to the Write instruction. The Write instruction writes 16 bits at a time into one of the word locations of the M93Sx6, the Page Write instruction writes up to 4 words of 16 bits to sequential locations, assuming in both cases that all addresses are outside the Write Protected area.

Up to 4 words may be written with help of the Page Write instruction and the whole memory may also be erased, or written to a predetermined pattern by using the Write All instruction, within the time required by a write cycle (t_W).

After the start of the write cycle, a Busy/Ready signal is available on Serial Data Output (Q) when Chip Select Input (S) is driven High.

Within the memory, a user defined area may be protected against further Write instructions. The size of this area is defined by the content of a Protection Register, located outside of the memory array.

As a final protection step, data in this user defined area may be permanently protected by programming a One Time Programming bit (OTP bit) which locks the Protection Register content.

4 Clock pulse counter

In a noisy environment, the number of pulses received on Serial Clock (C) may be greater than the number delivered by the Bus Master (the micro- controller). This can lead to a misalignment of the instruction of one or more bits (as shown in *Figure 3: "Write sequence with one clock glitch"*.) and may lead to the writing of erroneous data at an erroneous address.

To combat this problem, the M93Sx6 has an on-chip counter that counts the clock pulses from the start bit until the falling edge of the Chip Select Input (S). If the number of clock pulses received is not the number expected, the WRITE, PAWRITE, WRALL, PRWRITE or PRCLEAR instruction isaborted, and the contents of the memory are not modified.

The number of clock cycles expected for each in- struction, and for each member of the M93Sx6 family, are summarized in *Table 2: "Instruction set for the M93S46"* and *Table 3: "Instruction set for the M93S66, M93S56"*. For example, a Write Data to Memory (WRITE) instruction on the M93S56 (or M93S66) expects 27 clock cycles from the start bit to the falling edge of Chip Select Input (S). That is:

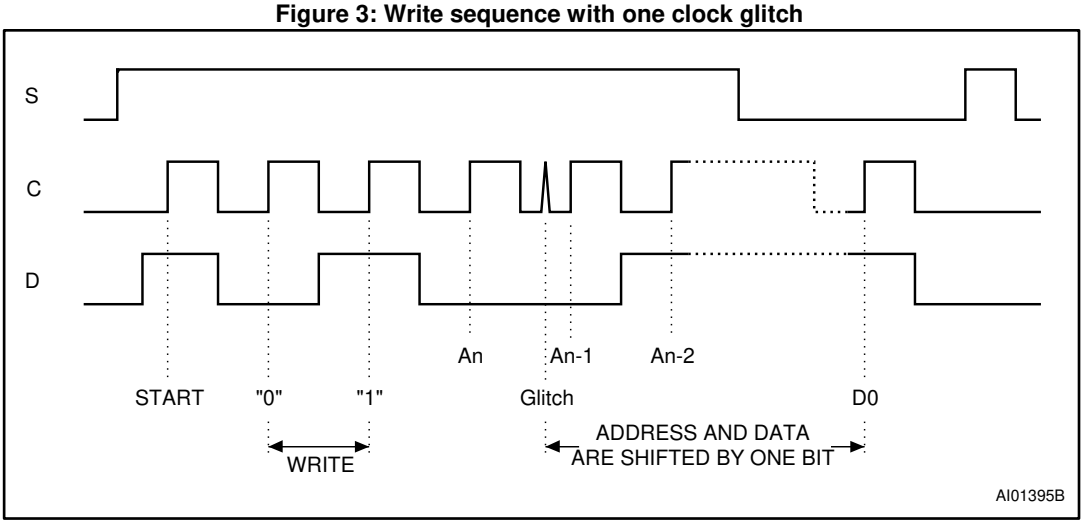
1 Start bit

+ 2 Op-code bits

+ 8 Address bits

+ 16 Data bits

Figure 3: Write sequence with one clock glitch



5 Instructions

The instruction set of the M93Sx6 devices contains seven instructions, as summarized in *Table 2: "Instruction set for the M93S46"* and *Table 3: "Instruction set for the M93S66, M93S56"*. Each instruction consists of the following parts, as shown in *Figure 4: "READ sequence"*, *Figure 5: "WRITE sequence"* and *Figure 6: "WEN and WDS sequences"*:

- Each instruction is preceded by a rising edge on Chip Select Input (S) with Serial Clock (C) being held Low.
- A start bit, which is the first '1' read on Serial Data Input (D) during the rising edge of Serial Clock (C).
- Two op-code bits, read on Serial Data Input (D) during the rising edge of Serial Clock (C). (Some instructions also use the first two bits of the address to define the op-code).
- The address bits of the byte or word that is to be accessed. For the M93S46, the address is made up of 6 bits (see *Table 2: "Instruction set for the M93S46"*). For the M93S56 and M93S66, the address is made up of 8 bits (see *Table 3: "Instruction set for the M93S66, M93S56"*).

The M93Sx6 devices are fabricated in CMOS technology and are therefore able to run as slow as 0 Hz (static input signals) or as fast as the maximum ratings specified in *Table 11: "AC Characteristics (M93Sx6-W, device grade 6)"*.

Table 2: Instruction set for the M93S46

Instruction	Description	W	PRE	Start bit	Op-code	Address (1)	Data	Required clock cycles	Additional comments
READ	Read Data from Memory	X	0	1	10	A5-A0	Q15-Q0	-	-
WRITE	Write Data to Memory	1	0	1	01	A5-A0	D15-D0	25	Write is executed if the address is not inside the Protected area
PAWRITE	Page Write to Memory	1	0	1	11	A5-A0	N x D15-D0	9 + N x 16	Write is executed if all the N addresses are not inside the Protected area
WRAL	Write All Memory with same Data	1	0	1	00	01 XXXX	D15-D0	25	Write all data if the Protection Register is cleared
WEN	Write Enable	1	0	1	00	11 XXXX	-	9	-
WDS	Write Disable	X	0	1	00	00 XXXX	-	9	-
PRREAD	Protection Register Read	X	1	1	10	XXXXXX	Q5-Q0 + Flag	-	Data Output = Protection Register content + Protection Flag bit
PRWRITE	Protection Register Write	1	1	1	01	A5-A0	-	9	Data above specified address A5-A0 are protected

Instruction	Description	W	PRE	Start bit	Op-code	Address (1)	Data	Required clock cycles	Additional comments
PRCLEAR	Protection Register Clear	1	1	1	11	111111	-	9	Protect Flag is also cleared (cleared Flag = 1)
PREN	Protection Register Enable	1	1	1	00	11XXXX	-	9	-
PRDS	Protection Register Disable	1	1	1	00	000000	-	9	OTP bit is set permanently

Note:
(1)X = Don't Care bit.

Table 3: Instruction set for the M93S66, M93S56

Instruction	Description	W	PRE	Start bit	Op-code	Address (1)(2)	Data	Required clock cycles	Additional comments
READ	Read Data from Memory	X	0	1	10	A7-A0	Q15-Q0	-	-
WRITE	Write Data to Memory	1	0	1	01	A7-A0	D15-D0	27	Write is executed if the address is not inside the Protected area
PAWRITE	Page Write to Memory	1	0	1	11	A7-A0	N x D15-D0	11 + N x 16	Write is executed if all the N addresses are not inside the Protected area
WRAL	Write All Memory with same Data	1	0	1	00	01XXXXXX	D15-D0	27	Write all data if the Protection Register is cleared
WEN	Write Enable	1	0	1	00	11XXXXXX	-	11	-
WDS	Write Disable	X	0	1	00	00XXXXXX	-	11	-
PRREAD	Protection Register Read	X	1	1	10	XXXXXXXX	Q7-Q0 + Flag	-	Data Output = Protection Register content + Protection Flag bit
PRWRITE	Protection Register Write	1	1	1	01	A7-A0	-	11	Data above specified address A7-A0 are protected
PRCLEAR	Protection Register Clear	1	1	1	11	11111111	-	11	Protect Flag is also cleared (cleared Flag = 1)

Instruction	Description	W	PRE	Start bit	Op-code	Address (1)(2)	Data	Required clock cycles	Additional comments
PREN	Protection Register Enable	1	1	1	00	11XXXXXX	-	11	-
PRDS	Protection Register Disable	1	1	1	00	00000000	-	11	OTP bit is set permanently

Notes:

(1)Address bit A7 is not decoded by the M93S56.

(2)X = Don't Care bit.

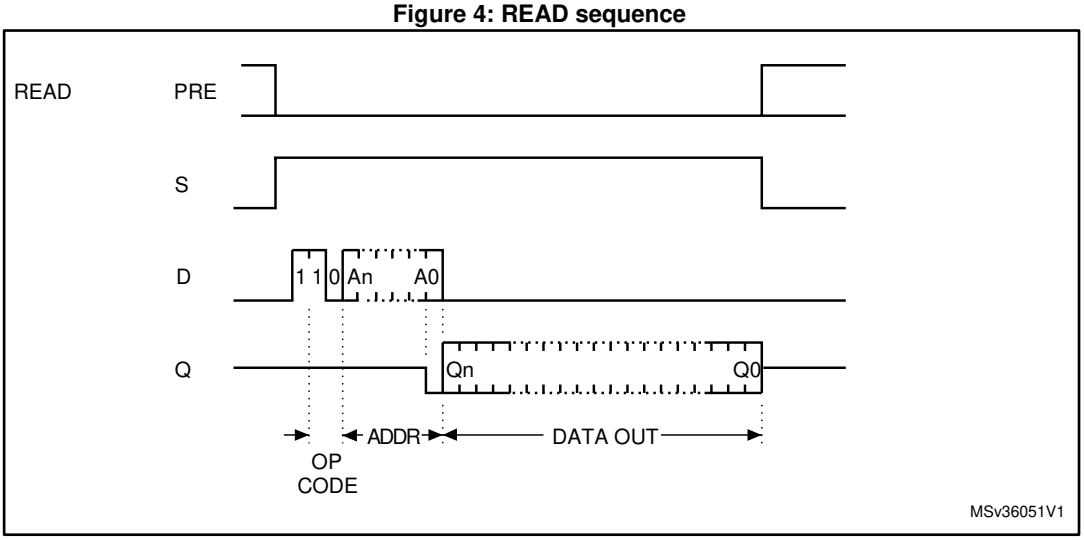
5.1 Read

The Read Data from Memory (READ) instruction outputs serial data on Serial Data Output (Q). When the instruction is received, the op-code and address are decoded, and the data from the memory is transferred to an output shift register. A dummy 0 bit is output first, followed by the 16-bit word, with the most significant bit first. Output data changes are triggered by the rising edge of Serial Clock (C). The M93Sx6 automatically increments the internal address counter and clocks out the next byte (or word) as long as the Chip Select Input (S) is held High. In this case, the dummy 0 bit is not output between bytes (or words) and a continuous stream of data can be read.

5.2 Write enable and write disable

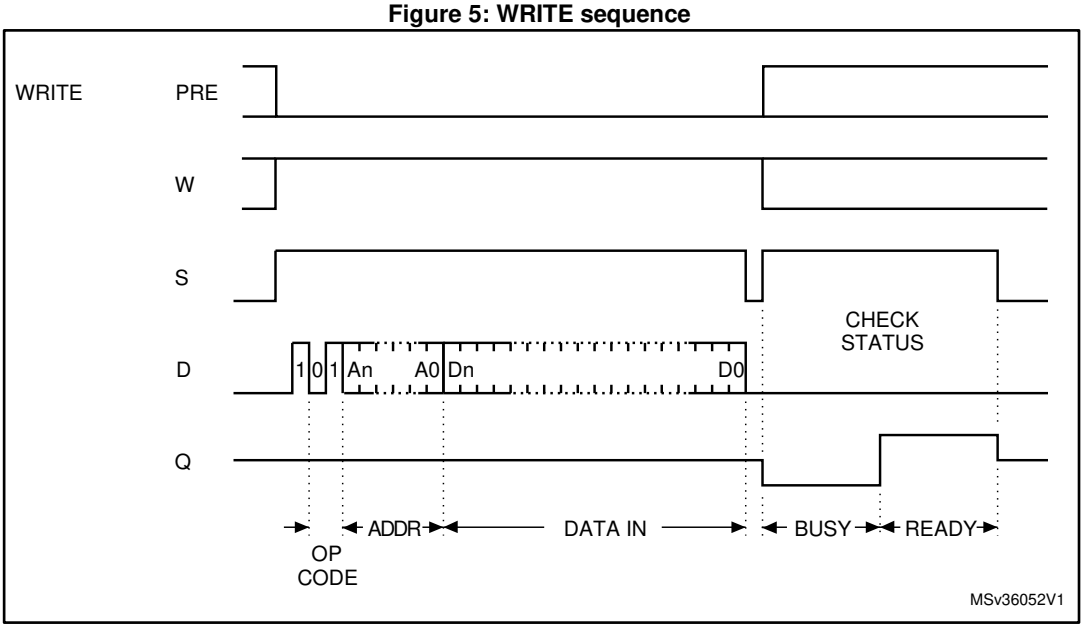
The Write Enable (WEN) instruction enables the future execution of write instructions, and the Write Disable (WDS) instruction disables it. When power is first applied, the M93Sx6 initializes itself so that write instructions are disabled. After a Write Enable (WEN) instruction has been executed, writing remains enabled until an Write Disable (WDS) instruction is executed, or until VCC falls below the power-on reset threshold voltage. To protect the memory contents from accidental corruption, it is advisable to issue the Write Disable (WDS) instruction after every write cycle. The Read Data from Memory (READ) instruction is not affected by the Write Enable (WEN) or Write Disable (WDS) instructions.

Figure 4: READ sequence



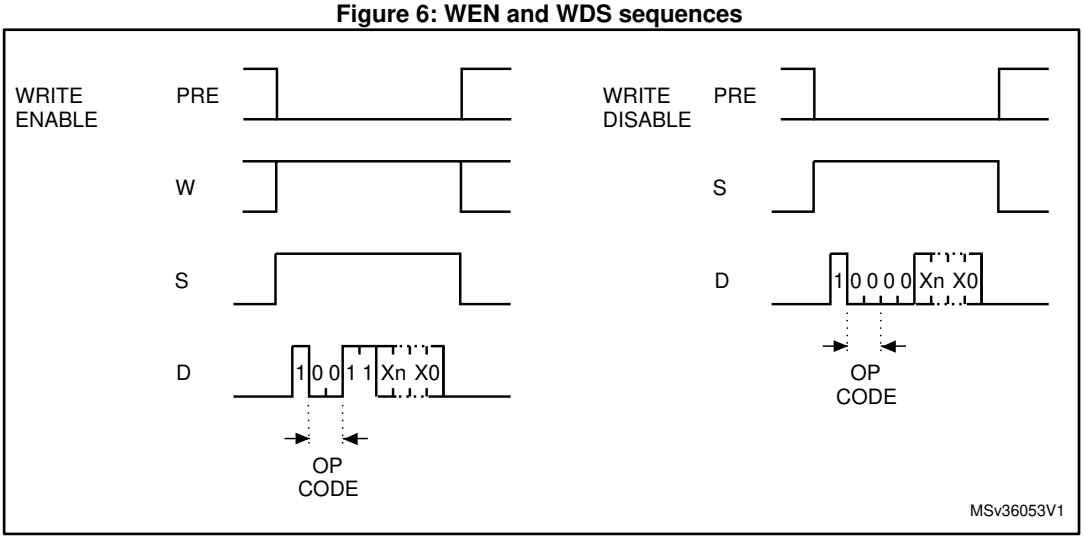
1. For the meanings of An and Qn, see *Table 2: "Instruction set for the M93S46"* and *Table 3: "Instruction set for the M93S66, M93S56"*.

Figure 5: WRITE sequence



1. For the meanings of An and Dn, see *Table 2: "Instruction set for the M93S46"* and *Table 3: "Instruction set for the M93S66, M93S56"*.

Figure 6: WEN and WDS sequences



1. For the meanings of Xn, see *Table 2: "Instruction set for the M93S46"* and *Table 3: "Instruction set for the M93S66, M93S56"*.

5.3 Write to memory array (WRITE)

The Write Data to Memory instruction is composed of the Start bit plus the op-code followed by the address and the 16 data bits to be written.

Write Enable (W) must be held High before and during the instruction. Input address and data, on Serial Data Input (D) are sampled on the rising edge of Serial Clock (C).

After the last data bit has been sampled, *the Chip Select Input (S) must be taken Low before* the next rising edge of Serial Clock (C). If Chip Select Input (S) is brought Low before or after this specific time frame, the self-timed programming cycle will not be started, and the addressed location will not be programmed.

While the M93Sx6 is performing a write cycle, but after a delay (t_{SLSH}) before the status information becomes available, Chip Select Input (S) can be driven High to monitor the status of the write cycle.

Serial Data Output (Q) is driven Low while the M93Sx6 is still busy, and High when the cycle is complete, and the M93Sx6 is ready to receive a new instruction. The M93Sx6 ignores any data on the bus while it is busy on a write cycle. Once the M93Sx6 is Ready, Serial Data Output (Q) is driven High, and remains in this state until a new start bit is decoded or the Chip Select Input (S) is brought Low.

Programming is internally self-timed, so the external Serial Clock (C) may be disconnected or left running after the start of a write cycle.

5.4 Page write

A Page Write to Memory (PAWRITE) instruction contains the first address to be written, followed by up to 4 data words. After the receipt of each data word, bits A1-A0 of the internal address counter are incremented, the high order bits remaining unchanged (A7-A2 for M93S66, M93S56; A5-A2 for M93S46). Users must take care, in the software, to ensure that the last word address has the same upper order address bits as the initial address transmitted to avoid address roll-over.

The Page Write to Memory (PAWRITE) instruction will not be executed if any of the 4 words addresses the protected area.

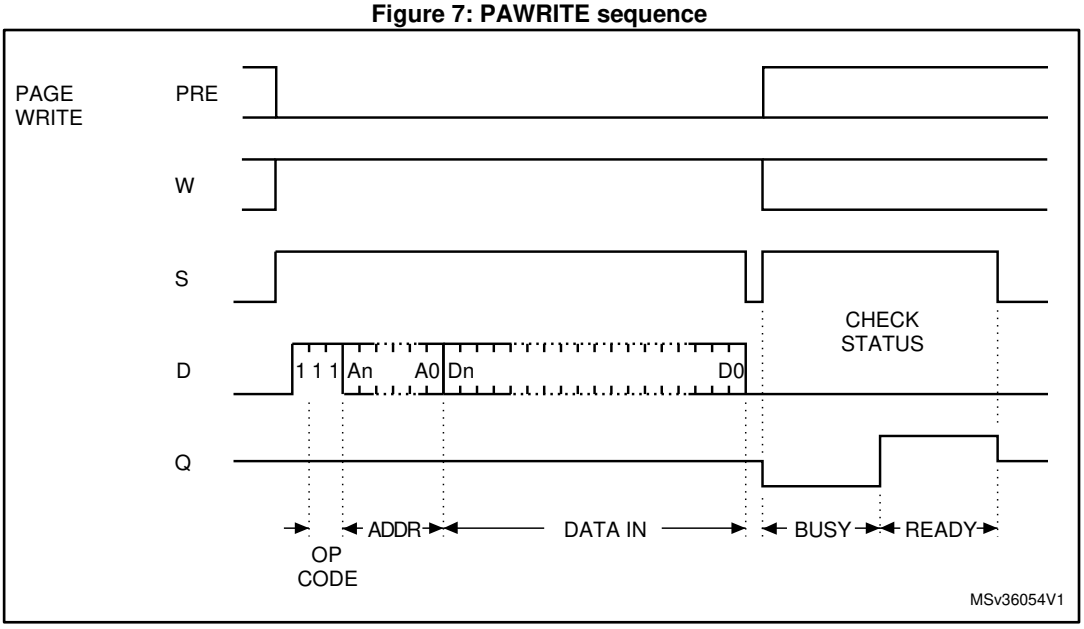
Write Enable (W) must be held High before and during the instruction. Input address and data, on Serial Data Input (D) are sampled on the rising edge of Serial Clock (C).

After the last data bit has been sampled, *the Chip Select Input (S) must be taken Low before* the next rising edge of Serial Clock (C). If Chip Select Input (S) is brought Low before or after this specific time frame, the self-timed programming cycle will not be started, and the addressed location will not be programmed.

While the M93Sx6 is performing a write cycle, but after a delay (t_{SLSH}) before the status information becomes available, Chip Select Input (S) can be driven High to monitor the status of the write cycle. Serial Data Output (Q) is driven Low while the M93Sx6 is still busy, and High when the cycle is complete, and the M93Sx6 is ready to receive a new instruction. The M93Sx6 ignores any data on the bus while it is busy on a write cycle. Once the M93Sx6 is Ready, Serial Data Output (Q) is driven High, and remains in this state until a new start bit is decoded or the Chip Select Input (S) is brought Low.

Programming is internally self-timed, so the external Serial Clock (C) may be disconnected or left running after the start of a write cycle.

Figure 7: PAWRITE sequence

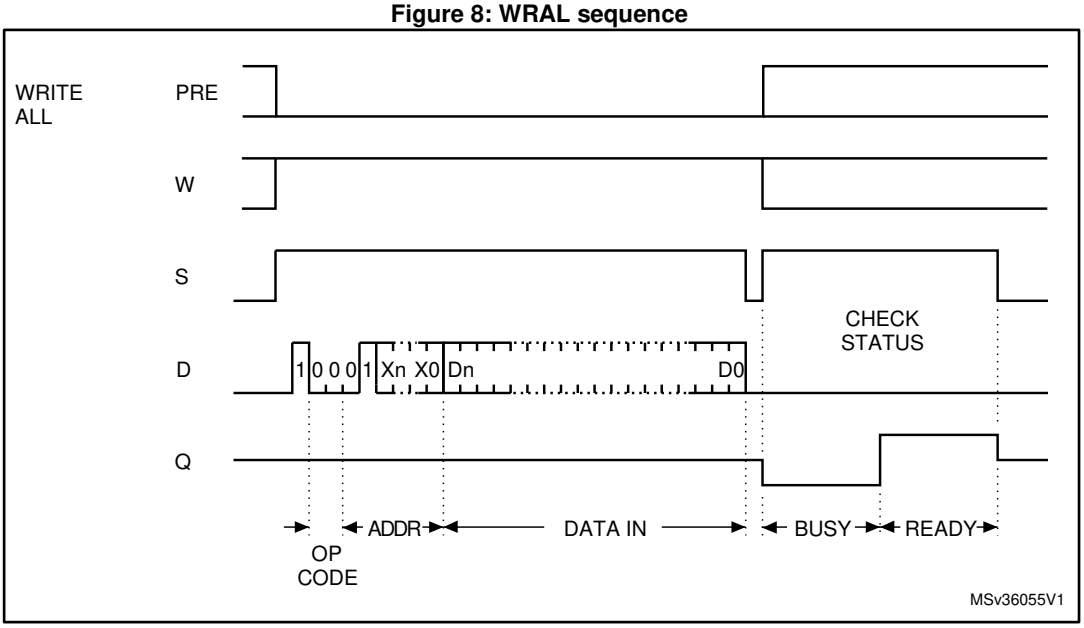


1. For the meanings of An and Dn, see *Table 2: "Instruction set for the M93S46"* and *Table 3: "Instruction set for the M93S66, M93S56"*.

5.5 Write all

The Write All Memory with same data (WRAL) instruction is valid only after the Protection Register has been cleared by executing a Protection Register Clear (PRCLEAR) instruction. The Write All Memory with same data (WRAL) instruction simultaneously writes the whole memory with the same data word given in the instruction.

Figure 8: WRAL sequence



1. For the meanings of Xn and Dn, see *Table 2: "Instruction set for the M93S46"* and *Table 3: "Instruction set for the M93S66, M93S56"*.

Write Enable (W) must be held High before and during the instruction. Input address and data, on Serial Data Input (D) are sampled on the rising edge of Serial Clock (C).

After the last data bit has been sampled, *the Chip Select Input (S) must be taken Low before* the next rising edge of Serial Clock (C). If Chip Select Input (S) is brought Low before or after this specific time frame, the self-timed programming cycle will not be started, and the addressed location will not be programmed.

While the M93Sx6 is performing a write cycle, and after a delay (t_{SLSH}) before the status information becomes available, Chip Select Input (S) can be driven High to monitor the status of the write cycle. Serial Data Output (Q) is driven Low while the M93Sx6 is still busy, and High when the cycle is complete, and the M93Sx6 is ready to receive a new instruction. The M93Sx6 ignores any data on the bus while it is busy on a write cycle. Once the M93Sx6 is Ready, Serial Data Output (Q) is driven High, and remains in this state until a new start bit is decoded or the Chip Select Input (S) is brought Low.

Programming is internally self-timed, so the external Serial Clock (C) may be disconnected or left running after the start of a write cycle.

5.6 Write protection and protect register

The Protection Register on the M93Sx6 is used to adjust the amount of memory that is to be write protected. The write protected area extends from the address given in the Protection Register, up to the top address in the M93Sx6 device.

Two flag bits are used to indicate the Protection Register status:

- Protection Flag: this is used to enable/disable protection of the write-protected area of the M93Sx6 memory
- OTP bit: when set, this disables access to the Protection Register, and thus prevents any further modifications to the value in the Protection Register.

The lower-bound memory address is written to the Protection Register using the Protection Register Write (PRWRITE) instruction. It can be read using the Protection Register Read (PRREAD) instruction.

The Protection Register Enable (PREN) instruction must be executed before any PRCLEAR, PRWRITE or PRDS instruction, and with appropriate levels applied to the Protection Enable (PRE) and Write Enable (W) signals.

Write-access to the Protection Register is achieved by executing the following sequence:

- Execute the Write Enable (WEN) instruction
- Execute the Protection Register Enable (PREN) instruction
- Execute one PRWRITE, PRCLEAR or PRDS instructions, to set a new boundary address in the Protection Register, to clear the protection address (to all 1s), or permanently to freeze the value held in the Protection Register.

Protection register read

The Protection Register Read (PRREAD) instruction outputs, on Serial Data Output (Q), the content of the Protection Register, followed by the Protection Flag bit. The Protection Enable (PRE) signal must be driven High before and during the instruction.

As with the Read Data from Memory (READ) instruction, a dummy 0 bit is output first. Since it is not possible to distinguish between the Protection Register being cleared (all 1s) or having been written with all 1s, the user must check the Protection Flag status (and not the Protection Register content) to ascertain the setting of the memory protection.

Protection register enable

The Protection Register Enable (PREN) instruction is used to authorize the use of instructions that modify the Protection Register (PRWRITE, PRCLEAR, PRDS). The

Protection Register Enable (PREN) instruction does not modify the Protection Flag bit value.

A Write Enable (WEN) instruction must be executed before the Protection Register Enable (PREN) instruction. Both the Protection Enable (PRE) and Write Enable (W) signals must be driven High during the instruction execution.

Protection register clear

The Protection Register Clear (PRCLEAR) instruction clears the address stored in the Protection Register to all 1s, so that none of the memory is write-protected by the Protection Register. However, it should be noted that all the memory remains protected, in the normal way, using the Write Enable (WEN) and Write Disable (WDS) instructions.

The Protection Register Clear (PRCLEAR) instruction clears the Protection Flag to 1. Both the Protection Enable (PRE) and Write Enable (W) signals must be driven High during the instruction execution.

A Protection Register Enable (PREN) instruction must immediately precede the Protection Register Clear (PRCLEAR) instruction.

Protection register write

The Protection Register Write (PRWRITE) instruction is used to write an address into the Protection Register. This is the address of the first word to be protected. After the Protection Register Write (PRWRITE) instruction has been executed, all memory locations equal to and above the specified address are protected from writing.

The Protection Flag bit is set to 0, and can be read with Protection Register Read (PRREAD) instruction.

Both the Protection Enable (PRE) and Write Enable (W) signals must be driven High during the instruction execution.

A Protection Register Enable (PREN) instruction must immediately precede the Protection Register Write (PRWRITE) instruction, but it is not necessary to execute first a Protection Register Clear (PRCLEAR).

Protection register disable

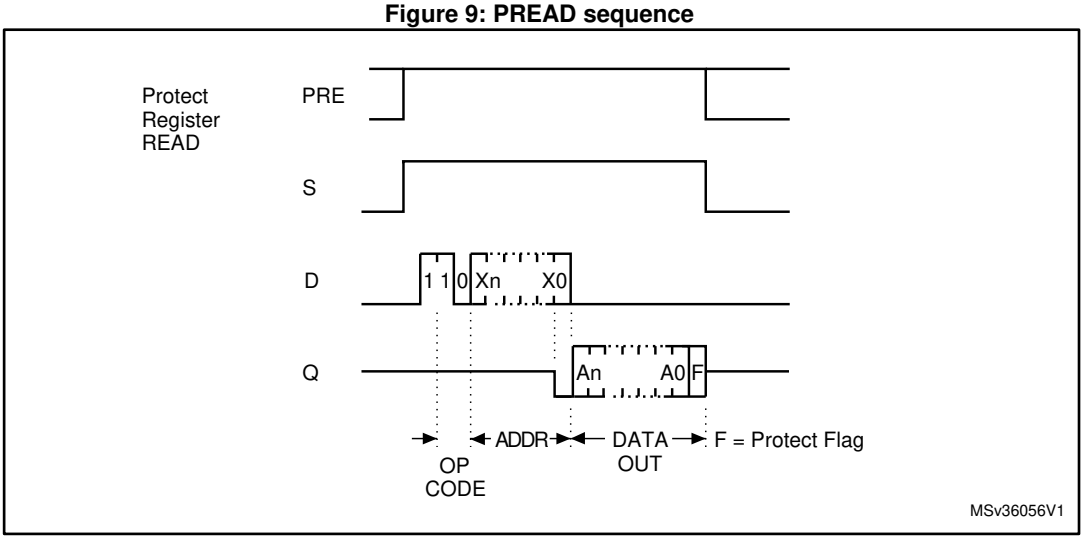
The Protection Register Disable (PRDS) instruction sets the One Time Programmable (OTP) bit.

This instruction is a ONE TIME ONLY instruction which latches the Protection Register content, this content is therefore unalterable in the future. Both the Protection Enable (PRE) and Write Enable (W) signals must be driven High during the instruction execution. The OTP bit cannot be directly read, it can be checked by reading the content of the Protection Register, using the Protection Register Read (PRREAD) instruction, then by writing this same value back into the Protection Register, using the Protection Register Write (PRWRITE) instruction.

When the OTP bit is set, the Ready/Busy status cannot appear on Serial Data Output (Q).
When the OTP bit is not set, the Busy status appears on Serial Data Output (Q).

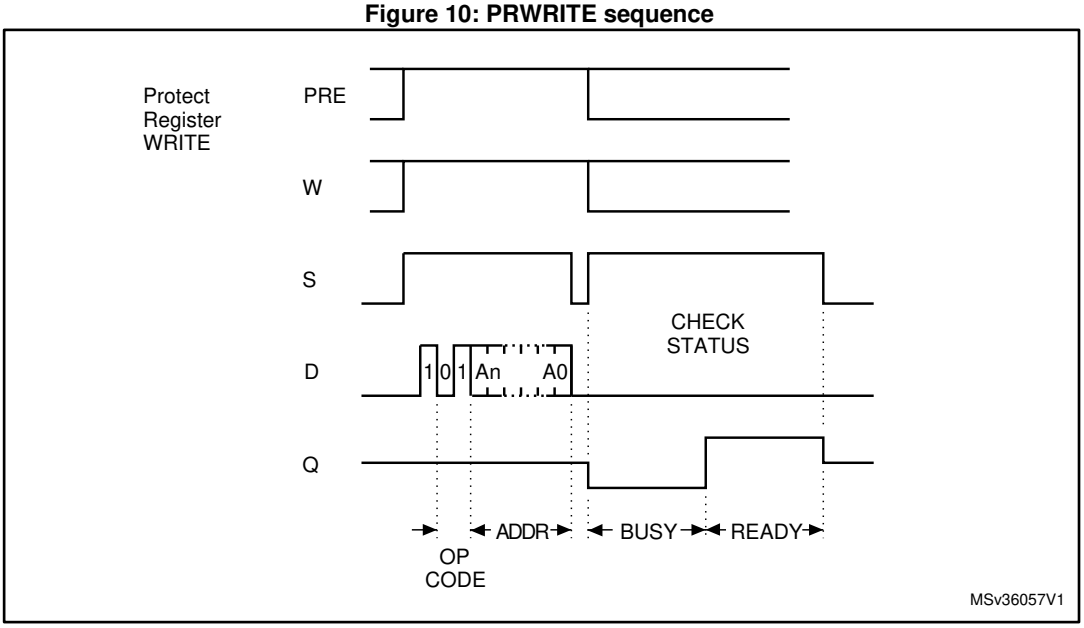
A Protection Register Enable (PREN) instruction must immediately precede the Protection Register Disable (PRDS) instruction.

Figure 9: PREAD sequence



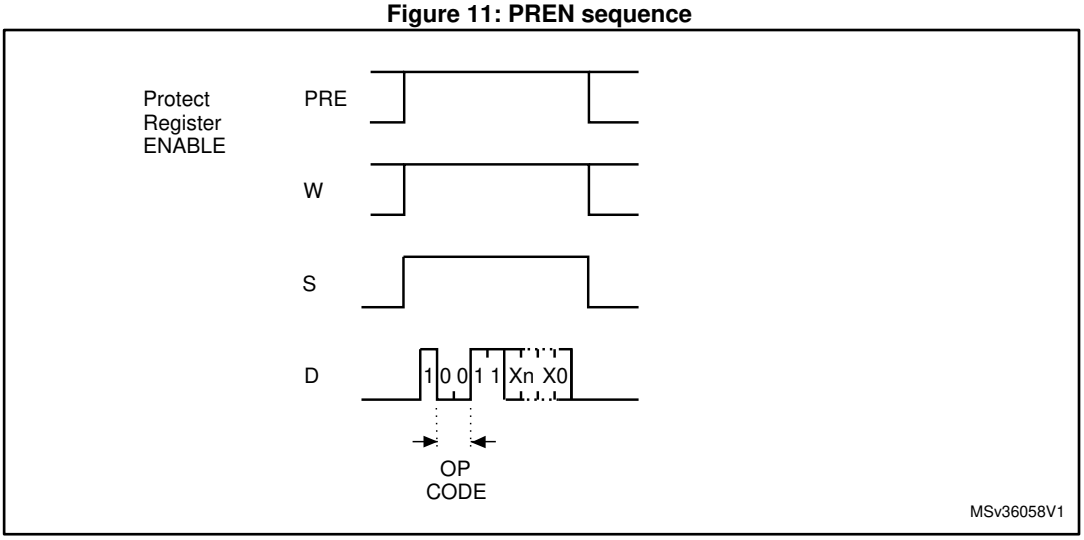
1. For the meanings of An and Xn, see *Table 2: "Instruction set for the M93S46"* and *Table 3: "Instruction set for the M93S66, M93S56"*.

Figure 10: PRWRITE sequence



1. For the meanings of An, see *Table 2: "Instruction set for the M93S46"* and *Table 3: "Instruction set for the M93S66, M93S56"*.

Figure 11: PREN sequence



1. For the meanings of Xn, see *Table 2: "Instruction set for the M93S46"* and *Table 3: "Instruction set for the M93S66, M93S56"*.

Figure 12: PRCLEAR sequence

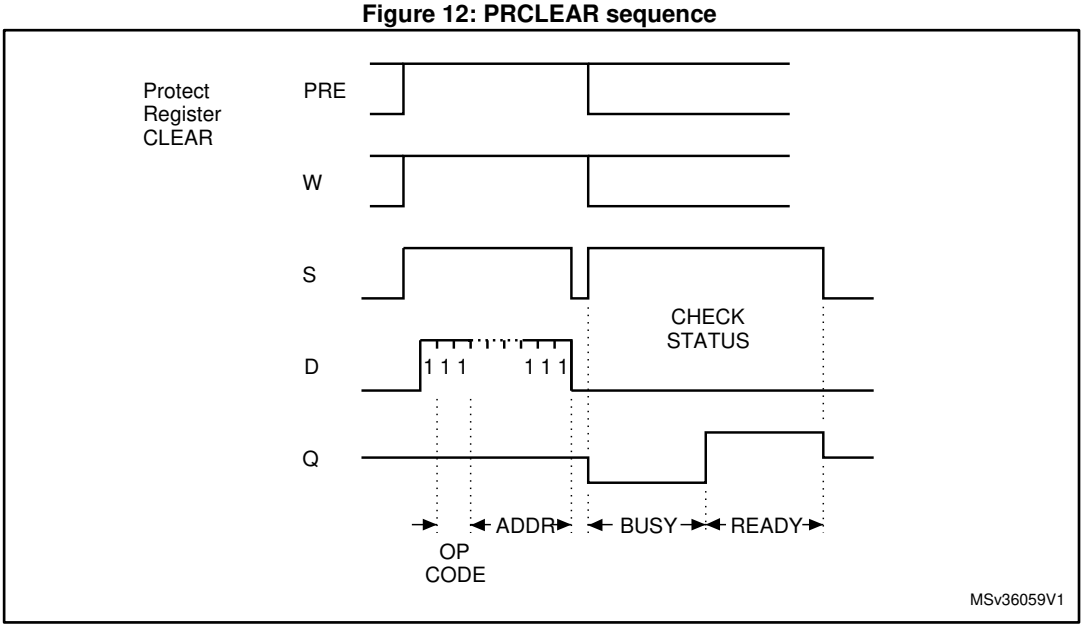
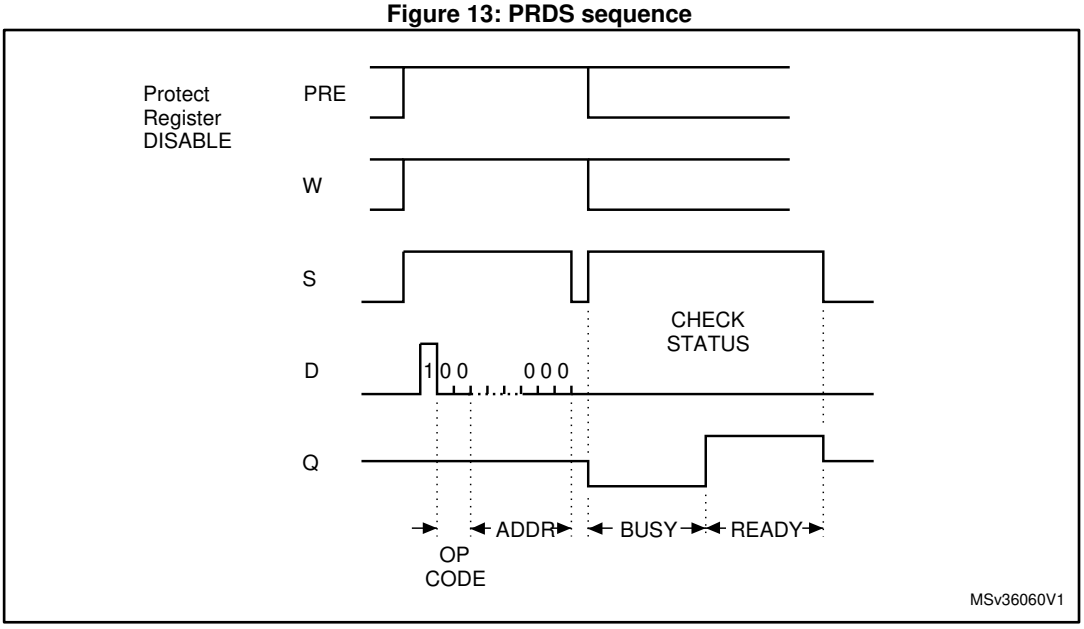


Figure 13: PRDS sequence



6 Power-up and delivery states

6.1 Power-up state

After Power-up, the device is in the following state:

- low power Standby Power mode
- deselected

6.2 Initial delivery state

The device is delivered with the memory array set at all 1s (FFh).

7 Maximum ratings

Stressing the device outside the ratings listed in *Table 4: "Absolute maximum ratings"* may cause permanent damage to the device. These are stress ratings only, and operation of the device at these, or any other conditions outside those indicated in the operating sections of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 4: Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
T_{AMR}	Ambient operating temperature	–40	130	°C
T_{STG}	Storage temperature	–65	150	°C
T_{LEAD}	Lead temperature during soldering	see note (1)		°C
V_O	Output voltage	–0.50	V_{CC}+0.5	V
V_I	Input voltage	–0.50	V_{CC}+1.0	V
I_{OL}	DC output current (Q = 0)	-	5	mA
I_{OH}	DC output current (Q = 1)	-	5	mA
V_{CC}	Supply voltage	–0.50	6.5	V
V_{ESD}	Electrostatic pulse (Human Body Model) voltage (2)	-	4000	V

Notes:

(1)Compliant with JEDEC standard J-STD-020D (for small-body, Sn-Pb or Pb assembly), the ST ECOPACK® 7191395 specification, and the European directive on Restrictions on Hazardous Substances (RoHS directive 2011/65/EU of July 2011).

(2)Positive and negative pulses applied on pin pairs, according to the AEC-Q100-002 (compliant with JEDEC Std JESD22-A114, C1=100 pF, R1=1500 Ω, R2=500 Ω)

8 DC and AC parameters

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device.

Table 5: Operating conditions (M93Sx6-W)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage	2.5	5.5	V
T_A	Ambient operating temperature (device grade 6)	–40	85	°C

Table 6: AC test measurement conditions

Symbol	Parameter	Min.	Max.	Unit
CL	Load capacitance	100		pF
-	Input rise and fall times	-	50	ns
-	Input pulse voltages	0.2 VCC to 0.8 VCC		V
-	Input and output timing reference voltages(1)	0.3 VCC to 0.7 VCC		V

Note:
(1)Output Hi-Z is defined as the point where data out is no longer driven.

Figure 14: AC test measurement I/O waveform

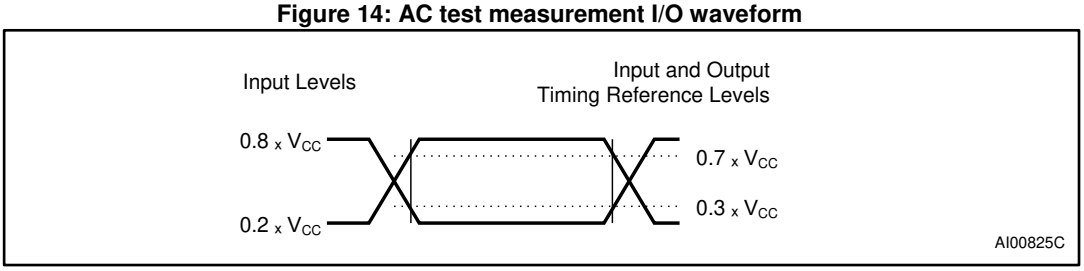


Table 7: Capacitance

Symbol	Parameter	Test condition	Min.	Max.	Unit
COUT(1)	Output capacitance (Q)	V_{OUT} = 0 V	-	5	pF
CIN(1)	Input capacitance	V_{IN} = 0 V	-	5	pF

Note:
(1)Sampled only, not 100% tested, at TA= 25 °C.

Table 8: Memory cell data retention

Parameter	Test conditions	Min.	Unit
Data retention (1)	TA = 55 °C	200	Year

Note:
(1)For products identified by process letter K (previous products were specified with a data retention of 40 years at 55 °C) . The data retention behavior is checked in production, while the Min. value (40 years or 200 years) limit is defined from characterization and qualification results.

Table 9: Cycling performance

Symbol	Parameter	Test conditions	Min.	Max.	Unit
Ncycle[(1)]	Write cycle endurance	TA ≤ 25 °C, $V_{CC}(min) < V_{CC} < V_{CC}(max)$	-	4,000,000	Write cycle
		TA = 85 °C, $V_{CC}(min) < V_{CC} < V_{CC}(max)$	-	1,200,000	

Note:
(1)Cycling performance for products identified by process letter K (previous products were specified with 1 million cycles at 25 °C).

Table 10: DC Characteristics (M93Sx6-W, device grade 6)

Symbol	Parameter	Test condition	Min.	Max.	Unit
I_{LI}	Input leakage current	0 V ≤ V_{IN} ≤ V_{CC}	-	±2.5	µA
I_{LO}	Output leakage current	0 V ≤ V_{OUT} ≤ V_{CC}, Q in Hi-Z	-	±2.5	µA
I_{CC}	Supply current (CMOS inputs)	V_{CC} = 5 V, S = V_{IH}, f = 1 MHz	-	1.5	mA
		V_{CC} = 2.5 V, S = V_{IH}, f = 1 MHz	-	1	mA
		V_{CC} = 5 V, S = V_{IH}, f = 2 MHz	-	2	mA
		V_{CC} = 2.5 V, S = V_{IH}, f = 2 MHz	-	1	mA
I_{CC1}	Supply current (stand-by)	V_{CC} = 2.5 V, S = V_{SS}, C = V_{SS}	-	10	µA
		V_{CC} = 2.5 V, S = V_{SS}, C = V_{SS}	-	5	µA
V_{IL}	Input low voltage (D, C, S, PRE, W)	-	–0.45	0.2 V_{CC}	V
V_{IH}	Input high voltage (D, C, S, PRE, W)	-	0.7 V_{CC}	V_{CC} + 1	V
V_{OL}	Output low voltage (Q)	V_{CC} = 5 V, I_{OL} = 2.1 mA	-	0.4	V
		V_{CC} = 2.5 V, I_{OL} = 100 µA	-	0.2	V
V_{OH}	Output high voltage (Q)	V_{CC} = 5 V, I_{OH} = –400 µA	2.4	-	V
		V_{CC} = 2.5 V, I_{OH} = –100 µA	V_{CC}–0.2	-	V

Table 11: AC Characteristics (M93Sx6-W, device grade 6)

Test conditions specified in *Table 5: "Operating conditions (M93Sx6-W)"* and *Table 6: "AC test measurement conditions"*					
Symbol	**Alt.**	**Parameter**	**Min.**	**Max.**	**Unit**
f_C	f_{SK}	Clock frequency	D.C.	2	MHz
t_{PRVCH}	t_{PRES}	Protect enable valid to clock high	50	-	ns
t_{WVCH}	t_{PES}	Write enable valid to clock high	50	-	ns
t_{CLPRX}	t_{PREH}	Clock low to protect enable transition	0	-	ns
t_{SLWX}	t_{PEH}	Chip select low to write enable transition	250	-	ns
t_{SLCH}		Chip select low to clock high	50	-	ns
t_{SHCH}	t_{CSS}	Chip select set-up time	50	-	ns

Test conditions specified in *Table 5: "Operating conditions (M93Sx6-W)"* and *Table 6: "AC test measurement conditions"*					
Symbol	**Alt.**	**Parameter**	**Min.**	**Max.**	**Unit**
t_{SLSH} (1)	t_{CS}	Chip select low to chip select high	200	-	ns
t_{CHCL} (2)	t_{SKH}	Clock high time	200	-	ns
t_{CLCH}	t_{SKL}	Clock low time	200	-	ns
t_{DVCH}	t_{DIS}	Data in set-up time	50	-	ns
t_{CHDX}	t_{DIH}	Data in hold time	50	-	ns
t_{CLSH}	t_{SKS}	Clock set-up time (relative to S)	50	-	ns
t_{CLSL}	t_{CSH}	Chip select hold time	0	-	ns
t_{SHQV}	t_{SV}	Chip select to ready/busy status	-	200	ns
t_{SLQZ}	t_{DF}	Chip Select low to output Hi-Z	-	100	ns
t_{CHQL}	t_{PD0}	Delay to output low	-	200	ns
t_{CHQV}	t_{PD1}	Delay to output valid	-	200	ns
t_W	t_{WP}	Erase/Write cycle time	-	5	ms

Notes:

(1)Chip Select Input (S) must be brought Low for a minimum of t_{SLSH} between consecutive instruction cycles.

(2)$t_{CHCL} + t_{CLCH} \geq 1 / f_C$.

Figure 15: Synchronous timing (start and op-code input)