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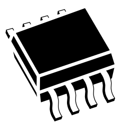
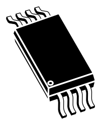
M950x0-W M950x0-R M950x0-DF

4 Kbit, 2 Kbit and 1 Kbit serial SPI bus EEPROM with high-speed clock

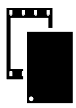
Datasheet - production data



SO8 (MN)
150 mil width



TSSOP8 (DW)
169 mil width



UFDFPN8 (MC)
2 x 3 mm

Features

- Compatible with SPI bus serial interface (Positive clock SPI modes)
- Single supply voltage:
  - 2.5 V to 5.5 V for M950x0-W
  - 1.8 V to 5.5 V for M950x0-R
  - 1.7 V to 5.5 V for M95040-DF
- High-speed 20 MHz clock rate, 5 ms write time
- Memory array:
  - 1/2/4 Kbit (128/256/512 bytes) of EEPROM
  - Page size: 16 bytes
  - Write protection by block: 1/4, 1/2 or whole memory
  - Additional Write lockable Page (Identification page)
- Enhanced ESD protection
- More than 4 million write cycles
- More than 200-year data retention
- Packages RoHS-compliant and Halogen-free (ECOPACK®)

Table 1. Device summary

Reference	Part number
M950x0-W	M95040-W
	M95020-W
	M95010-W
M950x0-R	M95040-R
	M95020-R
	M95010-R
M950x0-DF	M95040-DF

Contents

List of tables

List of figures

1 Description

The M95010/ M95020/M95040 devices (M950x0) are electrically erasable programmable memories (EEPROMs) organized as 128/256/512 x 8 bits respectively, accessed through the SPI bus.

The M950x0-W can operate with a supply voltage from 2.5 V to 5.5 V, the M950x0-R can operate with a supply voltage from 1.8 V to 5.5 V, and the M950x0-DF can operate with a supply voltage from 1.7 V to 5.5 V, over an ambient temperature range of -40 °C / +85 °C.

The M950x0-DF offers an additional page, named the Identification Page (16 bytes). The Identification Page can be used to store sensitive application parameters which can be (later) permanently locked in Read-only mode.

Figure 1. Logic diagram

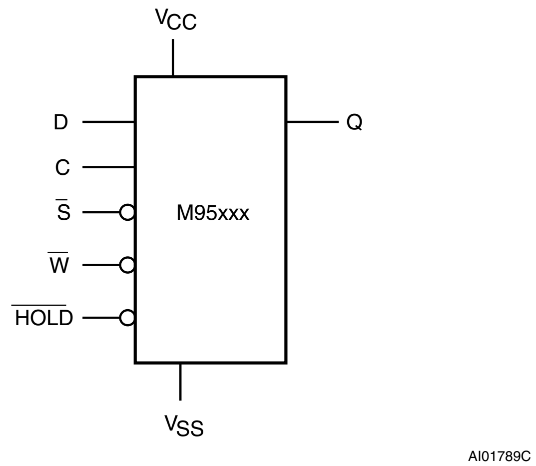
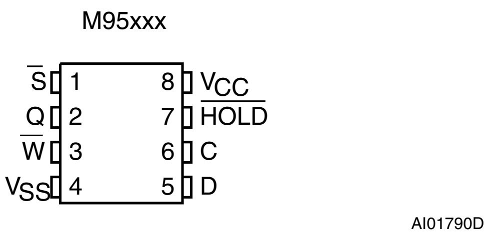


Figure 2. 8-pin package connections



1. See *Section 10: Package mechanical data* for package dimensions, and how to identify pin-1.

Table 2. Signal names

Signal name	Function
C	Serial Clock
D	Serial Data input
Q	Serial Data output
$\overline{S}$	Chip Select
$\overline{W}$	Write Protect
$\overline{HOLD}$	Hold
V_{CC}	Supply voltage
V_{SS}	Ground

2 Signal description

During all operations, V_{CC} must be held stable and within the specified valid range: V_{CC}(min) to V_{CC}(max).

All of the input and output signals can be held high or low (according to voltages of V_{IH}, V_{OH}, V_{IL} or V_{OL}, as specified in *Table 16: DC characteristics (M950x0-W, device grade 6)* and *Table 17: DC characteristics (M950x0-R or M95040-DF, device grade 6)*. These signals are described next.

2.1 Serial Data Output (Q)

This output signal transfers data serially out of the device. Data is shifted out on the falling edge of Serial Clock (C).

2.2 Serial Data Input (D)

This input signal transfers data serially into the device. It receives instructions, addresses, and the data to be written. Values are latched on the rising edge of Serial Clock (C).

2.3 Serial Clock (C)

This input signal provides the timing of the serial interface. Instructions, addresses, or data present at Serial Data Input (D) are latched on the rising edge of Serial Clock (C). Data on Serial Data Output (Q) changes after the falling edge of Serial Clock (C).

2.4 Chip Select ($\overline{S}$)

When this input signal is high, the device is deselected and Serial Data Output (Q) is at high impedance. Unless an internal Write cycle is in progress, the device will be in the Standby Power mode. Driving Chip Select ($\overline{S}$) low selects the device, placing it in the Active Power mode.

After Power-up, a falling edge on Chip Select ($\overline{S}$) is required prior to the start of any instruction.

2.5 Hold ($\overline{HOLD}$)

The Hold ($\overline{HOLD}$) signal is used to pause any serial communications with the device without deselecting the device.

During the Hold condition, the Serial Data Output (Q) is high impedance, and Serial Data Input (D) and Serial Clock (C) are Don’t Care.

To start the Hold condition, the device must be selected, with Chip Select ($\overline{S}$) driven low.

2.6 Write Protect ($\overline{W}$)

This input signal controls whether the memory is write protected. When Write Protect ($\overline{W}$) is held low, writes to the memory are disabled, but other operations remain enabled.
Write Protect ($\overline{W}$) must either be driven high or low, but must not be left floating.

2.7 V_{SS} ground

V_{SS} is the reference for the V_{CC} supply voltage.

2.8 Supply voltage (V_{CC})

2.8.1 Operating supply voltage (V_{CC})

Prior to selecting the memory and issuing instructions to it, a valid and stable V_{CC} voltage within the specified [V_{CC}(min), V_{CC}(max)] range must be applied (see *Table 9: Operating conditions (M950x0-W)*, *Table 10: Operating conditions (M950x0-R)* and *Table 11: Operating conditions (M95040-DF, device grade 6)*). This voltage must remain stable and valid until the end of the transmission of the instruction and, for a Write instruction, until the completion of the internal write cycle (t_W).
In order to secure a stable DC supply voltage, it is recommended to decouple the V_{CC} line with a suitable capacitor (usually of the order of 10 nF to 100 nF) close to the V_{CC}/V_{SS} package pins.

2.8.2 Device reset

In order to prevent inadvertent write operations during power-up, a power-on-reset (POR) circuit is included. At power-up, the device does not respond to any instruction until V_{CC} reaches the internal reset threshold voltage (this threshold is defined in *Table 9: Operating conditions (M950x0-W)*, *Table 10: Operating conditions (M950x0-R)* and *Table 11: Operating conditions (M95040-DF, device grade 6)* as V_{RES}).

When V_{CC} passes over the POR threshold, the device is reset and is in the following state:

- Standby Power mode
- Deselected (note that, to be executed, an instruction must be preceded by a falling edge on Chip Select ($\overline{S}$))
- Status register value:
  - Write Enable Latch (WEL) is reset to 0
  - Write In Progress (WIP) is reset to 0
  - SRWD, BP1 and BP0 bits remain unchanged (non-volatile bits)

When the device is in the above state, it must not be accessed until V_{CC} reaches a valid and stable V_{CC} voltage within the specified [V_{CC}(min), V_{CC}(max)] range defined in *Table 9: Operating conditions (M950x0-W)*, *Table 10: Operating conditions (M950x0-R)* and *Table 11: Operating conditions (M95040-DF, device grade 6)*.

2.8.3 Power-up conditions

When the power supply is turned on, V_{CC} rises continuously from V_{SS} to V_{CC}. During this time, the Chip Select ($\overline{S}$) line is not allowed to float but should follow the V_{CC} voltage. It is therefore recommended to connect the $\overline{S}$ line to V_{CC} via a suitable pull-up resistor (see *Figure 3: Bus master and memory devices on the SPI bus*).

In addition, the Chip Select ($\overline{S}$) input offers a built-in safety feature, as the $\overline{S}$ input is edge sensitive as well as level sensitive: after power-up, the device does not become selected until a falling edge has first been detected on Chip Select ($\overline{S}$). This ensures that Chip Select ($\overline{S}$) must have been high, prior to going low to start the first operation.

The V_{CC} voltage has to rise continuously from 0 V up to the minimum V_{CC} operating voltage defined in *Table 9: Operating conditions (M950x0-W)*, *Table 10: Operating conditions (M950x0-R)* and *Table 11: Operating conditions (M95040-DF, device grade 6)* and the rise time must not vary faster than 1 V/µs.

2.8.4 Power-down

During power-down (continuous decrease in the V_{CC} supply voltage below the minimum V_{CC} operating voltage defined in *Table 9: Operating conditions (M950x0-W)*, *Table 10: Operating conditions (M950x0-R)* and *Table 11: Operating conditions (M95040-DF, device grade 6)*), the device must be:

- Deselected (Chip Select $\overline{S}$ should be allowed to follow the voltage applied on V_{CC})
- In Standby Power mode (there should not be any internal write cycle in progress).

3 Connecting to the SPI bus

The device is fully compatible with the SPI protocol.

All instructions, addresses and input data bytes are shifted in to the device, most significant bit first. The Serial Data Input (D) is sampled on the first rising edge of the Serial Clock (C) after Chip Select ($\overline{S}$) goes low.

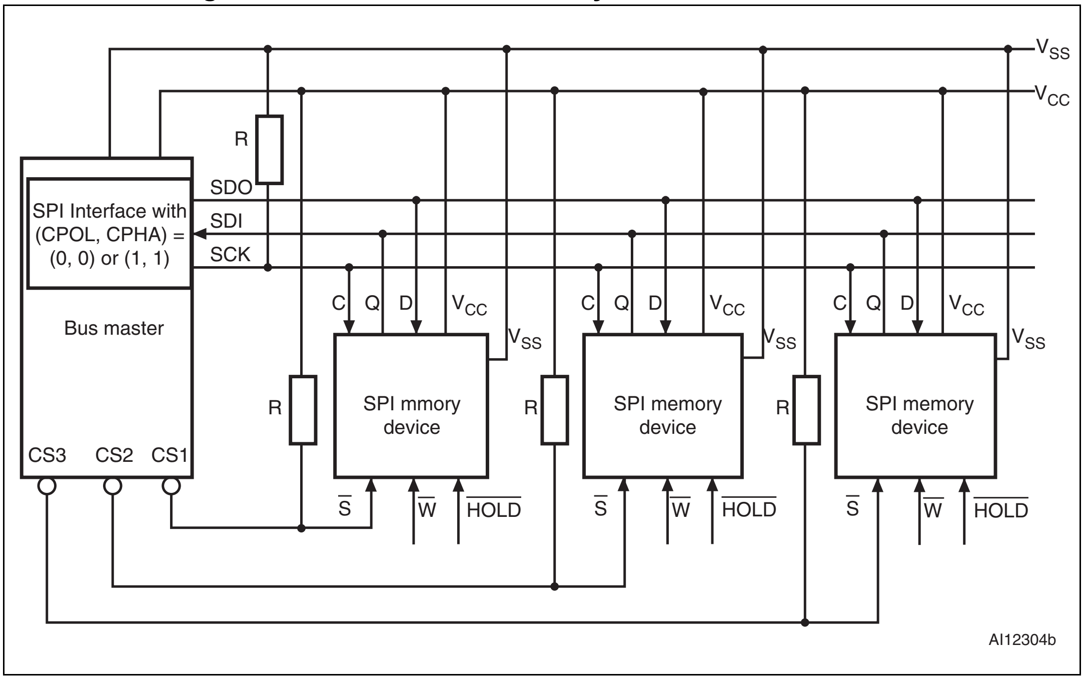
All output data bytes are shifted out of the device, most significant bit first. The Serial Data Output (Q) is latched on the first falling edge of the Serial Clock (C) after the instruction (such as the Read from Memory Array and Read Status Register instructions) have been clocked into the device.

Figure 3: Bus master and memory devices on the SPI bus shows an example of three memory devices connected to an MCU, on an SPI bus. Only one memory device is selected at a time, so only one memory device drives the Serial Data output (Q) line at a time, the other memory devices are high impedance.

The pull-up resistor R (represented in *Figure 3: Bus master and memory devices on the SPI bus*) ensures that a device is not selected if the bus master leaves the $\overline{S}$ line in the high impedance state.

In applications where the bus master might enter a state where all SPI bus inputs/outputs would be in high impedance at the same time (for example, if the bus master is reset during the transmission of an Instruction), the clock line (C) must be connected to an external pull-down resistor so that, if all inputs/outputs become high impedance, the C line is pulled low (while the $\overline{S}$ line is pulled high): this ensures that $\overline{S}$ and C do not become high at the same time, and so, that the t_{SHCH} requirement is met. The typical value of R is 100 kΩ.

Figure 3. Bus master and memory devices on the SPI bus



1. The Write Protect ($\overline{W}$) and Hold ($\overline{HOLD}$) signals should be driven, high or low as appropriate.

3.1 SPI modes

The device can be driven by a microcontroller with its SPI peripheral running in either of the following modes:

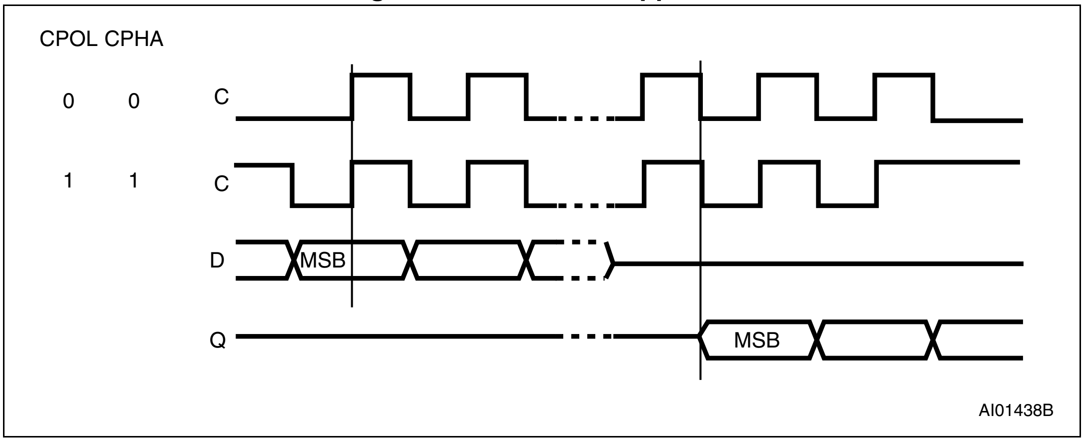
- CPOL=0, CPHA=0
- CPOL=1, CPHA=1

For these two modes, input data is latched in on the rising edge of Serial Clock (C), and output data is available from the falling edge of Serial Clock (C).

The difference between the two modes, as shown in *Figure 4: SPI modes supported*, is the clock polarity when the bus master is in Stand-by mode and not transferring data:

- C remains at 0 for (CPOL=0, CPHA=0)
- C remains at 1 for (CPOL=1, CPHA=1)

Figure 4. SPI modes supported



4 Operating features

4.1 Hold condition

The Hold ($\overline{\text{HOLD}}$) signal is used to pause any serial communications with the device without resetting the clocking sequence.

During the Hold condition, the Serial Data Output (Q) is high impedance, and Serial Data Input (D) and Serial Clock (C) are Don't Care.

To enter the Hold condition, the device must be selected, with Chip Select ($\overline{\text{S}}$) low.

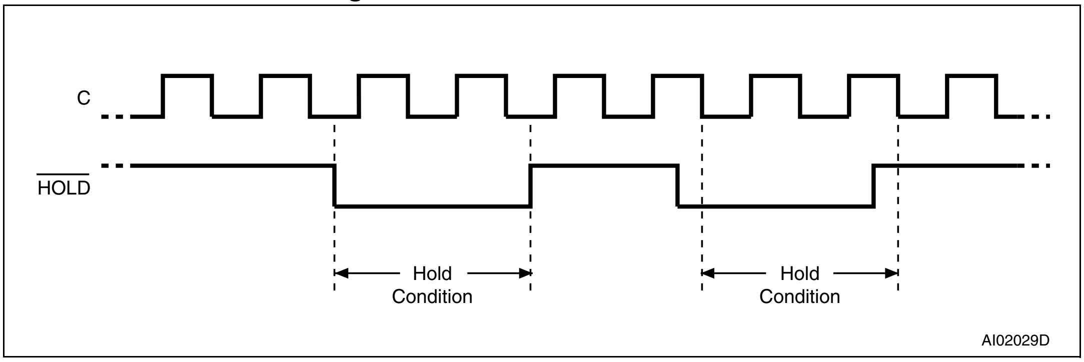
Normally, the device is kept selected, for the whole duration of the Hold condition. Deselecting the device while it is in the Hold condition has the effect of resetting the state of the device, and this mechanism can be used if it is required to reset any processes that had been in progress.

The Hold condition starts when the Hold ($\overline{\text{HOLD}}$) signal is driven low at the same time as Serial Clock (C) already being low (as shown in *Figure 5: Hold condition activation*).

The Hold condition ends when the Hold ($\overline{\text{HOLD}}$) signal is driven high at the same time as Serial Clock (C) already being low.

Figure 5: Hold condition activation also shows what happens if the rising and falling edges are not timed to coincide with Serial Clock (C) being low.

Figure 5. Hold condition activation



4.2 Status register

Figure 6 shows the position of the Status register in the control logic of the device. This register contains a number of control bits and status bits, as shown in *Table 6: Status register format* and as detailed in *Section 6.3: Read Status Register (RDSR)*.

4.3 Data protection and protocol control

To help protect the device from data corruption in noisy or poorly controlled environments, a number of safety features have been built in to the device. The main security measures can be summarized as follows:

- WEL bit is reset at power-up.
- Chip Select ($\overline{S}$) must rise after the eighth clock count (or multiple thereof) in order to start a non-volatile Write cycle (in the memory array or in the Status register).
- Accesses to the memory array are ignored during the non-volatile programming cycle, and the programming cycle continues unaffected.
- Invalid Chip Select ($\overline{S}$) and Hold ($\overline{HOLD}$) transitions are ignored.

For any instruction to be accepted and executed, Chip Select ($\overline{S}$) must be driven high after the rising edge of Serial Clock (C) that latches the last bit of the instruction, and before the next rising edge of Serial Clock (C).

For this, “the last bit of the instruction” can be the eighth bit of the instruction code, or the eighth bit of a data byte, depending on the instruction (except in the case of RDSR and READ instructions). Moreover, the “next rising edge of CLOCK” might (or might not) be the next bus transaction for some other device on the bus.

When a Write cycle is in progress, the device protects it against external interruption by ignoring any subsequent READ, WRITE or WRSR instruction until the present cycle is complete.

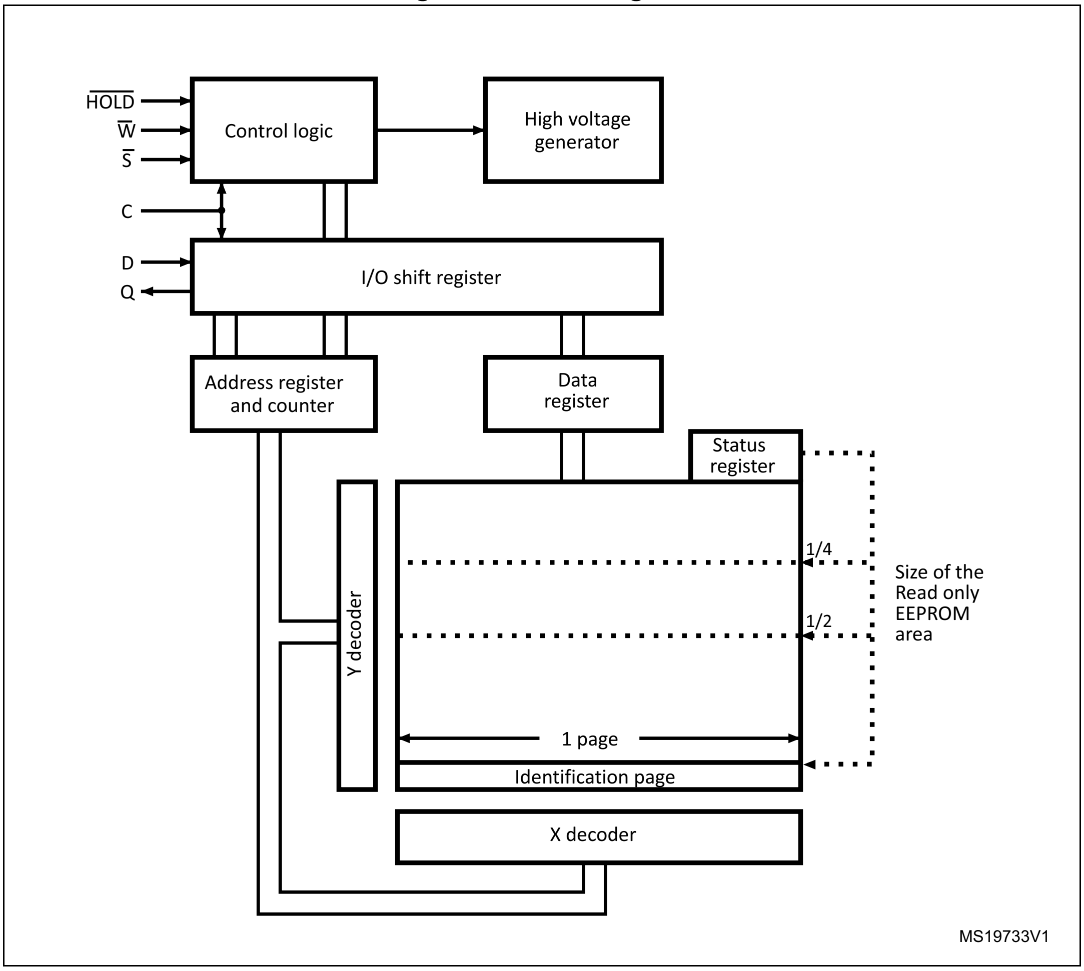
Table 3. Write-protected block size

Status register bits		Protected block	Protected array addresses		
BP1	BP0		M95040	M95020	M95010
0	0	none	none	none	none
0	1	Upper quarter	180h - 1FFh	C0h - FFh	60h - 7Fh
1	0	Upper half	100h - 1FFh	80h - FFh	40h - 7Fh
1	1	Whole memory	000h - 1FFh	00h - FFh	00h - 7Fh

5 Memory organization

The memory is organized as shown in *Figure 6*.

Figure 6. Block diagram



6 Instructions

Each command is composed of bytes (MSBit transmitted first), initiated with the instruction byte, as summarized in *Table 4*.

If an invalid instruction is sent (one not contained in *Table 4*), the device automatically enters a Wait state until deselected.

Table 4. Instruction set

Instruction	Description	Instruction format
WREN	Write Enable	0000 X110(1)
WRDI	Write Disable	0000 X100(1)
RDSR	Read Status Register	0000 X101(1)
WRSR	Write Status Register	0000 X001(1)
READ	Read from Memory Array	0000 $A_8$011(2)
WRITE	Write to Memory Array	0000 $A_8$010(2)
RDID(3)	Read Identification Page	1000 0011
WRID(3)	Write Identification Page	1000 0010
RDLS(3)	Reads the Identification Page lock status.	1000 0011
LID(3)	Locks the Identification page in read-only mode.	1000 0010

1. X = Don't Care.
2. For M95040, A8 = 1 for the upper half of the memory array and 0 for the lower half, while for M95010 and M95020, A8 is Don't Care.
3. Available only for the M95040-DF device.

Table 5. Significant bits within the address byte(1)(2)

Instructions	Bit b3 of the instruction byte	Address byte							
		b7	b6	b5	b4	b3	b2	b1	b0
READ or WRITE	A8/x(3)	A7	A6	A5	A4	A3	A2	A1	A0
RDID or WRID	0	0	0	0	0	A3	A2	A1	A0
RDLS or LID	0	1	0	0	0	0	0	0	0

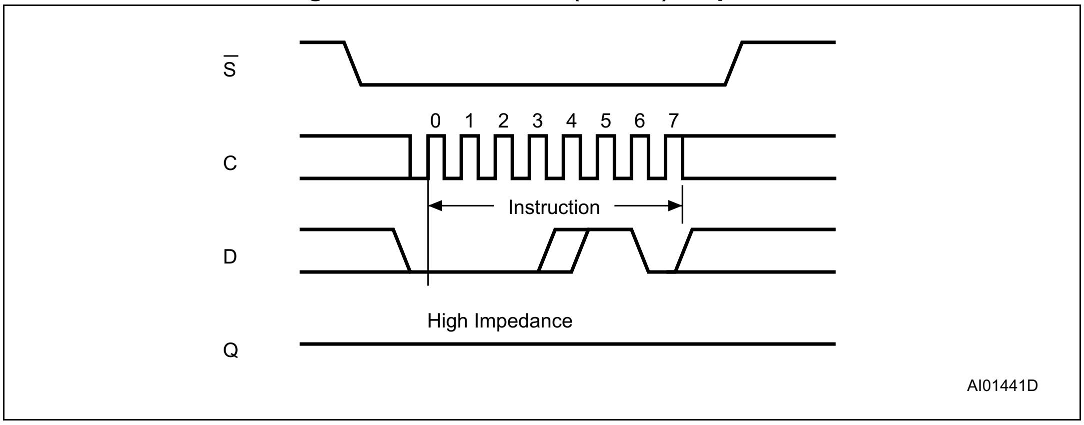
1. A: Significant address bit.
2. x: bit is Don't Care.
3. For M95040, A8 = 1 for the upper half of the memory array and 0 for the lower half, while for M95010 and M95020, A8 is Don't Care.

6.1 Write Enable (WREN)

The Write Enable Latch (WEL) bit must be set prior to each WRITE and WRSR instruction. The only way to do this is to send a Write Enable instruction to the device.

As shown in *Figure 7: Write Enable (WREN) sequence*, to send this instruction to the device, Chip Select ($\overline{S}$) is driven low, and the bits of the instruction byte are shifted in, on Serial Data Input (D). The device then enters a wait state. It waits for a the device to be deselected, by Chip Select ($\overline{S}$) being driven high.

Figure 7. Write Enable (WREN) sequence



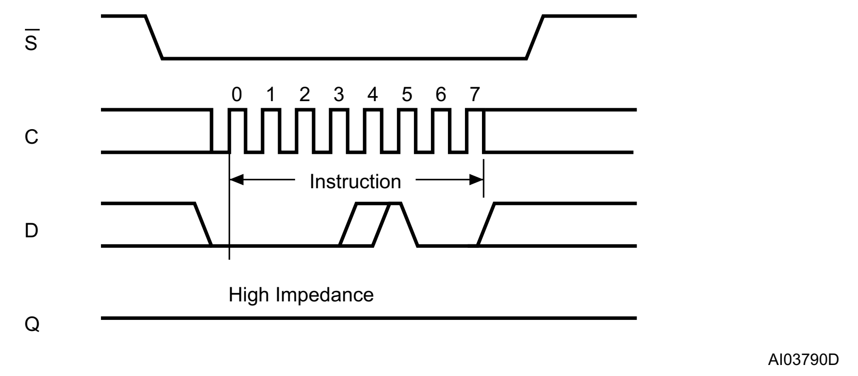
6.2 Write Disable (WRDI)

One way of resetting the Write Enable Latch (WEL) bit is to send a Write Disable instruction to the device. As shown in *Figure 8: Write Disable (WRDI) sequence*, to send this instruction to the device, Chip Select ($\overline{S}$) is driven low, and the bits of the instruction byte are shifted in, on Serial Data Input (D). The device then enters a wait state. It waits for a the device to be deselected, by Chip Select ($\overline{S}$) being driven high.

The Write Enable Latch (WEL) bit is reset by any of the following events:

- Power-up
- WRDI instruction execution
- WRSR instruction completion
- WRITE instruction completion
- Write Protect ($\overline{W}$) line being held low.

Figure 8. Write Disable (WRDI) sequence



6.3 Read Status Register (RDSR)

The Read Status Register instruction is used to read the Status Register.

As shown in *Figure 9*, to send this instruction to the device, Chip Select ($\overline{S}$) is first driven low. The bits of the instruction byte are then shifted in, on Serial Data Input (D). The current state of the bits in the Status register is shifted out, on Serial Data Out (Q). The Read Cycle is terminated by driving Chip Select ($\overline{S}$) high.

The Status Register is always readable, even if a Write or Write Status Register cycle is in progress. During a Write Status Register cycle, the values of the non-volatile bits (BP0, BP1) become available when a new RDSR instruction is executed, after completion of the Write cycle. On the other hand, the two read-only bits (Write Enable Latch (WEL), Write In Progress (WIP)) are dynamically updated during the ongoing Write cycle.

It is possible to read the Status Register contents continuously, as described in *Figure 9*.

Bits b7, b6, b5 and b4 are always read as 1. The status and control bits of the Status register are as follows:

Table 6. Status register format

b7							b0
1	1	1	1	BP1	BP0	WEL	WIP

Block Protect bits

Write Enable Latch bit

Write In Progress bit

6.3.1 WIP bit

The Write In Progress (WIP) bit indicates whether the memory is busy with a Write or Write Status register cycle. When set to 1, such a cycle is in progress, when reset to 0 no such cycle is in progress.

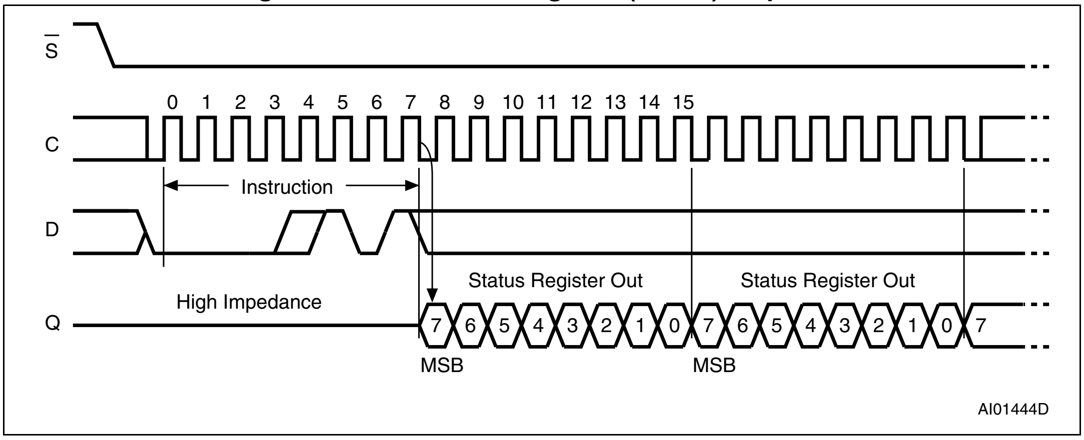
6.3.2 WEL bit

The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch. When set to 1 the internal Write Enable Latch is set, when set to 0 the internal Write Enable Latch is reset and no Write or Write Status Register instruction is accepted.

6.3.3 BP1, BP0 bits

The Block Protect (BP1, BP0) bits are non-volatile. They define the size of the area to be software protected against Write instructions. These bits are written with the Write Status Register (WRSR) instruction. When one or both of the Block Protect (BP1, BP0) bits is set to 1, the relevant memory area (as defined in *Table 3: Write-protected block size*) becomes protected against Write (WRITE) instructions. The Block Protect (BP1, BP0) bits can be written provided that the Hardware Protected mode has not been set.

Figure 9. Read Status Register (RDSR) sequence



6.4 Write Status Register (WRSR)

A Write Status Register (WRSR) instruction allows new values to be written to the Status register. Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed.

The WRSR instruction is entered by driving Chip Select ($\overline{S}$) low, sending the instruction code followed by the data byte on Serial Data input (D), and driving the Chip Select ($\overline{S}$) signal high. Chip Select ($\overline{S}$) must be driven high after the rising edge of Serial Clock (C) that latches in the eighth bit of the data byte, and before the next rising edge of Serial Clock (C). Otherwise, the WRSR instruction is not executed.

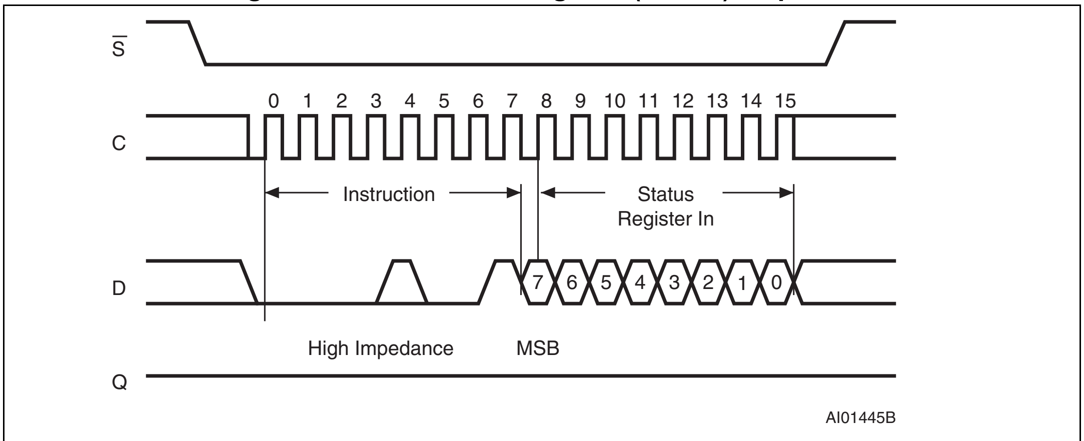
Driving the Chip Select ($\overline{S}$) signal high at a byte boundary of the input data triggers the self-timed write cycle that takes t_W to complete (as specified in *Table 16: DC characteristics (M950x0-W, device grade 6)* to *Table 19: AC characteristics (M950x0-R or M95040-DF, device grade 6)*). The instruction sequence is shown in *Figure 10: Write Status Register (WRSR) sequence*.

While the Write Status Register cycle is in progress, the Status register may still be read to check the value of the Write in progress (WIP) bit: the WIP bit is 1 during the self-timed write cycle t_W, and, 0 when the write cycle is complete. The WEL bit (Write enable latch) is also reset at the end of the write cycle t_W.

The WRSR instruction allows the user to change the values of the BP1, BP0 bits which define the size of the area that is to be treated as read only, as defined in *Table 3: Write-protected block size*. The contents of the BP1, BP0 bits are updated after the completion of the WRSR instruction, including the t_W write cycle.

The WRSR instruction has no effect on the b7, b6, b5, b4, b1 and b0 bits in the Status register which are always read as 0.

Figure 10. Write Status Register (WRSR) sequence



The WRSR instruction is not accepted, and is not executed, under the following conditions:

- if the Write Enable Latch (WEL) bit has not been set to 1 (by executing a Write Enable instruction just before)
- if a write cycle is already in progress
- if the device has not been deselected, by Chip Select ($\overline{S}$) being driven high, after the eighth bit, b0, of the data byte has been latched in
- if Write Protect ($\overline{W}$) is low during the WRSR command (instruction, address and data)

6.5 Read from Memory Array (READ)

As shown in *Figure 11: Read from Memory Array (READ) sequence*, to send this instruction to the device, Chip Select ($\overline{S}$) is first driven low. The bits of the instruction byte and address byte are then shifted in, on Serial Data Input (D). For the M95040, the most significant address bit, A8, is incorporated as bit b3 of the instruction byte, as shown in *Table 4: Instruction set*. The address is loaded into an internal address register, and the byte of data at that address is shifted out, on Serial Data Output (Q).

If Chip Select ($\overline{S}$) continues to be driven low, an internal bit-pointer is automatically incremented at each clock cycle, and the corresponding data bit is shifted out.

When the highest address is reached, the address counter rolls over to zero, allowing the Read cycle to be continued indefinitely. The whole memory can, therefore, be read with a single READ instruction.

The Read cycle is terminated by driving Chip Select ($\overline{S}$) high. The rising edge of the Chip Select ($\overline{S}$) signal can occur at any time during the cycle.

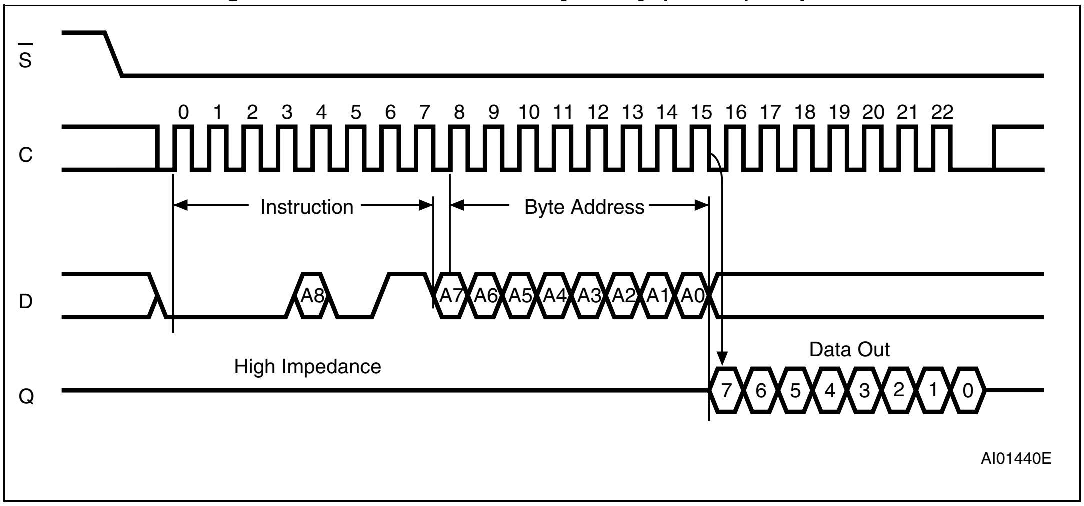
The first byte addressed can be any byte within any page.

The instruction is not accepted, and is not executed, if a Write cycle is currently in progress.

Table 7. Address range bits

Device	M95040	M95020	M95010
Address Bits	A8-A0	A7-A0	A6-A0

Figure 11. Read from Memory Array (READ) sequence



1. Depending on the memory size, as shown in *Table 7: Address range bits*, the most significant address bits are Don't Care.

6.6 Write to Memory Array (WRITE)

As shown in *Figure 12: Byte Write (WRITE) sequence*, to send this instruction to the device, Chip Select ($\overline{S}$) is first driven low. The bits of the instruction byte, address byte, and at least one data byte are then shifted in, on Serial Data input (D). The instruction is terminated by driving Chip Select ($\overline{S}$) high at a byte boundary of the input data. The self-timed Write cycle, triggered by the rising edge of Chip Select ($\overline{S}$), continues for a period t_W (as specified in *Table 16: DC characteristics (M950x0-W, device grade 6)* to *Table 19: AC characteristics (M950x0-R or M95040-DF, device grade 6)*). After this time, the Write in Progress (WIP) bit is reset to 0.

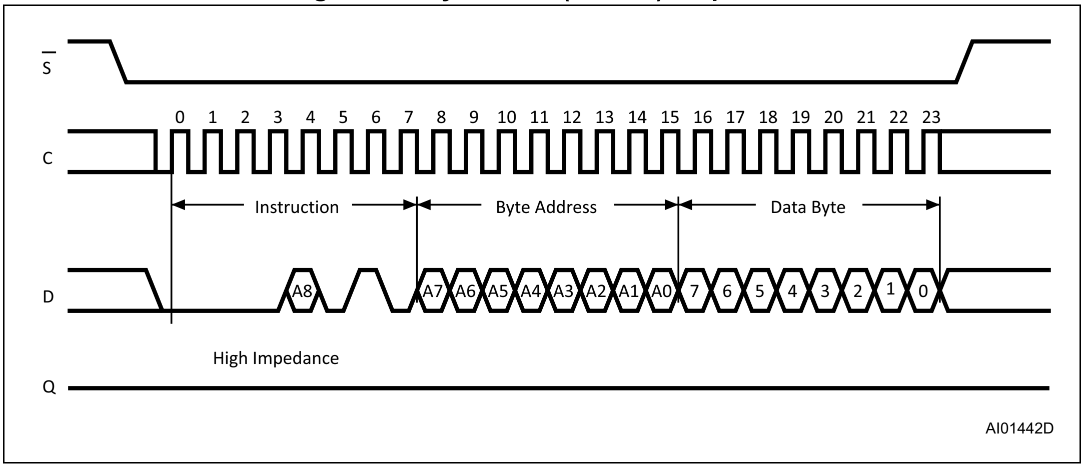
In the case of *Figure 12: Byte Write (WRITE) sequence*, Chip Select ($\overline{S}$) is driven high after the eighth bit of the data byte has been latched in, indicating that the instruction is being used to write a single byte. If, though, Chip Select ($\overline{S}$) continues to be driven low, as shown in *Figure 13: Page Write (WRITE) sequence*, the next byte of input data is shifted in, so that more than a single byte, starting from the given address towards the end of the same page, can be written in a single internal Write cycle. If Chip Select ($\overline{S}$) still continues to be driven low, the next byte of input data is shifted in, and used to overwrite the byte at the start of the current page.

The instruction is not accepted, and is not executed, under the following conditions:

- if the Write Enable Latch (WEL) bit has not been set to 1 (by executing a Write Enable instruction just before)
- if a Write cycle is already in progress
- if the device has not been deselected, by Chip Select ($\overline{S}$) being driven high, at a byte boundary (after the rising edge of Serial Clock (C) that latches the last data bit, and before the next rising edge of Serial Clock (C) occurs anywhere on the bus)
- if Write Protect ($\overline{W}$) is low or if the addressed page is in the area protected by the Block Protect (BP1 and BP0) bits

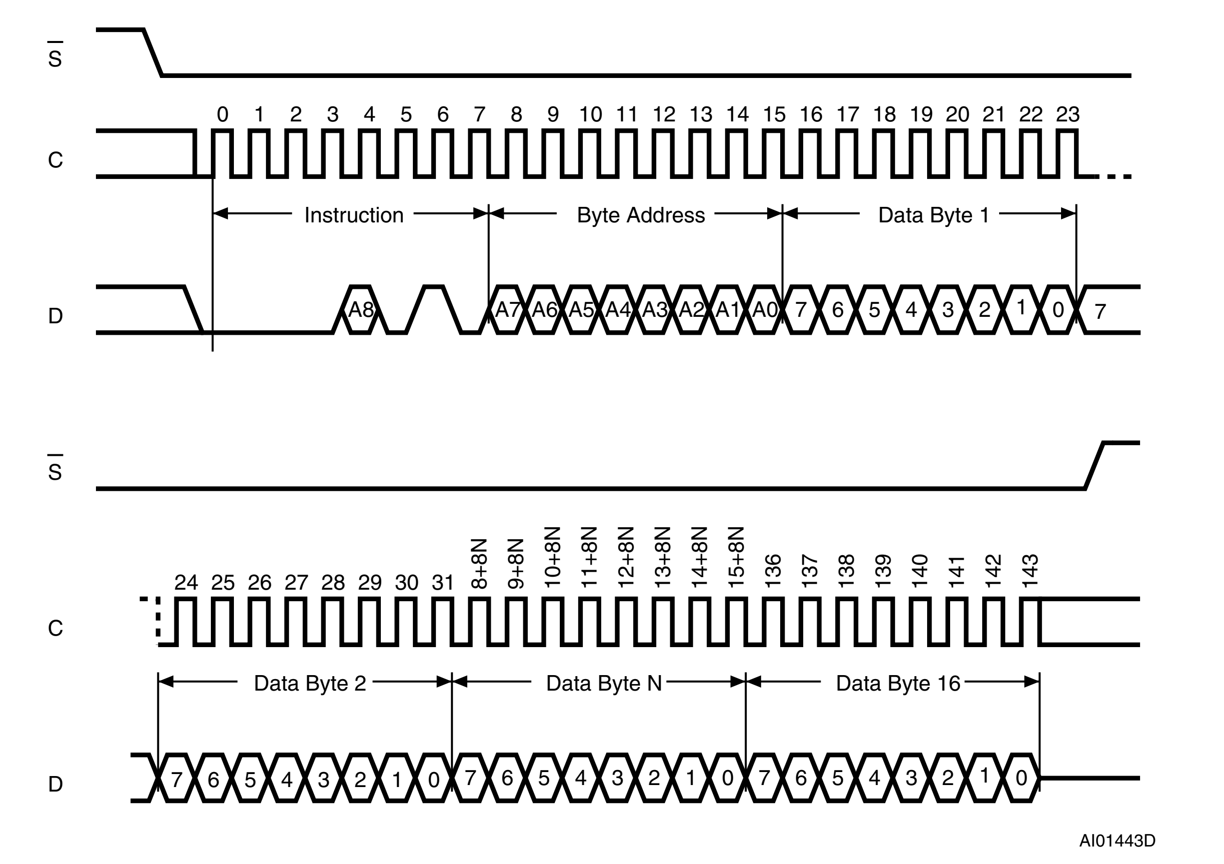
Note: The self-timed write cycle t_W is internally executed as a sequence of two consecutive events: [Erase addressed byte(s)], followed by [Program addressed byte(s)]. An erased bit is read as “0” and a programmed bit is read as “1”.

Figure 12. Byte Write (WRITE) sequence



1. Depending on the memory size, as shown in *Table 7: Address range bits*, the most significant address bits are Don’t Care.

Figure 13. Page Write (WRITE) sequence



1. Depending on the memory size, as shown in *Table 7: Address range bits*, the most significant address bits are Don't Care.

6.7 Read Identification Page (available only in M95040-D device)

The Read Identification Page (RDID) instruction is used to read the Identification Page (additional page of 16 bytes which can be written and later permanently locked in Read-only mode).

The Chip Select ($\overline{S}$) signal is first driven low, the bits of the instruction byte and address bytes are then shifted in (MSB first) on Serial Data input (D). Address bit A7 must be 0 and the other address bits are Don't Care except the lower address bits [A3:A0] (it might be easier to define these bits as 0, as shown in *Table 5*). Data is then shifted/clocked out (MSB first) on Serial Data output (Q).

The first byte addressed can be any byte within the identification page.

If Chip Select ($\overline{S}$) continues to be driven low, the internal address register is automatically incremented and the byte of data at the new address is shifted out.

Note that there is no roll over feature in the Identification Page. The address of bytes to read must not exceed the page boundary.

The read cycle is terminated by driving Chip Select ($\overline{S}$) high. The rising edge of the Chip Select ($\overline{S}$) signal can occur at any time when the data bits are shifted out.

The instruction is not accepted, and is not executed, if a Write cycle is currently in progress.

Figure 14. Read Identification Page sequence