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Parallel NOR Flash Embedded Memory

MT28EW128ABA

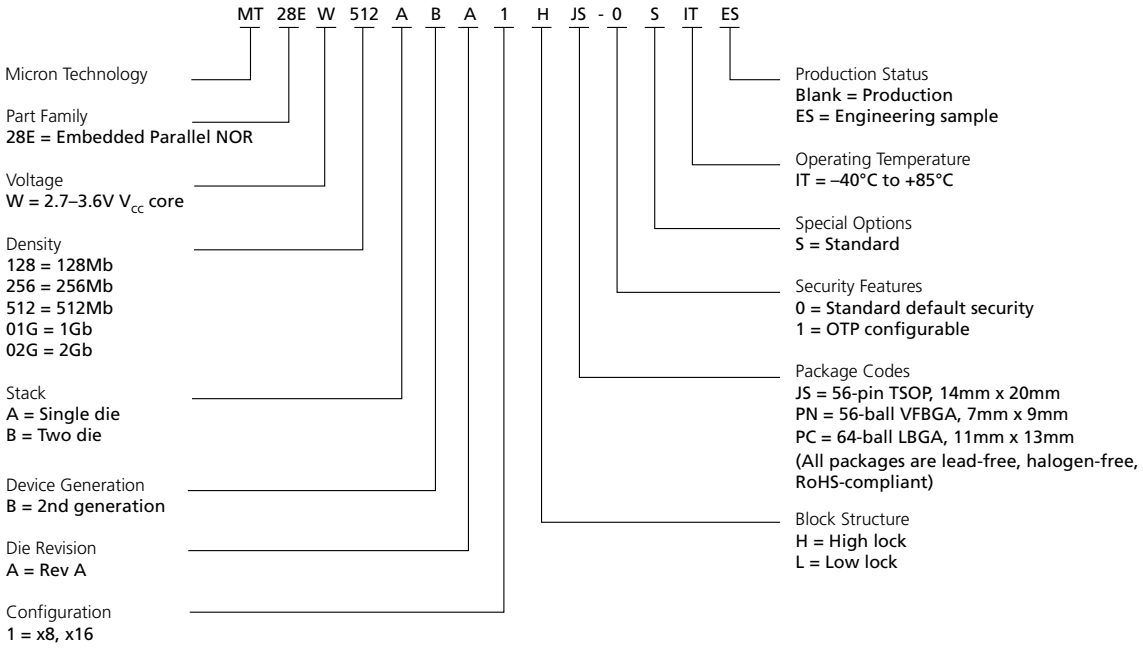
Features

- Single-level cell (SLC) process technology
- Density: 128Mb
- Supply voltage
  - V_{CC} = 2.7–3.6V (program, erase, read)
  - V_{CCQ} = 1.65 - V_{CC} (I/O buffers)
- Asynchronous random/page read
  - Page size: 16 words or 32 bytes
  - Page access: 20ns
  - Random access: 70ns (V_{CC} = V_{CCQ} = 2.7-3.6V)
  - Random access: 75ns (V_{CCQ} = 1.65-V_{CC})
- Buffer program (512-word program buffer)
  - 2.0 MB/s (TYP) when using full buffer program
  - 2.5 MB/s (TYP) when using accelerated buffer program (V_{HH})
- Word/Byte program: 25us per word (TYP)
- Block erase (128KB): 0.2s (TYP)
- Memory organization
  - Uniform blocks: 128KB or 64KW each
  - x8/x16 data bus
- Program/erase suspend and resume capability
  - Read from another block during a PROGRAM SUSPEND operation
  - Read or program another block during an ERASE SUSPEND operation
- Unlock bypass, block erase, chip erase, and write to buffer capability
- BLANK CHECK operation to verify an erased block
- CYCLIC REDUNDANCY CHECK (CRC) operation to verify a program pattern
- V_{PP}/WP# protection
  - Protects first or last block regardless of block protection settings
- Software protection
  - Volatile protection
  - Nonvolatile protection
  - Password protection
- Extended memory block
  - 128-word (256-byte) block for permanent, secure identification
  - Programmed or locked at the factory or by the customer
- JESD47-compliant
  - 100,000 (minimum) ERASE cycles per block
  - Data retention: 20 years (TYP)
- Package
  - 56-pin TSOP, 14 x 20mm (JS)
  - 64-ball LBGA, 11 x 13mm (PC)
  - 56-ball VFBGA, 7 x 9mm (PN)
- RoHS-compliant, halogen-free packaging
- Operating temperature
  - Ambient: –40°C to +85°C

Part Numbering Information

For available options, such as packages or high/low protection, or for further information, contact your Micron sales representative. Part numbers can be verified at www.micron.com. Feature and specification comparison by device type is available at www.micron.com/products. Contact the factory for devices not found.

Figure 1: Part Number Chart



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General Description

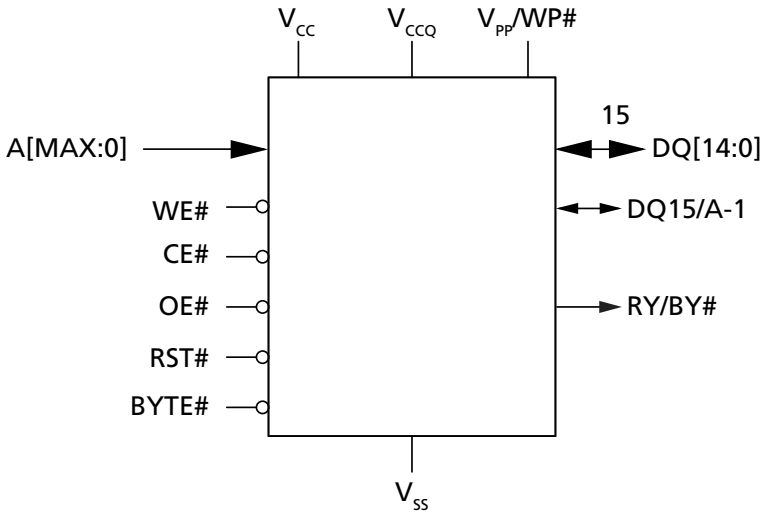
The device is an asynchronous, uniform block, parallel NOR Flash memory device. READ, ERASE, and PROGRAM operations are performed using a single low-voltage supply. Upon power-up, the device defaults to read array mode.

The main memory array is divided into uniform blocks that can be erased independently so that valid data can be preserved while old data is purged. PROGRAM and ERASE commands are written to the command interface of the memory. An on-chip program/erase controller simplifies the process of programming or erasing the memory by taking care of all special operations required to update the memory contents. The end of a PROGRAM or ERASE operation can be detected and any error condition can be identified. The command set required to control the device is consistent with JEDEC standards.

CE#, OE#, and WE# control the bus operation of the device and enable a simple connection to most microprocessors, often without additional logic.

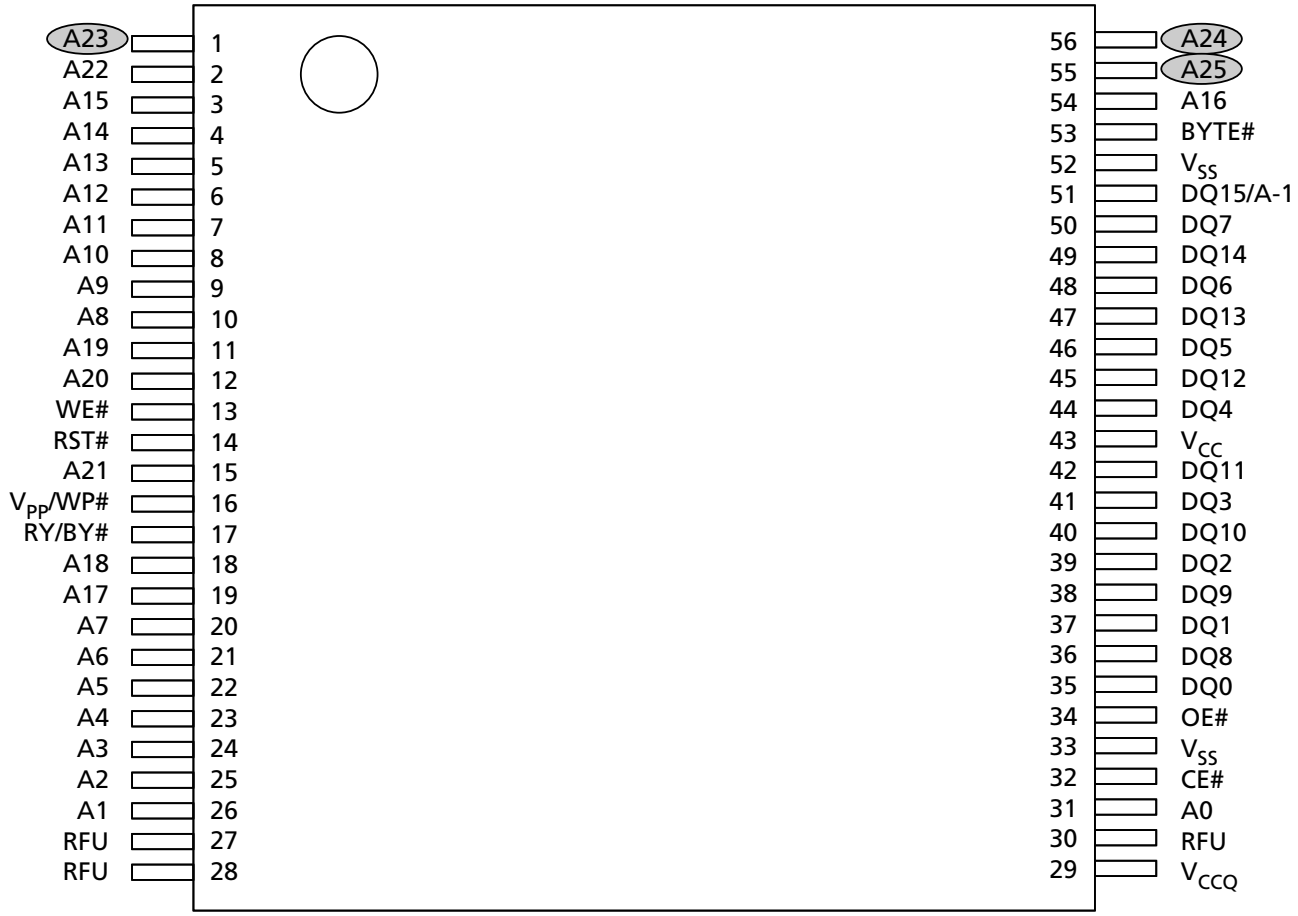
The device supports asynchronous random read and page read from all blocks of the array. It also features an internal program buffer that improves throughput by programming 512 words via one command sequence. A 128-word extended memory block overlaps addresses with array block 0. Users can program this additional space and then protect it to permanently secure the contents. The device also features different levels of hardware and software protection to secure blocks from unwanted modification.

Figure 2: Logic Diagram



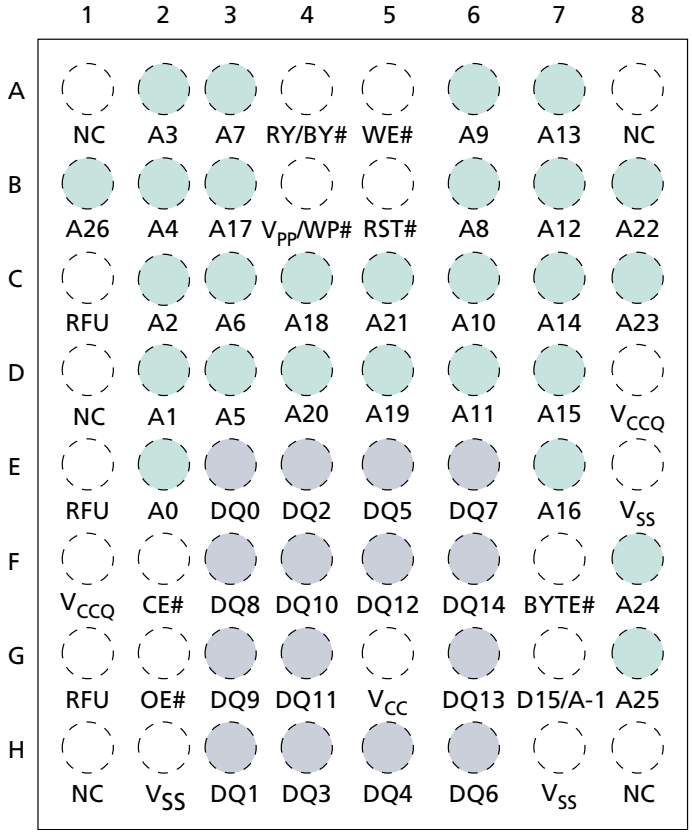
Signal Assignments

Figure 3: 56-Pin TSOP (Top View)



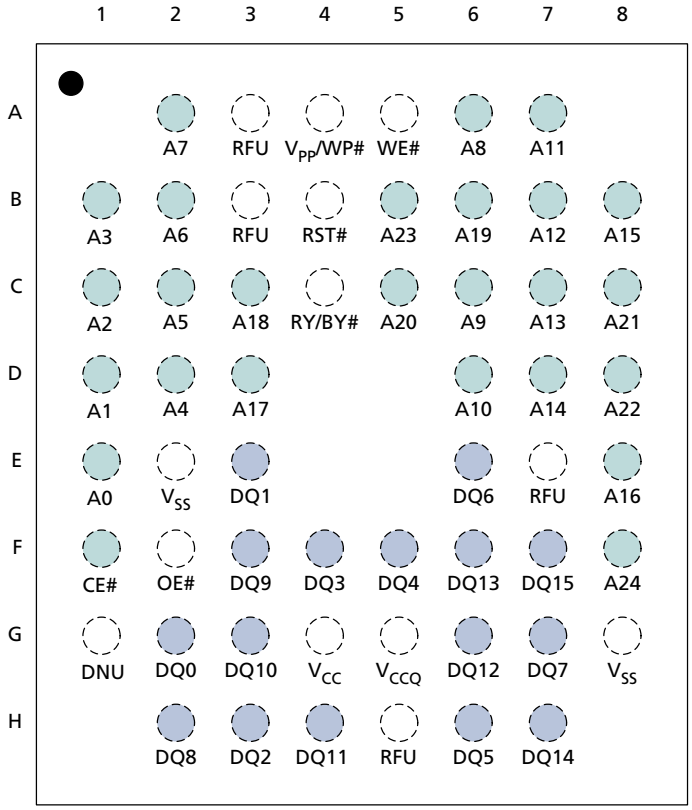
Notes:
1. A-1 is the least significant address bit in x8 mode.
2. A23 is valid for 256Mb and above; otherwise, it is RFU.
3. A24 is valid for 512Mb and above; otherwise, it is RFU.
4. A25 is valid for 1Gb and above; otherwise, it is RFU.

Figure 4: 64-Ball LBGA (Top View – Balls Down)



Notes:
1. A-1 is the least significant address bit in x8 mode.
2. A23 is valid for 256Mb and above; otherwise, it is RFU.
3. A24 is valid for 512Mb and above; otherwise, it is RFU.
4. A25 is valid for 1Gb and above; otherwise, it is RFU.

Figure 5: 56-Ball VFBGA (Top View – Balls Down)



Notes:
1. A-1 is the least significant address bit in x8 mode.
2. A23 is valid for 256Mb and above; otherwise, it is RFU.
3. A24 is valid for 512Mb and above; otherwise, it is RFU.
4. A25 is valid for 1Gb and above; otherwise, it is RFU.

Signal Descriptions

The signal description table below is a comprehensive list of signals for this device family. All signals listed may not be supported on this device. See Signal Assignments for information specific to this device.

Table 1: Signal Descriptions

Name	Type	Description
A[MAX:0]	Input	**Address:** Selects array cells to access during READ operations. Controls commands sent to the program/erase controller command interface during WRITE operations.
CE#	Input	**Chip enable:** Activates the device, enabling READ and WRITE operations. When CE# is HIGH, the device goes to standby and data outputs are High-Z.
OE#	Input	**Output enable:** Active LOW input. OE# LOW enables data output buffers during READ cycles. When OE# is HIGH, data outputs are High-Z.
WE#	Input	**Write enable:** Controls WRITE operations to the device. Address is latched on the falling edge of WE# and data is latched on the rising edge.
V_{PP}/WP#	Input	**V_{PP}/Write Protect:** Provides WRITE PROTECT and V_{HH} functionality, which protects the lowest or highest block and enables the device to enter unlock bypass mode.
BYTE#	Input	**Byte/word organization select:** Selects x8 or x16 bus mode. When BYTE# is LOW, the device is in x8 mode and when HIGH, the device is in x16 mode. Under byte configuration, BYTE# should not be toggled during any WRITE operation. Caution: This pin cannot be floated.
RST#	Input	**Reset:** When held LOW for at least ^{t}PLPH, applies a hardware reset to the device control logic and places it in standby. After RST# goes HIGH, the device is ready for READ and WRITE operations; that is, after ^{t}PHEL or ^{t}PHWL, whichever occurs last.
DQ[7:0]	I/O	**Data I/O:** During a READ operation, outputs data stored at the selected address. During a WRITE operation, represents the commands sent to the command interface.
DQ[14:8]	I/O	**Data I/O:** During a READ operation when BYTE# is HIGH, outputs data stored at the selected address. When BYTE# is LOW, these pins are High-Z and not used. During a WRITE operation, these bits are not used. When reading the data polling register, these bits should be ignored.
DQ15/A-1	I/O	**Data I/O or address input:** When device is in x16 bus mode, this pin behaves as data I/O, together with DQ[14:8]. When device is in x8 bus mode, this pin behaves as the least significant bit of the address. Unless explicitly stated elsewhere, DQ15 = data I/O (x16 mode) and A-1 = address input (x8 mode).
RY/BY#	Output	**Ready busy:** Open-drain output used to identify when the device is performing a PROGRAM or ERASE operation. During a PROGRAM or ERASE operation, RY/BY# is LOW. During read, auto select, and erase suspend modes, RY/BY# is High-Z. Enables RY/BY# pins from several devices to be connected to a single pull-up resistor which is connected to V_{CCQ}. Therefore, RYBY# LOW indicates when one or more of the devices are busy. A 10K Ohm or bigger resistor is recommended as pull-up resistor to achieve 0.1V V_{OL}.
V_{CC}	Supply	**Supply voltage:** Provides power supply for READ, PROGRAM, and ERASE operations. When $V_{CC} \le V_{LKO}$, the device is disabled, any PROGRAM or ERASE operation is aborted, and any altered content will be invalid. Capacitors of 0.1µF and 0.01µF should be connected between V_{CC} and V_{SS} to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during PROGRAM and ERASE operations.

Table 1: Signal Descriptions (Continued)

Name	Type	Description
V_{CCQ}	Supply	**I/O supply voltage:** Provides power supply to the I/O pins and enables all outputs to be powered independently from V_{CC}. Capacitors of 0.1µF and 0.01µF should be connected between V_{CCQ} and V_{SS} to decouple the current surges from the power supply.
V_{SS}	Supply	**Ground:** All V_{SS} pins must be connected to system ground.
RFU	—	**Reserved for future use:** Reserved by Micron for future device functionality and enhancement. Should be treated as a DNU signal.
DNU	—	**Do not use:** Do not connect to any other signal or power supply; Must be left floating.
NC	—	**No connect:** No internal connection; Can be driven or floated.

Memory Organization

Memory Configuration

The main memory array is divided into 128KB or 64KW uniform blocks.

Memory Map

Table 2: Blocks[2047:0]

Block	Block Size	Address Range (x8)		Block Size	Address Range (x16)	
		Start	End		Start	End
2047	128KB	FFE 0000h	FFF FFFFh	64KW	7FF 0000h	7FF FFFFh
⋮		⋮	⋮		⋮	⋮
1023		7FE 0000h	7FF FFFFh		3FF 0000h	3FF FFFFh
⋮		⋮	⋮		⋮	⋮
511		3FE 0000h	3FF FFFFh		1FF 0000h	1FF FFFFh
⋮		⋮	⋮		⋮	⋮
255		1FE 0000h	1FF FFFFh		0FF 0000h	0FF FFFFh
⋮		⋮	⋮		⋮	⋮
127		0FE 0000h	0FF FFFFh		07F 0000h	07F FFFFh
⋮		⋮	⋮		⋮	⋮
63		07E 0000h	07F FFFFh		03F 0000h	03F FFFFh
⋮		⋮	⋮		⋮	⋮
0		000 0000h	001 FFFFh		000 0000h	000 FFFFh

Note: 1. 128Mb device = Blocks 0–127; 256Mb device = Blocks 0–255; 512Mb device = Blocks 0–511; 1Gb device = Blocks 0–1023; 2Gb device = Blocks 0–2047.

Bus Operations

Table 3: Bus Operations

Notes 1 and 2 apply to entire table

Operation	CE#	OE#	WE#	RST#	V_{PP}/WP#	8-Bit Mode			16-Bit Mode	
						A[MAX:0], DQ15/A-1	DQ[14:8]	DQ[7:0]	A[MAX:0]	DQ15/A-1, DQ[14:0]
READ	L	L	H	H	X	Address	High-Z	Data output	Address	Data output
WRITE	L	H	L	H	H[3]	Command address	High-Z	Data input[4]	Command address	Data input[4]
STANDBY	H	X	X	H	X	X	High-Z	High-Z	X	High-Z
OUTPUT DISABLE	L	H	H	H	X	X	High-Z	High-Z	X	High-Z
RESET	X	X	X	L	X	X	High-Z	High-Z	X	High-Z

Notes:
1. Typical glitches of less than 3ns on CE#, OE#, and WE# are ignored by the device and do not affect bus operations.
2. H = Logic level HIGH (V_{IH}); L = Logic level LOW (V_{IL}); X = HIGH or LOW.
3. If WP# is LOW, then the highest or the lowest block remains protected, depending on line item.
4. Data input is required when issuing a command sequence or when performing data polling or block protection.

Read

Bus READ operations read from the memory cells, registers, extended memory block, or CFI space. To accelerate the READ operation, the memory array can be read in page mode where data is internally read and stored in a page buffer.

Page size is 16 words (32 bytes) and is addressed by address inputs A[3:0] in x16 bus mode and A[3:0] plus DQ15/A-1 in x8 bus mode. The extended memory blocks and CFI area support page read mode.

A valid bus READ operation involves setting the desired address on the address inputs, taking CE# and OE# LOW, and holding WE# HIGH. The data I/Os will output the value. If CE# goes HIGH and returns LOW for a subsequent access, a random read access is performed and ^{t}ACC or ^{t}CE is required. (See AC Characteristics for details about when the output becomes valid).

Write

Bus WRITE operations write to the command interface. A valid bus WRITE operation begins by setting the desired address on the address inputs. The address inputs are latched by the command interface on the falling edge of CE# or WE#, whichever occurs last. The data I/Os are latched by the command interface on the rising edge of CE# or WE#, whichever occurs first. OE# must remain HIGH during the entire bus WRITE operation (See AC Characteristics for timing requirement details).

Standby

Driving CE# HIGH in read mode causes the device to enter standby and data I/Os to be High-Z (See DC Characteristics).

During PROGRAM or ERASE operations, the device will continue to use the program/erase supply current (I_{CC3}) until the operation completes. The device cannot be placed into standby mode during a PROGRAM/ERASE operation.

Output Disable

Data I/Os are High-Z when OE# is HIGH.

Reset

During reset mode the device is deselected and the outputs are High-Z. The device is in reset mode when RST# is LOW. The power consumption is reduced to the standby level, independently from CE#, OE#, or WE# inputs.

When RST# is HIGH, a time of ^{t}PHEL is required before a READ operation can access the device, and a delay of ^{t}PHWL is required before a write sequence can be initiated. After this wake-up interval, normal operation is restored, the device defaults to read array mode, and the data polling register is reset.

If RST# is driven LOW during a PROGRAM/ERASE operation or any other operation that requires writing to the device, the operation will abort within ^{t}PLRH, and memory contents at the aborted block or address are no longer valid.

Registers

Data Polling Register

Table 4: Data Polling Register Bit Definitions

Note 1 applies to entire table

Bit	Name	Settings	Description	Notes
DQ7	Data polling bit	0 or 1, depending on operations	Monitors whether the program/erase controller has successfully completed its operation, or has responded to an ERASE SUSPEND operation.	2, 4
DQ6	Toggle bit	Toggles: 0 to 1; 1 to 0; and so on	Monitors whether the program, erase, or blank check controller has successfully completed its operations, or has responded to an ERASE SUSPEND operation. During a PROGRAM/ERASE/BLANK CHECK operation, DQ6 toggles from 0 to 1, 1 to 0, and so on, with each successive READ operation from any address.	3, 4, 5
DQ5	Error bit	0 = Success 1 = Failure	Identifies errors detected by the program/erase controller. DQ5 is set to 1 when a PROGRAM, BLOCK ERASE, or CHIP ERASE operation fails to write the correct data to the memory, or when a BLANK CHECK or CRC operation fails.	4, 6
DQ3	Erase timer bit	0 = Erase not in progress 1 = Erase in progress	Identifies the start of program/erase controller operation during a BLOCK ERASE command. Before the program/erase controller starts, this bit set to 0, and additional blocks to be erased can be written to the command interface.	4
DQ2	Alternative toggle bit	Toggles: 0 to 1; 1 to 0; and so on	During CHIP ERASE, BLOCK ERASE, and ERASE SUSPEND operations, DQ2 toggles from 0 to 1, 1 to 0, and so on, with each successive READ operation from addresses within the blocks being erased.	3, 4
DQ1	Buffered program abort bit	1 = Abort	Indicates a BUFFER PROGRAM, EFI BLANK CHECK, or CRC operation abort. The BUFFERED PROGRAM ABORT and RESET command must be issued to return the device to read mode (see WRITE TO BUFFER PROGRAM command).	–

Notes:
1. The data polling register can be read during PROGRAM, ERASE, or ERASE SUSPEND operations; the READ operation outputs data on DQ[7:0].
2. For a PROGRAM operation in progress, DQ7 outputs the complement of the bit being programmed. For a READ operation from the address previously programmed successfully, DQ7 outputs existing DQ7 data. For a READ operation from addresses with blocks to be erased while an ERASE SUSPEND operation is in progress, DQ7 outputs 0; upon successful completion of the ERASE SUSPEND operation, DQ7 outputs 1. For an ERASE operation in progress, DQ7 outputs 0; upon ERASE operation's successful completion, DQ7 outputs 1. During a BUFFER PROGRAM operation, the data polling bit is valid only for the last word being programmed in the write buffer.
3. After successful completion of a PROGRAM, ERASE, or BLANK CHECK operation, the device returns to read mode.
4. During erase suspend mode, READ operations to addresses within blocks not being erased output memory array data as if in read mode. A protected block is treated the same as a block not being erased. See the Toggle Flowchart for more information.

5. During erase suspend mode, DQ6 toggles when addressing a cell within a block being erased. The toggling stops when the program/erase controller has suspended the ERASE operation. See the Toggle Flowchart for more information.
6. When DQ5 is set to 1, a READ/RESET (F0h) command must be issued before any subsequent command.

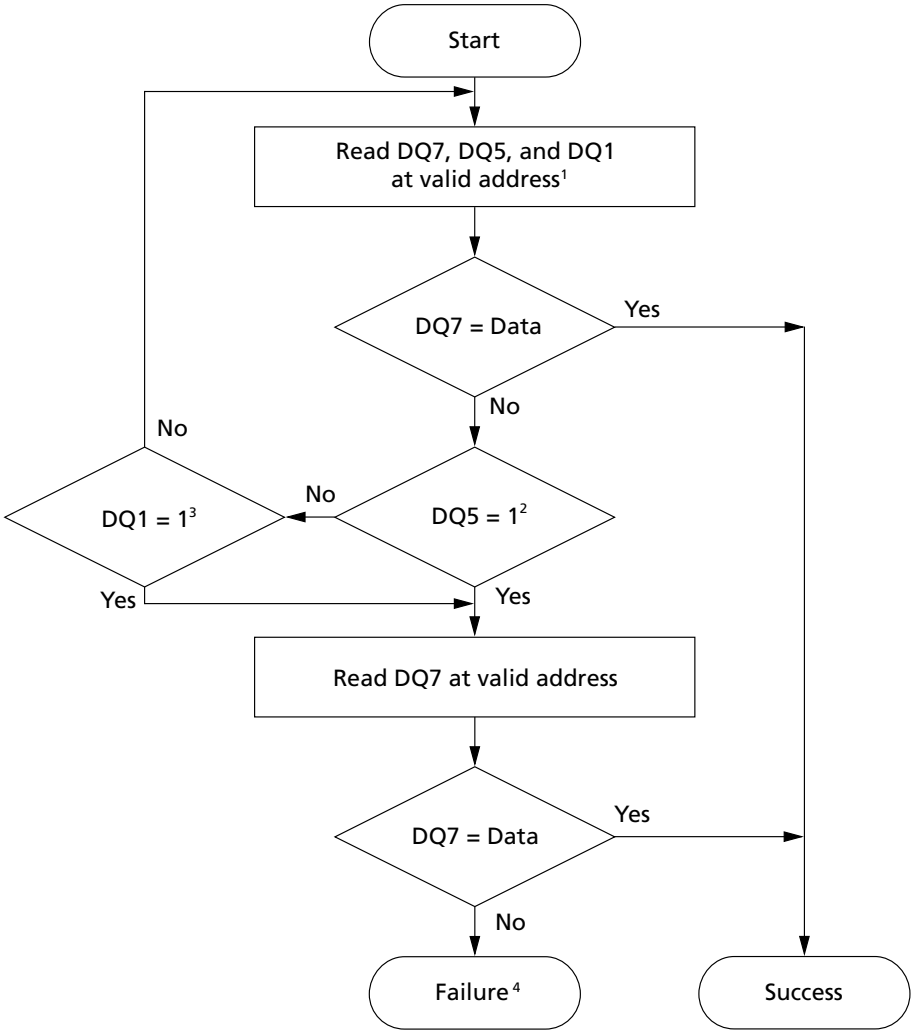
Table 5: Operations and Corresponding Bit Settings

Note 1 applies to entire table

Operation	Address	DQ7	DQ6	DQ5	DQ3	DQ2	DQ1	RY/BY#	Notes
PROGRAM	Any address	DQ7#	Toggle	0	–	–	0	0	2
EFI BLANK CHECK	Any address	1	Toggle	0	–	–	0	0	3
CRC range of blocks	Any address	1	Toggle	0	–	–	0	0	
CRC chip	Any address	DQ7#	Toggle	0	–	–	0	0	4
CHIP ERASE	Any address	0	Toggle	0	1	Toggle	–	0	–
BLOCK ERASE before time-out	Erasing block	0	Toggle	0	0	Toggle	–	0	–
	Non-erasing block	0	Toggle	0	0	No toggle	–	0	–
BLOCK ERASE	Erasing block	0	Toggle	0	1	Toggle	–	0	–
	Non-erasing block	0	Toggle	0	1	No toggle	–	0	–
PROGRAM SUSPEND	Programming block	Invalid operation						High-Z	–
	Nonprogramming block	Outputs memory array data as if in read mode						High-Z	–
ERASE SUSPEND	Erasing block	1	No Toggle	0	–	Toggle	–	High-Z	–
	Non-erasing block	Outputs memory array data as if in read mode						High-Z	–
PROGRAM during ERASE SUSPEND	Erasing block	DQ7#	Toggle	0	–	Toggle	–	0	2
	Non-erasing block	DQ7#	Toggle	0	–	No Toggle	–	0	2
BUFFERED PROGRAM ABORT	Any address	DQ7#	Toggle	0	–	–	1	High-Z	–
PROGRAM Error	Any address	DQ7#	Toggle	1	–	–	–	High-Z	2
ERASE Error	Any address	0	Toggle	1	1	Toggle	–	High-Z	–
EFI BLANK CHECK Error	Any address	0	Toggle	1	1	Toggle	–	High-Z	–
CRC range of blocks error	Any address	1	Toggle	1	–	–	–	High-Z	–
CRC chip error	Any address	DQ7#	Toggle	1	–	–	–	High-Z	4

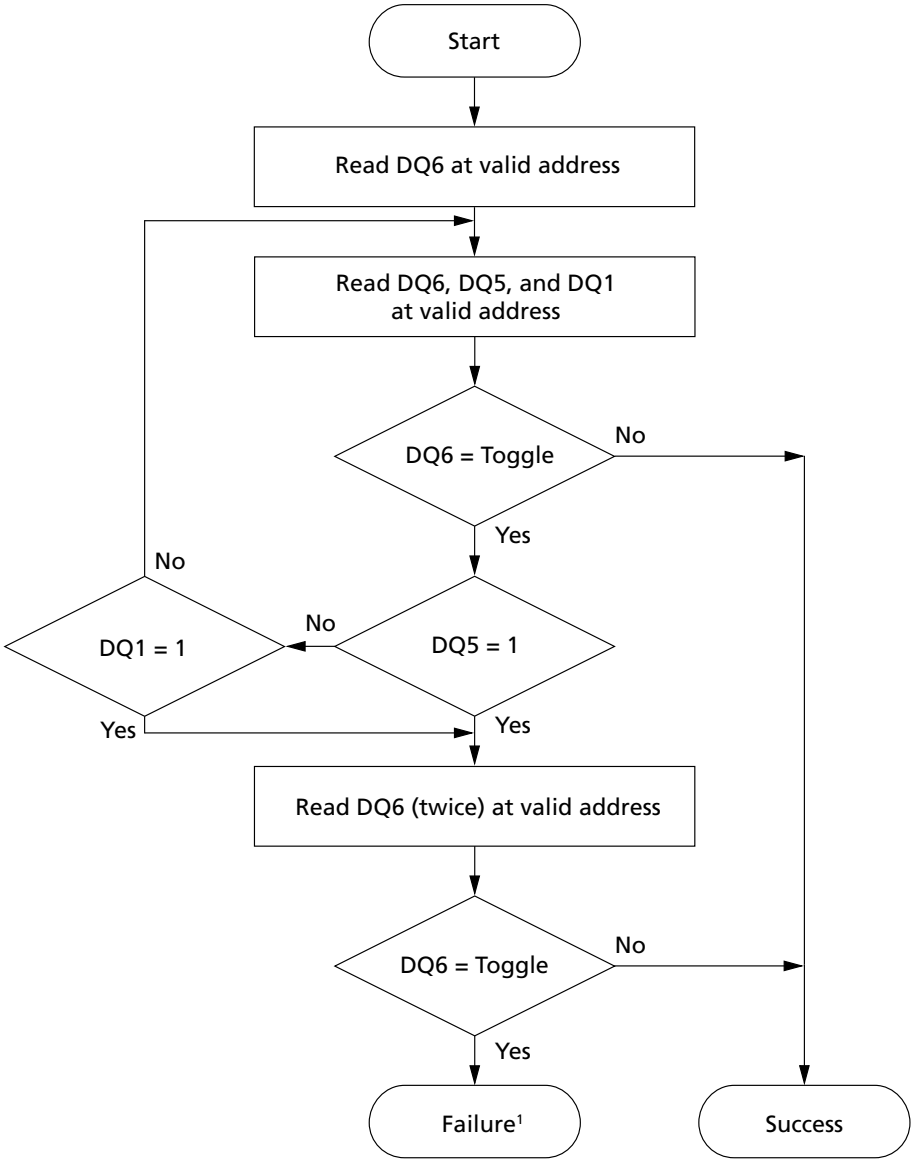
Notes:
1. Unspecified data bits should be ignored.
2. DQ7# for buffer program is related to the last address location loaded.
3. EFI = enhanced Flash interface.
4. DQ7# is the reverse DQ7 of the last word or byte loaded before CRC chip confirm command cycle.

Figure 6: Data Polling Flowchart



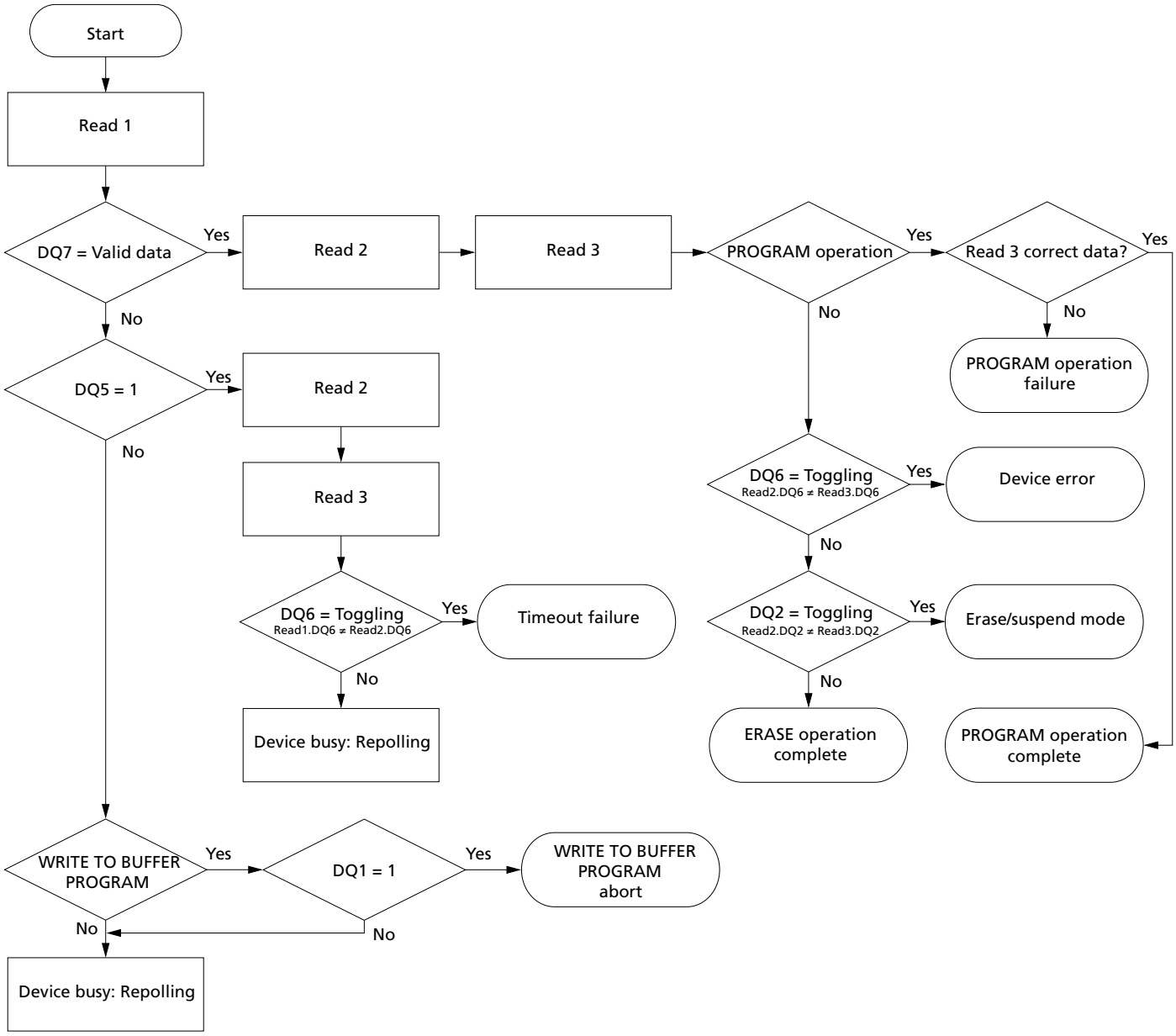
Notes:
1. Valid address is the last address being programmed or an address within the block being erased.
2. Failure results: DQ5 = 1 indicates an operation error. A READ/RESET (F0h) command must be issued before any subsequent command.
3. Failure results: DQ1 = 1 indicates a WRITE TO BUFFER PROGRAM ABORT operation. A full three-cycle RESET (AAh/55h/F0h) command sequence must be used to reset the aborted device.
4. The data polling process does not support the BLANK CHECK operation. The process represented in the Toggle Bit Flowchart figure can provide information on the BLANK CHECK operation.

Figure 7: Toggle Bit Flowchart



Notes:
1. Failure results: DQ5 = 1 indicates an operation error; DQ1 = 1 indicates a WRITE TO BUFFER PROGRAM ABORT operation.
2. The toggle bit process supports the BLANK CHECK operation.

Figure 8: Data Polling/Toggle Bit Flowchart



Lock Register

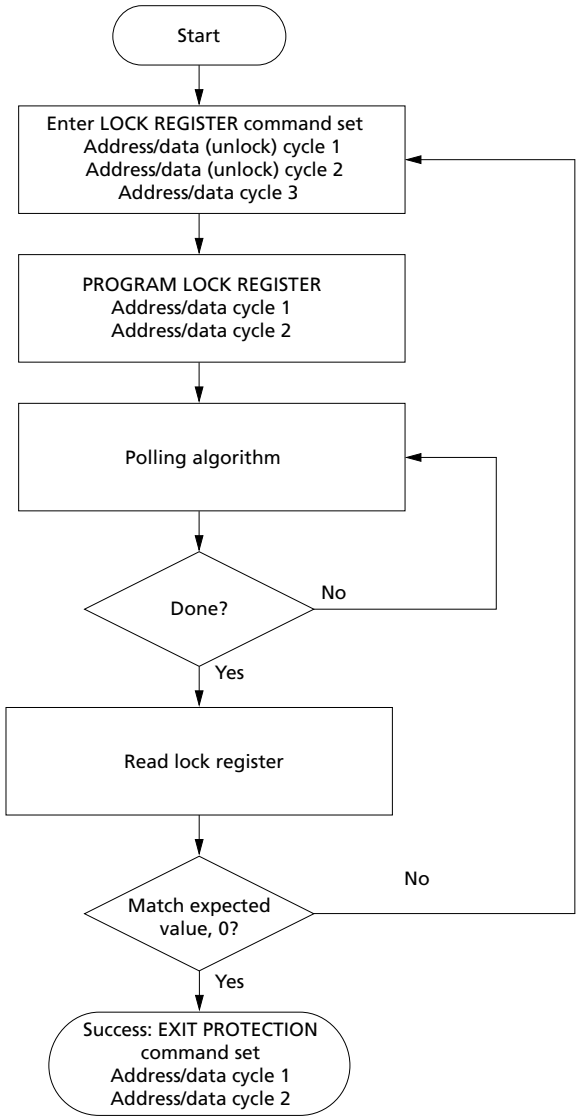
Table 6: Lock Register Bit Definitions

Note 1 applies to entire table

Bit	Name	Settings	Description	Notes
DQ2	Password protection mode lock bit	0 = Password protection mode enabled 1 = Password protection mode disabled (Default)	Places the device permanently in password protection mode.	2
DQ1	Nonvolatile protection mode lock bit	0 = Nonvolatile protection mode enabled with password protection mode permanently disabled 1 = Nonvolatile protection mode enabled (Default)	Places the device in nonvolatile protection mode with password protection mode permanently disabled. When shipped from the factory, the device will operate in nonvolatile protection mode, and the memory blocks are unprotected.	2
DQ0	Extended memory block protection bit	0 = Protected 1 = Unprotected (Default)	If the device is shipped with the extended memory block unlocked, the block can be protected by setting this bit to 0. The extended memory block protection status can be read in auto select mode by issuing an AUTO SELECT command.	–

Notes:
1. The lock register is a 16-bit, one-time programmable register. DQ[15:3] are reserved and are set to a default value of 1.
2. The password protection mode lock bit and nonvolatile protection mode lock bit cannot both be programmed to 0. Any attempt to program one while the other is programmed causes the operation to abort, and the device returns to read mode. The device is shipped from the factory with the default setting.

Figure 9: Lock Register Program Flowchart



Notes:
1. Each lock register bit can be programmed only once.
2. See the Block Protection Command Definitions table for address-data cycle details.
3. DQ5 and DQ1 are ignored in this algorithm flow.

Standard Command Definitions – Address-Data Cycles

Table 7: Standard Command Definitions – Address-Data Cycles, 8-Bit and 16-Bit

Note 1 applies to entire table

Command and Code/Subcode	Bus Size	Address and Data Cycles												Notes
		1st		2nd		3rd		4th		5th		6th		
		A	D	A	D	A	D	A	D	A	D	A	D	
READ and AUTO SELECT Operations														
READ/RESET (F0h)	x8	X	F0											2
		AAA	AA	555	55	X	F0							
	x16	X	F0											
		555	AA	2AA	55	X	F0							
READ CFI (98h)	x8	AAA	98											
	x16	555												
EXIT READ CFI (F0h)	x8	X	F0											
	x16													
AUTO SELECT (90h)	x8	AAA	AA	555	55	AAA	90	Note 3	Note 3					4, 5
	x16	555		2AA		555								
EXIT AUTO SELECT (F0h)	x8	X	F0											
	x16													
BYPASS Operations														
UNLOCK BYPASS (20h)	x8	AAA	AA	555	55	AAA	20							
	x16	555		2AA		555								
UNLOCK BYPASS RESET (90h/00h)	x8	X	90	X	00									
	x16													
PROGRAM Operations														
PROGRAM (A0h)	x8	AAA	AA	555	55	AAA	A0	PA	PD					
	x16	555		2AA		555								
UNLOCK BYPASS PROGRAM (A0h)	x8	X	A0	PA	PD									6
	x16													
WRITE TO BUFFER PROGRAM (25h)	x8	AAA	AA	555	55	BAd	25	BAd	N	PA	PD			7, 8, 9
	x16	555		2AA										
UNLOCK BYPASS WRITE TO BUFFER PROGRAM (25h)	x8	BAd	25	BAd	N	PA	PD							6
	x16													
WRITE TO BUFFER PROGRAM CONFIRM (29h)	x8	BAd	29											7
	x16													
BUFFERED PROGRAM ABORT and RESET (F0h)	x8	AAA	AA	555	55	AAA	F0							
	x16	555		2AA		555								
PROGRAM SUSPEND (B0h)	x8	X	B0											
	x16													

Table 7: Standard Command Definitions – Address-Data Cycles, 8-Bit and 16-Bit (Continued)

Note 1 applies to entire table

Command and Code/Subcode	Bus Size	Address and Data Cycles												Notes
		1st		2nd		3rd		4th		5th		6th		
		A	D	A	D	A	D	A	D	A	D	A	D	
PROGRAM RESUME (30h)	x8	X	30											
	x16													
ERASE Operations														
CHIP ERASE (80/10h)	x8	AAA	AA	555	55	AAA	80	AAA	AA	555	55	AAA	10	
	x16	555		2AA		555		555		2AA		555		
UNLOCK BYPASS CHIP ERASE (80/10h)	x8	X	80	X	10									6
	x16													
BLOCK ERASE (80/30h)	x8	AAA	AA	555	55	AAA	80	AAA	AA	555	55	BAd	30	10
	x16	555		2AA		555		555		2AA				
UNLOCK BYPASS BLOCK ERASE (80/30h)	x8	X	80	BAd	30									6
	x16													
ERASE SUSPEND (B0h)	x8	X	B0											
	x16													
ERASE RESUME (30h)	x8	X	30											
	x16													
Enhanced Flash Interface (EFI) BLANK CHECK Operations														
EFI BLANK CHECK SETUP (EB/76h)	x8	AAA	AA	555	55	BAd + 00	EB	BAd + 00	76	BAd + 00	00	BAd + 00	00	
	x16	555		2AA										
EFI BLANK CHECK CONFIRM and READ (29h)	x8	BAd + 00	29											
	x16													

Notes:
1. A = Address; D = Data; X = "Don't Care"; BAd = Any address in the block; N = Number of bytes (x8) or words (x16) to be programmed; PA = Program address; PD = Program data; Gray shading = Not applicable. All values in the table are hexadecimal. Some commands require both a command code and subcode.
2. A full three-cycle RESET command sequence must be used to reset the device in the event of a buffered program abort error (DQ1 = 1).
3. These cells represent READ cycles (versus WRITE cycles for the others).
4. AUTO SELECT enables the device to read the manufacturer code, device code, block protection status, and extended memory block protection indicator.
5. AUTO SELECT addresses and data are specified in the Electronic Signature table and the Extended Memory Block Protection table.
6. For any UNLOCK BYPASS ERASE/PROGRAM command, the first two UNLOCK cycles are unnecessary.
7. BAd must be the same as the address loaded during the WRITE TO BUFFER PROGRAM 3rd and 4th cycles.
8. WRITE TO BUFFER PROGRAM operation: maximum cycles = 261 (x8) and 517 (x16). UNLOCK BYPASS WRITE TO BUFFER PROGRAM operation: maximum cycles = 259 (x8), 515

(x16). WRITE TO BUFFER PROGRAM operation: N + 1 = bytes (x8) or words (x16) to be programmed; maximum buffer size = 256 bytes (x8) and 512 words (x16).

9. For x8, A[MAX:7] address pins should remain unchanged while A[6:0] and A-1 pins are used to select a byte within the N + 1 byte page. For x16, A[MAX:9] address pins should remain unchanged while A[8:0] pins are used to select a word within the N+1 word page.
10. BLOCK ERASE address cycles can extend beyond six address-data cycles, depending on the number of blocks to erase.