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PIC18F87J90 Family Data Sheet

**64/80-Pin, High-Performance
Microcontrollers with LCD Driver
and nanoWatt Technology**

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MICROCHIP

PIC18F87J90 FAMILY

64/80-Pin, High-Performance Microcontrollers with LCD Driver and nanoWatt Technology

LCD Driver and Keypad Interface

Features:

- Direct LCD Panel Drive Capability:
 - Can drive LCD panel while in Sleep mode
- Up to 48 Segments and 192 Pixels, Software Selectable
- Programmable LCD Timing module:
 - Multiple LCD timing sources available
 - Up to four commons: static, 1/2, 1/3 or 1/4 multiplex
 - Static, 1/2 or 1/3 bias configuration
- On-Chip LCD Boost Voltage Regulator for Contrast Control
- Charge Time Measurement Unit (CTMU) for Capacitive Touch Sensing
- ADC for Resistive Touch Sensing

Low-Power Features:

- Power-Managed modes:
 - Run: CPU On, Peripherals On
 - Idle: CPU Off, Peripherals On
 - Sleep: CPU Off, Peripherals Off
- Two-Speed Oscillator Start-up

Flexible Oscillator Structure:

- Two Crystal modes, 4-25 MHz
- Two External Clock modes, up to 48 MHz
- 4x Phase Lock Loop (PLL)
- Internal Oscillator Block with PLL:
 - Eight user-selectable frequencies from 31.25 kHz to 8 MHz
- Secondary Oscillator using Timer1 at 32 kHz
- Fail-Safe Clock Monitor:
 - Allows for safe shutdown if peripheral clock fails

Peripheral Highlights:

- High-Current Sink/Source 25 mA/25 mA (PORTB and PORTC)
- Up to Four External Interrupts
- Four 8-Bit/16-Bit Timer/Counter modules
- Two Capture/Compare/PWM (CCP) modules
- Master Synchronous Serial Port (MSSP) module with Two Modes of Operation:
 - 3-Wire/4-Wire SPI (supports all four SPI modes)
 - I²C™ Master and Slave mode
- One Addressable USART module
- One Enhanced Addressable USART module:
 - LIN/J2602 support
 - Auto-wake-up on Start bit and Break character
 - Auto-Baud Detect (ABD)
- 10-Bit, up to 12-Channel A/D Converter:
 - Auto-acquisition
 - Conversion available during Sleep
- Two Analog Comparators
- Programmable Reference Voltage for Comparators
- Hardware Real-Time Clock and Calendar (RTCC) with Clock, Calendar and Alarm Functions
- Charge Time Measurement Unit (CTMU):
 - Capacitance measurement
 - Time measurement with 1 ns typical resolution

Special Microcontroller Features:

- 10,000 Erase/Write Cycle Flash Program Memory, Typical
- Flash Retention 20 Years, Minimum
- Self-Programmable under Software Control
- Word Write Capability for Flash Program Memory for Data EEPROM Emulators

Device	Flash Program Memory (Bytes)	SRAM Data Memory (Bytes)	I/O	LCD (Pixels)	Timers 8/16-Bit	CCP	MSSP		EUSART AUSART	10-Bit A/D (Channels)	Comparators	BOR/LVD	RTCC	CTMU
							SPI	Master I ² C™						
PIC18F66J90	64K	3,923	51	132	1/3	2	Yes	Yes	1/1	12	2	Yes	Yes	Yes
PIC18F67J90	128K	3,923	51	132	1/3	2	Yes	Yes	1/1	12	2	Yes	Yes	Yes
PIC18F86J90	64K	3,923	67	192	1/3	2	Yes	Yes	1/1	12	2	Yes	Yes	Yes
PIC18F87J90	128K	3,923	67	192	1/3	2	Yes	Yes	1/1	12	2	Yes	Yes	Yes

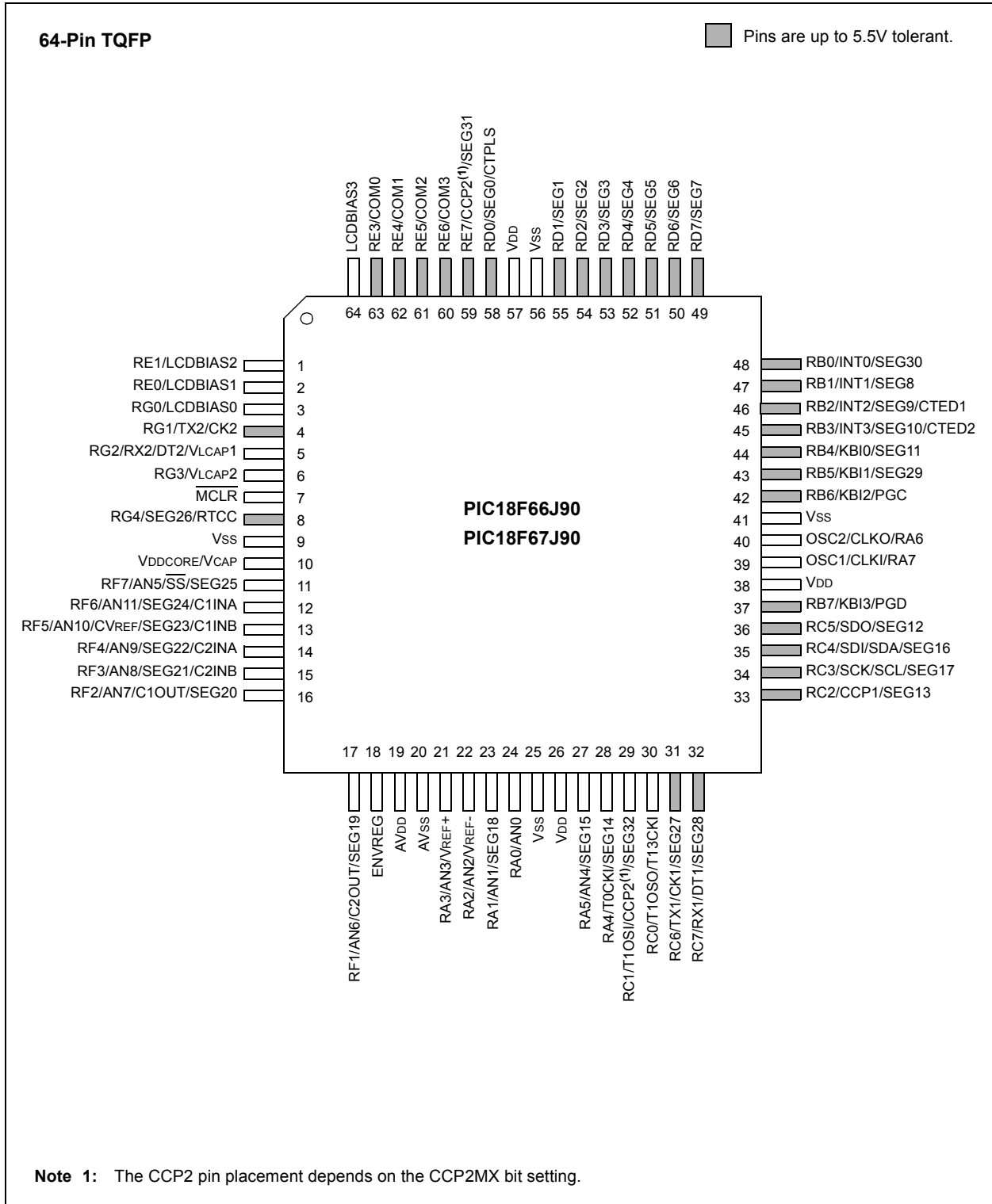
PIC18F87J90 FAMILY

Special Microcontroller Features (Continued):

- Priority Levels for Interrupts
- 8 x 8 Single-Cycle Hardware Multiplier
- Extended Watchdog Timer (WDT):
 - Programmable period from 4 ms to 131s
- In-Circuit Serial Programming™ (ICSP™) via Two Pins
- In-Circuit Debug via Two Pins
- Operating Voltage Range: 2.0V to 3.6V
- 5.5V Tolerant Input (digital pins only)
- Selectable Open-Drain Configuration for Serial Communication and CCP Pins for Driving Outputs up to 5V
- On-Chip 2.5V Regulator

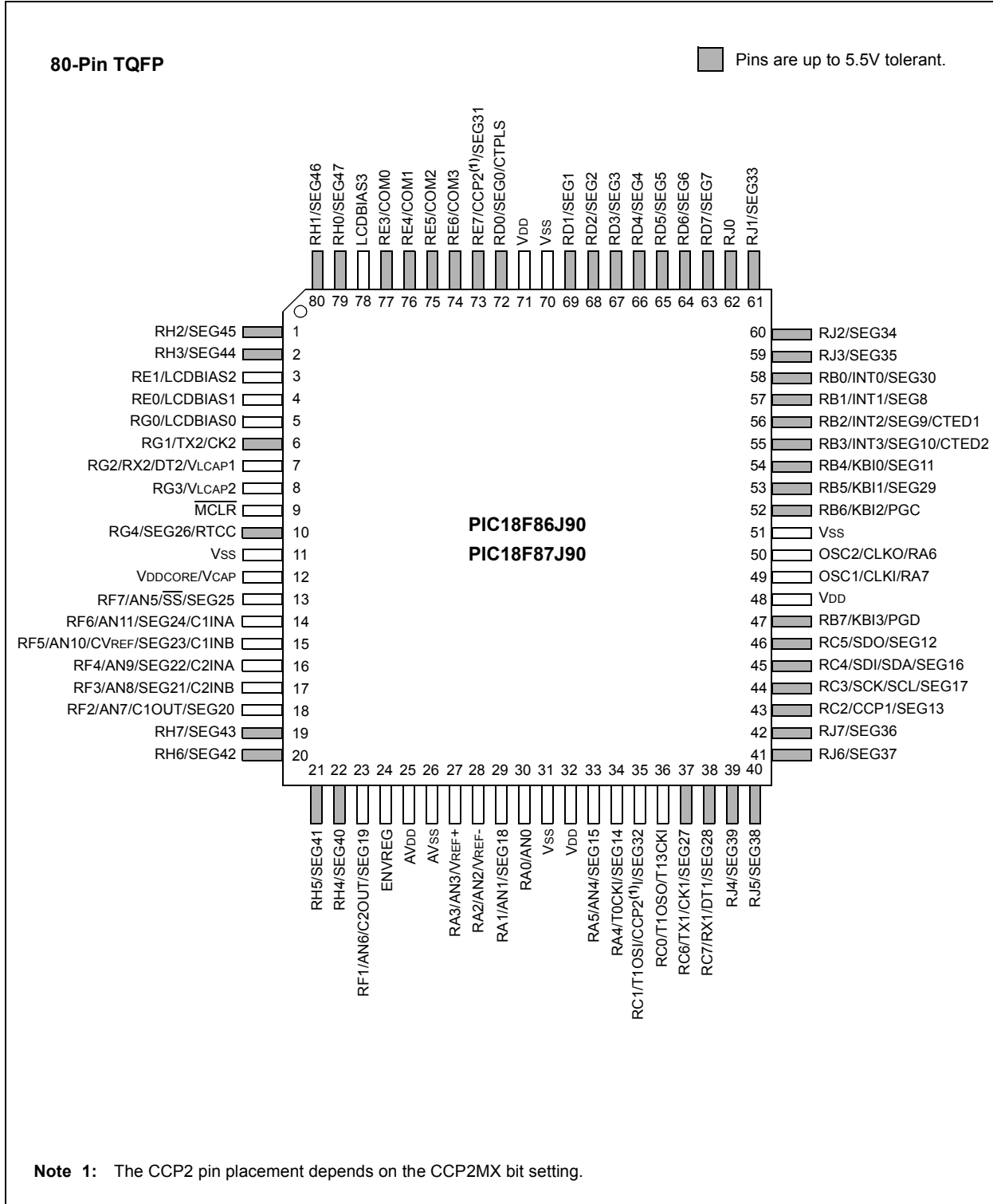
PIC18F87J90 FAMILY

Pin Diagrams – PIC18F6XJ90



PIC18F87J90 FAMILY

Pin Diagrams – PIC18F8XJ90



Note 1: The CCP2 pin placement depends on the CCP2MX bit setting.

PIC18F87J90 FAMILY

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1.0 DEVICE OVERVIEW

This document contains device-specific information for the following devices:

- PIC18F66J90
- PIC18F67J90
- PIC18F86J90
- PIC18F87J90

This family combines the traditional advantages of all PIC18 microcontrollers – namely, high computational performance and a rich feature set – with a versatile, on-chip LCD driver, while maintaining an extremely competitive price point. These features make the PIC18F87J90 family a logical choice for many high-performance applications where price is a primary consideration.

1.1 Core Features

1.1.1 nanoWatt TECHNOLOGY

All of the devices in the PIC18F87J90 family incorporate a range of features that can significantly reduce power consumption during operation. Key items include:

- **Alternate Run Modes:** By clocking the controller from the Timer1 source or the Internal RC oscillator, power consumption during code execution can be reduced by as much as 90%.
- **Multiple Idle Modes:** The controller can also run with its CPU core disabled but the peripherals still active. In these states, power consumption can be reduced even further, to as little as 4% of normal operation requirements.
- **On-the-Fly Mode Switching:** The power-managed modes are invoked by user code during operation, allowing the user to incorporate power-saving ideas into their application's software design.

1.1.2 OSCILLATOR OPTIONS AND FEATURES

All of the devices in the PIC18F87J90 family offer six different oscillator options, allowing users a range of choices in developing application hardware. These include:

- Two Crystal modes, using crystals or ceramic resonators.
- Two External Clock modes, offering the option of a divide-by-4 clock output.
- A Phase Lock Loop (PLL) frequency multiplier, available to the External Oscillator modes which allows clock speeds of up to 40 MHz. PLL can also be used with the internal oscillator.
- An internal oscillator block which provides an 8 MHz clock ($\pm 2\%$ accuracy) and an INTRC source (approximately 31 kHz, stable over temperature and VDD), as well as a range of six user-selectable clock frequencies, between 125 kHz to 4 MHz, for a total of eight clock frequencies. This option frees the two oscillator pins for use as additional general purpose I/O.

The internal oscillator block provides a stable reference source that gives the family additional features for robust operation:

- **Fail-Safe Clock Monitor:** This option constantly monitors the main clock source against a reference signal provided by the internal oscillator. If a clock failure occurs, the controller is switched to the internal oscillator, allowing for continued low-speed operation or a safe application shutdown.
- **Two-Speed Start-up:** This option allows the internal oscillator to serve as the clock source from Power-on Reset, or wake-up from Sleep mode, until the primary clock source is available.

1.1.3 MEMORY OPTIONS

The PIC18F87J90 family provides ample room for application code, from 64 Kbytes to 128 Kbytes of code space. The Flash cells for program memory are rated to last up to 10,000 erase/write cycles. Data retention without refresh is conservatively estimated to be greater than 20 years.

The Flash program memory is readable and writable. During normal operation, the PIC18F87J90 family also provides plenty of room for dynamic application data with up to 3,923 bytes of data RAM.

1.1.4 EXTENDED INSTRUCTION SET

The PIC18F87J90 family implements the optional extension to the PIC18 instruction set, adding 8 new instructions and an Indexed Addressing mode. Enabled as a device configuration option, the extension has been specifically designed to optimize re-entrant application code originally developed in high-level languages, such as 'C'.

1.1.5 EASY MIGRATION

Regardless of the memory size, all devices share the same rich set of peripherals, allowing for a smooth migration path as applications grow and evolve.

The consistent pinout scheme used throughout the entire family also aids in migrating to the next larger device. This is true when moving between the 64-pin members, between the 80-pin members, or even jumping from 64-pin to 80-pin devices.

The PIC18F87J90 family is also largely pin-compatible with other PIC18 families, such as the PIC18F8720 and PIC18F8722, the PIC18F85J11, and the PIC18F8490 and PIC18F85J90 families of microcontrollers with LCD drivers. This allows a new dimension to the evolution of applications, allowing developers to select different price points within Microchip's PIC18 portfolio, while maintaining a similar feature set.

PIC18F87J90 FAMILY

1.2 LCD Driver

The on-chip LCD driver includes many features that make the integration of displays in low-power applications easier. These include an integrated voltage regulator with charge pump that allows contrast control in software and display operation above device VDD.

1.3 Other Special Features

- **Communications:** The PIC18F87J90 family incorporates a range of serial communication peripherals, including an Addressable USART, a separate Enhanced USART that supports LIN/J2602 specification 1.2, and one Master SSP module capable of both SPI and I²C™ (Master and Slave) modes of operation.
- **CCP Modules:** All devices in the family incorporate two Capture/Compare/PWM (CCP) modules. Up to four different time bases may be used to perform several different operations at once.
- **10-Bit A/D Converter:** This module incorporates programmable acquisition time, allowing for a channel to be selected and a conversion to be initiated without waiting for a sampling period and thus, reducing code overhead.
- **Charge Time Measurement Unit (CTMU):** The CTMU is a flexible analog module that provides accurate differential time measurement between pulse sources, as well as asynchronous pulse generation.

Together with other on-chip analog modules, the CTMU can precisely measure time, measure capacitance or relative changes in capacitance, or generate output pulses that are independent of the system clock.

- **Extended Watchdog Timer (WDT):** This enhanced version incorporates a 16-bit prescaler, allowing an extended time-out range that is stable across operating voltage and temperature. See **Section 28.0 “Electrical Characteristics”** for time-out periods.
- **Real-Time Clock and Calendar Module (RTCC):** The RTCC module is intended for applications requiring that accurate time be maintained for extended periods of time with minimum to no intervention from the CPU.

The module is a 100-year clock and calendar with automatic leap year detection. The range of the clock is from 00:00:00 (midnight) on January 1, 2000 to 23:59:59 on December 31, 2099.

1.4 Details on Individual Family Members

Devices in the PIC18F87J90 family are available in 64-pin and 80-pin packages. Block diagrams for the two groups are shown in Figure 1-1 and Figure 1-2.

The devices are differentiated from each other in four ways:

1. Flash program memory (two sizes, 64 Kbytes for PIC18FX6J90 devices and 128 Kbytes for PIC18FX7J90 devices).
2. Data RAM (3,923 bytes RAM for both PIC18FX6J90 and PIC18FX7J90 devices).
3. I/O ports (7 bidirectional ports on PIC18F6XJ90 devices, 9 bidirectional ports on PIC18F8XJ90 devices).
4. LCD Pixels: 132 pixels (33 SEGs x 4 COMs) can be driven by 64-pin devices; 192 pixels (48 SEGs x 4 COMs) can be driven by 80-pin devices.

All other features for devices in this family are identical. These are summarized in Table 1-1 and Table 1-2.

The pinouts for all devices are listed in Table 1-3 and Table 1-4.

PIC18F87J90 FAMILY

TABLE 1-1: DEVICE FEATURES FOR THE PIC18F6XJ90 (64-PIN DEVICES)

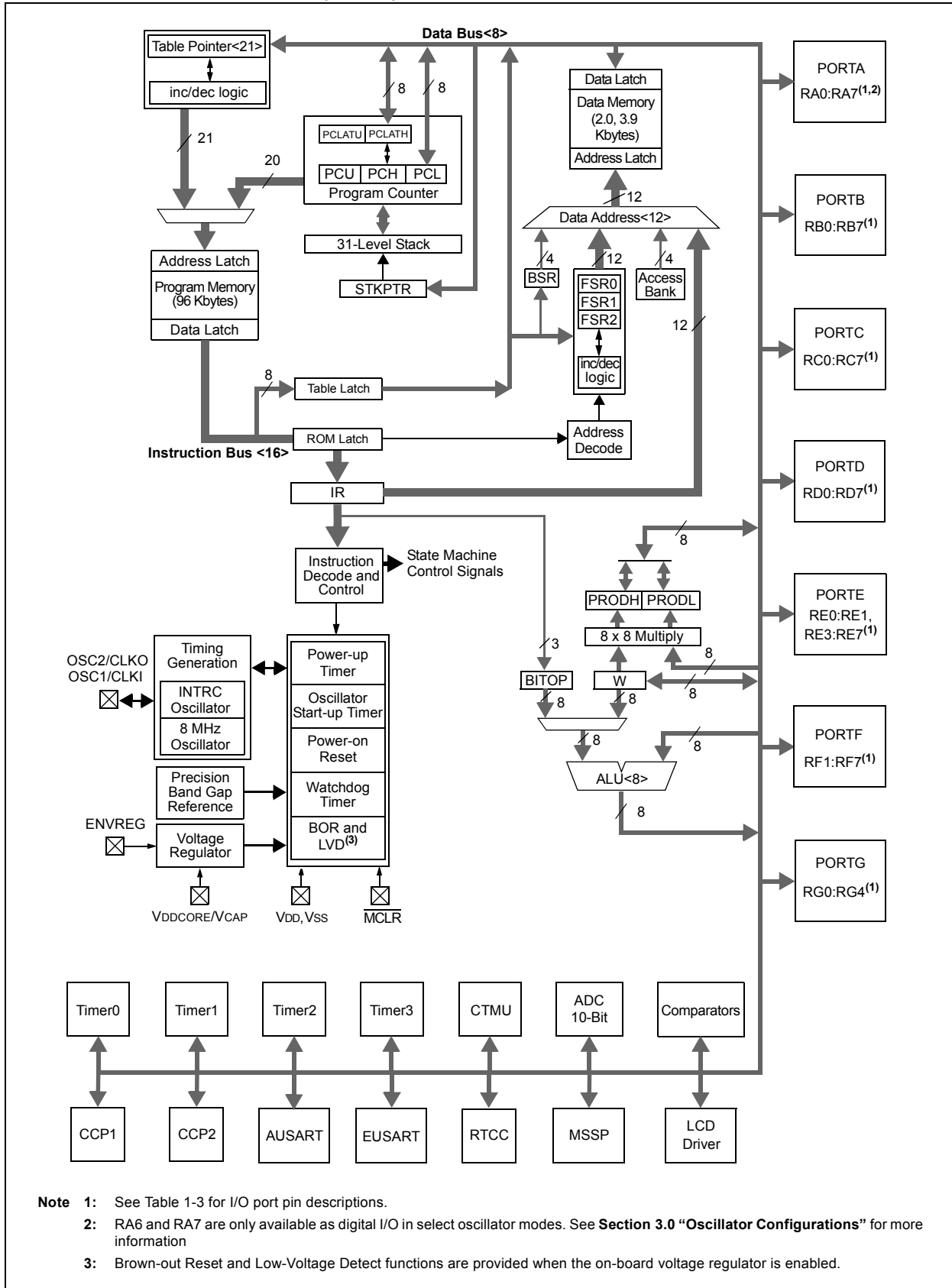
Features	PIC18F66J90	PIC18F67J90
Operating Frequency	DC – 48 MHz	
Program Memory (Bytes)	64K	128K
Program Memory (Instructions)	32,768	65,536
Data Memory (Bytes)	3,923	3,923
Interrupt Sources	29	
I/O Ports	Ports A, B, C, D, E, F, G	
LCD Driver (available pixels to drive)	132 (33 SEGs x 4 COMs)	
Timers	4	
Comparators	2	
CTMU	Yes	
RTCC	Yes	
Capture/Compare/PWM Modules	2	
Serial Communications	MSSP, Addressable USART, Enhanced USART	
10-Bit Analog-to-Digital Module	12 Input Channels	
Resets (and Delays)	POR, BOR, RESET Instruction, Stack Full, Stack Underflow, MCLR, WDT (PWRT, OST)	
Instruction Set	75 Instructions, 83 with Extended Instruction Set Enabled	
Packages	64-Pin TQFP	

TABLE 1-2: DEVICE FEATURES FOR THE PIC18F8XJ90 (80-PIN DEVICES)

Features	PIC18F86J90	PIC18F87J90
Operating Frequency	DC – 48 MHz	
Program Memory (Bytes)	64K	128K
Program Memory (Instructions)	32,768	65,536
Data Memory (Bytes)	3,923	3,923
Interrupt Sources	29	
I/O Ports	Ports A, B, C, D, E, F, G, H, J	
LCD Driver (available pixels to drive)	192 (48 SEGs x 4 COMs)	
Timers	4	
Comparators	2	
CTMU	Yes	
RTCC	Yes	
Capture/Compare/PWM Modules	2	
Serial Communications	MSSP, Addressable USART, Enhanced USART	
10-Bit Analog-to-Digital Module	12 Input Channels	
Resets (and Delays)	POR, BOR, RESET Instruction, Stack Full, Stack Underflow, MCLR, WDT (PWRT, OST)	
Instruction Set	75 Instructions, 83 with Extended Instruction Set Enabled	
Packages	80-Pin TQFP	

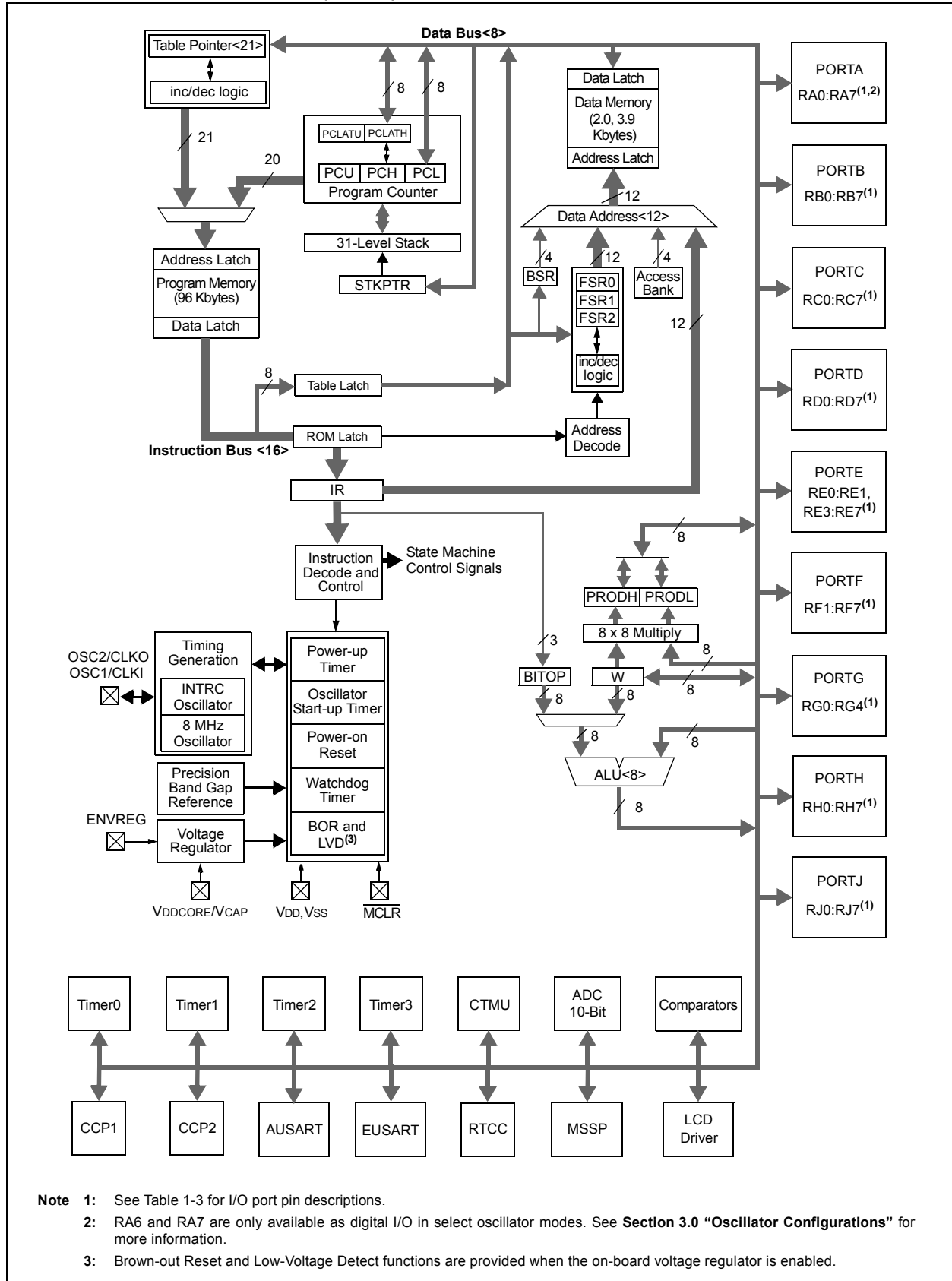
PIC18F87J90 FAMILY

FIGURE 1-1: PIC18F6XJ90 (64-PIN) BLOCK DIAGRAM



PIC18F87J90 FAMILY

FIGURE 1-2: PIC18F8XJ90 (80-PIN) BLOCK DIAGRAM



PIC18F87J90 FAMILY

TABLE 1-3: PIC18F6XJ90 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
MCLR	7	I	ST	Master Clear (input) or programming voltage (input). This pin is an active-low Reset to the device.
OSC1/CLKI/RA7 OSC1 CLKI RA7	39	I I I/O	CMOS CMOS TTL	Oscillator crystal or external clock input. Oscillator crystal input. External clock source input. Always associated with pin function, OSC1. (See related OSC1/CLKI, OSC2/CLKO pins.) General purpose I/O pin.
OSC2/CLKO/RA6 OSC2 CLKO RA6	40	O O I/O	— — TTL	Oscillator crystal or clock output. Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. In EC modes, OSC2 pin outputs CLKO, which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate. General purpose I/O pin.
RA0/AN0 RA0 AN0	24	I/O I	TTL Analog	PORTA is a bidirectional I/O port. Digital I/O. Analog Input 0.
RA1/AN1/SEG18 RA1 AN1 SEG18	23	I/O I O	TTL Analog Analog	Digital I/O. Analog Input 1. SEG18 output for LCD.
RA2/AN2/VREF- RA2 AN2 VREF-	22	I/O I I	TTL Analog Analog	Digital I/O. Analog Input 2. A/D reference voltage (low) input.
RA3/AN3/VREF+ RA3 AN3 VREF+	21	I/O I I	TTL Analog Analog	Digital I/O. Analog Input 3. A/D reference voltage (high) input.
RA4/T0CKI/SEG14 RA4 T0CKI SEG14	28	I/O I O	ST ST Analog	Digital I/O. Timer0 external clock input. SEG14 output for LCD.
RA5/AN4/SEG15 RA5 AN4 SEG15	27	I/O I O	TTL Analog Analog	Digital I/O. Analog Input 4. SEG15 output for LCD.
RA6				See the OSC2/CLKO/RA6 pin.
RA7				See the OSC1/CLKI/RA7 pin.

Legend: TTL = TTL compatible input CMOS = CMOS compatible input or output
 ST = Schmitt Trigger input with CMOS levels Analog = Analog input
 I = Input O = Output
 P = Power OD = Open-Drain (no P diode to VDD)
 I²C™ = I²C/SMBus

Note 1: Default assignment for CCP2 when the CCP2MX Configuration bit is set.
2: Alternate assignment for CCP2 when the CCP2MX Configuration bit is cleared.

PIC18F87J90 FAMILY

TABLE 1-3: PIC18F6XJ90 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
RB0/INT0/SEG30 RB0 INT0 SEG30	48	I/O I O	TTL ST Analog	PORTB is a bidirectional I/O port. PORTB can be software programmed for internal weak pull-ups on all inputs. Digital I/O. External Interrupt 0. SEG30 output for LCD.
RB1/INT1/SEG8 RB1 INT1 SEG8	47	I/O I O	TTL ST Analog	Digital I/O. External Interrupt 1. SEG8 output for LCD.
RB2/INT2/SEG9/CTED1 RB2 INT2 CTED1 SEG9	46	I/O I I O	TTL ST ST Analog	Digital I/O. External Interrupt 2. CTMU Edge 1 input. SEG9 output for LCD.
RB3/INT3/SEG10/CTED2 RB3 INT3 SEG10 CTED2	45	I/O I O I	TTL ST Analog ST	Digital I/O. External Interrupt 3. SEG10 output for LCD. CTMU Edge 2 input.
RB4/KBI0/SEG11 RB4 KBI0 SEG11	44	I/O I O	TTL TTL Analog	Digital I/O. Interrupt-on-change pin. SEG11 output for LCD.
RB5/KBI1/SEG29 RB5 KBI1 SEG29	43	I/O I O	TTL TTL Analog	Digital I/O. Interrupt-on-change pin. SEG29 output for LCD.
RB6/KBI2/PGC RB6 KBI2 PGC	42	I/O I I/O	TTL TTL ST	Digital I/O. Interrupt-on-change pin. In-Circuit Debugger and ICSP™ programming clock pin.
RB7/KBI3/PGD RB7 KBI3 PGD	37	I/O I I/O	TTL TTL ST	Digital I/O. Interrupt-on-change pin. In-Circuit Debugger and ICSP programming data pin.

Legend: TTL = TTL compatible input
 ST = Schmitt Trigger input with CMOS levels
 I = Input
 P = Power
 I²C™ = I²C/SMBus
 CMOS = CMOS compatible input or output
 Analog = Analog input
 O = Output
 OD = Open-Drain (no P diode to VDD)

Note 1: Default assignment for CCP2 when the CCP2MX Configuration bit is set.
2: Alternate assignment for CCP2 when the CCP2MX Configuration bit is cleared.

PIC18F87J90 FAMILY

TABLE 1-3: PIC18F6XJ90 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
RC0/T1OSO/T13CKI	30			PORTC is a bidirectional I/O port.
RC0		I/O	ST	Digital I/O.
T1OSO		O	—	Timer1 oscillator output.
T13CKI		I	ST	Timer1/Timer3 external clock input.
RC1/T1OSI/CCP2/SEG32	29			
RC1		I/O	ST	Digital I/O.
T1OSI		I	CMOS	Timer1 oscillator input.
CCP2 ⁽¹⁾		I/O	ST	Capture 2 input/Compare 2 output/PWM2 output.
SEG32		O	Analog	SEG32 output for LCD.
RC2/CCP1/SEG13	33			
RC2		I/O	ST	Digital I/O.
CCP1		I/O	ST	Capture 1 input/Compare 1 output/PWM1 output.
SEG13		O	Analog	SEG13 output for LCD.
RC3/SCK/SCL/SEG17	34			
RC3		I/O	ST	Digital I/O.
SCK		I/O	ST	Synchronous serial clock input/output for SPI mode.
SCL		I/O	I ² C	Synchronous serial clock input/output for I ² C™ mode.
SEG17		O	Analog	SEG17 output for LCD.
RC4/SDI/SDA/SEG16	35			
RC4		I/O	ST	Digital I/O.
SDI		I	ST	SPI data in.
SDA		I/O	I ² C	I ² C data I/O.
SEG16		O	Analog	SEG16 output for LCD.
RC5/SDO/SEG12	36			
RC5		I/O	ST	Digital I/O.
SDO		O	—	SPI data out.
SEG12		O	Analog	SEG12 output for LCD.
RC6/TX1/CK1/SEG27	31			
RC6		I/O	ST	Digital I/O.
TX1		O	—	EUSART asynchronous transmit.
CK1		I/O	ST	EUSART synchronous clock (see related RX1/DT1).
SEG27		O	Analog	SEG27 output for LCD.
RC7/RX1/DT1/SEG28	32			
RC7		I/O	ST	Digital I/O.
RX1		I	ST	EUSART asynchronous receive.
DT1		I/O	ST	EUSART synchronous data (see related TX1/CK1).
SEG28		O	Analog	SEG28 output for LCD.

Legend: TTL = TTL compatible input

ST = Schmitt Trigger input with CMOS levels

I = Input

P = Power

I²C™ = I²C/SMBus

CMOS = CMOS compatible input or output

Analog = Analog input

O = Output

OD = Open-Drain (no P diode to VDD)

Note 1: Default assignment for CCP2 when the CCP2MX Configuration bit is set.

2: Alternate assignment for CCP2 when the CCP2MX Configuration bit is cleared.

PIC18F87J90 FAMILY

TABLE 1-3: PIC18F6XJ90 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
RD0/SEG0/CTPLS	58	I/O	ST	PORTD is a bidirectional I/O port. Digital I/O. SEG0 output for LCD. CTMU pulse generator output.
RD0		O	Analog	
SEG0 CTPLS		O	—	
RD1/SEG1	55	I/O	ST	Digital I/O. SEG1 output for LCD.
RD1 SEG1		O	Analog	
RD2/SEG2	54	I/O	ST	Digital I/O. SEG2 output for LCD.
RD2 SEG2		O	Analog	
RD3/SEG3	53	I/O	ST	Digital I/O. SEG3 output for LCD.
RD3 SEG3		O	Analog	
RD4/SEG4	52	I/O	ST	Digital I/O. SEG4 output for LCD.
RD4 SEG4		O	Analog	
RD5/SEG5	51	I/O	ST	Digital I/O. SEG5 output for LCD.
RD5 SEG5		O	Analog	
RD6/SEG6	50	I/O	ST	Digital I/O. SEG6 output for LCD.
RD6 SEG6		O	Analog	
RD7/SEG7	49	I/O	ST	Digital I/O. SEG7 output for LCD.
RD7 SEG7		O	Analog	

Legend: TTL = TTL compatible input CMOS = CMOS compatible input or output
 ST = Schmitt Trigger input with CMOS levels Analog = Analog input
 I = Input O = Output
 P = Power OD = Open-Drain (no P diode to VDD)
 I²C™ = I²C/SMBus

- Note 1:** Default assignment for CCP2 when the CCP2MX Configuration bit is set.
2: Alternate assignment for CCP2 when the CCP2MX Configuration bit is cleared.

PIC18F87J90 FAMILY

TABLE 1-3: PIC18F6XJ90 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
RE0/LCDBIAS1 RE0 LCDBIAS1	2	I/O I	ST Analog	PORTC is a bidirectional I/O port. Digital I/O. BIAS1 input for LCD.
RE1/LCDBIAS2 RE1 LCDBIAS2	1	I/O I	ST Analog	Digital I/O. BIAS2 input for LCD.
LCDBIAS3	64	I	Analog	BIAS3 input for LCD.
RE3/COM0 RE3 COM0	63	I/O O	ST Analog	Digital I/O. COM0 output for LCD.
RE4/COM1 RE4 COM1	62	I/O O	ST Analog	Digital I/O. COM1 output for LCD.
RE5/COM2 RE5 COM2	61	I/O O	ST Analog	Digital I/O. COM2 output for LCD.
RE6/COM3 RE6 COM3	60	I/O O	ST Analog	Digital I/O. COM3 output for LCD.
RE7/CCP2/SEG31 RE7 CCP2 ⁽²⁾ SEG31	59	I/O I/O O	ST ST Analog	Digital I/O. Capture 2 input/Compare 2 output/PWM2 output. SEG31 output for LCD.

Legend: TTL = TTL compatible input CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels Analog = Analog input
I = Input O = Output
P = Power OD = Open-Drain (no P diode to VDD)
I²C™ = I²C/SMBus

Note 1: Default assignment for CCP2 when the CCP2MX Configuration bit is set.
2: Alternate assignment for CCP2 when the CCP2MX Configuration bit is cleared.

PIC18F87J90 FAMILY

TABLE 1-3: PIC18F6XJ90 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
RF1/AN6/C2OUT/SEG19	17			PORTF is a bidirectional I/O port.
RF1		I/O	ST	Digital I/O.
AN6		I	Analog	Analog Input 6.
C2OUT		O	—	Comparator 2 output.
SEG19		O	Analog	SEG19 output for LCD.
RF2/AN7/C1OUT/SEG20	16			
RF2		I/O	ST	Digital I/O.
AN7		I	Analog	Analog Input 7.
C1OUT		O	—	Comparator 1 output.
SEG20		O	Analog	SEG20 output for LCD.
RF3/AN8/SEG21/C2INB	15			
RF3		I/O	ST	Digital I/O.
AN8		I	Analog	Analog Input 8.
SEG21		O	Analog	SEG21 output for LCD.
C2INB		I	Analog	Comparator 2 Input B.
RF4/AN9/SEG22/C2INA	14			
RF4		I/O	ST	Digital I/O.
AN9		I	Analog	Analog Input 9.
SEG22		O	Analog	SEG22 output for LCD
C2INA		I	Analog	Comparator 2 Input A.
RF5/AN10/CVREF/SEG23/C1INB	13			
RF5		I/O	ST	Digital I/O.
AN10		I	Analog	Analog Input 10.
CVREF		O	Analog	Comparator reference voltage output.
SEG23		O	Analog	SEG23 output for LCD.
C1INB		I	Analog	Comparator 1 Input B.
RF6/AN11/SEG24/C1INA	12			
RF6		I/O	ST	Digital I/O.
AN11		I	Analog	Analog Input 11.
SEG24		O	Analog	SEG24 output for LCD
C1INA		I	Analog	Comparator 1 Input A.
RF7/AN5/ \overline{SS} /SEG25	11			
RF7		I/O	ST	Digital I/O.
AN5		O	Analog	Analog Input 5.
\overline{SS}		I	TTL	SPI slave select input.
SEG25		O	Analog	SEG25 output for LCD.

Legend: TTL = TTL compatible input CMOS = CMOS compatible input or output
 ST = Schmitt Trigger input with CMOS levels Analog = Analog input
 I = Input O = Output
 P = Power OD = Open-Drain (no P diode to VDD)
 I^2C^{TM} = I^2C /SMBus

Note 1: Default assignment for CCP2 when the CCP2MX Configuration bit is set.
2: Alternate assignment for CCP2 when the CCP2MX Configuration bit is cleared.

PIC18F87J90 FAMILY

TABLE 1-3: PIC18F6XJ90 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
RG0/LCDBIAS0 RG0 LCDBIAS0	3	I/O I	ST Analog	PORTG is a bidirectional I/O port. Digital I/O. BIAS0 input for LCD.
RG1/TX2/CK2 RG1 TX2 CK2	4	I/O O I/O	ST — ST	Digital I/O. AUSART asynchronous transmit. AUSART synchronous clock (see related RX2/DT2).
RG2/RX2/DT2/VLCAP1 RG2 RX2 DT2 VLCAP1	5	I/O I I/O I	ST ST ST Analog	Digital I/O. AUSART asynchronous receive. AUSART synchronous data (see related TX2/CK2). LCD charge pump capacitor input.
RG3/VLCAP2 RG3 VLCAP2	6	I/O I	ST Analog	Digital I/O. LCD charge pump capacitor input.
RG4/SEG26/RTCC RG4 SEG26 RTCC	8	I/O O O	ST Analog —	Digital I/O. SEG26 output for LCD. RTCC output
VSS	9, 25, 41, 56	P	—	Ground reference for logic and I/O pins.
VDD	26, 38, 57	P	—	Positive supply for logic and I/O pins.
AVSS	20	P	—	Ground reference for analog modules.
AVDD	19	P	—	Positive supply for analog modules.
ENVREG	18	I	ST	Enable for on-chip voltage regulator.
VDDCORE/VCAP VDDCORE VCAP	10	P P	— —	Core logic power or external filter capacitor connection. Positive supply for microcontroller core logic (regulator disabled). External filter capacitor connection (regulator enabled).

Legend: TTL = TTL compatible input CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels Analog = Analog input
I = Input O = Output
P = Power OD = Open-Drain (no P diode to VDD)
I²C™ = I²C/SMBus

Note 1: Default assignment for CCP2 when the CCP2MX Configuration bit is set.
2: Alternate assignment for CCP2 when the CCP2MX Configuration bit is cleared.

PIC18F87J90 FAMILY

TABLE 1-4: PIC18F8XJ90 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
MCLR	9	I	ST	Master Clear (input) or programming voltage (input). This pin is an active-low Reset to the device.
OSC1/CLKI/RA7 OSC1 CLKI RA7	49	I I I/O	CMOS CMOS TTL	Oscillator crystal or external clock input. Oscillator crystal input. External clock source input. Always associated with pin function, OSC1. (See related OSC1/CLKI, OSC2/CLKO pins.) General purpose I/O pin.
OSC2/CLKO/RA6 OSC2 CLKO RA6	50	O O I/O	— — TTL	Oscillator crystal or clock output. Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. In EC modes, OSC2 pin outputs CLKO, which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate. General purpose I/O pin.
RA0/AN0 RA0 AN0	30	I/O I	TTL Analog	PORTA is a bidirectional I/O port. Digital I/O. Analog Input 0.
RA1/AN1/SEG18 RA1 AN1 SEG18	29	I/O I O	TTL Analog Analog	Digital I/O. Analog Input 1. SEG18 output for LCD.
RA2/AN2/VREF- RA2 AN2 VREF-	28	I/O I I	TTL Analog Analog	Digital I/O. Analog Input 2. A/D reference voltage (low) input.
RA3/AN3/VREF+ RA3 AN3 VREF+	27	I/O I I	TTL Analog Analog	Digital I/O. Analog Input 3. A/D reference voltage (high) input.
RA4/T0CKI/SEG14 RA4 T0CKI SEG14	34	I/O I O	ST ST Analog	Digital I/O. Timer0 external clock input. SEG14 output for LCD.
RA5/AN4/SEG15 RA5 AN4 SEG15	33	I/O I O	TTL Analog Analog	Digital I/O. Analog Input 4. SEG15 output for LCD.
RA6				See the OSC2/CLKO/RA6 pin.
RA7				See the OSC1/CLKI/RA7 pin.

Legend: TTL = TTL compatible input
ST = Schmitt Trigger input with CMOS levels
I = Input
P = Power
I²C™ = I²C/SMBus
CMOS = CMOS compatible input or output
Analog = Analog input
O = Output
OD = Open-Drain (no P diode to VDD)

Note 1: Default assignment for CCP2 when the CCP2MX Configuration bit is set.
2: Alternate assignment for CCP2 when the CCP2MX Configuration bit is cleared.

PIC18F87J90 FAMILY

TABLE 1-4: PIC18F8XJ90 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
RB0/INT0/SEG30 RB0 INT0 SEG30	58	I/O I O	TTL ST Analog	PORTB is a bidirectional I/O port. PORTB can be software programmed for internal weak pull-ups on all inputs. Digital I/O. External Interrupt 0. SEG30 output for LCD.
RB1/INT1/SEG8 RB1 INT1 SEG8	57	I/O I O	TTL ST Analog	Digital I/O. External Interrupt 1. SEG8 output for LCD.
RB2/INT2/SEG9/CTED1 RB2 INT2 SEG9 CTED1	56	I/O I O I	TTL ST Analog ST	Digital I/O. External Interrupt 2. SEG9 output for LCD. CTMU Edge 1 input.
RB3/INT3/SEG10/ CTED2 RB3 INT3 SEG10 CTED2	55	I/O I O I	TTL ST Analog ST	Digital I/O. External Interrupt 3. SEG10 output for LCD. CTMU Edge 2 input.
RB4/KBI0/SEG11 RB4 KBI0 SEG11	54	I/O I O	TTL TTL Analog	Digital I/O. Interrupt-on-change pin. SEG11 output for LCD.
RB5/KBI1/SEG29 RB5 KBI1 SEG29	53	I/O I O	TTL TTL Analog	Digital I/O. Interrupt-on-change pin. SEG29 output for LCD.
RB6/KBI2/PGC RB6 KBI2 PGC	52	I/O I I/O	TTL TTL ST	Digital I/O. Interrupt-on-change pin. In-Circuit Debugger and ICSP™ programming clock pin.
RB7/KBI3/PGD RB7 KBI3 PGD	47	I/O I I/O	TTL TTL ST	Digital I/O. Interrupt-on-change pin. In-Circuit Debugger and ICSP programming data pin.

Legend: TTL = TTL compatible input CMOS = CMOS compatible input or output
 ST = Schmitt Trigger input with CMOS levels Analog = Analog input
 I = Input O = Output
 P = Power OD = Open-Drain (no P diode to VDD)
 I²C™ = I²C/SMBus

Note 1: Default assignment for CCP2 when the CCP2MX Configuration bit is set.
2: Alternate assignment for CCP2 when the CCP2MX Configuration bit is cleared.

PIC18F87J90 FAMILY

TABLE 1-4: PIC18F8XJ90 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
RC0/T1OSO/T13CKI	36			PORTC is a bidirectional I/O port.
RC0		I/O	ST	Digital I/O.
T1OSO		O	—	Timer1 oscillator output.
T13CKI		I	ST	Timer1/Timer3 external clock input.
RC1/T1OSI/CCP2/SEG32	35			
RC1		I/O	ST	Digital I/O.
T1OSI		I	CMOS	Timer1 oscillator input.
CCP2 ⁽¹⁾ SEG32		I/O O	ST Analog	Capture 2 input/Compare 2 output/PWM2 output. SEG32 output for LCD.
RC2/CCP1/SEG13	43			
RC2		I/O	ST	Digital I/O.
CCP1 SEG13		I/O O	ST Analog	Capture 1 input/Compare 1 output/PWM1 output. SEG13 output for LCD.
RC3/SCK/SCL/SEG17	44			
RC3		I/O	ST	Digital I/O.
SCK		I/O	ST	Synchronous serial clock input/output for SPI mode.
SCL SEG17		I/O O	I ² C Analog	Synchronous serial clock input/output for I ² C™ mode. SEG17 output for LCD.
RC4/SDI/SDA/SEG16	45			
RC4		I/O	ST	Digital I/O.
SDI		I	ST	SPI data in.
SDA SEG16		I/O O	I ² C Analog	I ² C data I/O. SEG16 output for LCD.
RC5/SDO/SEG12	46			
RC5		I/O	ST	Digital I/O.
SDO SEG12		O O	— Analog	SPI data out. SEG12 output for LCD.
RC6/TX1/CK1/SEG27	37			
RC6		I/O	ST	Digital I/O.
TX1		O	—	EUSART asynchronous transmit.
CK1 SEG27		I/O O	ST Analog	EUSART synchronous clock (see related RX1/DT1). SEG27 output for LCD.
RC7/RX1/DT1/SEG28	38			
RC7		I/O	ST	Digital I/O.
RX1		I	ST	EUSART asynchronous receive.
DT1 SEG28		I/O O	ST Analog	EUSART synchronous data (see related TX1/CK1). SEG28 output for LCD.

Legend: TTL = TTL compatible input CMOS = CMOS compatible input or output
 ST = Schmitt Trigger input with CMOS levels Analog = Analog input
 I = Input O = Output
 P = Power OD = Open-Drain (no P diode to VDD)
 I²C™ = I²C/SMBus

- Note 1:** Default assignment for CCP2 when the CCP2MX Configuration bit is set.
2: Alternate assignment for CCP2 when the CCP2MX Configuration bit is cleared.

PIC18F87J90 FAMILY

TABLE 1-4: PIC18F8XJ90 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
RD0/SEG0/CTPLS	72	I/O	ST	PORTD is a bidirectional I/O port. Digital I/O. SEG0 output for LCD. CTMU pulse generator output.
RD0		O	Analog	
SEG0		O	ST	
CTPLS				
RD1/SEG1	69	I/O	ST	
RD1		O	Analog	
SEG1				
RD2/SEG2	68	I/O	ST	
RD2		O	Analog	
SEG2				
RD3/SEG3	67	I/O	ST	Digital I/O.
RD3		O	Analog	SEG3 output for LCD.
SEG3				
RD4/SEG4	66	I/O	ST	Digital I/O.
RD4		O	Analog	SEG4 output for LCD.
SEG4				
RD5/SEG5	65	I/O	ST	Digital I/O.
RD5		O	Analog	SEG5 output for LCD.
SEG5				
RD6/SEG6	64	I/O	ST	Digital I/O.
RD6		O	Analog	SEG6 output for LCD.
SEG6				
RD7/SEG7	63	I/O	ST	Digital I/O.
RD7		O	Analog	SEG7 output for LCD.
SEG7				

Legend: TTL = TTL compatible input CMOS = CMOS compatible input or output
 ST = Schmitt Trigger input with CMOS levels Analog = Analog input
 I = Input O = Output
 P = Power OD = Open-Drain (no P diode to VDD)
 I²C™ = I²C/SMBus

Note 1: Default assignment for CCP2 when the CCP2MX Configuration bit is set.
2: Alternate assignment for CCP2 when the CCP2MX Configuration bit is cleared.

PIC18F87J90 FAMILY

TABLE 1-4: PIC18F8XJ90 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number	Pin Type	Buffer Type	Description
	TQFP			
RE0/LCDBIAS1 RE0 LCDBIAS1	4	I/O I	ST Analog	<p>PORTE is a bidirectional I/O port.</p> <p>Digital I/O. BIAS1 input for LCD.</p>
RE1/LCDBIAS2 RE1 LCDBIAS2	3	I/O I	ST Analog	<p>Digital I/O. BIAS2 input for LCD.</p>
LCDBIAS3	78	I	Analog	BIAS3 input for LCD.
RE3/COM0 RE3 COM0	77	I/O O	ST Analog	<p>Digital I/O. COM0 output for LCD.</p>
RE4/COM1 RE4 COM1	76	I/O O	ST Analog	<p>Digital I/O. COM1 output for LCD.</p>
RE5/COM2 RE5 COM2	75	I/O O	ST Analog	<p>Digital I/O. COM2 output for LCD.</p>
RE6/COM3 RE6 COM3	74	I/O O	ST Analog	<p>Digital I/O. COM3 output for LCD.</p>
RE7/CCP2/SEG31 RE7 CCP2 ⁽²⁾ SEG31	73	I/O I/O O	ST ST Analog	<p>Digital I/O. Capture 2 input/Compare 2 output/PWM2 output. SEG31 output for LCD.</p>

Legend: TTL = TTL compatible input CMOS = CMOS compatible input or output
ST = Schmitt Trigger input with CMOS levels Analog = Analog input
I = Input O = Output
P = Power OD = Open-Drain (no P diode to VDD)
I²C™ = I²C/SMBus

Note 1: Default assignment for CCP2 when the CCP2MX Configuration bit is set.
2: Alternate assignment for CCP2 when the CCP2MX Configuration bit is cleared.