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PIC18F97J94 FAMILY

8-Bit LCD Flash Microcontroller with USB and XLP Technology

eXtreme Low-Power Features

- Multiple Power Management Options for Extreme Power Reduction:
  - VBAT allows for lowest power consumption on back-up battery (with or without RTCC)
  - Deep Sleep allows near total power-down with the ability to wake-up on external triggers
  - Sleep and Idle modes selectively shut down peripherals and/or core for substantial power reduction and fast wake-up
- Alternate Clock modes Allow On-the-Fly Switching to a Lower Clock Speed for Selective Power Reduction
- Extreme Low-Power Current Consumption for Deep Sleep:
  - WDT: 650 nA @ 2V typical
  - RTCC: 650 nA @ 32 kHz, 2V typical
  - Deep Sleep current, 80 nA typical

Universal Serial Bus Features

- USB V2.0 Compliant
- Low Speed (1.5 Mb/s) and Full Speed (12 Mb/s)
- Supports Control, Interrupt, Isochronous and Bulk Transfers
- Supports up to 32 Endpoints (16 bidirectional)
- USB module can use Any RAM Location on the Device as USB Endpoint Buffers
- On-Chip USB Transceiver

Peripheral Features

- LCD Display Controller:
  - Up to 60 segments by 8 commons
  - Internal charge pump and low-power, internal resistor biasing
  - Operation in Sleep mode
- Up to Four External Interrupt Sources
- Peripheral Pin Select Lite (PPS-Lite):
  - Allows independent I/O mapping of many peripherals
- Four 16-Bit and Four 8-Bit Timers/Counters with Prescaler
- Seven Capture/Compare/PWM (CCP) modules
- Three Enhanced Capture/Compare/PWM (ECCP) modules:
  - One, two or four PWM outputs
  - Selectable polarity
  - Programmable dead time
  - Auto-shutdown and auto-restart
  - Pulse steering control
- Hardware Real-Time Clock/Calendar (RTCC):
  - Runs in Deep Sleep and VBAT modes
- Two Master Synchronous Serial Ports (MSSP) modules Featuring:
  - 3-Wire/4-Wire SPI (all 4 modes)
  - SPI Direct Memory Access (DMA) channel w/1024 byte count
  - Two I^2C modules Support Multi-Master/Slave mode and 7-Bit/10-Bit Addressing
- Four Enhanced Addressable USART modules:
  - Support RS-485, RS-232 and LIN/J2602
  - On-chip hardware encoder/decoder for IrDA®
  - Auto-wake-up on Auto-Baud Detect
- Digital Signal Modulator Provides On-Chip OOK, FSK and PSK Modulation for a Digital Signal Stream
- High-Current Sink/Source 18 mA/18 mA on all Digital I/O
- Configurable Open-Drain Outputs on ECCP/CCP/USART/MSSP
- Extended Microcontroller mode Using 12, 16 or 20-Bit Addressing mode

Analog Features

- 10/12-Bit, 24-Channel Analog-to-Digital (A/D) Converter:
  - Conversion rate of 500 ksps (10-bit), 200 kbps (12-bit)
  - Conversion available during Sleep and Idle
- Three Rail-to-Rail Enhanced Analog Comparators with Programmable Input/Output Configuration
- On-Chip Programmable Voltage Reference
- Charge Time Measurement Unit (CTMU):
  - Used for capacitive touch sensing, up to 24 channels
  - Time measurement down to 1 ns resolution
  - CTMU temperature sensing

High-Performance CPU

- High-Precision PLL for USB
- Two External Clock modes, Up to 64 MHz (16 MIPS®)
- Internal 31 kHz Oscillator
- High-Precision Internal Oscillator with Clock Recovery from SOSC to Achieve 0.15% Precision, 31 kHz to 8 MHz or 64 MHz w/PLL, ±0.15% Typical, ±1.5% Max.
- Secondary Oscillator using Timer1 @ 32 kHz
- C Compiler Optimized Instruction Set Architecture
- Two Address Generation Units for Separate Read and Write Addressing of Data Memory

Special Microcontroller Features

- Operating Voltage Range of 2.0V to 3.6V
- Two On-Chip Voltage Regulators (1.8V and 1.2V) for Regular and Extreme Low-Power Operation
- 20,000 Erase/Write Cycle Endurance Flash Program Memory, Typical
- Flash Data Retention: 10 Years Minimum
- Self-Programmable under Software Control
- Two Configurable Reference Clock Outputs (REFO1 and REFO2)
- In-Circuit Serial Programming™ (ICSP™)
- Fail-Safe Clock Monitor Operation:
  - Detects clock failure and switches to on-chip, low-power RC oscillator
- Power-on Reset (POR), Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Brown-out Reset (BOR) with Operation Below V_{BOR}, with Regulator Enabled
- High/Low-Voltage Detect (HLVD)
- Flexible Watchdog Timer (WDT) with its Own RC Oscillator for Reliable Operation
- Standard and Ultra Low-Power Watchdog Timers (WDT) for Reliable Operation in Standard and Deep Sleep modes

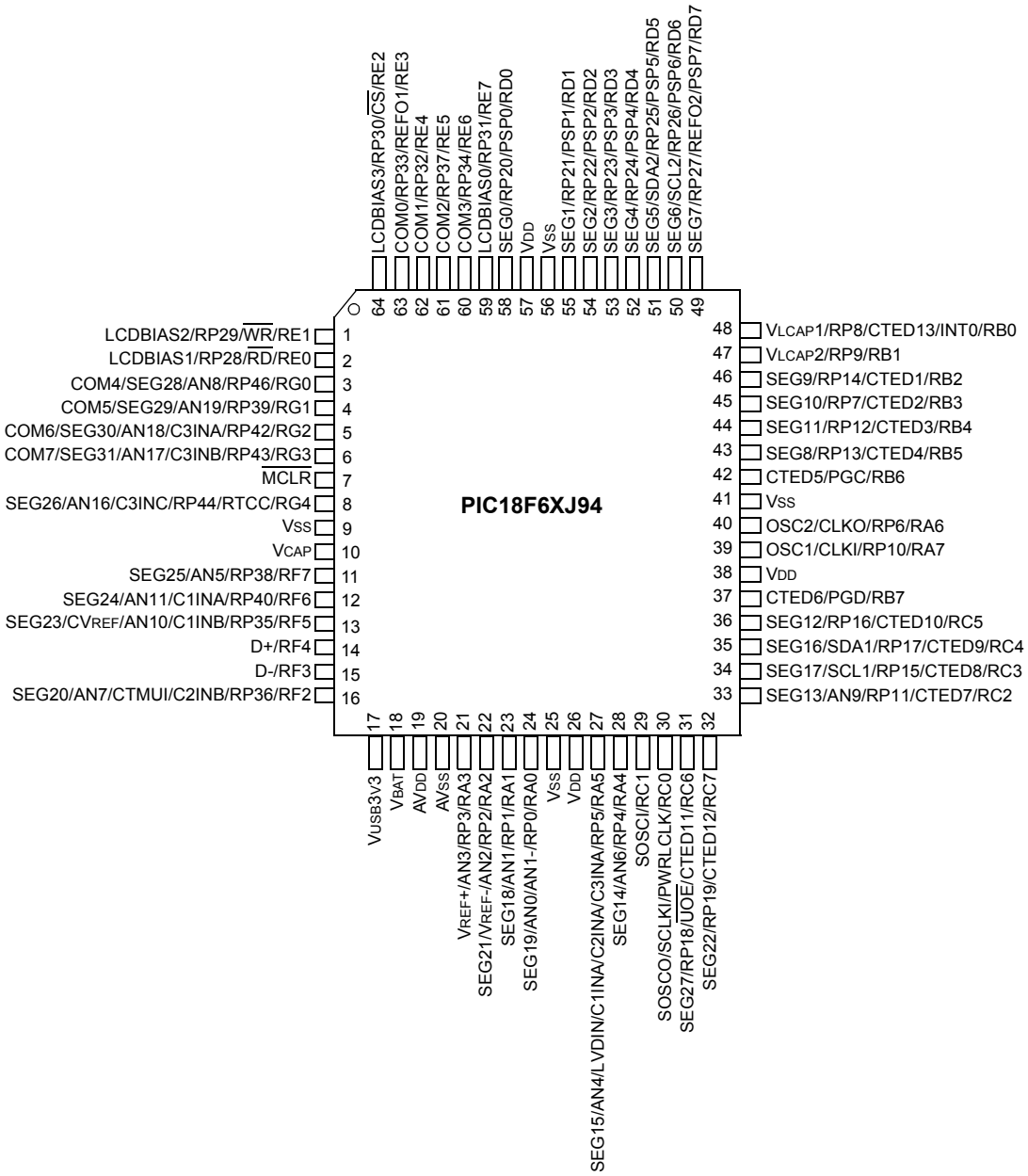
TABLE 1: PIC18F97J94 FAMILY TYPES

Device	Pins	Memory		Remappable Peripherals					I^2C	10/12-Bit A/D (ch)	CTMU	LCD (pixels)	USB	Deep Sleep w/V_{BAT}	PPS (Lite)
		Flash Program (bytes)	Data SRAM (bytes)	Timers 8-Bit/16-Bit	USART w/IrDA®	SPI w/ DMA	Comparators	CCP/ECCP							
PIC18F97J94	100	128K	4K	4	4	2	3	Y	2	24	Y	480	Y	Y	Lite
PIC18F87J94	80	128K	4K	4	4	2	3	Y	2	24	Y	352	Y	Y	Lite
PIC18F67J94	64	128K	4K	4	4	2	3	Y	2	16	Y	224	Y	Y	Lite
PIC18F96J94	100	64K	4K	4	4	2	3	Y	2	24	Y	480	Y	Y	Lite
PIC18F86J94	80	64K	4K	4	4	2	3	Y	2	24	Y	352	Y	Y	Lite
PIC18F66J94	64	64K	4K	4	4	2	3	Y	2	16	Y	224	Y	Y	Lite
PIC18F95J94	100	32K	4K	4	4	2	3	Y	2	24	Y	480	Y	Y	Lite
PIC18F85J94	80	32K	4K	4	4	2	3	Y	2	24	Y	352	Y	Y	Lite
PIC18F65J94	64	32K	4K	4	4	2	3	Y	2	16	Y	224	Y	Y	Lite

For other small form-factor package availability and marking information, visit http://www.microchip.com/packaging or contact your local sales office.

PIN DIAGRAMS

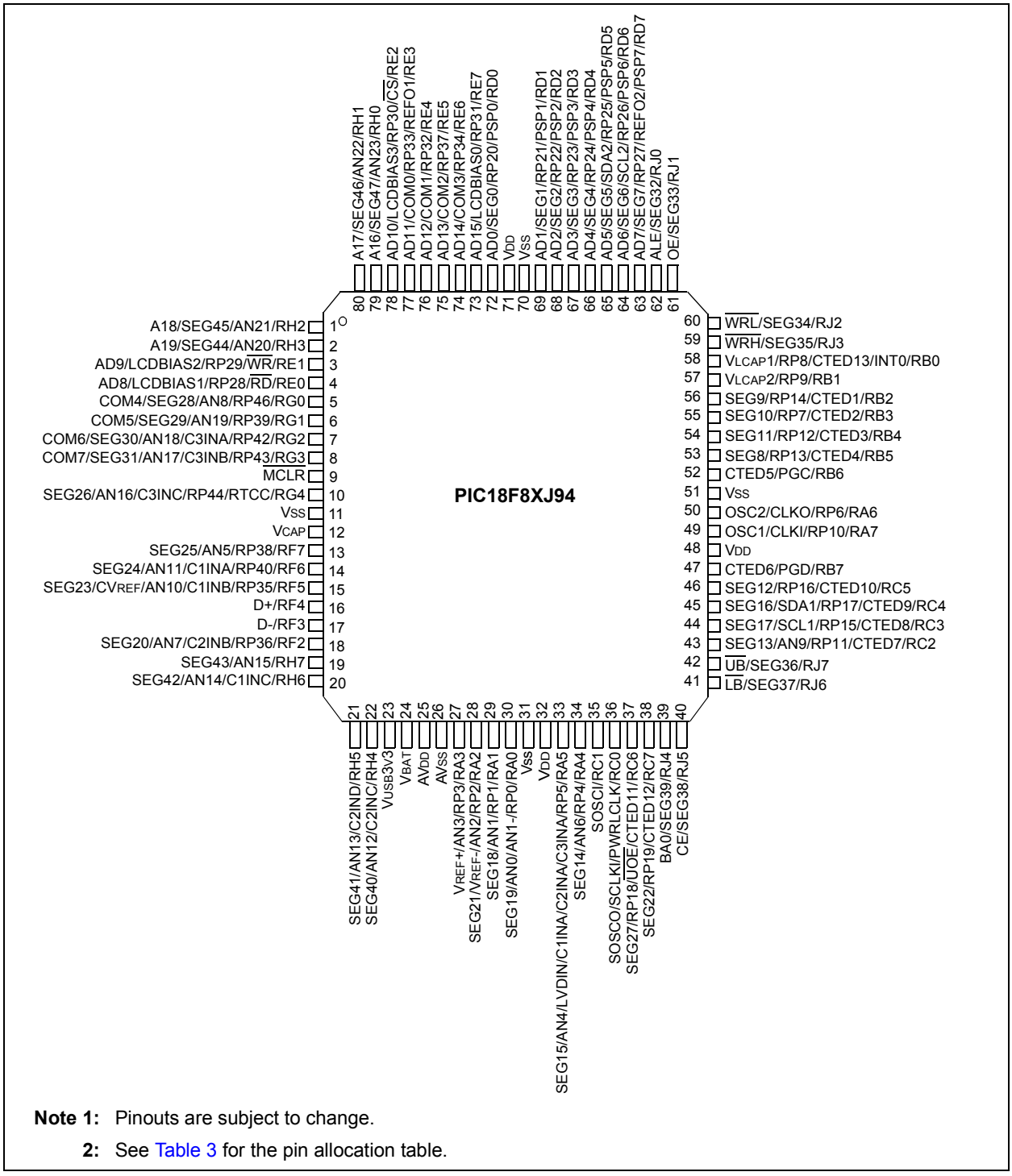
FIGURE 1: 64-PIN TQFP, QFN DIAGRAM FOR PIC18F6XJ94



Note 1: Pinouts are subject to change.

2: See Table 2 for the pin allocation table.

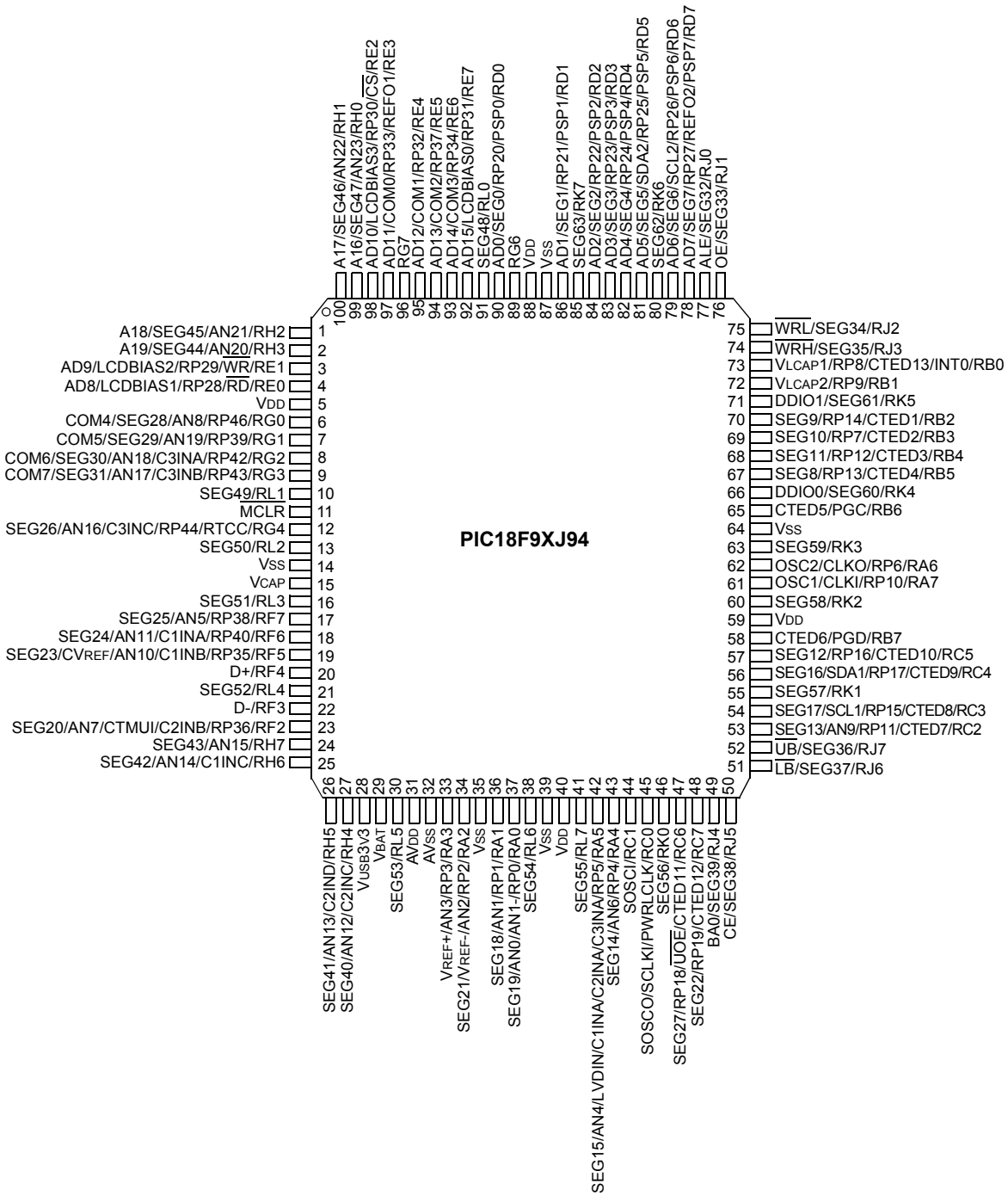
FIGURE 2: 80-PIN TQFP DIAGRAM FOR PIC18F8XJ94



Note 1: Pinouts are subject to change.

2: See Table 3 for the pin allocation table.

FIGURE 3: 100-PIN TQFP DIAGRAM FOR PIC18F9XJ94



Note 1: Pinouts are subject to change.

2: See Table 4 for the pin allocation table.

PIN ALLOCATION TABLES

TABLE 2: 64-PIN ALLOCATION TABLE (PIC18F6XJ94)

I/O	64-Pin TQFP/QFN	ADC	Comparator	HLVD	CTMU	USB	LCD	MSSP	PSP	Interrupt	REFO	PPS-Lite(1)	Pull-up	Basic
RA0	24	AN0/ AN1-	—	—	—	—	SEG19	—	—	—	—	RP0	—	—
RA1	23	AN1	—	—	—	—	SEG18	—	—	—	—	RP1	—	—
RA2	22	AN2/ VREF-	—	—	—	—	SEG21	—	—	—	—	RP2	—	—
RA3	21	AN3/ VREF+	—	—	—	—	—	—	—	—	—	RP3	—	—
RA4	28	AN6	—	—	—	—	SEG14	—	—	—	—	RP4	—	—
RA5	27	AN4	C1INA/ C2INA/ C3INA	LVDIN	—	—	SEG15	—	—	—	—	RP5	—	—
RA6	40	—	—	—	—	—	—	—	—	—	—	RP6	—	OSC2/ CLKO
RA7	39	—	—	—	—	—	—	—	—	—	—	RP10	—	OSC1/ CLKI
RB0	48	—	—	—	CTED13	—	VLCAP1	—	—	INT0	—	RP8	—	—
RB1	47	—	—	—	—	—	VLCAP2	—	—	—	—	RP9	—	—
RB2	46	—	—	—	CTED1	—	SEG9	—	—	—	—	RP14	—	—
RB3	45	—	—	—	CTED2	—	SEG10	—	—	—	—	RP7	—	—
RB4	44	—	—	—	CTED3	—	SEG11	—	—	—	—	RP12	—	—
RB5	43	—	—	—	CTED4	—	SEG8	—	—	—	—	RP13	—	—
RB6	42	—	—	—	CTED5	—	—	—	—	—	—	—	—	PGC
RB7	37	—	—	—	CTED6	—	—	—	—	—	—	—	—	PGD
RC0	30	—	—	—	—	—	—	—	—	—	—	—	—	SOSCO/ SCKI/ PWRCLK
RC1	29	—	—	—	—	—	—	—	—	—	—	—	—	SOSCI
RC2	33	AN9	—	—	CTED7	—	SEG13	—	—	—	—	RP11	—	—
RC3	34	—	—	—	CTED8	—	SEG17	SCL1	—	—	—	RP15	—	—
RC4	35	—	—	—	CTED9	—	SEG16	SDA1	—	—	—	RP17	—	—
RC5	36	—	—	—	CTED10	—	SEG12	—	—	—	—	RP16	—	—
RC6	31	—	—	—	CTED11	$\overline{UOE}$	SEG27	—	—	—	—	RP18	—	—
RC7	32	—	—	—	CTED12	—	SEG22	—	—	—	—	RP19	—	—
RD0	58	—	—	—	—	—	SEG0	—	PSP0	—	—	RP20	Y	—
RD1	55	—	—	—	—	—	SEG1	—	PSP1	—	—	RP21	Y	—
RD2	54	—	—	—	—	—	SEG2	—	PSP2	—	—	RP22	Y	—
RD3	53	—	—	—	—	—	SEG3	—	PSP3	—	—	RP23	Y	—
RD4	52	—	—	—	—	—	SEG4	—	PSP4	—	—	RP24	Y	—
RD5	51	—	—	—	—	—	SEG5	SDA2	PSP5	—	—	RP25	Y	—
RD6	50	—	—	—	—	—	SEG6	SCL2	PSP6	—	—	RP26	Y	—
RD7	49	—	—	—	—	—	SEG7	—	PSP7	—	REFO2	RP27	Y	—
RE0	2	—	—	—	—	—	LCDBIAS1	—	$\overline{RD}$	—	—	RP28	Y	—
RE1	1	—	—	—	—	—	LCDBIAS2	—	$\overline{WR}$	—	—	RP29	Y	—
RE2	64	—	—	—	—	—	LCDBIAS3	—	$\overline{CS}$	—	—	RP30	Y	—
RE3	63	—	—	—	—	—	COM0	—	—	—	REFO1	RP33	Y	—
RE4	62	—	—	—	—	—	COM1	—	—	—	—	RP32	Y	—
RE5	61	—	—	—	—	—	COM2	—	—	—	—	RP37	Y	—

TABLE 2: 64-PIN ALLOCATION TABLE (PIC18F6XJ94) (CONTINUED)

I/O	64-Pin TQFP/QFN	ADC	Comparator	HLVD	CTMU	USB	LCD	MSSP	PSP	Interrupt	REFO	PPS-Lite(1)	Pull-up	Basic
RE6	60	—	—	—	—	—	COM3	—	—	—	—	RP34	Y	—
RE7	59	—	—	—	—	—	LCDBIAS0	—	—	—	—	RP31	Y	—
RF2	16	AN7	C2INB	—	CTMUI	—	SEG20	—	—	—	—	RP36	Y	—
RF3	15	—	—	—	—	D-	—	—	—	—	—	—	Y	—
RF4	14	—	—	—	—	D+	—	—	—	—	—	—	Y	—
RF5	13	AN10	C1INB/ CVREF	—	—	—	SEG23	—	—	—	—	RP35	Y	—
RF6	12	AN11	C1INA	—	—	—	SEG24	—	—	—	—	RP40	Y	—
RF7	11	AN5	—	—	—	—	SEG25	—	—	—	—	RP38	Y	—
RG0	3	AN8	—	—	—	—	COM4/ SEG28	—	—	—	—	RP46	Y	—
RG1	4	AN19	—	—	—	—	COM5/ SEG29	—	—	—	—	RP39	Y	—
RG2	5	AN18	C3INA	—	—	—	COM6/ SEG30	—	—	—	—	RP42	Y	—
RG3	6	AN17	C3INB	—	—	—	COM7/ SEG31	—	—	—	—	RP43	Y	—
RG4	8	AN16	C3INC	—	—	—	SEG26	—	—	—	—	RP44	Y	—
RG5/ MCLR	7	—	—	—	—	—	—	—	—	—	—	—	Y	$\overline{\text{MCLR}}$
AVDD	19	AVDD	—	—	—	—	—	—	—	—	—	—	—	—
AVSS	20	AVSS	—	—	—	—	—	—	—	—	—	—	—	—
VBAT	18	—	—	—	—	—	—	—	—	—	—	—	—	VBAT
VCAP/ VDDCORE	10	—	—	—	—	—	—	—	—	—	—	—	—	VCAP/ VDDCORE
VDD	26, 38, 57	—	—	—	—	—	—	—	—	—	—	—	—	VDD
VSS	9, 25, 41, 56	—	—	—	—	—	—	—	—	—	—	—	—	VSS
VUSB3V3	17	—	—	—	—	—	—	—	—	—	—	—	—	VUSB3V3

Note 1: The peripheral inputs and outputs that support PPS have no default pins.

TABLE 3: 80-PIN ALLOCATION TABLE (PIC18F8XJ94)

I/O	80-Pin TQFP	ADC	Comparator	HLVD	CTMU	USB	LCD	MSSP	PSP	Interrupt	REFO	EMB	PPS-Lite(1)	Pull-up	Basic
RA0	30	AN0/ AN1-	—	—	—	—	SEG19	—	—	—	—	—	RP0	—	—
RA1	29	AN1	—	—	—	—	SEG18	—	—	—	—	—	RP1	—	—
RA2	28	AN2/ VREF-	—	—	—	—	SEG21	—	—	—	—	—	RP2	—	—
RA3	27	AN3/ VREF+	—	—	—	—	—	—	—	—	—	—	RP3	—	—
RA4	34	AN6	—	—	—	—	SEG14	—	—	—	—	—	RP4	—	—
RA5	33	AN4	C1INA/ C2INA/ C3INA	LVDIN	—	—	SEG15	—	—	—	—	—	RP5	—	—
RA6	50	—	—	—	—	—	—	—	—	—	—	—	RP6	—	OSC2/ CLKO
RA7	49	—	—	—	—	—	—	—	—	—	—	—	RP10	—	OSC1/ CLKI
RB0	58	—	—	—	CTED13	—	VLCAP1	—	—	INT0	—	—	RP8	—	—
RB1	57	—	—	—	—	—	VLCAP2	—	—	—	—	—	RP9	—	—
RB2	56	—	—	—	CTED1	—	SEG9	—	—	—	—	—	RP14	—	—
RB3	55	—	—	—	CTED2	—	SEG10	—	—	—	—	—	RP7	—	—
RB4	54	—	—	—	CTED3	—	SEG11	—	—	—	—	—	RP12	—	—
RB5	53	—	—	—	CTED4	—	SEG8	—	—	—	—	—	RP13	—	—
RB6	52	—	—	—	CTED5	—	—	—	—	—	—	—	—	—	PGC
RB7	47	—	—	—	CTED6	—	—	—	—	—	—	—	—	—	PGD
RC0	36	—	—	—	—	—	—	—	—	—	—	—	—	—	SOSCO/ SCKI/ PWRCLK
RC1	35	—	—	—	—	—	—	—	—	—	—	—	—	—	SOSCI
RC2	43	AN9	—	—	CTED7	—	SEG13	—	—	—	—	—	RP11	—	—
RC3	44	—	—	—	CTED8	—	SEG17	SCL1	—	—	—	—	RP15	—	—
RC4	45	—	—	—	CTED9	—	SEG16	SDA1	—	—	—	—	RP17	—	—
RC5	46	—	—	—	CTED10	—	SEG12	—	—	—	—	—	RP16		
RC6	37	—	—	—	CTED11	$\overline{UOE}$	SEG27	—	—	—	—	—	RP18	—	—
RC7	38	—	—	—	CTED12	—	SEG22	—	—	—	—	—	RP19	—	—
RD0	72	—	—	—	—	—	SEG0	—	PSP0	—	—	AD0	RP20	Y	—
RD1	69	—	—	—	—	—	SEG1	—	PSP1	—	—	AD1	RP21	Y	—
RD2	68	—	—	—	—	—	SEG2	—	PSP2	—	—	AD2	RP22	Y	—
RD3	67						SEG3		PSP3			AD3	RP23	Y	—
RD4	66	—	—	—	—	—	SEG4	—	PSP4	—	—	AD4	RP24	Y	—
RD5	65	—	—	—	—	—	SEG5	SDA2	PSP5	—	—	AD5	RP25	Y	—
RD6	64	—	—	—	—	—	SEG6	SCL2	PSP6	—	—	AD6	RP26	Y	—
RD7	63	—	—	—	—	—	SEG7	—	PSP7	—	REFO2	AD7	RP27	Y	—
RE0	4	—	—	—	—	—	LCDBIAS1	—	$\overline{RD}$	—	—	AD8	RP28	Y	—
RE1	3	—	—	—	—	—	LCDBIAS2	—	$\overline{WR}$	—	—	AD9	RP29	Y	—
RE2	78	—	—	—	—	—	LCDBIAS3	—	$\overline{CS}$	—	—	AD10	RP30	Y	—
RE3	77	—	—	—	—	—	COM0	—	—	—	REFO1	AD11	RP33	Y	—
RE4	76	—	—	—	—	—	COM1	—	—	—	—	AD12	RP32	Y	—
RE5	75	—	—	—	—	—	COM2	—	—	—	—	AD13	RP37	Y	—
RE6	74	—	—	—	—	—	COM3	—	—	—	—	AD14	RP34	Y	—
RE7	73	—	—	—	—	—	LCDBIAS0	—	—	—	—	AD15	RP31	Y	—
RF2	18	AN7	C2INB		CTMUI		SEG20	—	—	—	—	—	RP36	Y	—

TABLE 3: 80-PIN ALLOCATION TABLE (PIC18F8XJ94) (CONTINUED)

I/O	80-Pin TQFP	ADC	Comparator	HLVD	CTMU	USB	LCD	MSSP	PSP	Interrupt	REFO	EMB	PPS-Lite(1)	Pull-up	Basic
RF3	17	—	—	—	—	D-	—	—	—	—	—	—	—	Y	—
RF4	16	—	—	—	—	D+	—	—	—	—	—	—	—	Y	—
RF5	15	AN10	C1INB/ CVREF	—	—	—	SEG23	—	—	—	—	—	RP35	Y	—
RF6	14	AN11	C1INA	—	—	—	SEG24	—	—	—	—	—	RP40	Y	—
RF7	13	AN5	—	—	—	—	SEG25	—	—	—	—	—	RP38	Y	—
RG0	5	AN8	—	—	—	—	COM4/ SEG28	—	—	—	—	—	RP46	Y	—
RG1	6	AN19	—	—	—	—	COM5/ SEG29	—	—	—	—	—	RP39	Y	—
RG2	7	AN18	C3INA	—	—	—	COM6/ SEG30	—	—	—	—	—	RP42	Y	—
RG3	8	AN17	C3INB	—	—	—	COM7/ SEG31	—	—	—	—	—	RP43	Y	—
RG4	10	AN16	C3INC	—	—	—	SEG26	—	—	—	—	—	RP44	Y	—
RG5/ MCLR	9	—	—	—	—	—	—	—	—	—	—	—	—	Y	$\overline{MCLR}$
RH0	79	AN23	—	—	—	—	SEG47	—	—	—	—	A16	—	Y	—
RH1	80	AN22	—	—	—	—	SEG46	—	—	—	—	A17	—	Y	—
RH2	1	AN21	—	—	—	—	SEG45	—	—	—	—	A18	—	Y	—
RH3	2	AN20	—	—	—	—	SEG44	—	—	—	—	A19	—	Y	—
RH4	22	AN12	C2INC	—	—	—	SEG40	—	—	—	—	—	—	Y	—
RH5	21	AN13	C2IND	—	—	—	SEG41	—	—	—	—	—	—	Y	—
RH6	20	AN14	C1INC	—	—	—	SEG42	—	—	—	—	—	—	Y	—
RH7	19	AN15	—	—	—	—	SEG43	—	—	—	—	—	—	Y	—
RJ0	62	—	—	—	—	—	SEG32	—	—	—	—	ALE	—	Y	—
RJ1	61	—	—	—	—	—	SEG33	—	—	—	—	$\overline{OE}$	—	Y	—
RJ2	60	—	—	—	—	—	SEG34	—	—	—	—	$\overline{WRL}$	—	Y	—
RJ3	59	—	—	—	—	—	SEG35	—	—	—	—	$\overline{WRH}$	—	Y	—
RJ4	39	—	—	—	—	—	SEG39	—	—	—	—	BA0	—	Y	—
RJ5	40	—	—	—	—	—	SEG38	—	—	—	—	$\overline{CE}$	—	Y	—
RJ6	41	—	—	—	—	—	SEG37	—	—	—	—	$\overline{LB}$	—	Y	—
RJ7	42	—	—	—	—	—	SEG36	—	—	—	—	$\overline{UB}$	—	Y	—
AVDD	25	AVDD	—	—	—	—	—	—	—	—	—	—	—	—	—
AVSS	26	AVSS	—	—	—	—	—	—	—	—	—	—	—	—	—
VBAT	24	—	—	—	—	—	—	—	—	—	—	—	—	—	VBAT
VCAP/ VDDCORE	12	—	—	—	—	—	—	—	—	—	—	—	—	—	VCAP/ VDDCORE
VDD	32, 48, 71	—	—	—	—	—	—	—	—	—	—	—	—	—	VDD
VSS	11, 31, 51, 70	—	—	—	—	—	—	—	—	—	—	—	—	—	VSS
VUSB3V3	23	—	—	—	—	—	—	—	—	—	—	—	—	—	VUSB3V3

Note 1: The peripheral inputs and outputs that support PPS have no default pins.

TABLE 4: 100-PIN ALLOCATION TABLE (PIC18F9XJ94)

I/O	100-Pin TQFP	ADC	Comparator	HLVD	CTMU	USB	LCD	MSSP	PSP	Interrupt	REFO	EMB	PPS-Lite(1)	Pull-up	Basic
RA0	37	AN0/ AN1-	—	—	—	—	SEG19	—	—	—	—	—	RP0	—	—
RA1	36	AN1	—	—	—	—	SEG18	—	—	—	—	—	RP1	—	—
RA2	34	AN2/ VREF-	—	—	—	—	SEG21	—	—	—	—	—	RP2	—	—
RA3	33	AN3/ VREF+	—	—	—	—	—	—	—	—	—	—	RP3	—	—
RA4	43	AN6	—	—	—	—	SEG14	—	—	—	—	—	RP4	—	—
RA5	42	AN4	C1INA/ C2INA/ C3INA	LVDIN	—	—	SEG15	—	—	—	—	—	RP5	—	—
RA6	62	—	—	—	—	—	—	—	—	—	—	—	RP6	—	OSC2/ CLKO
RA7	61	—	—	—	—	—	—	—	—	—	—	—	RP10	—	OSC1/ CLKI
RB0	73	—	—	—	CTED13	—	VLCAP1	—	—	INT0	—	—	RP8	—	—
RB1	72	—	—	—	—	—	VLCAP2	—	—	—	—	—	RP9	—	—
RB2	70	—	—	—	CTED1	—	SEG9	—	—	—	—	—	RP14	—	—
RB3	69	—	—	—	CTED2	—	SEG10	—	—	—	—	—	RP7	—	—
RB4	68	—	—	—	CTED3	—	SEG11	—	—	—	—	—	RP12	—	—
RB5	67	—	—	—	CTED4	—	SEG8	—	—	—	—	—	RP13	—	—
RB6	65	—	—	—	CTED5	—	—	—	—	—	—	—	—	—	PGC
RB7	58	—	—	—	CTED6	—	—	—	—	—	—	—	—	—	PGD
RC0	45	—	—	—	—	—	—	—	—	—	—	—	—	—	SOSCO/ SCKI/ PWRCLK
RC1	44	—	—	—		—	—	—	—	—	—	—	—	—	SOSCI
RC2	53	AN9	—	—	CTED7	—	SEG13	—	—	—	—	—	RP11	—	—
RC3	54	—	—	—	CTED8	—	SEG17	SCL1	—	—	—	—	RP15	—	—
RC4	56	—	—	—	CTED9	—	SEG16	SDA1	—	—	—	—	RP17	—	—
RC5	57	—	—	—	CTED10	—	SEG12	—	—	—	—	—	RP16	—	—
RC6	47	—	—	—	CTED11	$\overline{\text{UOE}}$	SEG27	—	—	—	—	—	RP18	—	—
RC7	48	—	—	—	CTED12	—	SEG22	—	—	—	—	—	RP19	—	—
RD0	90	—	—	—	—	—	SEG0	—	PSP0	—	—	AD0	RP20	Y	—
RD1	86	—	—	—	—	—	SEG1	—	PSP1	—	—	AD1	RP21	Y	—
RD2	84	—	—	—	—	—	SEG2	—	PSP2	—	—	AD2	RP22	Y	—
RD3	83	—	—	—	—	—	SEG3	—	PSP3	—	—	AD3	RP23	Y	—
RD4	82	—	—	—	—	—	SEG4	—	PSP4	—	—	AD4	RP24	Y	—
RD5	81	—	—	—	—	—	SEG5	SDA2	PSP5	—	—	AD5	RP25	Y	—
RD6	79	—	—	—	—	—	SEG6	SCL2	PSP6	—	—	AD6	RP26	Y	—
RD7	78	—	—	—	—	—	SEG7	—	PSP7	—	REFO2	AD7	RP27	Y	—
RE0	4	—	—	—	—	—	LCDBIAS1	—	RD-bar	—	—	AD8	RP28	Y	—
RE1	3	—	—	—	—	—	LCDBIAS2	—	WR-bar	—	—	AD9	RP29	Y	—
RE2	98	—	—	—	—	—	LCDBIAS3	—	CS-bar	—	—	AD10	RP30	Y	—
RE3	97	—	—	—	—	—	COM0	—	—	—	REFO1	AD11	RP33	Y	—
RE4	95	—	—	—	—	—	COM1	—	—	—	—	AD12	RP32	Y	—
RE5	94	—	—	—	—	—	COM2	—	—	—	—	AD13	RP37	Y	—
RE6	93	—	—	—	—	—	COM3	—	—	—	—	AD14	RP34	Y	—
RE7	92	—	—	—	—	—	LCDBIAS0	—	—	—	—	AD15	RP31	Y	—

TABLE 4: 100-PIN ALLOCATION TABLE (PIC18F9XJ94) (CONTINUED)

I/O	100-Pin TQFP	ADC	Comparator	HLVD	CTMU	USB	LCD	MSSP	PSP	Interrupt	REFO	EMB	PPS-Lite(1)	Pull-up	Basic
RF2	23	AN7	C2INB	—	CTMUI	—	SEG20	—	—	—	—	—	RP36	Y	—
RF3	22	—	—	—	—	D-	—	—	—	—	—	—	—	Y	—
RF4	20	—	—	—	—	D+	—	—	—	—	—	—	—	Y	—
RF5	19	AN10	C1INB/ CVREF	—	—	—	SEG23	—	—	—	—	—	RP35	Y	—
RF6	18	AN11	C1INA	—	—	—	SEG24	—	—	—	—	—	RP40	Y	—
RF7	17	AN5	—	—	—	—	SEG25	—	—	—	—	—	RP38	Y	—
RG0	6	AN8	—	—	—	—	COM4/ SEG28	—	—	—	—	—	RP46	Y	—
RG1	7	AN19	—	—	—	—	COM5/ SEG29	—	—	—	—	—	RP39	Y	—
RG2	8	AN18	C3INA	—	—	—	COM6/ SEG30	—	—	—	—	—	RP42	Y	—
RG3	9	AN17	C3INB	—	—	—	COM7/ SEG31	—	—	—	—	—	RP43	Y	—
RG4	12	AN16	C3INC	—	—	—	SEG26	—	—	—	—	—	RP44	Y	—
RG5/ MCLR	11	—	—	—	—	—	—	—	—	—	—	—	—	Y	$\overline{\text{MCLR}}$
RG6	89	—	—	—	—	—	—	—	—	—	—	—	—	Y	—
RG7	96	—	—	—	—	—	—	—	—	—	—	—	—	Y	—
RH0	99	AN23	—	—	—	—	SEG47	—	—	—	—	A16	—	Y	—
RH1	100	AN22	—	—	—	—	SEG46	—	—	—	—	A17	—	Y	—
RH2	1	AN21	—	—	—	—	SEG45	—	—	—	—	A18	—	Y	—
RH3	2	AN20	—	—	—	—	SEG44	—	—	—	—	A19	—	Y	—
RH4	27	AN12	C2INC	—	—	—	SEG40	—	—	—	—	—	—	Y	—
RH5	26	AN13	C2IND	—	—	—	SEG41	—	—	—	—	—	—	Y	—
RH6	25	AN14	C1INC	—	—	—	SEG42	—	—	—	—	—	—	Y	—
RH7	24	AN15	—	—	—	—	SEG43	—	—	—	—	—	—	Y	—
RJ0	77	—	—	—	—	—	SEG32	—	—	—	—	ALE	—	Y	—
RJ1	76	—	—	—	—	—	SEG33	—	—	—	—	$\overline{\text{OE}}$	—	Y	—
RJ2	75	—	—	—	—	—	SEG34	—	—	—	—	$\overline{\text{WRL}}$	—	Y	—
RJ3	74	—	—	—	—	—	SEG35	—	—	—	—	$\overline{\text{WRH}}$	—	Y	—
RJ4	49	—	—	—	—	—	SEG39	—	—	—	—	BA0	—	Y	—
RJ5	50	—	—	—	—	—	SEG38	—	—	—	—	$\overline{\text{CE}}$	—	Y	—
RJ6	51	—	—	—	—	—	SEG37	—	—	—	—	$\overline{\text{LB}}$	—	Y	—
RJ7	52	—	—	—	—	—	SEG36	—	—	—	—	$\overline{\text{UB}}$	—	Y	—
RK0	46	—	—	—	—	—	SEG56	—	—	—	—	—	—	Y	—
RK1	55	—	—	—	—	—	SEG57	—	—	—	—	—	—	Y	—
RK2	60	—	—	—	—	—	SEG58	—	—	—	—	—	—	Y	—
RK3	63	—	—	—	—	—	SEG59	—	—	—	—	—	—	Y	—
RK4	66	—	—	—	—	—	SEG60	—	—	—	—	—	—	Y	—
RK5	71	—	—	—	—	—	SEG61	—	—	—	—	—	—	Y	—
RK6	80	—	—	—	—	—	SEG62	—	—	—	—	—	—	Y	—
RK7	85	—	—	—	—	—	SEG63	—	—	—	—	—	—	Y	—
RL0	91	—	—	—	—	—	SEG48	—	—	—	—	—	—	Y	—
RL1	10	—	—	—	—	—	SEG49	—	—	—	—	—	—	Y	—
RL2	13	—	—	—	—	—	SEG50	—	—	—	—	—	—	Y	—
RL3	16	—	—	—	—	—	SEG51	—	—	—	—	—	—	Y	—
RL4	21	—	—	—	—	—	SEG52	—	—	—	—	—	—	Y	—
RL5	30	—	—	—	—	—	SEG53	—	—	—	—	—	—	Y	—

TABLE 4: 100-PIN ALLOCATION TABLE (PIC18F9XJ94) (CONTINUED)

I/O	100-Pin TQFP	ADC	Comparator	HLVD	CTMU	USB	LCD	MSSP	PSP	Interrupt	REFO	EMB	PPS-Lite(1)	Pull-up	Basic
RL6	38	—	—	—	—	—	SEG54	—	—	—	—	—	—	Y	—
RL7	41	—	—	—	—	—	SEG55	—	—	—	—	—	—	Y	—
AVDD	31	AVDD	—	—	—	—	—	—	—	—	—	—	—	—	—
AVSS	32	AVSS	—	—	—	—	—	—	—	—	—	—	—	—	—
VBAT	29	—	—	—	—	—	—	—	—	—	—	—	—	—	VBAT
VCAP/ VDDCORE	15	—	—	—	—	—	—	—	—	—	—	—	—	—	VCAP/ VDDCORE
VDD	5, 40, 59, 88	—	—	—	—	—	—	—	—	—	—	—	—	—	VDD
VSS	14, 35, 39, 64, 87	—	—	—	—	—	—	—	—	—	—	—	—	—	VSS
VUSB3V3	28	—	—	—	—	—	—	—	—	—	—	—	—	—	VUSB3V3

Note 1: The peripheral inputs and outputs that support PPS have no default pins.

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Errata

An errata sheet, describing minor operational differences from the data sheet and recommended workarounds, may exist for current devices. As device/documentation issues become known to us, we will publish an errata sheet. The errata will specify the revision of silicon and revision of document to which it applies.

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1.0 DEVICE OVERVIEW

This document contains device-specific information for the following devices:

- PIC18F97J94
- PIC18F87J94
- PIC18F67J94
- PIC18F96J94
- PIC18F86J94
- PIC18F66J94
- PIC18F95J94
- PIC18F85J94
- PIC18F65J94

This family introduces a new line of low-voltage LCD microcontrollers with Universal Serial Bus (USB). It combines all the main traditional advantage of all PIC18 microcontrollers, namely, high computational performance and a rich feature set at an extremely competitive price point. These features make the PIC18F9XJ94 family a logical choice for many high-performance applications, where cost is a primary consideration.

1.1 Core Features

1.1.1 TECHNOLOGY

All of the devices in the PIC18F9XJ94 family incorporate a range of features that can significantly reduce power consumption during operation. Key items include:

- **Alternate Run Modes:** By clocking the controller from the Timer1 source or the Internal RC oscillator, power consumption during code execution can be reduced.
- **Multiple Idle Modes:** The controller can also run with its CPU core disabled but the peripherals still active. In these states, power consumption can be reduced even further.
- **On-the-Fly Mode Switching:** The power-managed modes are invoked by user code during operation, allowing the user to incorporate power-saving ideas into their application's software design.
- **XLP:** An extra low-power Sleep, BOR, RTCC and Watchdog Timer.

1.1.2 OSCILLATOR OPTIONS AND FEATURES

All of the devices in the PIC18F9XJ94 family offer different oscillator options, allowing users a range of choices in developing application hardware. These include:

- Two Crystal modes (HS, MS)
- One External Clock mode (EC)
- A Phase Lock Loop (PLL) frequency multiplier, which allows clock speeds of up to 64 MHz.
- A fast Internal Oscillator (FRC) block that provides an 8 MHz clock (±0.15% accuracy) with Active Clock Tuning (ACT) from USB or SOSC source.
  - Offers multiple divider options from 8 MHz to 500 kHz
  - Frees the two oscillator pins for use as additional general purpose I/O
- A separate Low-Power Internal RC Oscillator (LPRC) (31 kHz nominal) for low-power, timing-insensitive applications.

The internal oscillator block provides a stable reference source that gives the family additional features for robust operation:

- **Fail-Safe Clock Monitor (FSCM):** This option constantly monitors the main clock source against a reference signal provided by the internal oscillator. If a clock failure occurs, the controller is switched to the internal oscillator, allowing for continued low-speed operation or a safe application shutdown.
- **Two-Speed Start-up (IESO):** This option allows the internal oscillator to serve as the clock source from Power-on Reset, or wake-up from Sleep mode, until the primary clock source is available.

1.1.3 MEMORY OPTIONS

The PIC18F9XJ94 family provides ample room for application code, from 32 Kbytes to 128 Kbytes of code space. The Flash cells for program memory are rated to last up to 20,000 erase/write cycles. Data retention without refresh is conservatively estimated to be greater than 10 years.

The Flash program memory is readable and writable. During normal operation, the PIC18F9XJ94 family also provides plenty of room for dynamic application data with up to 3,578 bytes of data RAM.

1.1.4 UNIVERSAL SERIAL BUS (USB)

Devices in the PIC18F9XJ94 family incorporate a fully-featured USB communications module with a built-in transceiver that is compliant with the USB Specification Revision 2.0. The module supports both low-speed and full-speed communication for all supported data transfer types.

1.1.5 EXTERNAL MEMORY BUS

Should 128 Kbytes of memory be inadequate for an application, the 80-pin and 100-pin members of the PIC18F9XJ94 family have an External Memory Bus (EMB), enabling the controller's internal Program Counter to address a memory space of up to 2 Mbytes. This is a level of data access that few 8-bit devices can claim and enables:

- Using combinations of on-chip and external memory of up to 2 Mbytes
- Using external Flash memory for reprogrammable application code or large data tables
- Using external RAM devices for storing large amounts of variable data

1.1.6 EXTENDED INSTRUCTION SET

The PIC18F9XJ94 family implements the optional extension to the PIC18 instruction set, adding eight new instructions and an Indexed Addressing mode. Enabled as a device configuration option, the extension has been specifically designed to optimize re-entrant application code originally developed in high-level languages, such as 'C'.

1.1.7 EASY MIGRATION

All devices share the same rich set of peripherals. This provides a smooth migration path within the device family as applications evolve and grow.

The consistent pinout scheme, used throughout the entire family, also aids in migrating to the next larger device. This is true when moving between the 64-pin members, between the 80-pin members, between the 100-pin members or even jumping from 64-pin to 80-pin to 100-pin devices.

The PIC18F9XJ94 family is also largely pin compatible with other PIC18 families, such as the PIC18F87J90, PIC18F87J11 and the PIC18F87J50. This allows a new dimension to the evolution of applications, allowing developers to select different price points within Microchip's PIC18 portfolio, while maintaining a similar feature set.

1.2 LCD Controller

The on-chip LCD driver includes many features that make the integration of displays in low-power applications easier. These include an integrated voltage regulator with charge pump and an integrated internal resistor ladder that allows contrast control in software and display operation above device V_{DD}.

1.3 Other Special Features

- **Communications:** The PIC18F9XJ94 family incorporates a range of serial communication peripherals, including USB, four Enhanced Addressable USARTs with IrDA, and two Master Synchronous Serial Port MSSP modules capable of both SPI and I^2C (Master and Slave) modes of operation.
- **CCP Modules:** PIC18F9XJ94 family devices incorporate up to seven Capture/Compare/PWM (CCP) modules. Up to six different time bases can be used to perform several different operations at once.
- **ECCP Modules:** The PIC18F9XJ94 family has three Enhanced CCP (ECCP) modules to maximize flexibility in control applications:
  - Up to eight different time bases for performing several different operations at once
  - Up to four PWM outputs for each module – for a total of 12 PWMs
  - Other beneficial features, such as polarity selection, programmable dead time, auto-shutdown and restart, and Half-Bridge and Full-Bridge Output modes
- **12-Bit A/D Converter:** The PIC18F9XJ94 family has a software selectable, 10/12-bit Analog-to-Digital (A/D) Converter. It incorporates programmable acquisition time, allowing for a channel to be selected and a conversion to be initiated without waiting for a sampling period, and thus, reducing code overhead.
- **Charge Time Measurement Unit (CTMU):** The CTMU is a flexible analog module that provides accurate differential time measurement between pulse sources, as well as asynchronous pulse generation.
- Together with other on-chip analog modules, the CTMU can precisely measure time, measure capacitance or relative changes in capacitance, or generate output pulses that are independent of the system clock.
- **LP Watchdog Timer (WDT):** This enhanced version incorporates a 22-bit prescaler, allowing an extended time-out range that is stable across operating voltage and temperature. See **Section 30.0 "Electrical Specifications"** for time-out periods.
- **Real-Time Clock and Calendar Module (RTCC):** The RTCC module is intended for applications requiring that accurate time be maintained for extended periods of time, with minimum to no intervention from the CPU.
- The module is a 100-year clock and calendar with automatic leap year detection. The range of the clock is from 00:00:00 (midnight) on January 1, 2000 to 23:59:59 on December 31, 2099.

1.4 Details on Individual Family Members

Devices in the PIC18F9XJ94 family are available in 64-pin, 80-pin and 100-pin packages. Block diagrams for the two groups are shown in Figure 1-1, Figure 1-2 and Figure 1-3.

The devices are differentiated from each other in these ways:

- Flash Program Memory:
  - PIC18FX5J94 – 32 Kbytes
  - PIC18FX6J94 – 64 Kbytes
  - PIC18FX7J94 – 128 Kbytes
- Data RAM:
  - All devices – 4 Kbytes
- I/O Ports:
  - PIC18F6XJ9X (64-pin devices) – seven bidirectional ports
  - PIC18F8XJ9X (80-pin devices) – nine bidirectional ports
  - PIC18F9XJ9X (100-pin devices) – eleven bidirectional ports
- A/D Channels:
  - PIC18F6XJXX (64-pin devices) – 16 channels
  - PIC18F8XJXX (80-pin devices) – 24 channels
  - PIC18F9XJXX (100-pin devices) – 24 channels

All other features for devices in this family are identical. These are summarized in Table 1-1, Table 1-2 and Table 1-3.

The pinouts for all devices are listed in Table 1-4.

TABLE 1-1: DEVICE FEATURES FOR THE 64-PIN DEVICES

Features	PIC18F65J94	PIC18F66J94	PIC18F67J94
Operating Frequency	DC – 64 MHz		
Program Memory (Bytes)	32K	64K	128K
Program Memory (Instructions)	16,384	32,768	65,536
Data Memory (Bytes)	4K	4K	4K
Interrupt Sources	42	48	
I/O Ports	Ports A, B, C, D, E, F, G		
Parallel Communications	Parallel Slave Port (PSP)		
Timers	8		
Comparators	3		
LCD	224 pixels		
CTMU	Yes		
RTCC	Yes		
Enhanced Capture/Compare/PWM Modules	3 ECCPs and 7 CCPs		
Serial Communications	Two MSSPs, Four Enhanced USARTs (EUSART) and USB		
10/12-Bit Analog-to-Digital Module	16 Input Channels		
Resets (and Delays)	POR, BOR, CM RESET Instruction, Stack Full, Stack Underflow, $\overline{\text{MCLR}}$, WDT (PWRT, OST)		
Instruction Set	75 Instructions, 83 with Extended Instruction Set Enabled		
Packages	64-Pin QFN, 64-Pin TQFP		

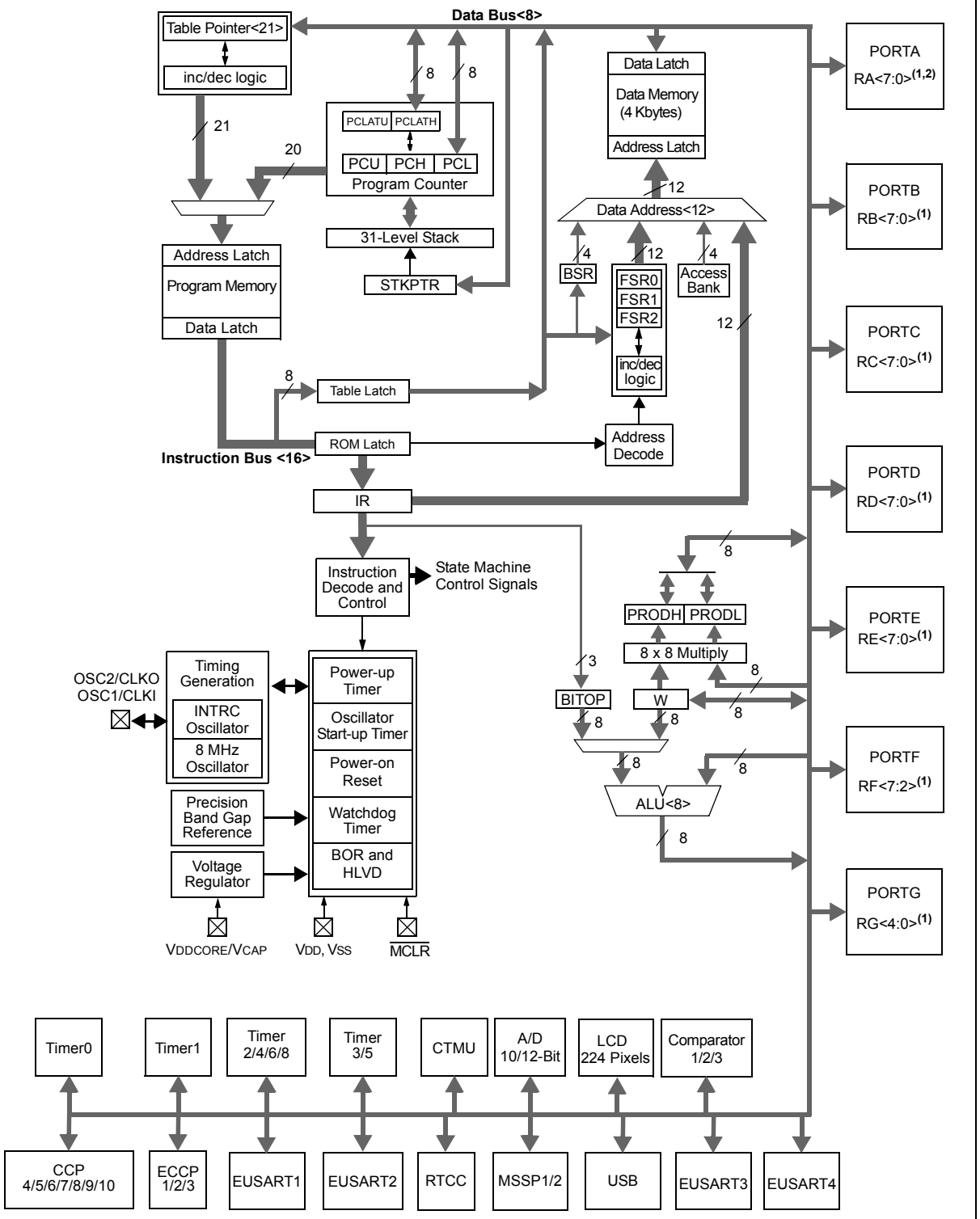
TABLE 1-2: DEVICE FEATURES FOR THE 80-PIN DEVICES

Features	PIC18F85J94	PIC18F86J94	PIC18F87J94
Operating Frequency	DC – 64 MHz		
Program Memory (Bytes)	32 K	64K	128K
	(Up to 2 Mbytes with Extended Memory)		
Program Memory (Instructions)	16,384	32,768	65,536
Data Memory (Bytes)	4K	4K	4K
Interrupt Sources	42	48	
I/O Ports	Ports A, B, C, D, E, F, G, H, J		
Parallel Communications	Parallel Slave Port (PSP)		
Timers	8		
Comparators	3		
LCD	352 pixels		
CTMU	Yes		
RTCC	Yes		
Enhanced Capture/Compare/PWM Modules	3 ECCPs and 7 CCPs		
Serial Communications	Two MSSPs, Four Enhanced USARTs (EUSART) and USB		
12-Bit Analog-to-Digital Module	24 Input Channels		
Resets (and Delays)	POR, BOR, CM RESET Instruction, Stack Full, Stack Underflow, $\overline{\text{MCLR}}$, WDT (PWRT, OST)		
Instruction Set	75 Instructions, 83 with Extended Instruction Set Enabled		
Packages	80-Pin TQFP		

TABLE 1-3: DEVICE FEATURES FOR THE 100-PIN DEVICES

Features	PIC18F95J94	PIC18F96J94	PIC18F97J94
Operating Frequency	DC – 64 MHz		
Program Memory (Bytes)	32 K	64K	128K
	(Up to 2 Mbytes with Extended Memory)		
Program Memory (Instructions)	16,384	32,768	65,536
Data Memory (Bytes)	4K	4K	4K
Interrupt Sources	42	48	
I/O Ports	Ports A, B, C, D, E, F, G, H, J, K, L		
Parallel Communications	Parallel Slave Port (PSP)		
Timers	8		
Comparators	3		
LCD	480 pixels		
CTMU	Yes		
RTCC	Yes		
Enhanced Capture/Compare/PWM Modules	3 ECCPs and 7 CCPs		
Serial Communications	Two MSSPs, Four Enhanced USARTs (EUSART) and USB		
12-Bit Analog-to-Digital Module	24 Input Channels		
Resets (and Delays)	POR, BOR, CM RESET Instruction, Stack Full, Stack Underflow, $\overline{\text{MCLR}}$, WDT (PWRT, OST)		
Instruction Set	75 Instructions, 83 with Extended Instruction Set Enabled		
Packages	100-Pin TQFP		

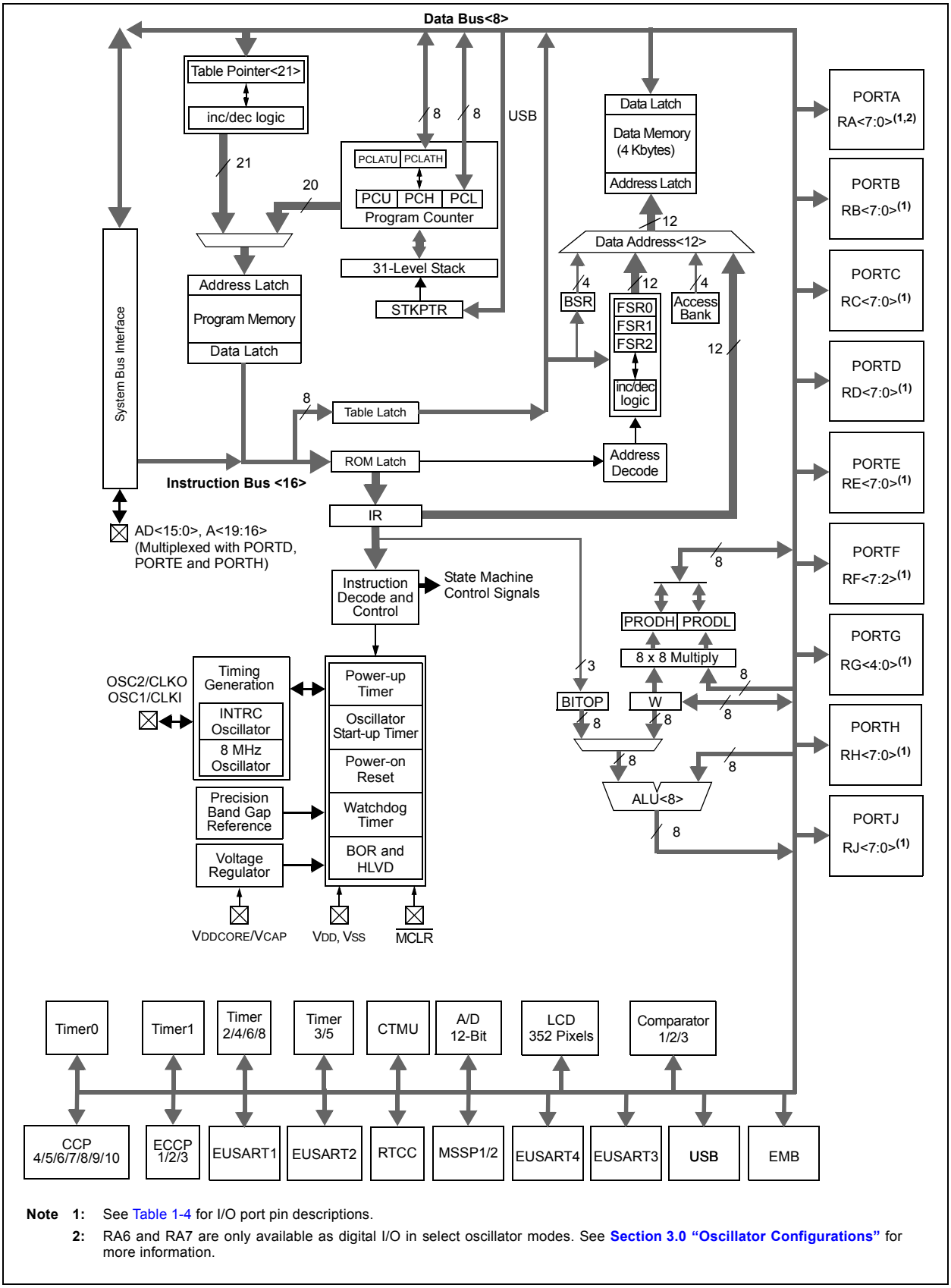
FIGURE 1-1: 64-PIN DEVICE BLOCK DIAGRAM



Note 1: See Table 1-4 for I/O port pin descriptions.

2: RA6 and RA7 are only available as digital I/O in select oscillator modes. For more information, see **Section 3.0 "Oscillator Configurations"**.

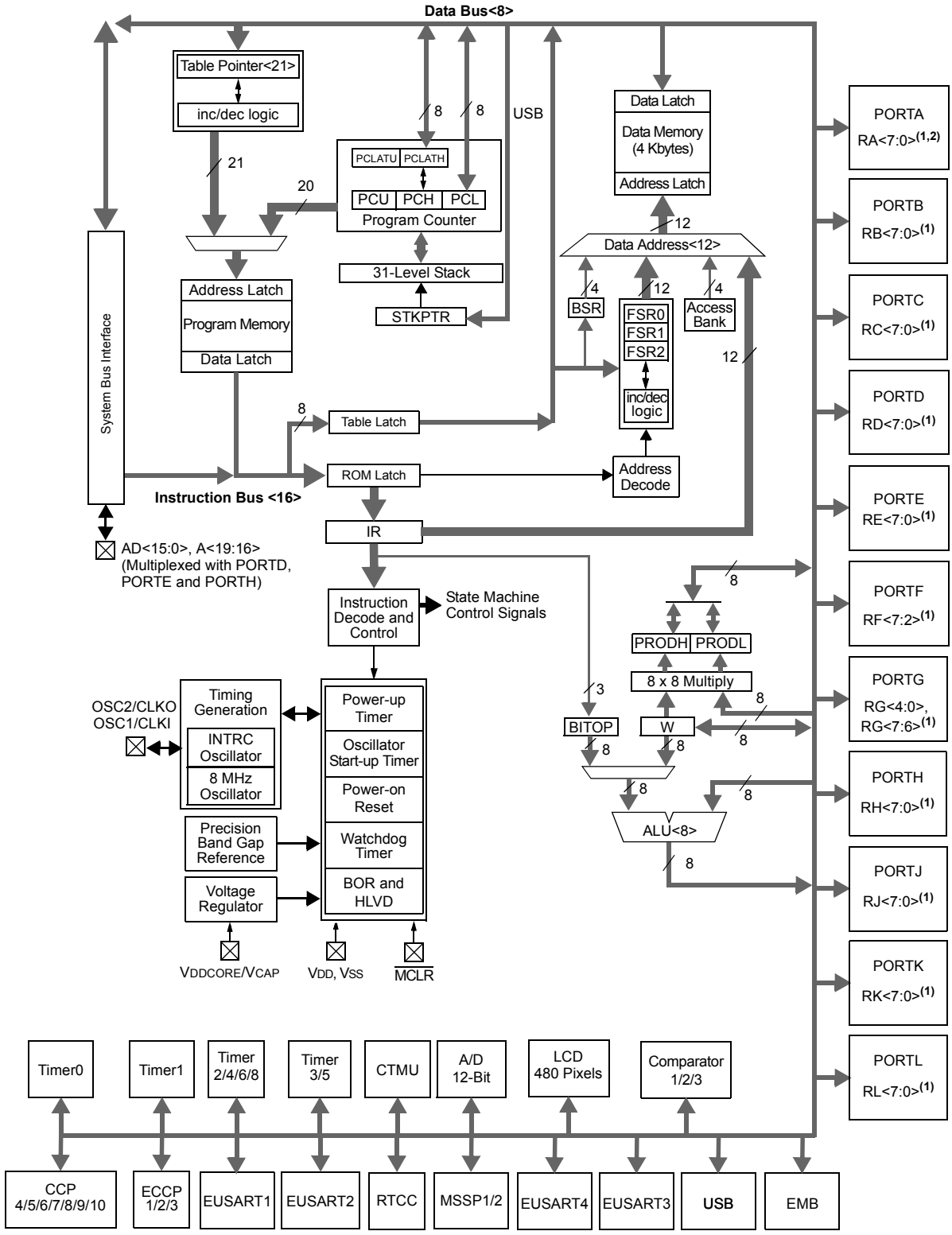
FIGURE 1-2: 80-PIN DEVICE BLOCK DIAGRAM



Note 1: See Table 1-4 for I/O port pin descriptions.

2: RA6 and RA7 are only available as digital I/O in select oscillator modes. See **Section 3.0 "Oscillator Configurations"** for more information.

FIGURE 1-3: 100-PIN DEVICE BLOCK DIAGRAM



Note 1: See Table 1-4 for I/O port pin descriptions.

2: RA6 and RA7 are only available as digital I/O in select oscillator modes. See **Section 3.0 "Oscillator Configurations"** for more information.

TABLE 1-4: PIC18FXXJ94 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	100	80	64			
$\overline{MCLR}$	11	9	7	I	ST	Master Clear (input) or programming voltage (input). This pin is an active-low Reset to the device.
OSC1/CLKI/RP10/RA7	61	49	39			Oscillator crystal or external clock input.
OSC1				I	ST	Oscillator crystal input.
CLKI				I	CMOS	External clock source input. Always associated with pin function, OSC1. (See related OSC1/CLKI,OSC2/CLKO pins.)
RP10				I/O	ST/DIG	Remappable Peripheral Pin 10 input/output.
RA7				I/O	ST/DIG	General purpose I/O pin.
OSC2/CLKO/RP6/RA6	62	50	40			Oscillator crystal or clock output.
OSC2				O	—	Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode.
CLKO				O	DIG	In certain oscillator modes, OSC2 pin outputs CLKO, which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate.
RP6				I/O	ST/DIG	Remappable Peripheral Pin 6 input/output.
RA6				I/O	ST/DIG	General purpose I/O pin.

Legend: TTL = TTL compatible input
ST = Schmitt Trigger input with CMOS levels
I = Input
P = Power
I^2C = I^2C/SMBus
CMOS = CMOS compatible input or output
Analog = Analog input
O = Output
OD = Open-Drain (no P diode to V_{DD})

TABLE 1-4: PIC18FXXJ94 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	100	80	64			
SEG19/AN0/AN1-/RP0/RA0	37	30	24			
SEG19				O	Analog	SEG19 output for LCD.
AN0				I	Analog	Analog Input 0.
AN1-				I	Analog	A/D negative input channel.
RP0				I/O	ST/DIG	Remappable Peripheral Pin 0 input/output.
RA0				I/O	ST/DIG	General purpose I/O pin.
SEG18/AN1/RP1/RA1	36	29	23			
SEG18				O	Analog	SEG18 output for LCD.
AN1				I	Analog	Analog Input 1.
RP1				I/O	ST/DIG	Remappable Peripheral Pin 1 input/output.
RA1				I/O	ST/DIG	General purpose I/O pin.
SEG21/VREF-/AN2/RP2/RA2	34	28	22			
SEG21				O	Analog	SEG21 output for LCD.
VREF-				I	Analog	A/D reference voltage (low) input.
AN2				I	Analog	Analog Input 2.
RP2				I/O	ST/DIG	Remappable Peripheral Pin 2 input/output.
RA2				I/O	ST/DIG	General purpose I/O pin.
VREF+/AN3/RP3/RA3	33	27	21			
VREF+				I	Analog	A/D reference voltage (high) input.
AN3				I	Analog	Analog Input 3.
RP3				I/O	ST/DIG	Remappable Peripheral Pin 3 input/output.
RA3				I/O	ST/DIG	General purpose I/O pin.
SEG14/AN6/RP4/RA4	43	34	28			
SEG14				O	Analog	SEG14 output for LCD.
AN6				I	Analog	Analog Input 6.
RP4				I/O	ST/DIG	Remappable Peripheral Pin 4 input/output.
RA4				I/O	ST/DIG	General purpose I/O pin.
SEG15/AN4/LVDIN/C1INA/ C2INA/C3INA/RP5/RA5	42	33	27			
SEG15				O	Analog	SEG15 output for LCD.
AN4				I	Analog	Analog Input 4.
LVDIN				I	Analog	High/Low-Voltage Detect (HLVD) input.
C1INA				I	Analog	Comparator 1 Input A.
C2INA				I	Analog	Comparator 2 Input A.
C3INA				I	Analog	Comparator 3 Input A.
RP5				I/O	ST/DIG	Remappable Peripheral Pin 5 input/output.
RA5				I/O	ST/DIG	General purpose I/O pin.

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I = Input
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I^2C = I^2C/SMBus
CMOS = CMOS compatible input or output
Analog = Analog input
O = Output
OD = Open-Drain (no P diode to VDD)

TABLE 1-4: PIC18FXXJ94 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number			Pin Type	Buffer Type	Description
	100	80	64			
VLCAP1/RP8/CTED13/INT0/RB0	73	58	48			
VLCAP1				I	Analog	LCD Drive Charge Pump Capacitor Input 1.
RP8				I/O	ST/DIG	Remappable Peripheral Pin 8 input/output.
CTED13				I	ST	CTMU Edge 13 input.
INT0				I	ST	External Interrupt 0.
RB0				I/O	ST/DIG	General purpose I/O pin.
VLCAP2/RP9/RB1	72	57	47			
VLCAP2				I	Analog	LCD Drive Charge Pump Capacitor Input 2.
RP9				I/O	ST/DIG	Remappable Peripheral Pin 9 input/output.
RB1				I/O	ST/DIG	General purpose I/O pin.
SEG9/RP14/CTED1/RB2	70	56	46			
SEG9				O	Analog	SEG9 output for LCD.
RP14				I/O	ST/DIG	Remappable Peripheral Pin 14 input/output.
CTED1				I	ST	CTMU Edge 1 input.
RB2				I/O	ST/DIG	General purpose I/O pin.
SEG10/RP7/CTED2/RB3	69	55	45			
SEG10				O	Analog	SEG10 output for LCD.
RP7				I/O	ST/DIG	Remappable Peripheral Pin 7 input/output.
CTED2				I	ST	CTMU Edge 2 input.
RB3				I/O	ST/DIG	General purpose I/O pin.
SEG11/RP12/CTED3/RB4	68	54	44			
SEG11				O	Analog	SEG11 output for LCD.
RP12				I/O	ST/DIG	Remappable Peripheral Pin 12 input/output.
CTED3				I	ST	CTMU Edge 3 input.
RB4				I/O	ST/DIG	General purpose I/O pin.
SEG8/RP13/CTED4/RB5	67	53	43			
SEG8				O	Analog	SEG8 output for LCD.
RP13				I/O	ST/DIG	Remappable Peripheral Pin 13 input/output.
CTED4				I	ST	CTMU Edge 4 input.
RB5				I/O	ST/DIG	General purpose I/O pin.
PGC/CTED5/RB6	65	52	42			
PGC				I/O	ST/DIG	In-Circuit Debugger and ICSP™ programming clock pin.
CTED5				I	ST	CTMU Edge Input.
RB6				I/O	ST/DIG	General purpose I/O pin.
PGD/CTED6/RB7	58	47	37			
PGD				I/O	ST/DIG	In-Circuit Debugger and ICSP™ programming data pin.
CTED6				I	ST	CTMU Edge 6 input.
RB7				I/O	ST/DIG	General purpose I/O pin.

Legend: TTL = TTL compatible input
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I^2C = I^2C/SMBus
CMOS = CMOS compatible input or output
Analog = Analog input
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