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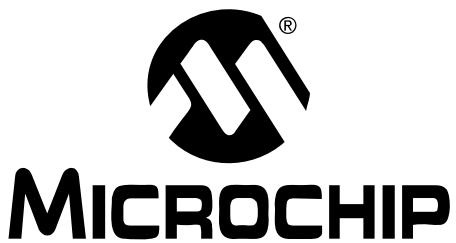


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dsPIC33F Family Data Sheet

High-Performance, 16-Bit
Digital Signal Controllers

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**MICROCHIP****dsPIC33F**

High-Performance, 16-bit Digital Signal Controllers

Operating Range:

- DC – 40 MIPS (40 MIPS @ 3.0-3.6V, -40°C to +85°C)
- Industrial temperature range (-40°C to +85°C)

High-Performance DSC CPU:

- Modified Harvard architecture
- C compiler optimized instruction set
- 16-bit wide data path
- 24-bit wide instructions
- Linear program memory addressing up to 4M instruction words
- Linear data memory addressing up to 64 Kbytes
- 83 base instructions: mostly 1 word/1 cycle
- Sixteen 16-bit General Purpose Registers
- Two 40-bit accumulators:
 - With rounding and saturation options
- Flexible and powerful addressing modes:
 - Indirect, Modulo and Bit-Reversed
- Software stack
- 16 x 16 fractional/integer multiply operations
- 32/16 and 16/16 divide operations
- Single-cycle multiply and accumulate:
 - Accumulator write back for DSP operations
 - Dual data fetch
- Up to \pm 16-bit shifts for up to 40-bit data

Direct Memory Access (DMA):

- 8-channel hardware DMA:
- 2 Kbytes dual ported DMA buffer area (DMA RAM) to store data transferred via DMA:
 - Allows data transfer between RAM and a peripheral while CPU is executing code (no cycle stealing)
- Most peripherals support DMA

Interrupt Controller:

- 5-cycle latency
- 118 interrupt vectors
- Up to 67 available interrupt sources
- Up to 5 external interrupts
- 7 programmable priority levels
- 5 processor exceptions

Digital I/O:

- Up to 85 programmable digital I/O pins
- Wake-up/Interrupt-on-Change on up to 24 pins
- Output pins can drive from 3.0V to 3.6V
- All digital input pins are 5V tolerant
- 4 mA sink on all I/O pins

On-Chip Flash and SRAM:

- Flash program memory, up to 256 Kbytes
- Data SRAM, up to 30 Kbytes (includes 2 Kbytes of DMA RAM):

System Management:

- Flexible clock options:
 - External, crystal, resonator, internal RC
 - Fully integrated PLL
 - Extremely low jitter PLL
- Power-up Timer
- Oscillator Start-up Timer/Stabilizer
- Watchdog Timer with its own RC oscillator
- Fail-Safe Clock Monitor
- Reset by multiple sources

Power Management:

- On-chip 2.5V voltage regulator
- Switch between clock sources in real time
- Idle, Sleep and Doze modes with fast wake-up

Timers/Capture/Compare/PWM:

- Timer/Counters, up to nine 16-bit timers:
 - Can pair up to make four 32-bit timers
 - 1 timer runs as Real-Time Clock with external 32.768 kHz oscillator
 - Programmable prescaler
- Input Capture (up to 8 channels):
 - Capture on up, down or both edges
 - 16-bit capture input functions
 - 4-deep FIFO on each capture
- Output Compare (up to 8 channels):
 - Single or Dual 16-Bit Compare mode
 - 16-bit Glitchless PWM mode

Communication Modules:

- 3-wire SPI (up to 2 modules):
 - Framing supports I/O interface to simple codecs
 - Supports 8-bit and 16-bit data
 - Supports all serial clock formats and sampling modes
- I²C™ (up to 2 modules):
 - Full Multi-Master Slave mode support
 - 7-bit and 10-bit addressing
 - Bus collision detection and arbitration
 - Integrated signal conditioning
 - Slave address masking
- UART (up to 2 modules):
 - Interrupt on address bit detect
 - Interrupt on UART error
 - Wake-up on Start bit from Sleep mode
 - 4-character TX and RX FIFO buffers
 - LIN bus support
 - IrDA® encoding and decoding in hardware
 - High-Speed Baud mode
 - Hardware Flow Control with CTS and RTS
- Data Converter Interface (DCI) module:
 - Codec interface
 - Supports I²S and AC'97 protocols
 - Up to 16-bit data words, up to 16 words per frame
 - 4-word deep TX and RX buffers
- Enhanced CAN (ECAN™ module) 2.0B active (up to 2 modules):
 - Up to 8 transmit and up to 32 receive buffers
 - 16 receive filters and 3 masks
 - Loopback, Listen Only and Listen All Messages modes for diagnostics and bus monitoring
 - Wake-up on CAN message
 - Automatic processing of Remote Transmission Requests
 - FIFO mode using DMA
 - DeviceNet™ addressing support

Motor Control Peripherals:

- Motor Control PWM (up to 8 channels):
 - 4 duty cycle generators
 - Independent or Complementary mode
 - Programmable dead time and output polarity
 - Edge or center-aligned
 - Manual output override control
 - Up to 2 Fault inputs
 - Trigger for ADC conversions
 - PWM frequency for 16-bit resolution (@ 40 MIPS) = 1220 Hz for Edge-Aligned mode, 610 Hz for Center-Aligned mode
 - PWM frequency for 11-bit resolution (@ 40 MIPS) = 39.1 kHz for Edge-Aligned mode, 19.55 kHz for Center-Aligned mode
- Quadrature Encoder Interface module:
 - Phase A, Phase B and index pulse input
 - 16-bit up/down position counter
 - Count direction status
 - Position Measurement (x2 and x4) mode
 - Programmable digital noise filters on inputs
 - Alternate 16-bit Timer/Counter mode
 - Interrupt on position counter rollover/underflow

Analog-to-Digital Converters (ADCs):

- Up to two ADC modules in a device
- 10-bit, 1.1 Msps or 12-bit, 500 Ksps conversion:
 - 2, 4 or 8 simultaneous samples
 - Up to 32 input channels with auto-scanning
 - Conversion start can be manual or synchronized with 1 of 4 trigger sources
 - Conversion possible in Sleep mode
 - ±2 Lsb max integral nonlinearity
 - ±1 Lsb max differential nonlinearity

CMOS Flash Technology:

- Low-power, high-speed Flash technology
- Fully static design
- 3.3V (±10%) operating voltage
- Industrial temperature
- Low-power consumption

Packaging:

- 100-pin TQFP (14x14x1 mm and 12x12x1 mm)
- 80-pin TQFP (12x12x1 mm)
- 64-pin TQFP (10x10x1 mm)

Note:	See the device variant tables for exact peripheral features per device.
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dsPIC33F PRODUCT FAMILIES

There are two device subfamilies within the dsPIC33F family of devices. They are the General Purpose Family and the Motor Control Family.

The General Purpose Family is ideal for a wide variety of 16-bit MCU embedded applications. The variants with codec interfaces are well-suited for speech and audio processing applications.

The Motor Control Family supports a variety of motor control applications, such as brushless DC motors, single and 3-phase induction motors and switched reluctance motors. These products are also well-suited

for Uninterrupted Power Supply (UPS), inverters, Switched mode power supplies, power factor correction and also for controlling the power management module in servers, telecommunication equipment and other industrial equipment.

The device names, pin counts, memory sizes and peripheral availability of each family are listed below, followed by their pinout diagrams.

dsPIC33F General Purpose Family Variants

Device	Pins	Program Flash Memory (Kbyte)	RAM (Kbyte) ⁽¹⁾	16-bit Timer	Input Capture	Output Compare Std. PWM	Codec Interface	ADC	UART	SPI	I ² C™	Enhanced CAN	I/O Pins (Max) ⁽²⁾	Packages
dsPIC33FJ64GP206	64	64	8	9	8	8	1	1 ADC, 18 ch	2	2	1	0	53	PT
dsPIC33FJ64GP306	64	64	16	9	8	8	1	1 ADC, 18 ch	2	2	2	0	53	PT
dsPIC33FJ64GP310	100	64	16	9	8	8	1	1 ADC, 32 ch	2	2	2	0	85	PF, PT
dsPIC33FJ64GP706	64	64	16	9	8	8	1	2 ADC, 18 ch	2	2	2	2	53	PT
dsPIC33FJ64GP708	80	64	16	9	8	8	1	2 ADC, 24 ch	2	2	2	2	69	PT
dsPIC33FJ64GP710	100	64	16	9	8	8	1	2 ADC, 32 ch	2	2	2	2	85	PF, PT
dsPIC33FJ128GP206	64	128	8	9	8	8	1	1 ADC, 18 ch	2	2	1	0	53	PT
dsPIC33FJ128GP306	64	128	16	9	8	8	1	1 ADC, 18 ch	2	2	2	0	53	PT
dsPIC33FJ128GP310	100	128	16	9	8	8	1	1 ADC, 32 ch	2	2	2	0	85	PF, PT
dsPIC33FJ128GP706	64	128	16	9	8	8	1	2 ADC, 18 ch	2	2	2	2	53	PT
dsPIC33FJ128GP708	80	128	16	9	8	8	1	2 ADC, 24 ch	2	2	2	2	69	PT
dsPIC33FJ128GP710	100	128	16	9	8	8	1	2 ADC, 32 ch	2	2	2	2	85	PF, PT
dsPIC33FJ256GP506	64	256	16	9	8	8	1	1 ADC, 18 ch	2	2	2	1	53	PT
dsPIC33FJ256GP510	100	256	16	9	8	8	1	1 ADC, 32 ch	2	2	2	1	85	PF, PT
dsPIC33FJ256GP710	100	256	30	9	8	8	1	2 ADC, 32 ch	2	2	2	2	85	PF, PT

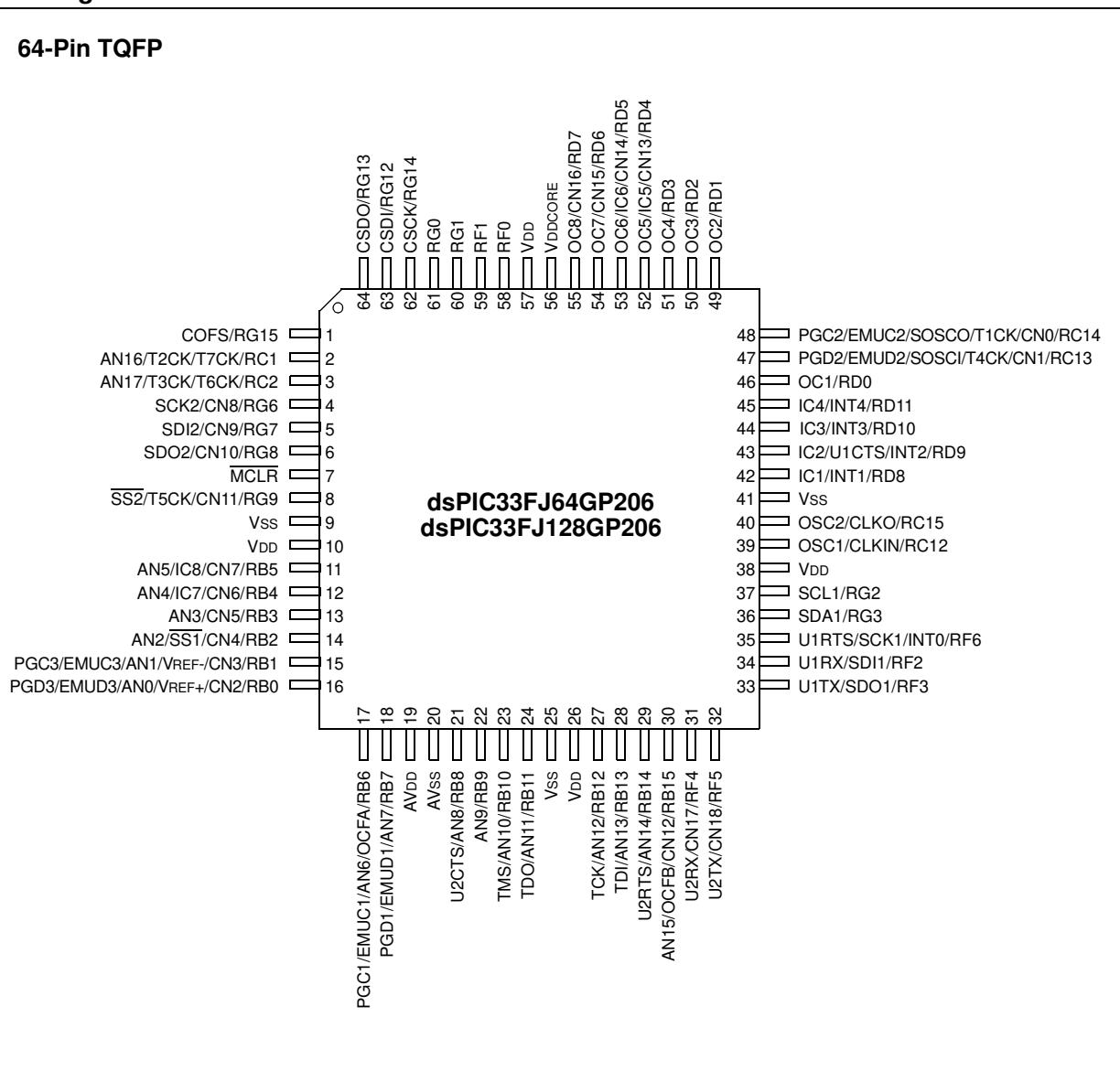
Note 1: RAM size is inclusive of 2 Kbytes DMA RAM.

2: Maximum I/O pin count includes pins shared by the peripheral functions.

dsPIC33F

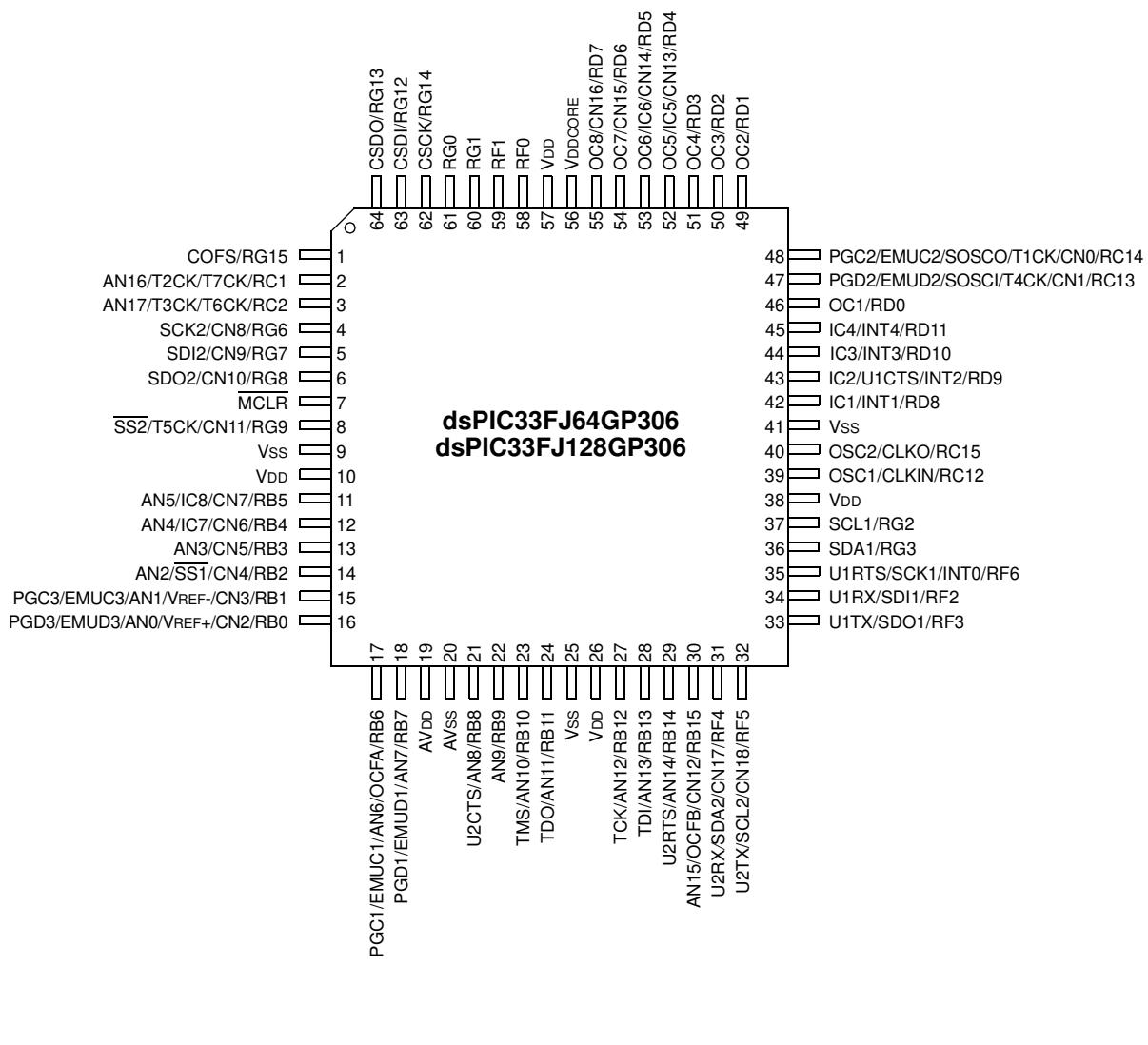
Pin Diagrams

64-Pin TQFP



Pin Diagrams (Continued)

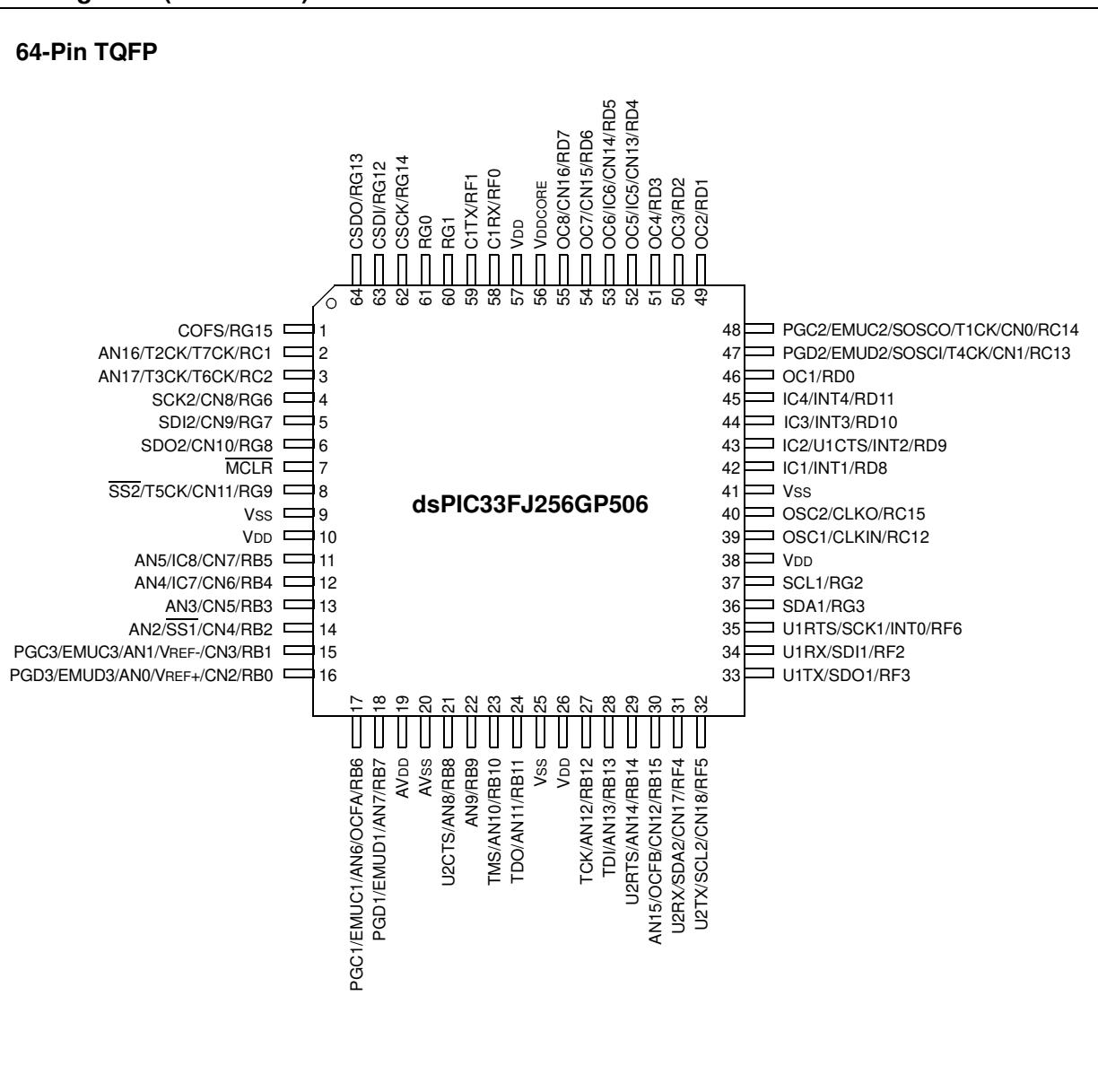
64-Pin TQFP



dsPIC33F

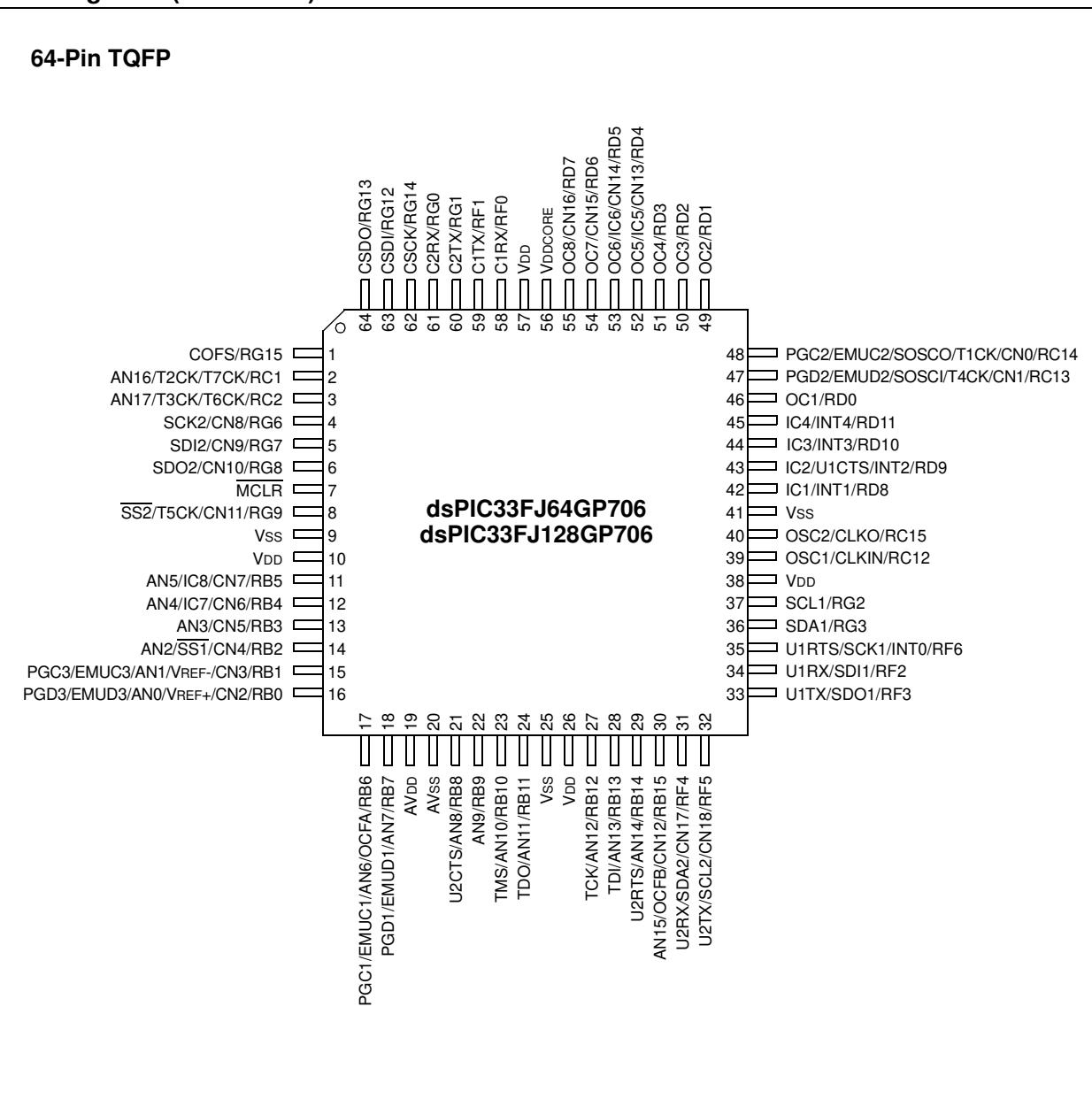
Pin Diagrams (Continued)

64-Pin TQFP



Pin Diagrams (Continued)

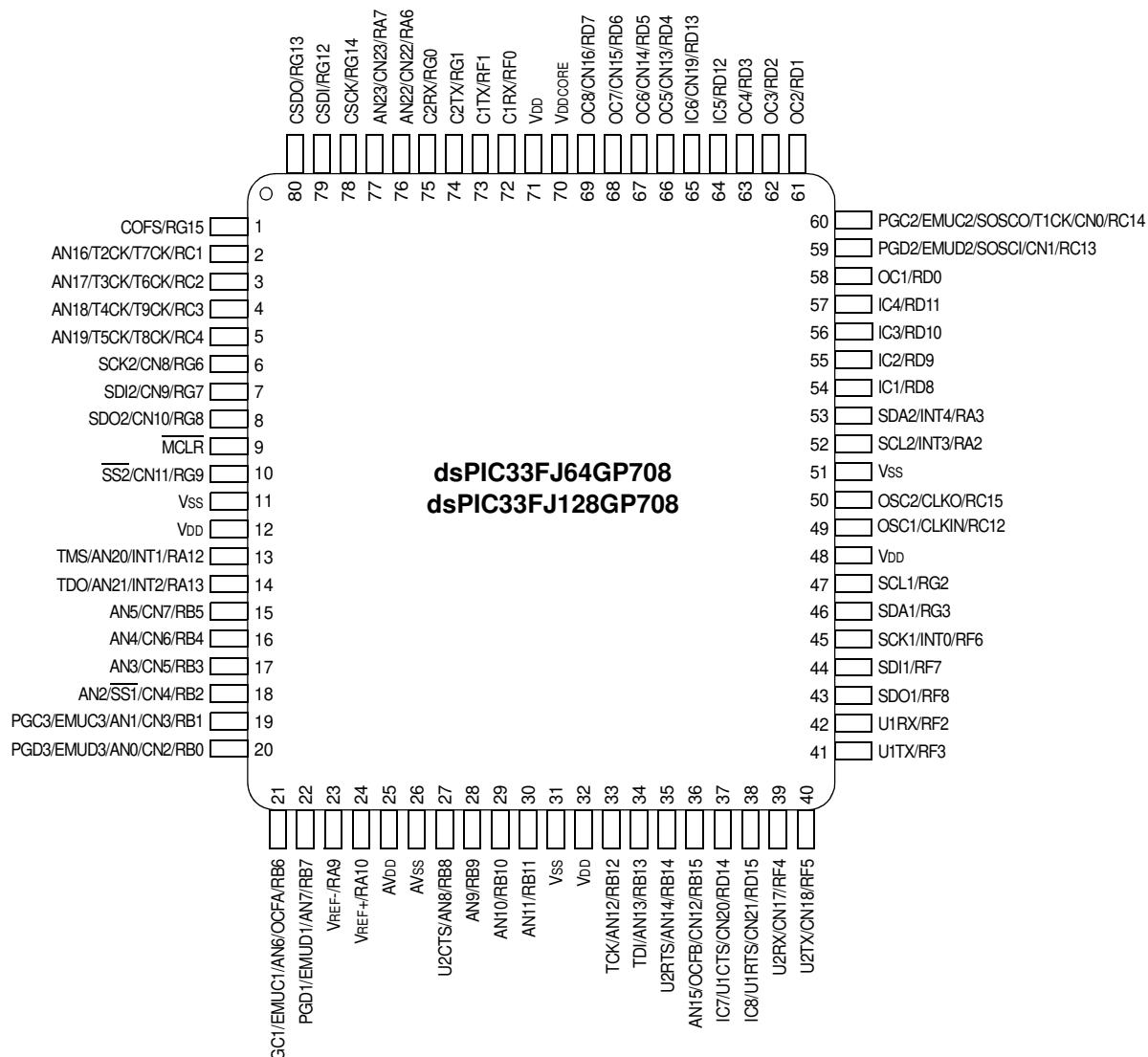
64-Pin TQFP



dsPIC33F

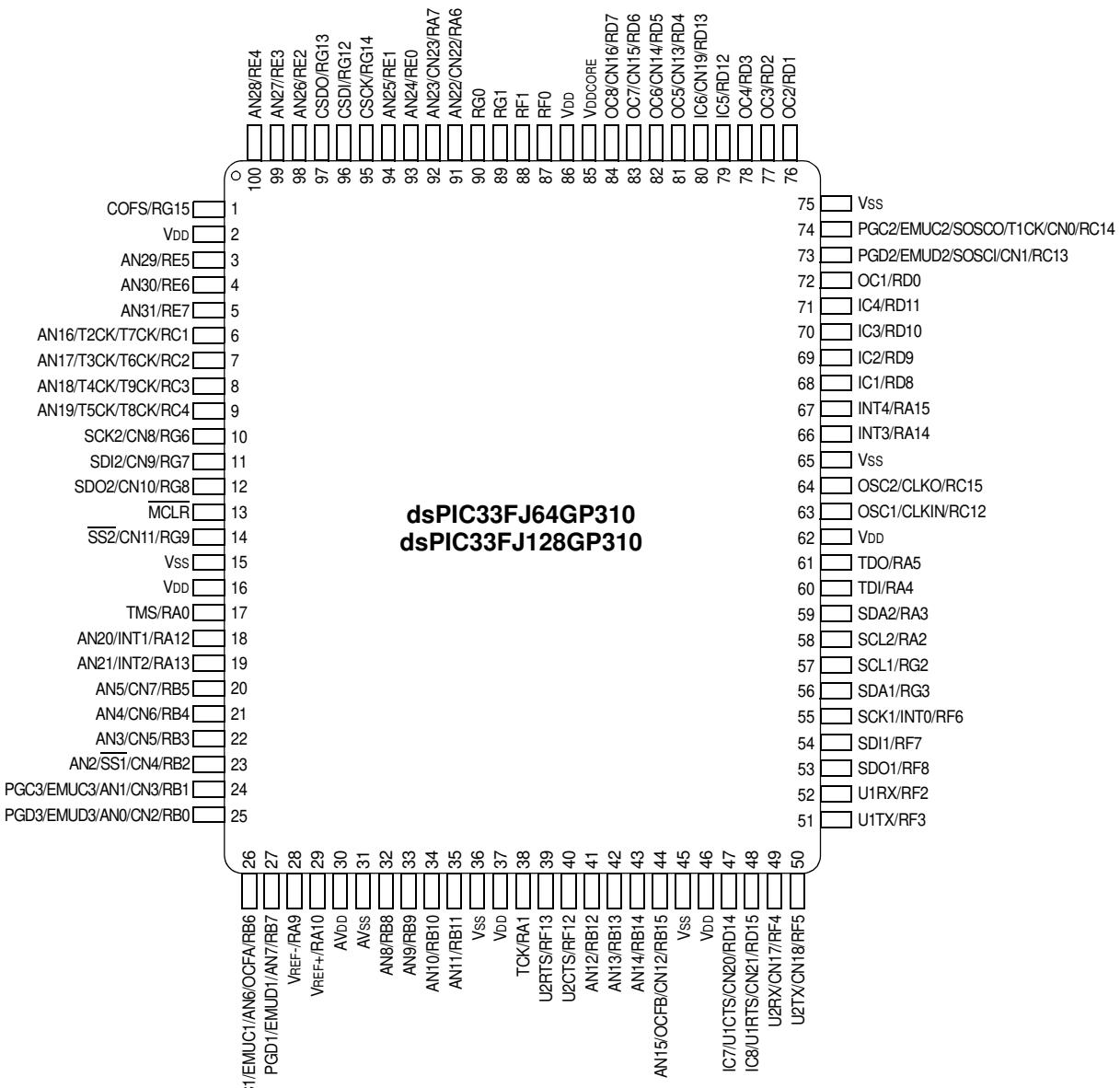
Pin Diagrams (Continued)

80-Pin TQFP



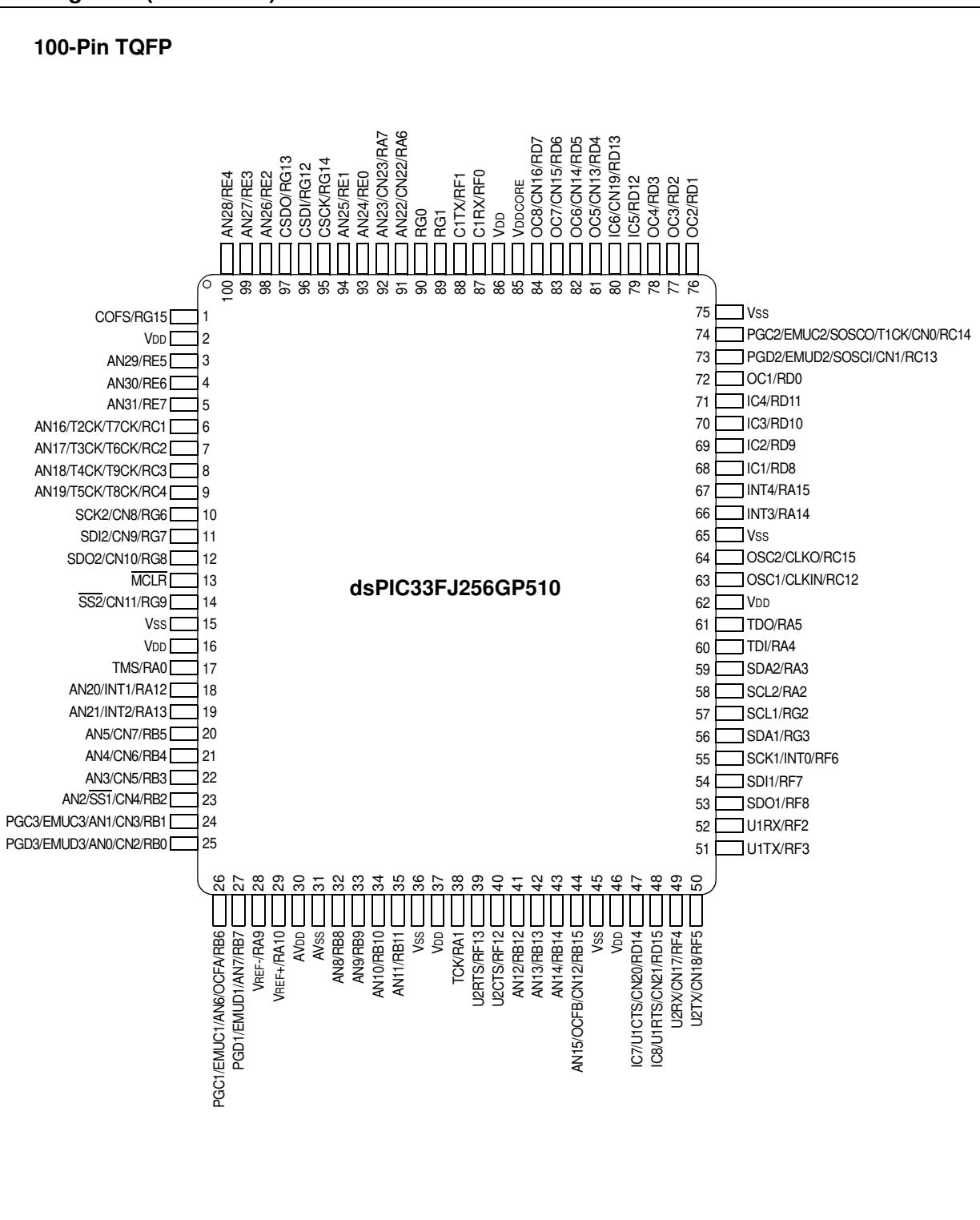
Pin Diagrams (Continued)

100-Pin TQFP



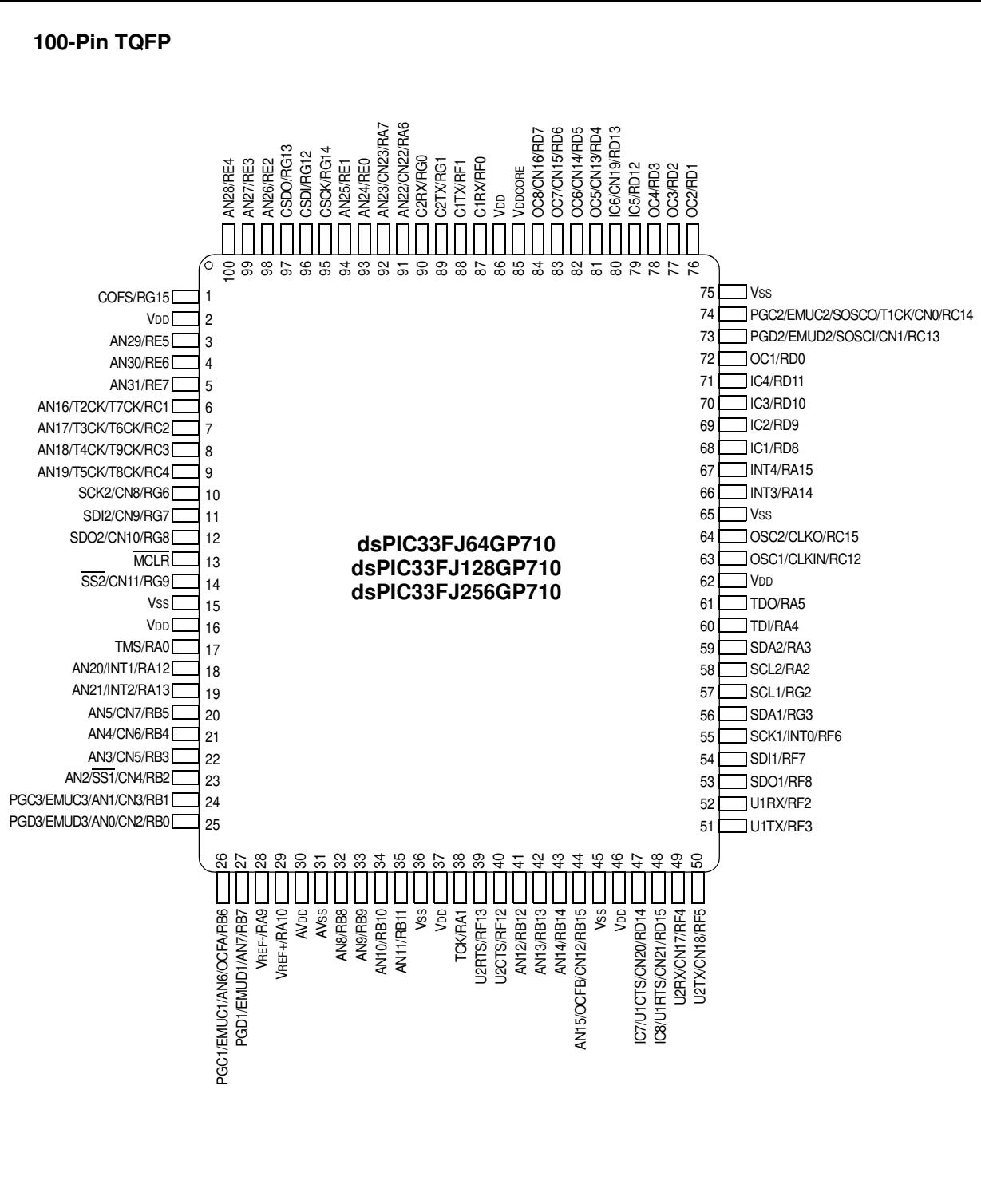
Pin Diagrams (Continued)

100-Pin TQFP



Pin Diagrams (Continued)

100-Pin TQFP



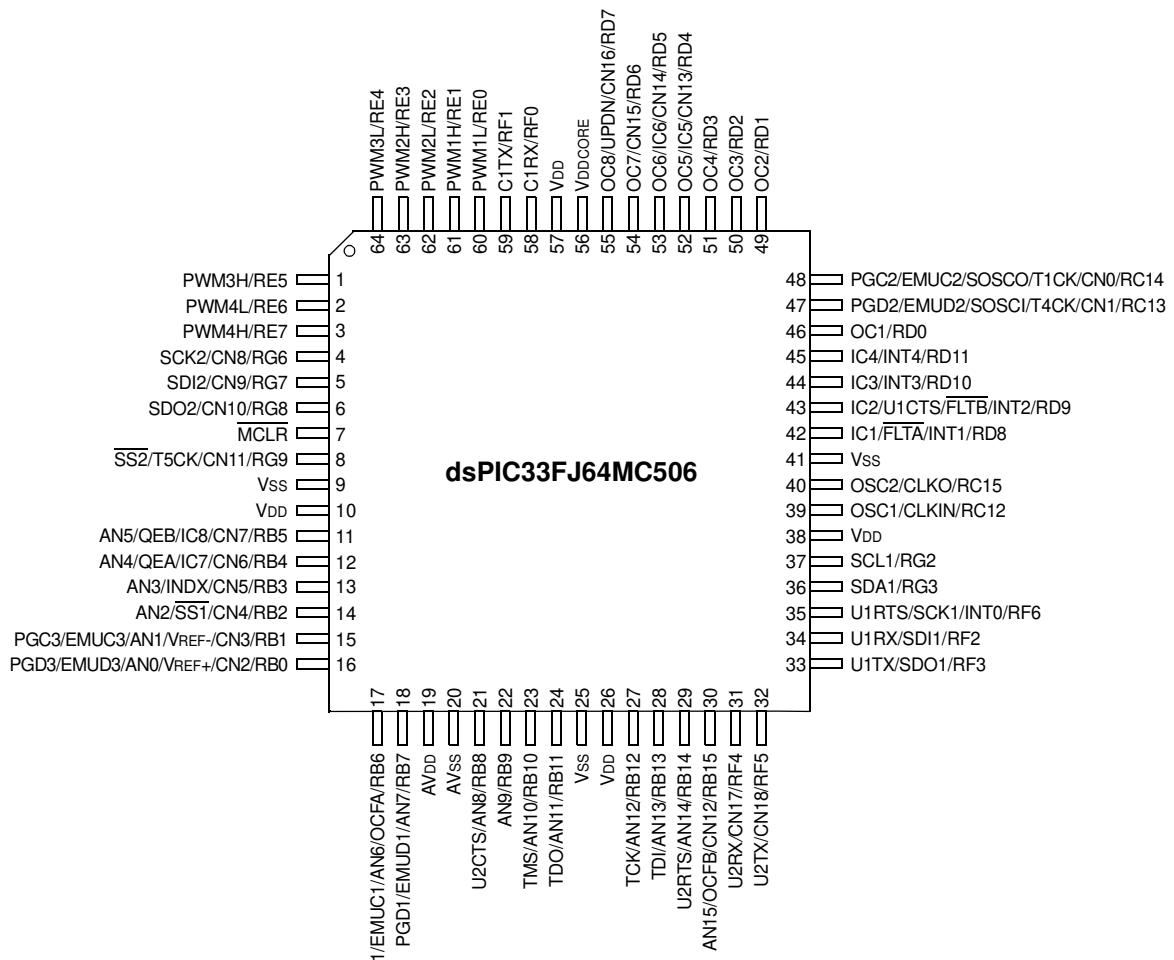
dsPIC33F

dsPIC33F Motor Control Family Variants

Device	Pins	Programmable Flash Memory (Kbyte)	RAM (Kbyte) ⁽¹⁾	Timer 16-bit	Input Capture	Output Compare Std. PWM	Motor Control PWM	Quadrature Encoder Interface	Codec Interface	ADC	UART	SPI	I ² C TM	Enhanced CAN	I/O Pins (Max) ⁽²⁾	Packages
dsPIC33FJ64MC506	64	64	8	9	8	8	8 ch	1	0	1 ADC, 16 ch	2	2	2	1	53	PT
dsPIC33FJ64MC508	80	64	8	9	8	8	8 ch	1	0	1 ADC, 18 ch	2	2	2	1	69	PT
dsPIC33FJ64MC510	100	64	8	9	8	8	8 ch	1	0	1 ADC, 24 ch	2	2	2	1	85	PF, PT
dsPIC33FJ64MC706	64	64	16	9	8	8	8 ch	1	0	2 ADC, 16 ch	2	2	2	1	53	PT
dsPIC33FJ64MC710	100	64	16	9	8	8	8 ch	1	0	2 ADC, 24 ch	2	2	2	2	85	PF, PT
dsPIC33FJ128MC506	64	128	8	9	8	8	8 ch	1	0	1 ADC, 16 ch	2	2	2	1	53	PT
dsPIC33FJ128MC510	100	128	8	9	8	8	8 ch	1	0	1 ADC, 24 ch	2	2	2	1	85	PF, PT
dsPIC33FJ128MC706	64	128	16	9	8	8	8 ch	1	0	2 ADC, 16 ch	2	2	2	1	53	PT
dsPIC33FJ128MC708	80	128	16	9	8	8	8 ch	1	0	2 ADC, 18 ch	2	2	2	2	69	PT
dsPIC33FJ128MC710	100	128	16	9	8	8	8 ch	1	0	2 ADC, 24 ch	2	2	2	2	85	PF, PT
dsPIC33FJ256MC510	100	256	16	9	8	8	8 ch	1	0	1 ADC, 24 ch	2	2	2	1	85	PF, PT
dsPIC33FJ256MC710	100	256	30	9	8	8	8 ch	1	0	2 ADC, 24 ch	2	2	2	2	85	PF, PT

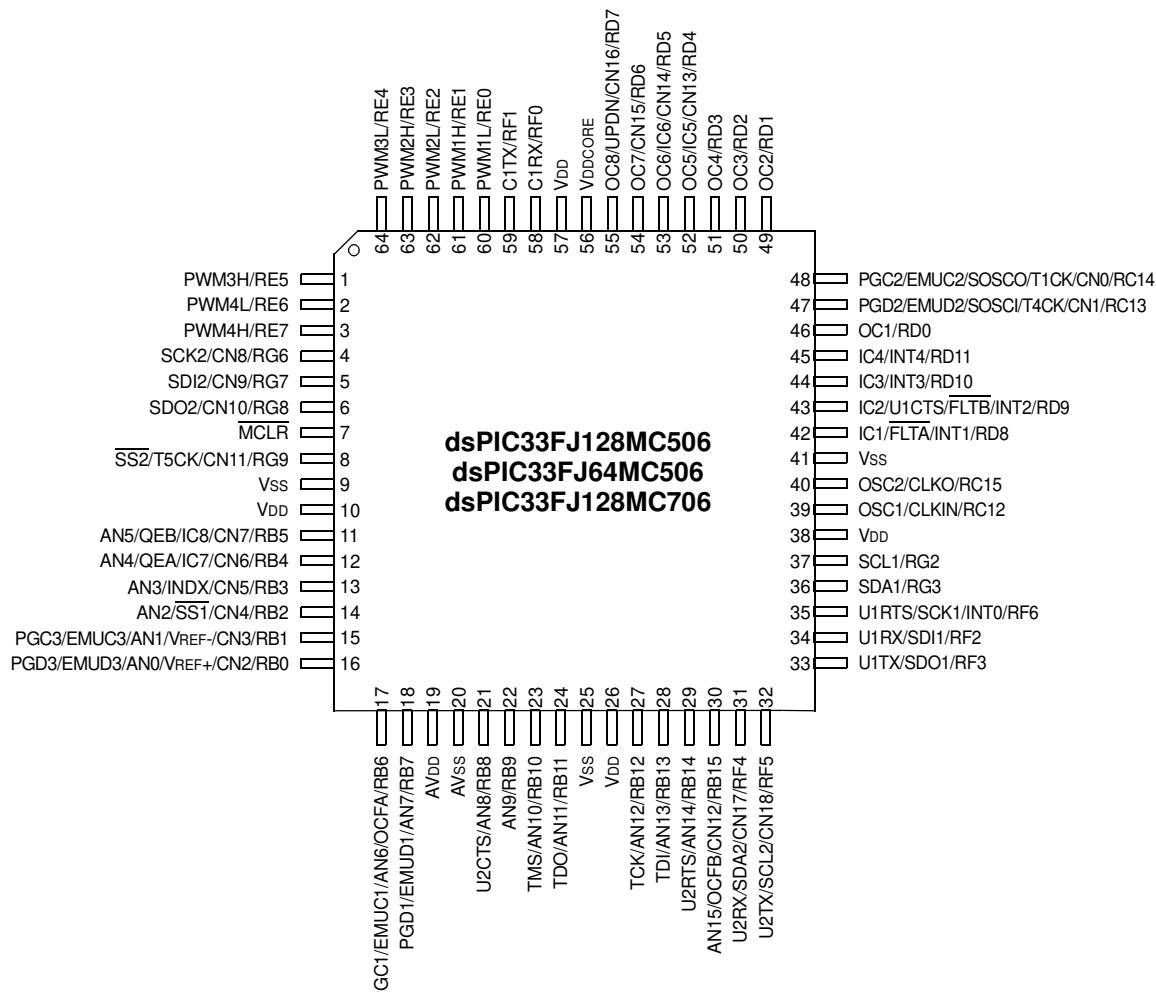
Note 1: RAM size is inclusive of 2 Kbytes DMA RAM.

2: Maximum I/O pin count includes pins shared by the peripheral functions.

Pin Diagrams**64-Pin TQFP**

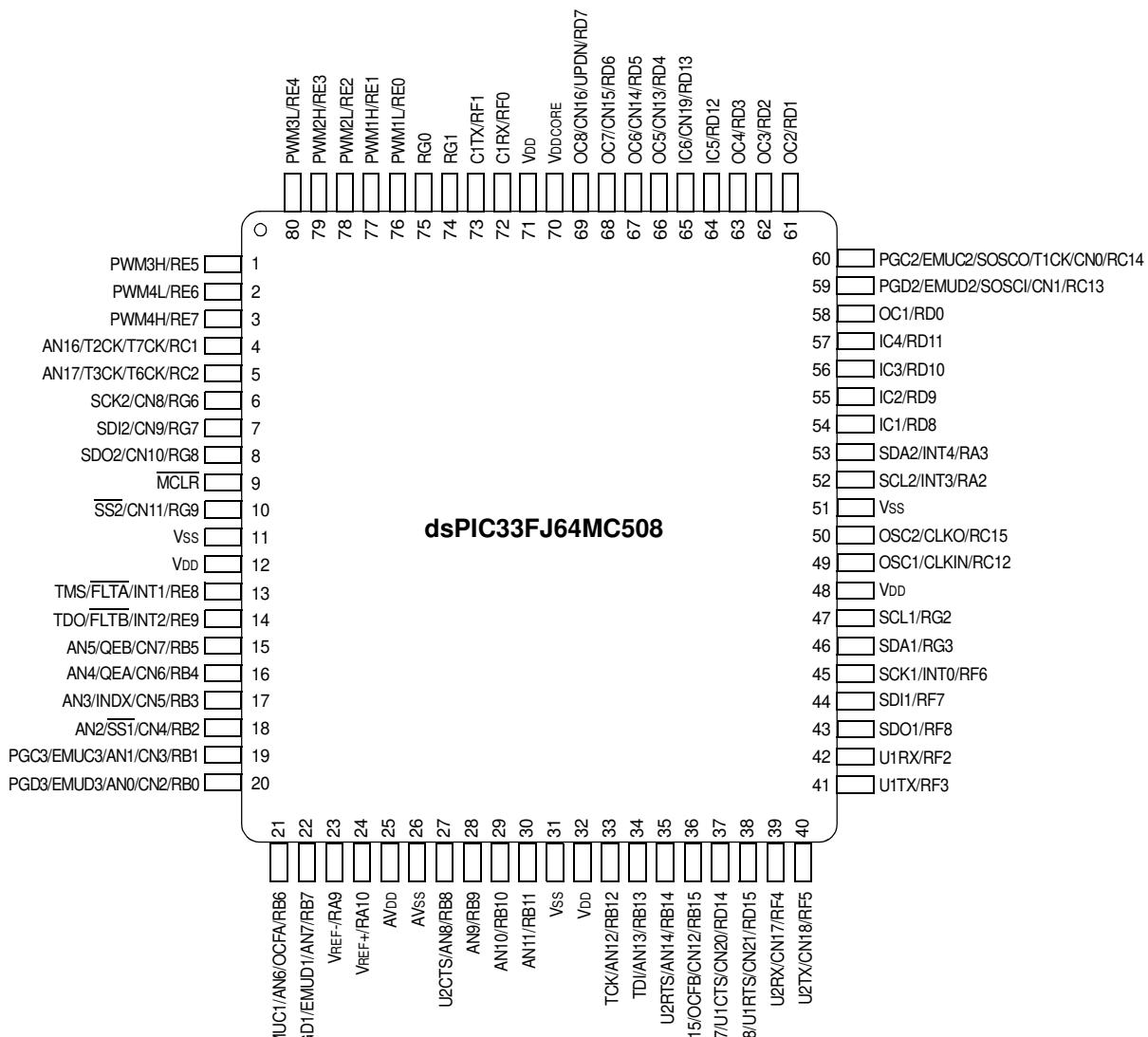
Pin Diagrams (Continued)

64-Pin TQFP



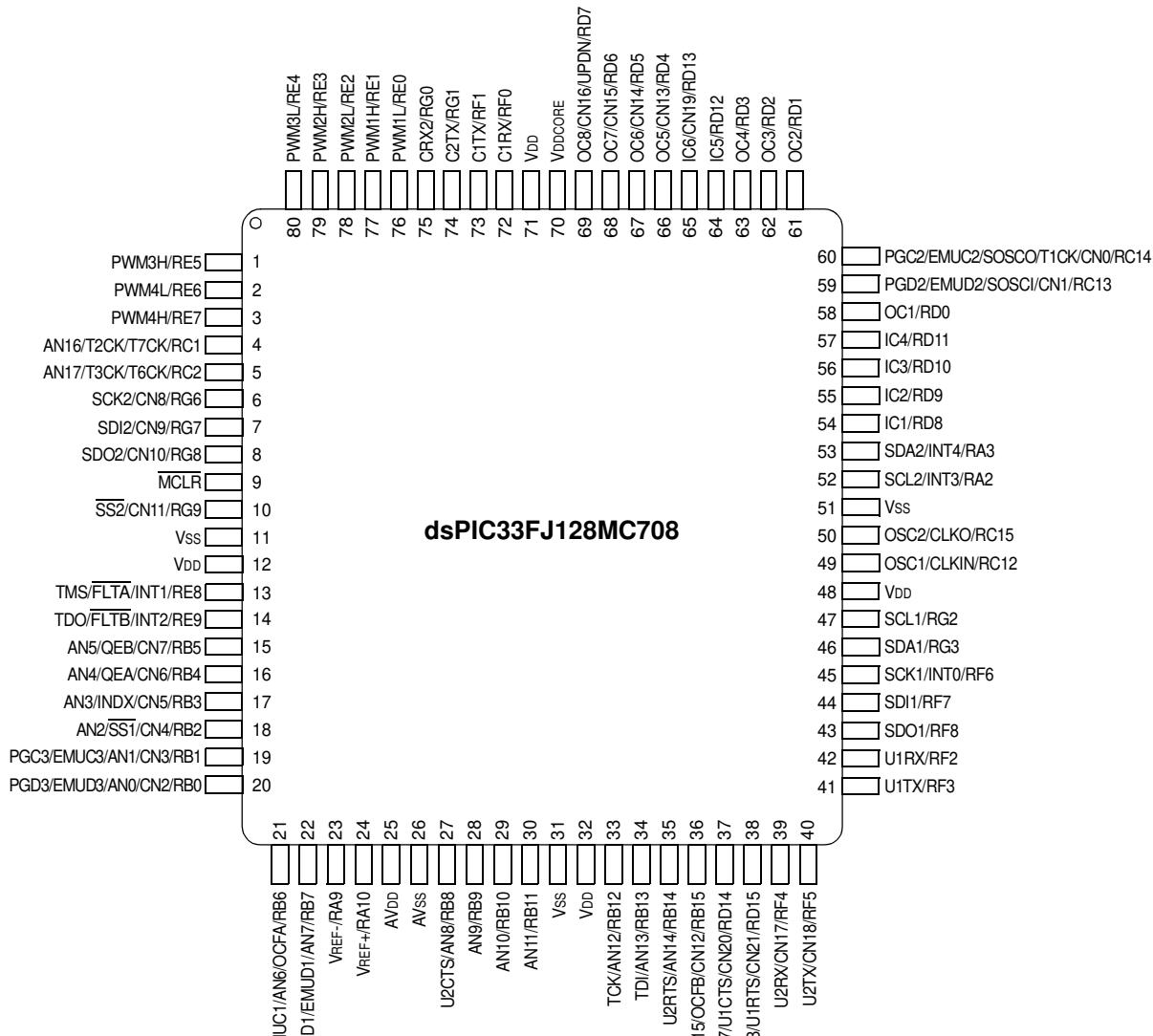
Pin Diagrams (Continued)

80-Pin TQFP



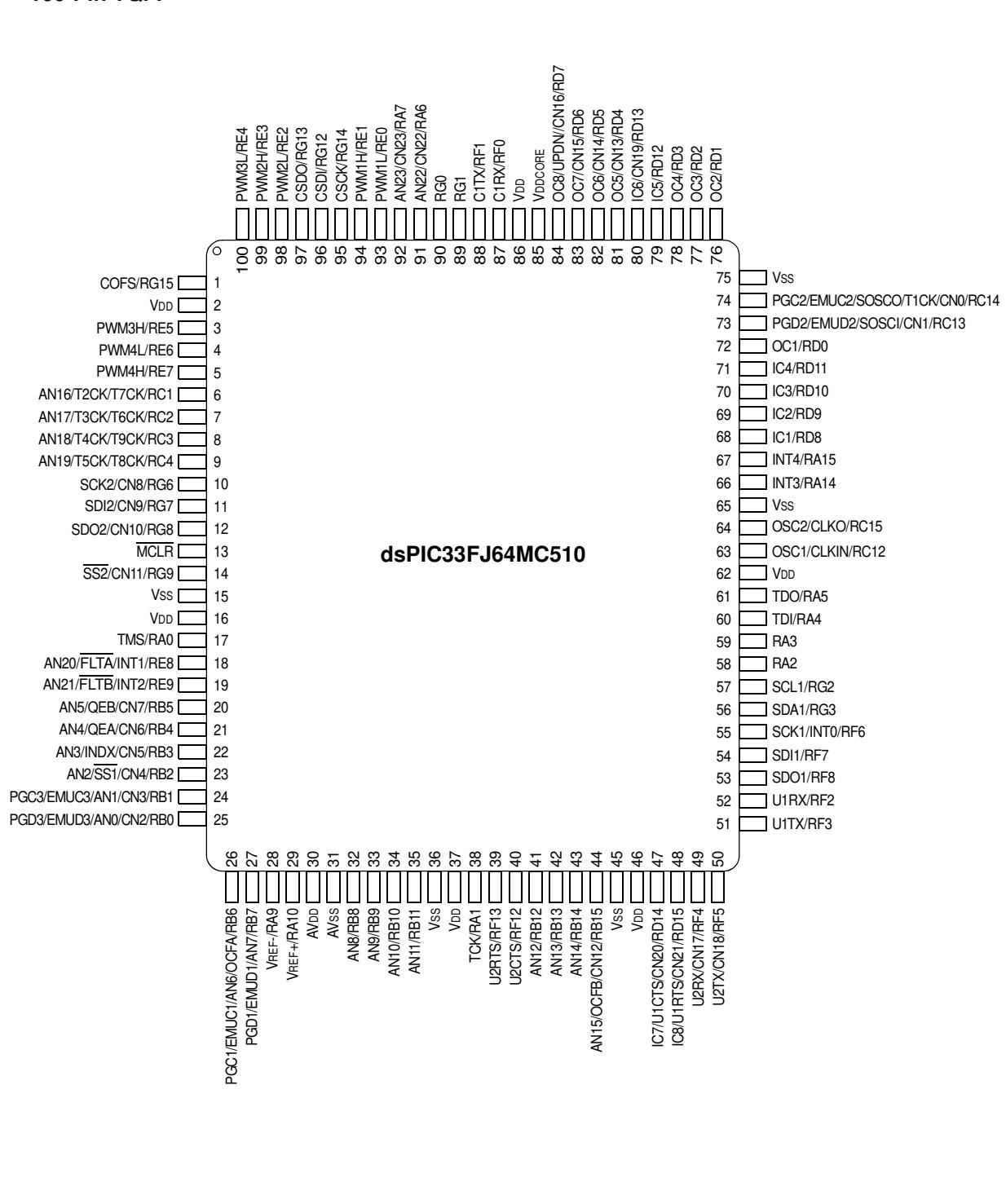
Pin Diagrams (Continued)

80-Pin TQFP



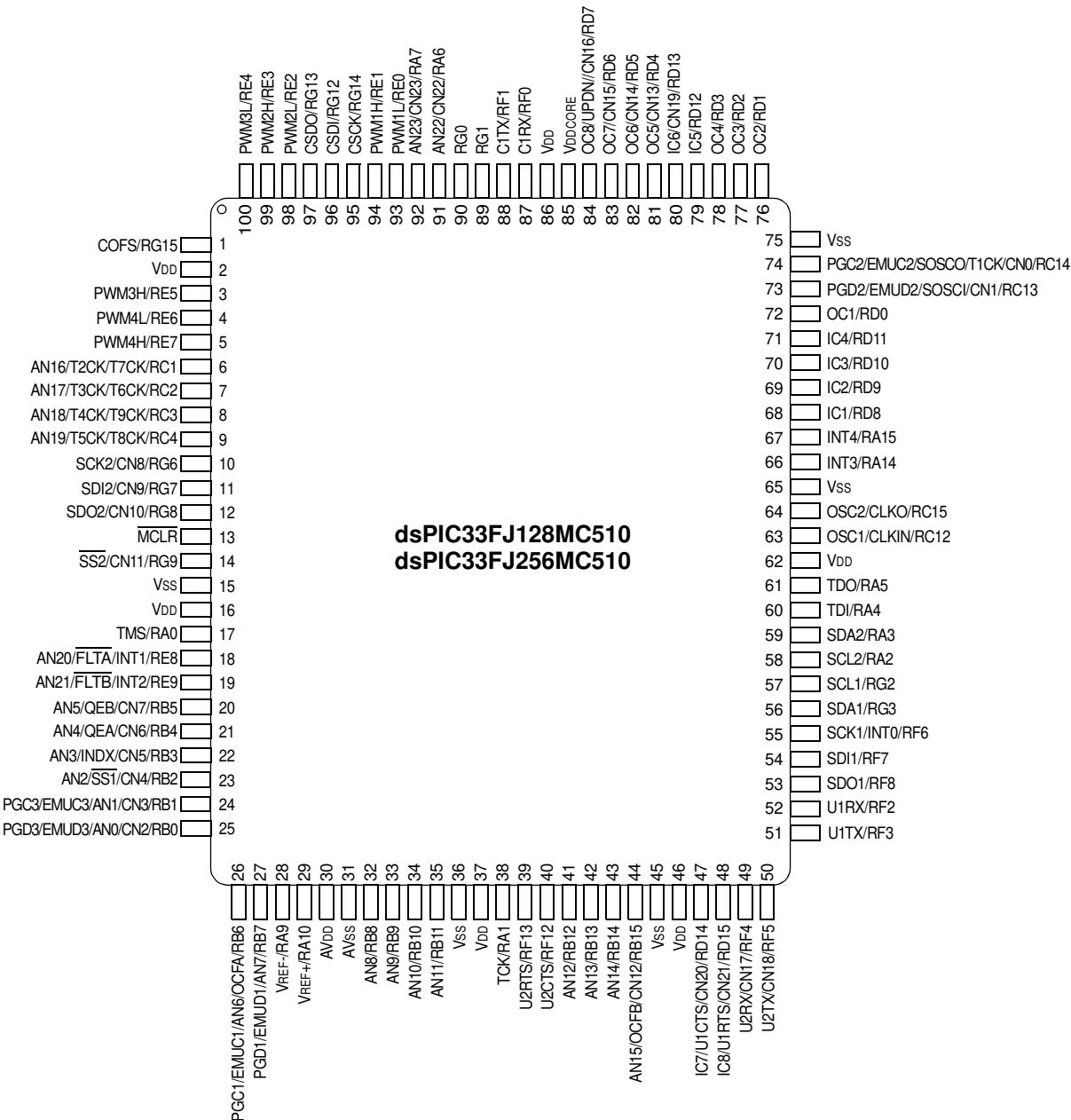
Pin Diagrams (Continued)

100-Pin TQFP



Pin Diagrams (Continued)

100-Pin TQFP



Pin Diagrams (Continued)

100-Pin TQFP

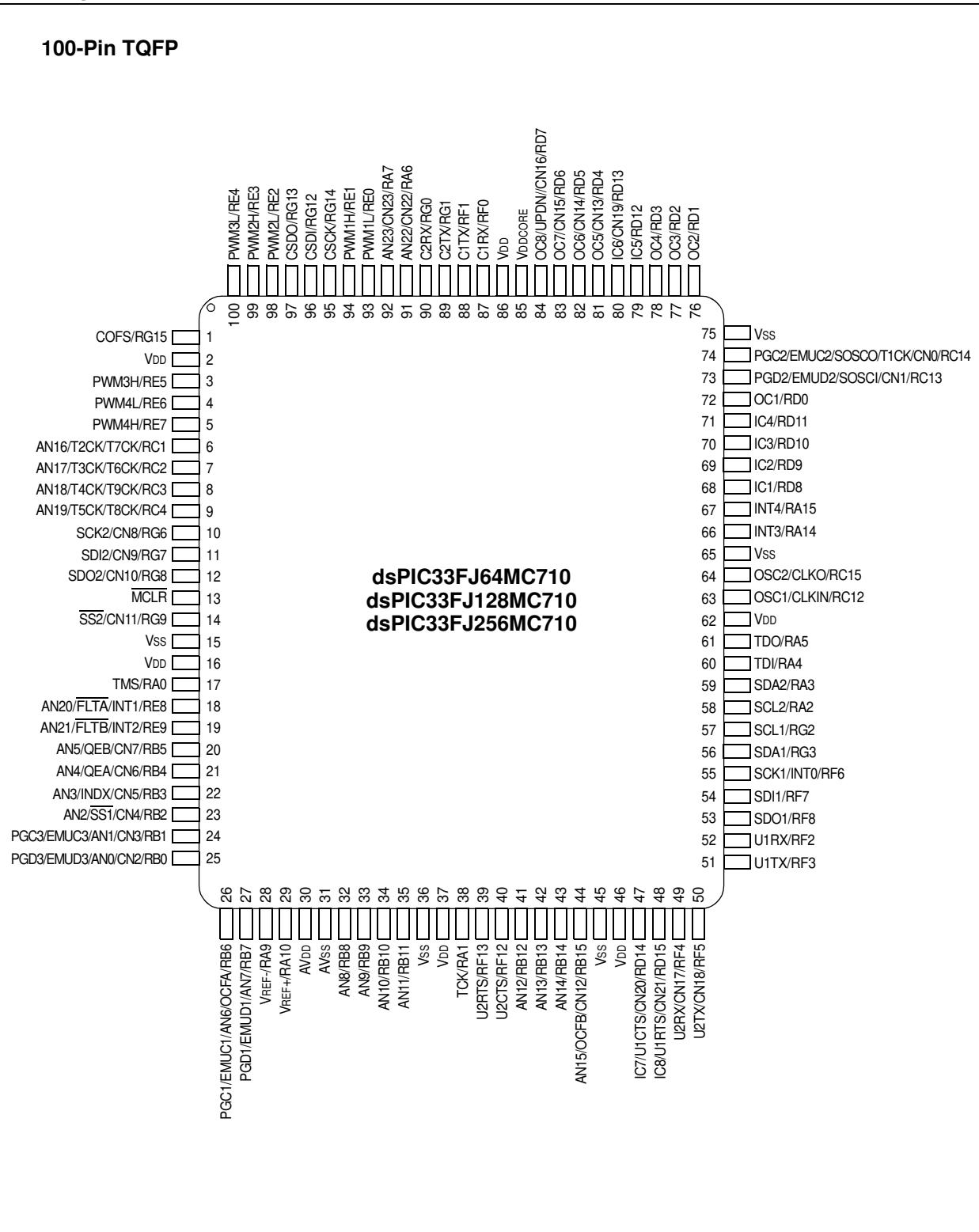


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dsPIC33F

NOTES:

1.0 DEVICE OVERVIEW

Note: This data sheet summarizes the features of this group of dsPIC33F devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the "dsPIC30F Family Reference Manual" (DS70046).

This document contains device specific information for the following devices:

- dsPIC33FJ64GP206
- dsPIC33FJ64GP306
- dsPIC33FJ64GP310
- dsPIC33FJ64GP706
- dsPIC33FJ64GP708
- dsPIC33FJ64GP710
- dsPIC33FJ128GP206
- dsPIC33FJ128GP306
- dsPIC33FJ128GP310
- dsPIC33FJ128GP706
- dsPIC33FJ128GP708
- dsPIC33FJ128GP710
- dsPIC33FJ256GP506
- dsPIC33FJ256GP510
- dsPIC33FJ256GP710
- dsPIC33FJ64MC506
- dsPIC33FJ64MC508
- dsPIC33FJ64MC510
- dsPIC33FJ64MC706
- dsPIC33FJ64MC710
- dsPIC33FJ128MC506
- dsPIC33FJ128MC510
- dsPIC33FJ128MC706
- dsPIC33FJ128MC708
- dsPIC33FJ128MC710
- dsPIC33FJ256MC510
- dsPIC33FJ256MC710

The dsPIC33F General Purpose and Motor Control Families of devices include devices with a wide range of pin counts (64, 80 and 100), different program memory sizes (64 Kbytes, 128 Kbytes and 256 Kbytes) and different RAM sizes (8 Kbytes, 16 Kbytes and 30 Kbytes)

This makes these families suitable for a wide variety of high-performance digital signal control application. The devices are pin compatible with the PIC24H family of devices, and also share a very high degree of compatibility with the dsPIC30F family devices. This allows easy migration between device families as may be necessitated by the specific functionality, computational resource and system cost requirements of the application.

The dsPIC33F device family employs a powerful 16-bit architecture that seamlessly integrates the control features of a Microcontroller (MCU) with the computational capabilities of a Digital Signal Processor (DSP). The resulting functionality is ideal for applications that rely on high-speed, repetitive computations, as well as control.

The DSP engine, dual 40-bit accumulators, hardware support for division operations, barrel shifter, 17 x 17 multiplier, a large array of 16-bit working registers and a wide variety of data addressing modes, together provide the dsPIC33F Central Processing Unit (CPU) with extensive mathematical processing capability. Flexible and deterministic interrupt handling, coupled with a powerful array of peripherals, renders the dsPIC33F devices suitable for control applications. Further, Direct Memory Access (DMA) enables overhead-free transfer of data between several peripherals and a dedicated DMA RAM. Reliable, field programmable Flash program memory ensures scalability of applications that use dsPIC33F devices.

Figure 1-1 shows a general block diagram of the various core and peripheral modules in the dsPIC33F family of devices, while Table 1-1 lists the functions of the various pins shown in the pinout diagrams.