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Freescale Semiconductor
User Guide

Document Number: MAC57D5xxUG
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MAC57D5xx Customer Evaluation Boards

1 Introduction

This user guide details the setup and configuration of the NXP MAC57D5xx Mother Board (MB) Customer Evaluation Board (hereafter referred to as the EVB) and its daughter cards (208 LQFP and 516 BGA).

The EVB is intended to provide a low cost mechanism for customer evaluation of the MAC57D5xx family of microcontrollers, and to facilitate hardware and software development. The EVB is intended for bench / laboratory use and has been designed using ambient temperature specified components. Two daughter cards are available which connect to the EVB via high-density connectors. Please consult your NXP representative for more details.

This product contains components that may be damaged by electrostatic discharge. Observe precautions for handling electrostatic sensitive devices when using this EVB and associated microcontroller.

Contents

2 Device overview MAC57D5xx Family

The MAC57D5xx family is the next generation platform of devices specifically targeted to the instrument cluster market using single and dual high resolution displays.

Leveraging the highly successful MPC56xxS product family, NXP is introducing a multi-core architecture powered by ARM Cortex-M (for real time) and Cortex-A processors (for applications and HMI), coupled with 2D Graphics Accelerators (GPU), Head Up Display (HUD) Warping Engine, Dual TFT display drive, integrated Stepper Motor Drivers and a powerful I/O processor, that will offer leading edge performance and scalability for cost-effective applications.

Powered by ARM® Cortex® -M and Cortex-A processors, coupled with 2D graphics accelerators, HUD warping engine, Dual TFT display drive, integrated Stepper Motor Controller and a powerful I/O processor, these products offer leading performance and scalability for cost-effective applications.

The family supports up to 2 WVGA resolution displays, including one with in-line Head up Display (HUD) warping hardware. Graphics content is generated using a powerful Viviane GPU supporting OpenVG1.1, and the 2D Animation and Composition Engine (2D-ACE), which significantly reduces memory footprint for content creation. Embedded memories include up to 4 MB Flash, 1 MB SRAM with ECC and up to 1.3 MB of graphics SRAM without ECC. Memory expansion is available through DDR2 and SDR DRAM interfaces while two flexible QuadSPI modules provide SDR and DDR serial Flash expansion. In response to the growing desire for security and safety, MAC57D5/4xx family integrates NXP's latest SHE-compliant CSE2 engine and delivers support for ISO26262 ASIL-B functional safety compliance.

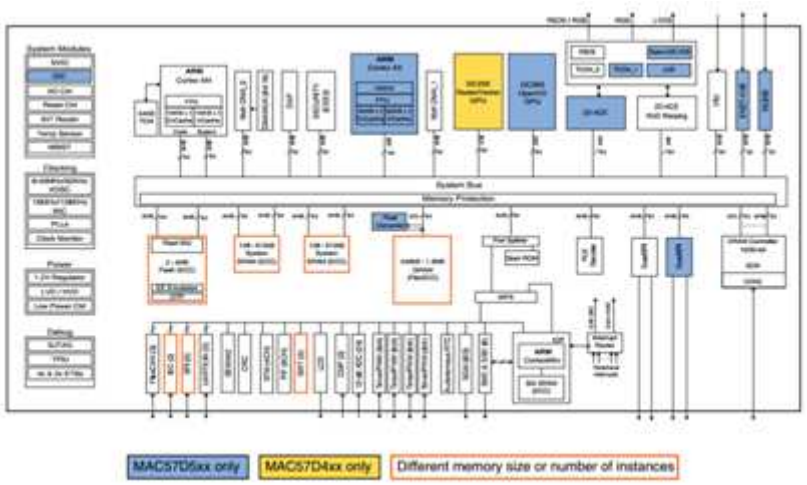

Figure 1. Block diagram

- Block Diagram shows the maximum configuration!.
- Not all pins or all peripherals are available on all devices and packages.
- Rerouting options are not shown.

3 Definitions, acronyms, and abbreviations

The following list defines the abbreviations used in this document.

Table 1. List of abbreviations

Abbreviations	Extension
CMOS	Complementary Metal Oxide Semiconductor
CPU	Central Processing Unit
CSI	Camera Sensor Imaging
DDR	Double Data Rate
EEPROM	Electrically Erasable Programmable Read Only Memory

Table continues on the next page...

Table 1. List of abbreviations (continued)

Abbreviations	Extension
EPROM	Erasable Programmable Read Only Memory
GPIO	General Purpose Input/Output
GPO	General Purpose Output
I2C	Inter-Integrated Circuit
I/O	Input/Output
JTAG	Joint Test Access Group
LAN	Local Area Network
LCD	Liquid Crystal Display
LED	Light Emitting Diode
MB	Megabyte
MCU	Microcontroller Unit
PC	Personal Computer
PCB	Printed Circuit Board
PHY	Physical interface
POR	Power on Reset
PWR	Power
PWM	Pulse Width Modulation
QVGA	Graphics Adapter
RAM	Random Access Memory
SD	SanDisk (Smart Media)
SDRAM	Synchronous Dynamic Random Access Memory
SI	System International (international system of units and measures)
TFT	Thin Film Transistor
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
HW	Hardware
SW	Software

4 MAC57D5MB – Evaluation Board features

MAC57D5MB provides the following key features:

- Master Power switch and regulators status LED's.
- High Speed CAN transceiver
- LIN interface
- Ethernet PHY and RJ45 socket configurable as RMII or MII
- 20-pin JTAG
- ARM Cortex Connector
- ART ETM Connector
- User RESET switch with reset status LED.
- User LED's

- User pushbutton switches
- Potentiometer connected to analogue input channel.
- VIU Interface
- TFT Display interface with Backlight power supply for EastRising - ER-TFT050-3
- 2 Stepper Motors Connectors

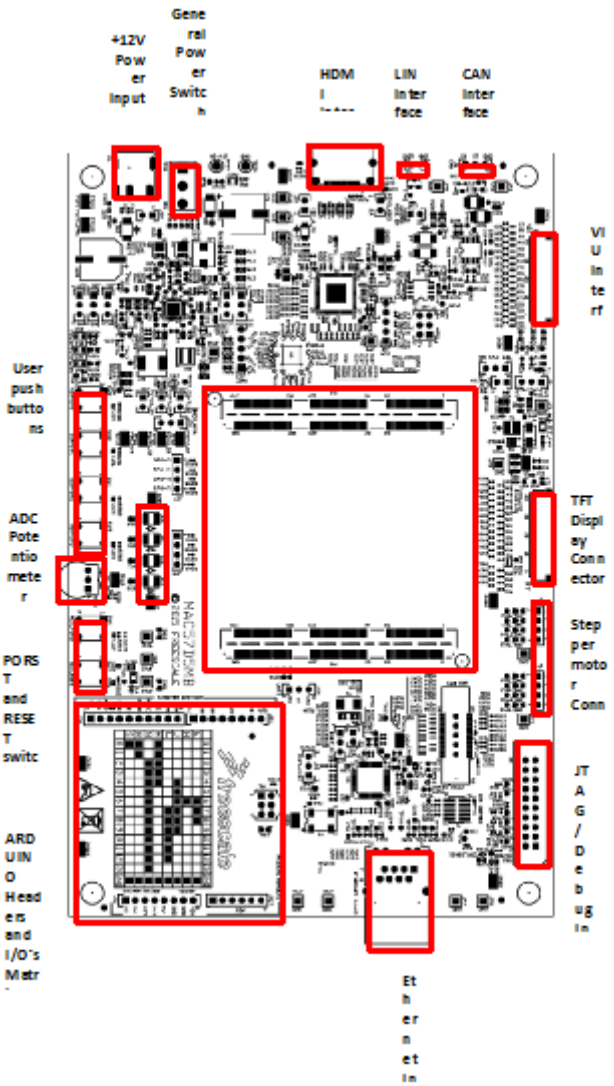

Figure 2. MAC57D5MB Evaluation Board

IMPORTANT

Before the EVB is used or power is applied, please fully read this user manual.
Failure to correctly configure the board may cause irreparable component, MCU or EVB damage.
Power must be removed from the EVB prior to:
- Removing or installing the MCU from the socket
- Re-configuring the board jumpers

5 Initial configuration

This section details the power, reset, clocks and debug configuration and is the minimum configuration needed in order to power on MAC57D5MB.

5.1 Main power supply

MAC57D5MB requires an external power supply voltage of 12 V, minimum 3 A. This allows the EVB to be easily used in a vehicle if required. The 12 V input is regulated on the EVB using two switching power supplies to provide the required voltages of 5.0 V, 3.3 V and 1.25 V in all interfaces of the Motherboard and the daughter cards.

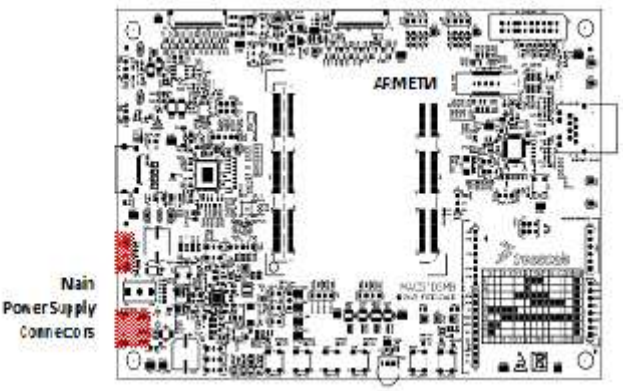

Figure 3. Main power supply connectors

For flexibility, there are two power supply inputs, the connector and test points on the EVB which are detailed below:

Table 2. Power Supply Connectors

CONNECTOR	DESCRIPTION
	2.1 mm Barrel Connector P6, this connector should be used to connect the supplied wall-plug mains adapter. **NOTE:** if a replacement or alternative adapter is used, care must be taken to ensure the 2.1 mm plug uses the correct polarization as shown.
	Two test points PC compact RED/BLACK TP79 and TP76, these test points can be used to connect a hook wire lead to the EVB, The polarization of the connectors is clearly marked on the EVB. Care must be taken to ensure correct connection.

5.2 Power switch (SW1)

Slide switch SW1 can be used to isolate the power supply input from the EVB voltage regulators if required.

- Moving the slide switch to the left (outward of the EVB) will turn the EVB off.
- Moving the slide switch to the right (inward of the EVB) will turn the EVB on.

5.3 Power jumpers of Regulators

All of the voltage regulators (switching and linear) are powered from the main 12 V supply line by a jumper with the exception of the 3.3 V and 1.8 V linear regulator which has a two way jumper to allow selection of the input voltage. The table below details the jumper configurations for the linear 1.25 V regulator source voltage. By default, the regulator is powered from a 12 V supply line.

Table 3. Regulators power jumpers

BOARD	REFERENCE	POSITION	PCB LEGEND	DESCRIPTION
MAC57D5MB	J32	1-2 (Default)	-	PMIC - switching regulators [5 V, 3.3 V and 1.25 V] are powered from VBAT [12 V].
		REMOVED	-	PMIC - switching regulators [5 V, 3.3 V and 1.25 V] are not powered.
	J35	1-2 (Default)	-	5.0 V switching regulator output is enabled
		2-3	-	5.0 V switching regulator output is disabled
		REMOVED	-	5.0 V switching regulator output is disabled
	J36	1-2 (Default)	-	3.3 V switching regulator output is enabled
		2-3	-	3.3 V switching regulator output is disabled
		REMOVED	-	3.3 V switching regulator output is disabled
	J37	1-2 (Default)	-	1.25 V switching regulator output is manually enabled
		2-3	-	1.25 V switching regulator output is disabled
		REMOVED	-	1.25 V switching regulator output is controlled by the MCU
	J30	1-2 (Default)	-	5.0 V switching regulator output is routed to all peripherals on the EVB.
		REMOVED	-	5.0 V switching regulator output is disconnected from all peripherals on the EVB. (Disabled)
	J26	1-2 (Default)	-	3.3 V switching regulator output is routed to all peripherals on the EVB.
		REMOVED	-	3.3 V switching regulator output is disconnected from all peripherals on the EVB. (Disabled)
	J33	1-2 (Default)	-	1.25 V switching regulator output is routed to all peripherals on the EVB.
		REMOVED	-	1.25 V switching regulator output is disconnected from all peripherals on the EVB. (Disabled)

5.4 Power status LED’s and Fuse

When power is applied to the EVB, five green LED's adjacent to the voltage regulators show the presence of the supply voltages as follows:

Table 4. Power status LEDs

BOARD	REFERENCE	DESCRIPTION
MAC57D5MB	DS2	Indicates that the 12 V is connected to the EVB correctly.
	DS4	Indicates that the 5 V switching regulator is enabled and working correctly.
	DS3	Indicates that the 3.3 V switching regulator is enabled and working correctly.
	DS5	Indicates that the 1.25 V switching regulator is enabled and working correctly.
	DS1	Indicates that the TFT Display – switching regulator is enabled and working correctly.
MAC57D5-208DC		
MAC57D5-506DC	DS1	Indicates that the 1.8 V switching regulator is enabled and working correctly.
	DS2	Indicates that the 0.9 V switching regulator is enabled and working correctly.

If no LED's are illuminated when power is applied to the EVB and the regulators are correctly enabled using the appropriate jumpers, it is possible that either power switch SW1 is in the "OFF" position or some jumper is missed, please refer to MCU power supply jumpers.

6 MCU power supply jumpers

Table 5. MCU power supply jumpers

BOARD	REFERENCE	POSITION	PCB LEGEND	DESCRIPTION
MAC57D5-208DC	J2	1-2 (Default)		5.0 V switching regulator output is routed to VDDEH_ADC_MCU and VDDA_MCU (MCU)
		2-3		3.3 V switching regulator output is routed to VDDEH_ADC_MCU and VDDA_MCU (MCU)
		REMOVED		VDDEH_ADC_MCU and VDDA_MCU are not powered (disabled).
	J1	1-2 (Default)		5.0 V switching regulator output is routed to VDDM_SMD_MCU (MCU)
		2-3		3.3 V switching regulator output is routed to VDDM_SMD_MCU (MCU)
		REMOVED		VDDM_SMD_MCU is not powered (disabled).
MAC57D5-516DC	J21	1-2 (Default)		3.3 V switching regulator output is routed to VDDE_A_MCU (MCU)
		REMOVED		VDDE_A_MCU is not powered (disabled).
	J22	1-2 (Default)		3.3 V switching regulator output is routed to VDDE_B_MCU (MCU)

Table continues on the next page...

Table 5. MCU power supply jumpers (continued)

BOARD	REFERENCE	POSITION	PCB LEGEND	DESCRIPTION
		REMOVED		VDDE_B_MCU is not powered (disabled).
	J27	1-2 (Default)		3.3 V switching regulator output is routed to VDDE_SDR_MCU (MCU)
		REMOVED		VDDE_SDR_MCU is not powered (disabled).
	J11	1-2 (Default)		3.3 V switching regulator output is routed to VDDM_SMD_MCU (MCU)
		2-3		5.0 V switching regulator output is routed to VDDM_SMD_MCU (MCU)
		REMOVED		VDDM_SMD_MCU is not powered (disabled).
	J2	1-2 (Default)		3.3 V switching regulator output is routed to VDDEH_ADC_MCU
		2-3		5.0 V switching regulator output is routed to VDDEH_ADC_MCU
		REMOVED		VDDEH_ADC_MCU is not powered (disabled).
	J3	1-2 (Default)		3.3 V switching regulator output is routed to VDDA_MCU (MCU)
		2-3		5.0 V switching regulator output is routed to VDDA_MCU (MCU)
		REMOVED		VDDA_MCU are not powered (disabled).
	J6	1-2 (Default)		3.3 V switching regulator output is routed to VDD_HV_BALLST (MCU)
		2-3		5.0 V switching regulator output is routed to VDD_HV_BALLST (MCU)
		REMOVED		VDD_HV_BALLST is not powered (disabled).
	J8	1-2 (Default)		1 V 25_SR switching voltage regulator is routed to VDD12_MCU (MCU)
		2-3		Output voltage of the ballast transistor is routed to VDD12_MCU (MCU)
		REMOVED		VDD12_MCU is not powered (disabled).
	J23	1-2 (Default)		1.8 V switching regulator output is routed to VDDE_DDR_MCU (MCU)
		REMOVED		VDDE_DDR_MCU is not powered (disabled).
	J18	1-2		P0V9_SR [P0V9_VTTREF] switching regulator output is routed to VREF_DDR2_MCU and VREF_DDR2M
		2-3 (Default)		Divider resistor reference (0.9 V) is routed to VREF_DDR2_MCU and VREF_DDR2M
		REMOVED		VDDP9_DDR_MCU is not powered (disabled).

6.1 Peripheral power supply jumper

There is an additional power supply jumper controlling the I/O voltage for the peripherals on the MAC57D5MB in the PER_HVA voltage domain. The default configuration matches the default configuration with the jumpers set to 3.3 V.

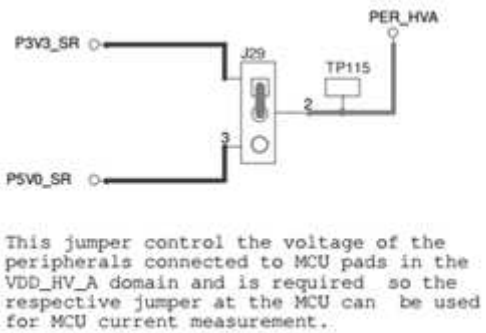

Table 6. Peripheral power supply jumper

BOARD	REFERENCE	POSITION	PCB LEGEND	DESCRIPTION
MAC57D5MB	J29	1-2 (Default)		3.3 V switching regulator output is routed to **PER_HVA** (MCU)
		2-3		5.0 V switching regulator output is routed to **PER_HVA** (MCU)
		REMOVED		**PER_HVA** is not powered (disabled).

6.2 EVB voltage regulators

The following table shows the usage of each EVB voltage regulator. This provides a useful cross reference point should any regulator be disabled.

Table 7. Voltage regulators

Regulator	Used on
12 V Unregulated P12V	All voltage regulators (switching and Linear, jumper selectable on 3.3V linear) LIN Interface.
3.3 V Linear P3V3_LR	VDDA_MCU VDDEH_ADC_MCU MLB Interface ADC Potentiometer
5.0 V Switcher P5V0_SR	PER_HVA VDDA_MCU VDDE_A_MCU VDDE_B_MCU

Table continues on the next page...

Table 7. Voltage regulators (continued)

Regulator	Used on
	VDDE_SDR_MCU
	VDDM_SMD_MCU
	VDD_HV_BALLST
	VDDEH_ADC_MCU
	CAN Interface
3.3 V Switcher P3V3_SR	VDDE_A_MCU
	VDDE_B_MCU
	VDDE_SDR_MCU
	VDDM_SMD_MCU
	VDD_HV_BALLST
	Reset LED indicators
	MLB Interface
	TFT Display
	Ethernet Interface
	User LEDSs (Active Low)
	User Switches (Active High)
	VIU Interface
	LVDS Display
	DDR-II VREF and VTT Power Supply
1.8 V Switcher P1V8_SR	VDDE_DDR_MCU
	DDR2_Intarface
	VIU Interface
0.9 V Switcher P0V9_SR	VDDP9_DDR_MCU
1.25 V Switcher 1V25_SR	VDD12_MCU

7 Reset control and Oscillators

7.1 Reset circuit

The MCU has a single bi-directional open drain reset pin. There is a reset LED – D14 (Red), placed adjacent to the EVB RESET switch to indicate the RESET status of the EVB and MCU.

7.2 Oscillators

For daughter cards, there are two external clock crystals:

- 40 MHz fast external crystal for clocking the main system clock
- 32.768 kHz slow external crystal for accurate time of day keeping.

The 32.768 kHz external crystal is permanently connected to the MCU EXTAL32 and XTAL32 pins and has no configuration options.

8 Debug connectors

The following figure shows the pinouts for each of the debug connectors used on the MAC57D5MB.

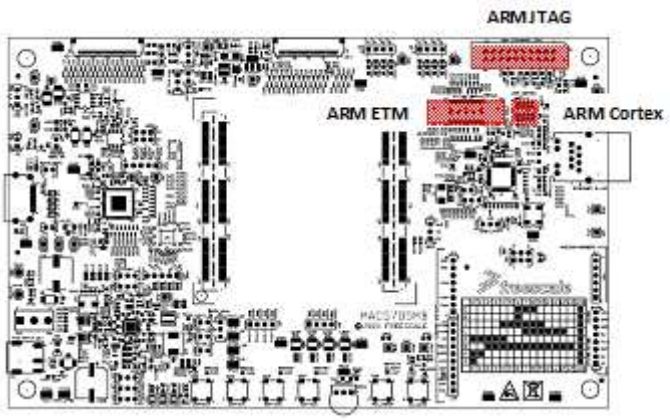

Figure 4. Debug connectors

8.1 ARM 20-PIN (JTAG)

The table below showcases the ARM 20-pin JTAG connector.

Table 8. JTAG debug connector Pinout

Pin No.	Function	Connection	Pin Number	Function	Connection
1	VCC	PER_HVA	**2**	VCC (optional)	---
3	TRST	Pull-up	**4**	GND	GND
5	NC/TDI	JTAG_TDI	**6**	GND	GND
7	SWDIO/TMS	JTAG_TMS	**8**	GND	GND
9	SWDCLK / TCK	JTAG_TCLK	**10**	GND	GND
11	RTCK	Pull down	**12**	GND	GND
13	SWO / TDO	JTAG_TD0	**14**	GND	GND
15	nRESET	JTAG_RSTx	**16**	GND	GND

Table continues on the next page...

Table 8. JTAG debug connector Pinout (continued)

Pin No.	Function	Connection	Pin Number	Function	Connection
17	NC/DBGRQ	---	**18**	GND	GND
19	NC/DBACK	---	**20**	GND	GND

8.2 ARM ETM 38-PIN

The table below showcases the pin arrangement for the ARM ETM 38-pin connector. The recommended connector is the Mictor connector (type 5767054-1 or compatible).

Table 9. ARM-ETM debug connector pinout

Pin No.	Function	Connection	Pin No.	Function	Connection
1	NC	---	**2**	NC	---
3	NC	---	**4**	NC	---
5	GND	---	**6**	TRACECLK	TRACE_CK
7	Pull down	Pull down	**8**	Pull down	Pull down
9	NC/ nSRST	JTAG_RSTx	**10**	Pull down	Pull down
11	TDO/SWV	JTAG_TD0	**12**	Pull-up (Vref)	PER_HVA
13	RTCK	TP	**14**	VSupply	PER_HVA
15	TCK/SWCLK	JTAG_TCLK	**16**	0 / TRACEDATA[7]	TRACED7
17	TMS/SWIO	JTAG_TMS	**18**	0 / TRACEDATA[6]	TRACED6
19	TDI	JTAG_TDI	**20**	0 / TRACEDATA[5]	TRACED5
21	nTRST	TP	**22**	0 / TRACEDATA[4]	TRACED4
23	0 / TRACEDATA[15]	TRACED15	**24**	TRACEDATA[3]	TRACED3
25	0 / TRACEDATA[14]	TRACED14	**26**	TRACEDATA[2]	TRACED2
27	0 / TRACEDATA[13]	TRACED13	**28**	TRACEDATA[1]	TRACED1
29	0 / TRACEDATA[12]	TRACED12	**30**	0	Pull down
31	0 / TRACEDATA[11]	TRACED11	**32**	0	Pull down
33	0 / TRACEDATA[10]	TRACED10	**34**	1	Pull down
35	0 / TRACEDATA[9]	TRACED9	**36**	0 / TRACECTRL	TRACE_CTL
37	0 / TRACEDATA[8]	TRACED8	**38**	TRACEDATA[0]	TRACED0

8.3 ARM CORTEX 10-PIN

The table below showcases the pin arrangement for the ARM Cortex 10-pin connector.

Table 10. ARM-Cortex debug connector pinout

Pin No.	Function	Connection	Pin No.	Function	Connection
1	VCC	PER_HVA	**2**	TMS	JTAG_TMS
3	GND	GND	**4**	TCLK	JTAG_TCLK
5	GND	GND	**6**	TDO	JTAG_TDO
7	NC	--	**8**	TDI	JTAG_TDI
9	NC	TP	**10**	(nSRST)	JTAG_RSTx

9 Communications interfaces

This section details the communication interface and storage peripherals that are implemented on the EVB.

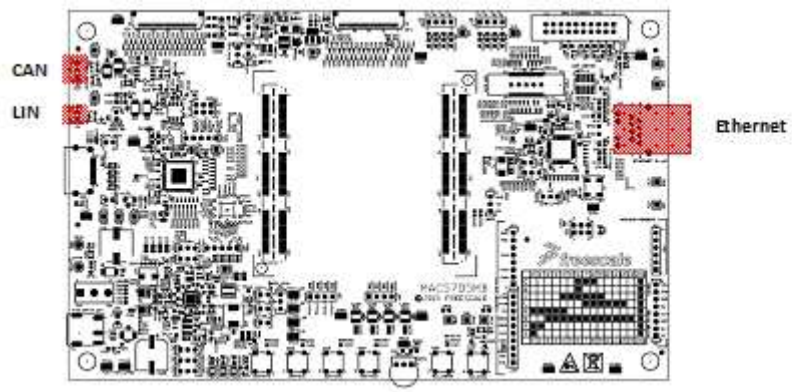

Figure 5. Communication interfaces

9.1 CAN interface

The EVB incorporates a CAN interface circuit connected to MCU CAN0 using MC33901-NXP transceiver. The transceiver is configured for normal speed operation by pull down resistor on STB [pin 8]. There are test points to allow the Select pin to be driven high if desired.

For flexibility, the CAN transceiver I/O is connected to a standard 0.1” connector (J9). The pinout of this header is detailed on the PCB silkscreen.

Table 11. CAN physical interface connector

Jumper	PIN	PCB Legend	Description
J9	1	CANH0	CAN High-Level Voltage I/O
	2	CANL0	CAN Low-Level Voltage I/O
	3	GND	GND

The MCU CAN Tx/Rx pins are powered from the VDDE_SDR_MCU domain, which is configured between 3.3V and 5.0V using jumper placed in daughter card. The CAN transceiver I/O voltage is connected to the PER_HVA net configured with jumper J29 on the EVB. Care must be taken to ensure that the MCU CAN I/O pins in domain VDDE_SDR_MCU and PER_HVA supply are the same when using the CAN transceiver.

9.2 LIN interface

MAC57D5MB incorporates one LIN transceiver circuit connected to MCU LIN0 using a NXP MC33662LEF transceiver supporting both master and slave mode (jumper selectable).

The LIN1 MCU TX/RX signals are jumpered as shown in the table below, so that the transceiver can be isolated from the respective MCU pin if desired. The default configuration is fitted routing the TX and RX signals to the MCU.

Table 12. LIN_TX/RX control jumper

Jumper	Position	Description
J10	1-3	PJ3 port is routed to the LIN interface, as LIN0_TX signal.
	3-5	PJ3 port is routed to the ARDUINO headers, as ARDN_TX signal.
	Removed	PJ3 port is disconnected of all interfaces.
	2-4	PJ2 port is routed to the LIN interface, as LIN0_RX signal.
	2-6	PJ2 port is routed to the ARDUINO headers, as ARDN_RX signal.
	Removed	PJ2 port is disconnected of all interfaces.

The LIN TX / RX MCU pins are powered from the VDDE_SDR_MCU domain, which is configured between 3.3 V and 5.0 V using jumper placed in daughter card. The LIN transceivers enable pin is connected to the PER_HVA net configured with jumper J29 on the EVB. Care must be taken to ensure that the VDDE_SDR_MCU and PER_HVA supplies are the same when using the LIN transceiver.

Table 13. LIN physical interface connector

Jumper	PIN	PCB Legend	Description
J11	1	LIN	LIN
	2	GND	GND Reference

9.3 Ethernet

MAC57D5xx supports both MII and RMII Ethernet interfaces. The EVB incorporates a DP83848c transceiver supporting both MII and RMII (configurable with a jumper). The transceiver is connected to a pulse J1011F21PNL RJ45 connector which includes a built-in isolation transformer.

The default configuration sets the transceiver for MII mode, with the reset signal to the PHY being driven from the MCU Reset out (e.g. any reset causing the MCU Reset line to assert will reset the PHY). To configure the Ethernet transceiver to RMII mode Jumper J18 has to be modified as well as the two clock jumpers J15 and J17 (to route the 50 MHz clock to the PHY). To change the reset routing so that the Ethernet PHY can be reset via MCU pin PR9 (rather than being tied to the MCU reset) R161 must be removed and R160 must be placed.

Table 14. Ethernet control jumpers

Jumper	Position	PCB Legend	Description
J18	1-2 (Default)		Ethernet PHY is configured in MII mode
	2-3		Ethernet PHY is configured in RMII mode
	REMOVED		Invalid Configuration, avoid!
J15	1-2 (Default)		Ethernet PHY X2 clock is connected to 25 MHz xtal
	2-3		Ethernet PHY X2 clock is not connected to 25 MHz xtal **
J17	1-2 (Default)		Ethernet PHY X1 clock is connected to 25 MHz xtal
	2-3		Ethernet PHY X1 clock is driven from 50 MHz xtal
	REMOVED		Ethernet PHY X1 clock is disconnected (invalid configuration, avoid)

NOTE

If jumper J17 is in position 1-2 (25 MHz XTAL), J15 must be fitted - If jumper J17 is in position 2-3 (50 MHz oscillator), J15 must be removed.

10 Graphics display and video interfaces

The figure below highlights the available video and display interfaces on the board.

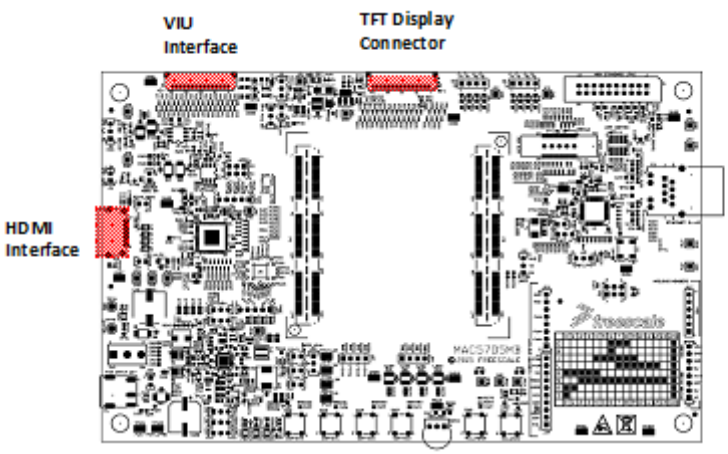

Figure 6. Graphics display and video interfaces

10.1 TFT displays interface

MAC57D5MB evaluation board has a connector routed to the 2D-ACE1 module of the MCU. The pinout connector is compatible with the WVGA (800x480) TFT Panel (part number ER-TFT050-3), and the SHARP - LQ050Y3DC01 TFT Display. Care should be taken when attaching and removing the TFT panel as the connectors are fragile. The pinout of the connector is shown below for reference.

Table 15. TFT display connector pinout

J2 - TFT Display INTERFACE [DCU 1]

Table continues on the next page...

Table 15. TFT display connector pinout (continued)

Pin No.	Signal	Description	MCU Connection
1	LEDK	BCKL Pwr supply Pos	
2	LDEA	BCKL Pwr supply Neg	
3	GND	Ground	GND
4	VCC	Pwr Supply	P3V3_SR
5	R0	Red data	VOUT1_D2
6	R1	Red data	VOUT1_D3
7	R2	Red data	VOUT1_D4
8	R3	Red data	VOUT1_D5
9	R4	Red data	VOUT1_D6
10	R5	Red data	VOUT1_D7
11	R6	Red data	VOUT1_D8
12	R7	Red data	VOUT1_D9
13	G0	Green data	VOUT1_D10
14	G1	Green data	VOUT1_D11
15	G2	Green data	VOUT1_D12
16	G3	Green data	VOUT1_D13
17	G4	Green data	VOUT1_D14
18	G5	Green data	VOUT1_D15
19	G6	Green data	VOUT1_D16
20	G7	Green data	VOUT1_D17
21	B0	Blue data	VOUT1_D18
22	B1	Blue data	VOUT1_D19
23	B2	Blue data	VOUT1_D20
24	B3	Blue data	VOUT1_D21
25	B4	Blue data	VOUT1_D22
26	B5	Blue data	VOUT1_D23
27	B6	Blue data	VOUT1_D24
28	B7	Blue data	VOUT1_D25
29	GND	Ground	GND
30	CLK	Clock Signal	VOUT1_D1
31	DISP	Display ON/OFF	TFTBCKL_DISP
32	HSYBC	Horizontal sync	VOUT1_C1
33	VSYNC	Vertical sync	VOUT1_C2
34	DE	Data Enable	VOUT1_D0
35	NC	-	VOUT1_C0
36	GND	Ground	GND
37	XR	X_RIGHT	TFT1_ADC1
38	YD	Y_DOWN	TFT1_ADC2
39	XL	X_LEFT	TFT1_ADC3
40	YU	Y_UP	TFT1_ADC4

10.2 HDMI

MAC57D5MB has an HDMI interface using the SiI9022A/SiI9024A HDMI transmitter routed to the Display Controller (2D-ACE0 - Two Dimensional Animation and Compositing Engine) of the MAC57D5xx microcontroller . This interface supports the High Definition Multimedia Interface (HDMI) Specification on a wide range of mobile products. High definition camcorders, digital still cameras, and personal mobile devices connect directly to a large installed base of HDMI TVs and DVI PC monitors by using the flexible audio and video interfaces provided by this ultra-low-power solution. S/PDIF or I 2 S inputs enable a pure digital audio connection to virtually any system audio processor or codec.

The SiI9024A transmitter supports High-bandwidth Digital Content Protection (HDCP) for devices that require secure content delivery.

10.3 Digital video input

The VIU is a bridge between video decoder and system memory. It accepts an ITU656 compatible video stream, or parallel YUV/RGB input, converting image data between YUV and RGB color spaces, scaling image size, adjusting the brightness/ contrast, and writing image data to memory with many kinds of image data formats.

MAC57D5MB evaluation board has a connector routed to the VIU Module of the MCU. The pinout of the connector is shown in the table below for reference.

Table 16. VIU connector pinout

J1 – VIU Interface		
Pin No.	Signal	Description
1	P5V0_SR	Disabled by R4
2	P3V3_SR	Disabled by R5
3	PWR_VIU	3.3 V or 5.0 V
4	GND	
5	VIU_DATA_16	VIU Pixel Data Input
6	VIU_DATA_17	VIU Pixel Data Input
7	VIU_DATA_18	VIU Pixel Data Input
8	VIU_DATA_19	VIU Pixel Data Input
9	VIU_DATA_20	VIU Pixel Data Input
10	VIU_DATA_21	VIU Pixel Data Input
11	VIU_DATA_22	VIU Pixel Data Input
12	VIU_DATA_23	VIU Pixel Data Input
13	VIU_DATA_8	VIU Pixel Data Input
14	VIU_DATA_9	VIU Pixel Data Input
15	VIU_DATA_10	VIU Pixel Data Input
16	VIU_DATA_11	VIU Pixel Data Input
17	VIU_DATA_12	VIU Pixel Data Input
18	VIU_DATA_13	VIU Pixel Data Input
19	VIU_DATA_14	VIU Pixel Data Input

Table continues on the next page...

Table 16. VIU connector pinout (continued)

20	VIU_DATA_15	VIU Pixel Data Input
21	VIU_DATA_0	VIU Pixel Data Input
22	VIU_DATA_1	VIU Pixel Data Input
23	VIU_DATA_2	VIU Pixel Data Input
24	VIU_DATA_3	VIU Pixel Data Input
25	VIU_DATA_4	VIU Pixel Data Input
26	VIU_DATA_5	VIU Pixel Data Input
27	VIU_DATA_6	VIU Pixel Data Input
28	VIU_DATA_7	VIU Pixel Data Input
29	GND	
30	VIU_PCLK	VIU Pixel Clock Input
31	GPIO	
32	VIU_HSYNC	VIU Horizontal Sync Input
33	VIU_VSYNC	VIU Vertical Sync Input
34	VIU_DE	VIU Data Enable Input
35	GPIO	
36	GND	
37	SDA	I2C Serial Data Output
38	SCL	I2C Serial Clock Output
39	VIU_FID	VIU Frame ID Input
40	VIU_RST	GPIO

NOTE

For MAC57D5-208DC daughterboard, some ENET and VIU data lines are shared from the MCU, each interface is separated by two 0 resistors, by default the VIU data lines are disabled.

10.4 LVDS interface

The LVDS module on MAC57D5-516DC is available in a 30-pin connector [DF19G-30P-1H(54)].

Table 17. LVDS interface

J20 – LVDS Interface		
Pin No.	Signal	Description
1	LVDS_BACKLITE_ON	PM10
2	P3V3_LVDS	3.3 V
3		
4		
5	LVDS_BACKLITE_BRIGHTNESS	PN13
6	OLDI_N3	Pixel Data

Table continues on the next page...

Table 17. LVDS interface (continued)

7	OLDI_P3	Pixel Data
8	OLDI_N0	Pixel Data
9	OLDI_P0	Pixel Data
10	GND	GND
11	OLDI_N1	Pixel Data
12	OLDI_P1	Pixel Data
13	GND	GND
14	OLDI_N2	Pixel Data
15	OLDI_P2	Pixel Data
16	GND	GND
17	OLDI_CLKN	Pixel Clock
18	OLDI_CLKP	Pixel Clock
19	GND	GND
20	P5V0_LVDS	3.3 V
21		
22	GND	GND
23	GND	GND
24	P5V0_LVDS	3.3 V
25		
26		
27	LVDS_TOUCH_SCL	I2C
28	LVDS_TOUCH_SDA	I2C
29	LVDS_TOUCH_INT_B	PM12
30	-	NC

11 User interface (I/O)

This section details the user and general purpose interfaces available in MAC57D5MB:

- ARDUINO headers
- GPIO matrix, switches
- LED’s
- ADC rotary potentiometer

11.1 ARDUINO headers

A part of the available GPIOs of the daughter cards is routed to an user interface in the MAC57D5MB board, this interface has form-factor compatible with the Arduino™ R3 pin layout, providing a broad range of expansion board options.

Table 18. ARDUINO connectors

ARDUINO HEADER		FUNCTION	BOARD	
REFERENCE	PIN		MAC57D5-208DC	MAC57D5-516DC
J31	1	-	-	-
	2	+5V0	+5V0	+5V0
	3	RESET	RESET	RESET
	4	+3V3	+3V3	+3V3
	5	+5V0	+5V0	+5V0
	6	GND	GND	GND
	7	GND	GND	GND
	8	+12V	+12V	+12V
JP17	1	ADC	PE5	PE5
	2	ADC	PE10	PE10
	3	ADC	PE11	PE11
	4	ADC	PE12	PE12
	5	ADC	PE13	PE13
	6	ADC	PE14	PE14
J34	1	SCL	PM7	PM7
	2	SDA	PM6	PM6
	3	AREF	PER_HVA	PER_HVA
	4	GND	GND	GND
	5	SCK	PF0	PF0
	6	MISO	PF1	PF1
	7	MOSI	PF2	PF2
	8	SS	PE15	PE15
	9	PWM	PC8	PC8
	10	PWM	PC9	PC9
J24	1	GPIO	PC0	PC0
	2	PWM	PC1	PC1
	3	PWM	PC2	PC2
	4	GPIO	PC3	PC3
	5	PWM	PC4	PC4
	6	GPIO	PC5	PC5
	7	TXD	PJ3	PJ3
	8	RXD	PJ4	PJ4

NOTE

Refer to the device RM and DS to check the additional functions in the pins routed at the ARDUINO headers.

11.2 GPIO matrix

All of the available GPIO pins in the daughter cards (those not already used for existing EVB peripherals) are routed at the GPIO matrix. The matrix provides an easy to follow, intuitive, space saving grid of 0.1” header through hole pads. Users can solder wires, fit headers or simply insert a scope probe into the respective pad.

To use the matrix, simply read the port letter from the top or bottom row of text then the pad number from the columns on the left or right of the matrix.

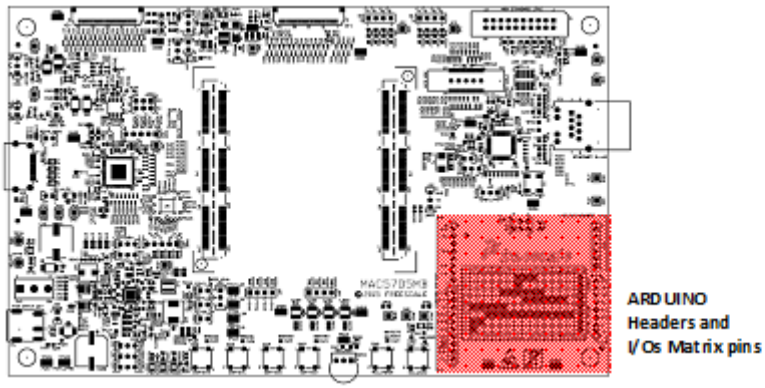

Figure 7. ARDUINO Headers and I/Os matrix pins

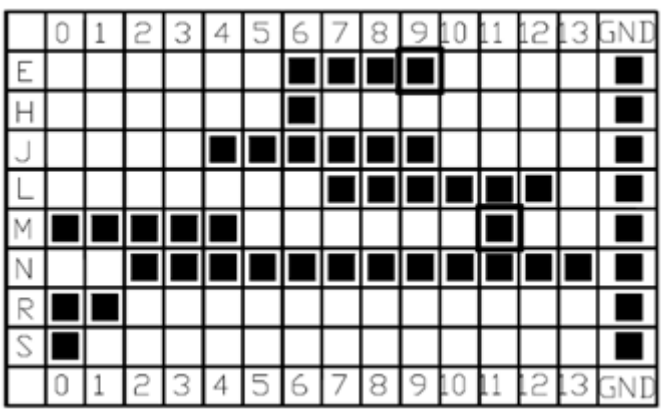

Figure 8. I/Os matrix pins

11.3 User switches

There are four active high pushbutton switches (SW2, SW3, SW4, and SW5), pulled low, driven to 3.3 V or 5.0 V by the PER_HVA rail. The switches are connected to a header (J27), and also directly wired to MCU ports so no wires need to be wired, unless it is required to route these to a different GPIO pad on the MCU.

11.4 User LED’s

There are four LEDs for general purpose (D10, D11, D12, and D13), pulled to 3.3 V or 5.0 V by the PER_HVA rail. The LEDs are connected to a header (J28), and also directly wired to MCU ports so no wired need to be wired, unless it is required to route these to a different GPIO pad on the MCU.

11.5 ADC input potentiometer

There is a rotary variable resistor R293 on the EVB which routes a voltage between 0v and PER_HVA (3.3 V or 5.0 V). This is useful for quick ADC testing.

11.6 Stepper Motor peripheral

The chip has one Stepper Motor Controller (SMC) module capable of driving up to six stepper motors for instrument cluster gauges. Each stepper motor is driven by four outputs to drive two coils. Control of this module will be typically, but not exclusively, by the Cortex M0+ IO processor subsystem.

The Stepper Motor Controller (SMC) block is a PWM motor controller suitable for driving small stepper and air core motors used in instrumentation applications. The module can also be used for other motor control or PWM applications that match the frequency, resolution and output drive capabilities of the module.

The SMC has 12 PWM channels associated with two pins each (24 pins in total).

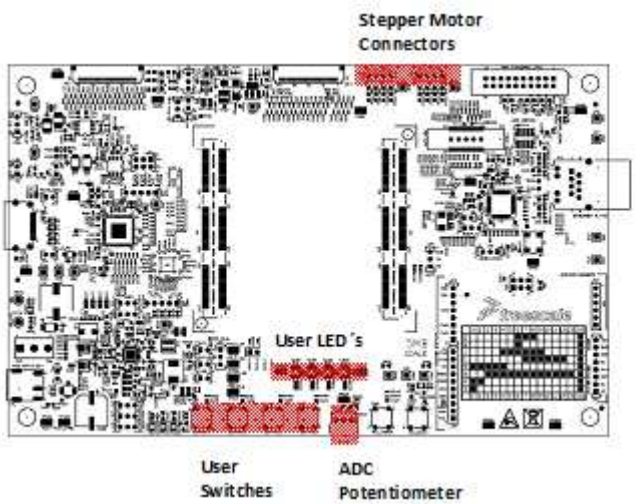

Figure 9. User interfaces

12 Jumper Default Configuration

The following table features the default jumper configuration for the available boards.

Table 19. Jumper Default Configuration

BOARD	JUMPER CONFIGURATION			
	Ref Des	Position	Circuit	Description

Table continues on the next page...

Table 19. Jumper Default Configuration (continued)

MAC57D5MB	**J32**	1-2	PMIC	PMIC - Switching Regulators [5 V, 3.3 V and 1.25 V] are powered from VBAT [12V].
	J30	1-2	PMIC	5.0 V Switching regulator output is routed to all peripherals on the EVB.
	J26	1-2	PWR	3.3 V Switching regulator output is routed to all peripherals on the EVB.
	J33	1-2	PWR	1.25 V Switching regulator output is routed to all peripherals on the EVB.
	J5	1-2	VIU	5.0 V Switching Regulator output is routed to PWR_VIU
	J29	1-2	PMIC	3.3 V Switching Regulator output is routed to **PER_HVA** (MCU)
	J35	1-2	PMIC	5.0 V Switching Regulator output is enabled
	J36	1-2	PMIC	3.3 V Switching Regulator output is enabled
	J37	1-2	PMIC	1.25 V Switching Regulator output is enabled
	J22	1-2	PMIC	Spread spectrum oscillator is enable
	J25	1-2	PMIC	Skip Mode is disable
	J17	1-2	ENET	Ethernet PHY X1 clock is connected to 25 MHz xtal
	J15	1-2	ENET	Ethernet PHY X1 clock is connected to 25 MHz xtal
	J18	1-2	ENET	Ethernet PHY is configured in MII mode
	J7	1-2	TFT	Step-Up Switching Regulator for TFT Displays is powered from P5V0 [5.0 V].

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Table 19. Jumper Default Configuration (continued)

	J8	1-2	TFT	Step-Up Switching Regulator for TFT Displays is enabled from P5V0 [5.0 V].
	J10	3-5	LIN	PJ2 port is routed to LIN Interface
		4-6	LIN	PJ3 port is routed to LIN Interface
	J14	1-2	HDMI	5.0 V Switching Regulator output is routed to the HDMI connector.
MAC57D5-208DC	**J2**	1-2	MCU	VDDEH_ADC_MCU is routed to P5V0
		1-2	MCU	VDDA is routed to P5V0
	J1	1-2	MCU	VDD_SMD_MCU is routed to P5V0
MAC57D5-516DC	**J2**	1-2	MCU	VDDEH_ADC_MCU is routed to P5V0
	J3	1-2	MCU	VDDA is routed to P5V0
	J11	1-2	MCU	VDD_SMD_MCU is routed to P5V0
	J21	1-2	MCU	VDDE_A_MCU is routed to P3V3_SR
	J22	1-2	MCU	VDDE_E_MCU is routed to P3V3_SR
	J6	1-2	MCU	VDD_HV_BALLST is routed to P3V3_SR
	J27	1-2	MCU	VDDE_SDR_MCU is routed to P3V3_SR
	J8	1-2	MCU	VDD12_MCU is routed to P1V25_SR
	J25	1-2	DDR	0.9 V Switching Regulator output is routed to **VTT_DDR2.**
	J23	1-2	MCU	1.8 V Switching Regulator output is routed to **VDDE_DDR_MCU** (MCU)
	J26	1-2	MCU	1.8 V Switching Regulator output is routed to **DDR2 Interface** (MCU)

Table continues on the next page...

Table 19. Jumper Default Configuration (continued)

	J18	1-2	DDR	VREF_DDR2_MCU and VREF_DDR2M are routed to a 0.9 V divider voltage.

12.1 Default Jumper Diagram

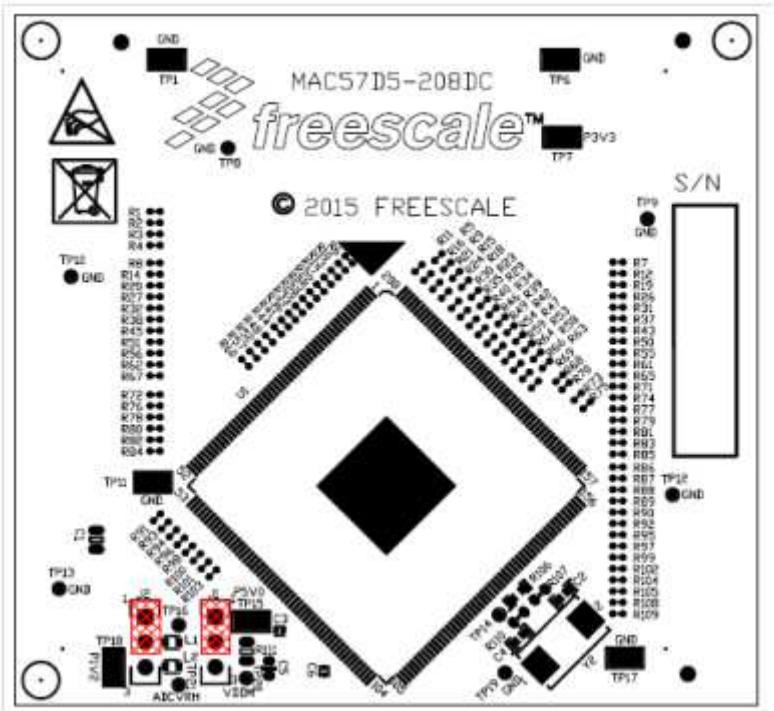

Figure 10. MAC57D5-208DC - default jumper configuration