Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

MAX30003

Ultra-Low Power, Single-Channel Integrated Biopotential (ECG, R-to-R Detection) AFE

General Description

The MAX30003 is a complete, biopotential, analog front-end solution for wearable applications. It offers high performance for clinical and fitness applications, with ultra-low power for long battery life. The MAX30003 is a single biopotential channel providing ECG waveforms and heart rate detection.

The biopotential channel has ESD protection, EMI filtering, internal lead biasing, DC leads-off detection, ultra-low power leads-on detection during standby mode, and extensive calibration voltages for built-in self-test. Soft power-up sequencing ensures no large transients are injected into the electrodes. The biopotential channel also has high input impedance, low noise, high CMRR, programmable gain, various low-pass and high-pass filter options, and a high resolution analog-to-digital converter. The biopotential channel is DC coupled, can handle large electrode voltage offsets, and has a fast recovery mode to quickly recover from overdrive conditions, such as defibrillation and electrosurgery.

The MAX30003 is available in a 28-pin TQFN and 30-bump wafer-level package (WLP), operating over the 0°C to +70°C commercial temperature range.

Applications

- Single-Lead Event Monitors for Arrhythmia Detection
- Single-Lead Wireless Patches for At-Home/ In-Hospital Monitoring
- Chest Band Heart Rate Monitors for Fitness Applications
- Bio Authentication and ECG-On-Demand Applications

***Ordering Information** appears at end of data sheet.*

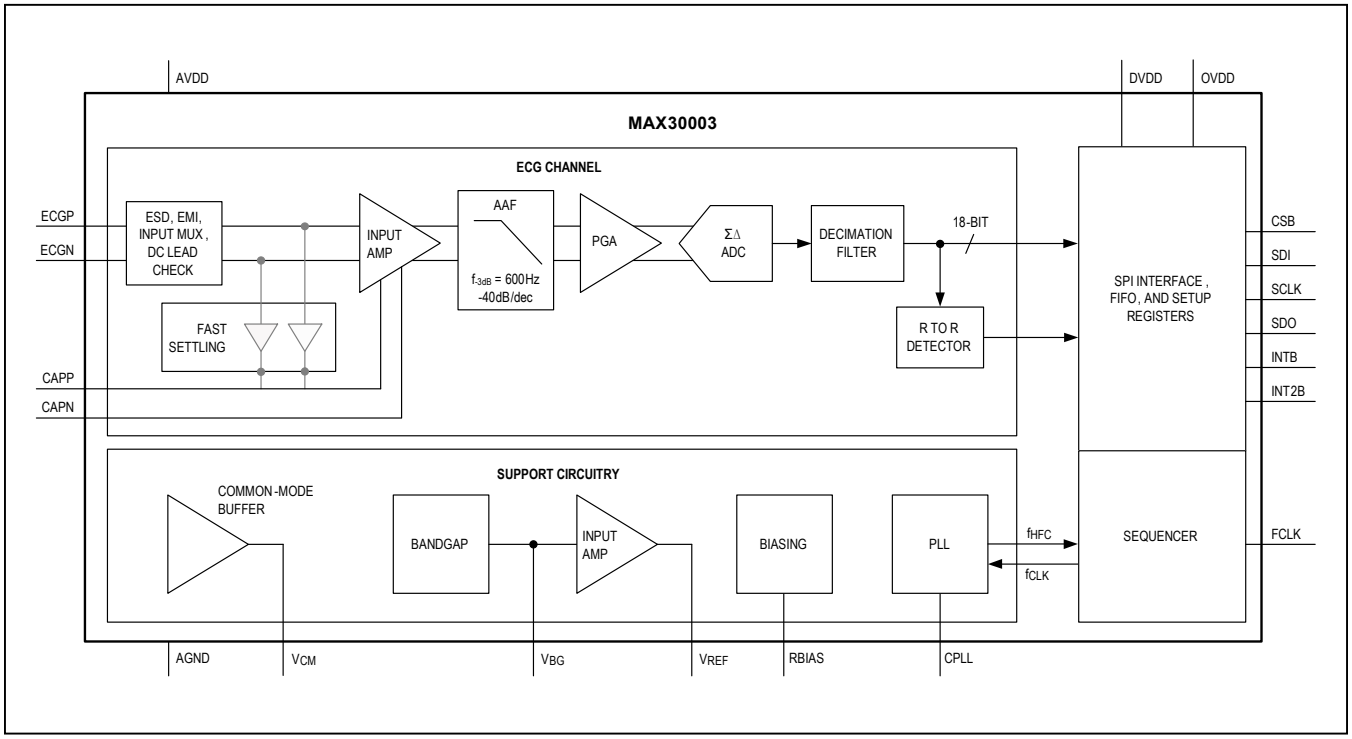
Benefits and Features

- Clinical-Grade ECG AFE with High-Resolution Data Converter
  - 15.5 Bits Effective Resolution with 5µV_{P-P} Noise
- Better Dry Starts Due to Much Improved Real World CMRR and High Input Impedance
  - Fully Differential Input Structure with CMRR > 100dB
- Offers Better Common-Mode to Differential Mode Conversion Due to High Input Impedance
  - High Input Impedance > 500MΩ for Extremely Low Common-to-Differential Mode Conversion
- Minimum Signal Attenuation at the Input During Dry Start Due to High Electrode Impedance
- High DC Offset Range of ±650mV (1.8V, typ) Allows to Be Used with Wide Variety of Electrodes
- High AC Dynamic Range of 65mV_{P-P} Will Help the AFE Not Saturate in the Presence of Motion/Direct Electrode Hits
- Longer Battery Life Compared to Competing Solutions
  - 85µW at 1.1V Supply Voltage
- Leads-On Interrupt Feature Allows to Keep µC in Deep Sleep Mode with RTC Off Until Valid Lead Condition is Detected
  - Lead-On Detect Current: 0.7µA (typ)
- Built-In Heart Rate Detection with Interrupt Feature Eliminates the Need to Run HR Algorithm on the µController
  - Robust R-R Detection in High Motion Environment at Extremely Low Power
- Configurable Interrupts Allows the µC Wake-Up Only on Every Heart Beat Reducing the Overall System Power
- High Accuracy Allows for More Physiological Data Extractions
- 32-Word FIFO Allows You to Wake Up µController Every 256ms with Full ECG Acquisition
- High-Speed SPI Interface
- Shutdown Current of 0.5µA (typ)

19-8558; Rev 1; 11/16

maxim integrated™

Functional Diagram



Absolute Maximum Ratings

AV_{DD} to AGND .....-0.3V to +2.0V
DV_{DD} to DGND .....-0.3V to +2.0V
AV_{DD} to DV_{DD}.....-0.3V to +0.3V
OV_{DD} to DGND .....-0.3V to +3.6V
AGND to DGND .....-0.3V to +0.3V
CSB, SCLK, SDI, FCLK to DGND .....-0.3V to +3.6V
SDO, INTB, INT2B to
DGND .....-0.3V to the lower of (3.6V and OV_{DD} + 0.3V)
All other pins to
AGND .....-0.3V to the lower of (2.0V and AV_{DD} + 0.3V)
Maximum Current into Any Pin.....±50mA

Continuous Power Dissipation (T_A = +70°C)
28-Pin TQFN (derate 34.5mW/°C above +70°C)...2758.6mW
30-Bump WLP (derate 24.3mW/°C
above +70°C).....1945.5mW
Operating Temperature Range.....0°C to +70°C
Junction Temperature.....+150°C
Storage Temperature Range.....-65ºC to +150°C
Lead Temperature (Soldering, 10sec).....+300°C
Soldering Temperature (reflow).....+260°C

Package Thermal Characteristics (Note 1)

TQFN
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....29°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....2°C/W

WLP
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....44°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V_{DVDD} = V_{AVDD} = +1.1V to +2.0V, V_{OVDD} = +1.65V to +3.6V, f_{FCLK} = 32.768kHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DVDD} = V_{AVDD} = +1.8V, V_{OVDD} = +2.5V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ECG CHANNEL						
AC Differential Input Range		V_{AVDD} = +1.1V, THD < 0.3%	-15		+15	mV_{p-p}
		V_{AVDD} = +1.8V, THD < 0.3%		±32.5		
DC Differential Input Range		V_{AVDD} = +1.1V, shift from nominal gain < 2%	-300		+300	mV
		V_{AVDD} = +1.8V		±650		
Common Mode Input Range		V_{AVDD} = +1.1V, from V_{MID}, shift from nominal gain < 2%	-150		+150	mV
		V_{AVDD} = +1.8V, from V_{MID}, shift from nominal gain < 2%		±550		
Common Mode Rejection Ratio	CMRR	0Ω source impedance, f = 64Hz (Note 3)	105	115		dB
		(Note 4)		77		
ECG Channel Input Referred Noise		BW = 0.05 - 150Hz, G_{CH} = 20x		0.82		μV_{RMS}
				5.4		μV_{p-p}
		BW = 0.05 - 40Hz, G_{CH} = 20x (Note 3)		0.53	1.0	μV_{RMS}
				3.5	6.6	μV_{p-p}
Input Leakage Current		T_A = +25°C	-1	0.1	+1	nA
Input Impedance (INA)		Common-mode, DC		45		GΩ
		Differential, DC		1500		MΩ

Electrical Characteristics (continued)

(V_{DVDD} = V_{AVDD} = +1.1V to +2.0V, V_{OVDD} = +1.65V to +3.6V, f_{FCLK} = 32.768kHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DVDD} = V_{AVDD} = +1.8V, V_{OVDD} = +2.5V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ECG Channel Total Harmonic Distortion	THD	V_{AVDD} = +1.80V, V_{IN} = 65mV_{p-p}, F_{IN} = 64Hz, G_{CH} = 20x, electrode offset = ±300mV			0.025		%
		V_{AVDD} = +1.1V, V_{IN} = 30mV_{p-p}, F_{IN} = 64Hz, G_{CH} = 20x, electrode offset = ±300mV				0.3	
ECG Channel Gain Setting	G_{CH}	Programmable, see register map			20 to 160		V/V
ECG Channel Gain Error		V_{AVDD} = +1.8V, G_{CH} = 20x, ECGP = ECGN = VMID		-2.5		+2.5	%
		V_{AVDD} = +1.1V, G_{CH} = 20x, ECGP = ECGN = VMID		-4.5		+4.5	%
ECG Channel Offset Error		(Note 5)			0.1		% of FSR
ADC Resolution					18		Bits
ADC Sample Rate		Programmable, see register map			125 to 512		SPS
CAPP to CAPN Impedance	R_{HPF}	FHP = 1/(2R x R_{HPF} x C_{HPF}), C_{HPF} = capacitance between CAPP and CAPN		320	450	600	kΩ
Analog High-Pass Filter Slew Current		Fast recovery enabled (1.8V)			160		µA
		Fast recovery enabled (1.1V)			55		
		Fast recovery disabled			0.09		
Fast Settling Recovery Time		C_{HPF} = 10µF, Note: varies by sample rate, see Table 3.			500		ms
Digital Low-Pass Filter		Linear phase FIR filter.	DLPF[0:1] = 01		40		Hz
			DLPF[0:1] = 10		100		
			DLPF[0:1] = 11		150		
Digital High-Pass Filter		Phase-corrected 1st-order IIR filter. DHPF = 1			0.5		Hz
ECG Power Supply Rejection	PSRR	Lead bias disabled, DC			107		dB
		Lead bias disabled, f_{SW} = 64Hz			110		
ECG INPUT MUX							
DC Lead Off Check		Pullup/ pulldown	DCLOFF_IMAG[2:0] = 001		5		nA
			DCLOFF_IMAG[2:0] = 010		10		
			DCLOFF_IMAG[2:0] = 011		20		
			DCLOFF_IMAG[2:0] = 100		50		
			DCLOFF_IMAG[2:0] = 101		100		

Electrical Characteristics (continued)

(V_{DVDD} = V_{AVDD} = +1.1V to +2.0V, V_{OVDD} = +1.65V to +3.6V, f_{FCLK} = 32.768kHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DVDD} = V_{AVDD} = +1.8V, V_{OVDD} = +2.5V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC Lead Off Comparator Low Threshold		DCLOFF_VTH[1:0] = 11 (Note 6)			V_{MID} - 0.50		V
		DCLOFF_VTH[1:0] = 10 (Note 7)			V_{MID} - 0.45		
		DCLOFF_VTH[1:0] = 01 (Note 8)			V_{MID} - 0.40		
		DCLOFF_VTH[1:0] = 00			V_{MID} - 0.30		
DC Lead Off Comparator High Threshold		DCLOFF_VTH[1:0] = 11 (Note 6)			V_{MID} + 0.50		V
		DCLOFF_VTH[1:0] = 10 (Note 7)			V_{MID} + 0.45		
		DCLOFF_VTH[1:0] = 01 (Note 8)			V_{MID} + 0.40		
		DCLOFF_VTH[1:0] = 00			V_{MID} + 0.30		
Lead Bias Impedance		Lead bias enabled	RBIASV[1:0] = 00		50		MΩ
			RBIASV[1:0] = 01		100		
			RBIASV[1:0] = 10		200		
Lead Bias Voltage	V_{MID}	Lead bias enabled			V_{AVDD}/ 2.15		V
Calibration Voltage Magnitude		Single-ended	VMAG = 0		0.25		mV
			VMAG = 1		0.50		
Calibration Voltage Magnitude Error		Single-ended (Note 9)		-2		+2	%
Calibration Voltage Frequency		Programmable, see register map			0.0156 to 256		Hz
Calibration Voltage Pulse Time		Programmable, see register map	FIFTY = 0		0.03052 to 62.474		ms
			FIFTY = 1		50		%
INTERNAL REFERENCE/COMMON-MODE							
V_{BG} Output Voltage	V_{BG}				0.650		V
V_{BG} Output Impedance					100		kΩ
External V_{BG} Compensation Capacitor	C_{VBG}			1			µF
V_{REF} Output Voltage	V_{REF}	T_A = +25°C		0.995	1.000	1.005	V
V_{REF} Temperature Coefficient	TC_{REF}	T_A = 0°C to +70°C			10		ppm/°C
V_{REF} Buffer Line Regulation					330		µV/V
V_{REF} Buffer Load Regulation		I_{LOAD} = 0 to 100µA			25		µV/µA

Electrical Characteristics (continued)

(V_{DVDD} = V_{AVDD} = +1.1V to +2.0V, V_{OVDD} = +1.65V to +3.6V, f_{FCLK} = 32.768kHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DVDD} = V_{AVDD} = +1.8V, V_{OVDD} = +2.5V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
External V_{REF} Compensation Capacitor	C_{REF}			1	10		µF
V_{CM} Output Voltage	V_{CM}				0.650		V
External V_{CM} Compensation Capacitor	C_{CM}			1	10		µF
DIGITAL INPUTS (SDI, SCLK, CSB, FCLK)							
Input-Voltage High	V_{IH}			0.7 × V_{OVDD}			V
Input-Voltage Low	V_{IL}					0.3 × V_{OVDD}	V
Input Hysteresis	V_{HYS}				0.05 × V_{OVDD}		V
Input Capacitance	C_{IN}				10		pF
Input Current	I_{IN}			-1		+1	µA
DIGITAL OUTPUTS (SDO, INTB, INT2B)							
Output Voltage High	V_{OH}	I_{SOURCE} = 1mA		V_{OVDD} – 0.04			V
Output Voltage Low	V_{OL}	I_{SINK} = 1mA				0.4	V
Three-State Leakage Current				-1		+1	µA
Three-State Output Capacitance					15		pF
POWER SUPPLY							
Analog Supply Voltage	V_{AVDD}	Connect V_{AVDD} to V_{DVDD}		1.1		2.0	V
Digital Supply Voltage	V_{DVDD}	Connect V_{DVDD} to V_{AVDD}		1.1		2.0	V
Interface Supply Voltage	V_{OVDD}	Power for I/O drivers only		1.65		3.6	V
Supply Current	I_{AVDD} + I_{DVDD}	ECG channel	V_{AVDD} = V_{DVDD} = +1.1V		76		µA
			V_{AVDD} = V_{DVDD} = +1.8V		100		
			V_{AVDD} = V_{DVDD} = +2.0V		109	120	
		ULP Lead On Detect	T_A = +70°C		0.98		
			T_A = +25°C		0.73	2.5	
Interface Supply Current	I_{OVDD}	V_{OVDD} = +1.65V, ECG channel at 512sps (Note 10)			0.2		µA
		V_{OVDD} = +3.6V, ECG channel at 512sps (Note 10)			0.6	1.6	

Electrical Characteristics (continued)

(V_{DVDD} = V_{AVDD} = +1.1V to +2.0V, V_{OVDD} = +1.65V to +3.6V, f_{FCLK} = 32.768kHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DVDD} = V_{AVDD} = +1.8V, V_{OVDD} = +2.5V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Shutdown Current	I_{SAVDD} + I_{SDVDD}	V_{AVDD} = V_{DVDD} = 2.0V (Note 5)	T_A = +70°C		0.79		µA
			T_A = +25°C		0.51	2.5	
	I_{SOVDD}	V_{OVDD} = +3.6V, V_{AVDD} = V_{DVDD} = +2.0V				1.1	
ESD PROTECTION							
ECGP, ECGN		IEC61000-4-2 Contact Discharge (Note 11)		±8			kV
		IEC61000-4-2 Air-Gap Discharge (Note 11)		±15			
		HMM		±8			

Timing Characteristics

(V_{DVDD} = V_{AVDD} = +1.1V to +2.0V, V_{OVDD} = +1.65V to +3.6V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DVDD} = +1.8V, V_{OVDD} = +2.5V, T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TIMING CHARACTERISTICS						
SCLK Frequency	f_{SCLK}		0		12	MHz
SCLK Period	t_{CP}		83			ns
SCLK Pulse Width High	t_{CH}		15			ns
SCLK Pulse Width Low	t_{CL}		15			ns
CSB Fall to SCLK Rise Setup Time	t_{CSS0}	To 1st SCLK rising edge (RE)	15			ns
CSB Fall to SCLK Rise Hold Time	t_{CSH0}	Applies to inactive RE preceding 1st RE	0			ns
CSB Rise to SCLK Rise Hold Time	t_{CSH1}	Applies to 32nd RE, executed write	10			ns
CSB Rise to SCLK Rise	t_{CSA}	Applies to 32nd RE, aborted write sequence	15			ns
SCLK Rise to CSB Fall	t_{CSF}	Applies to 32nd RE	100			ns
CSB Pulse-Width High	t_{CSPW}		20			ns
SDI-to-SCLK Rise Setup Time	t_{DS}		8			ns
SDI to SCLK Rise Hold Time	t_{DH}		8			ns
SCLK Fall to SDO Transition	t_{DOT}	C_{LOAD} = 20pf			40	ns
		C_{LOAD} = 20pf, V_{AVDD} = V_{DVDD} ≥ 1.8V, V_{DVDD} ≥ 2.5V			20	ns
SCLK Fall to SDO Hold	t_{DOH}	C_{LOAD} = 20pf	2			ns

Timing Characteristics (continued)

(V_{DVDD} = V_{AVDD} = +1.1V to +2.0V, V_{OVDD} = +1.65V to +3.6V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DVDD} = +1.8V, V_{OVDD} = +2.5V, T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CSB Fall to SDO Fall	t_{DOE}	Enable time, C_{LOAD} = 20pf			30	ns
CSB Rise to SDO Hi-Z	t_{DOZ}	Disable time			35	ns
FCLK Frequency	f_{FCLK}	External reference clock		32.768		kHz
FCLK Period	t_{FP}			30.52		µs
FCLK Pulse-Width High	t_{FH}	50% duty cycle assumed		15.26		µs
FCLK Pulse-Width Low	t_{FL}	50% duty cycle assumed		15.26		µs

Note 2: Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.
Note 3: Guaranteed by design and characterization. Not tested in production.
Note 4: One electrode drive with <10Ω source impedance, the other driven with 51kΩ in parallel with a 47nF per IEC60601-2-47.
Note 5: Inputs connected to 51kΩ in parallel with a 47nF to V_{CM}.
Note 6: Use this setting only for V_{AVDD} = V_{DVDD} ≥ 1.65V.
Note 7: Use this setting only for V_{AVDD} = V_{DVDD} ≥ 1.55V.
Note 8: Use this setting only for V_{AVDD} = V_{DVDD} ≥ 1.45V.
Note 9: This specification defines the accuracy of the calibration voltage source as applied to the ECG input, not as measured through the ADC channel.
Note 10: f_{SCLK} = 4MHz, burst mode, EFIT = 8, C_{SDO} = C_{INTB} = 50pF.
Note 11: ESD test performed with 1kΩ series resistor designed to withstand 8kV surge voltage.

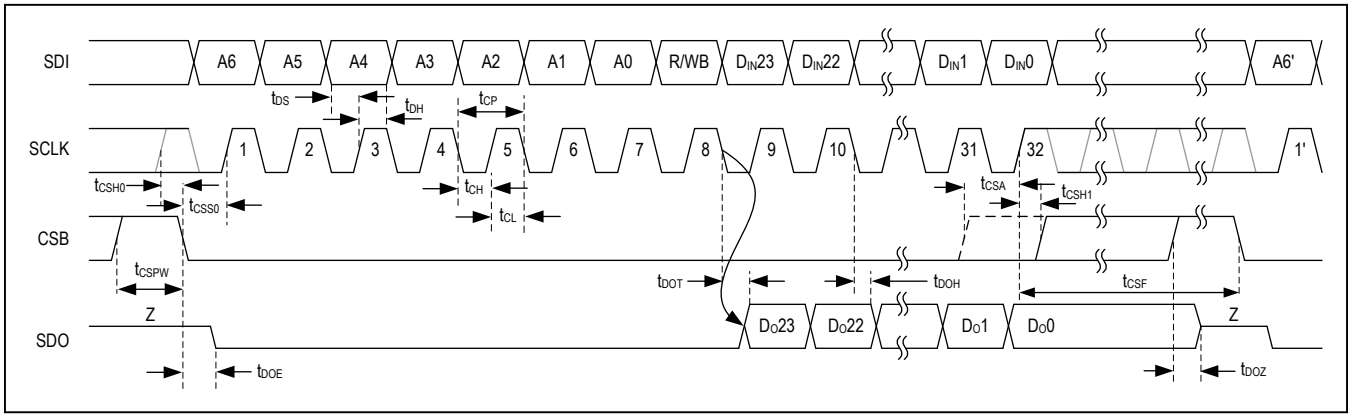


Figure 1a. SPI Timing Diagram

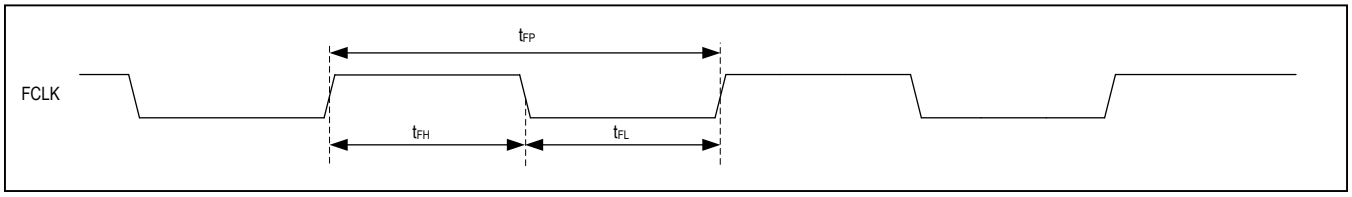
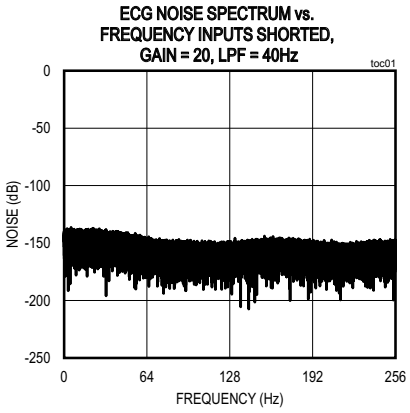
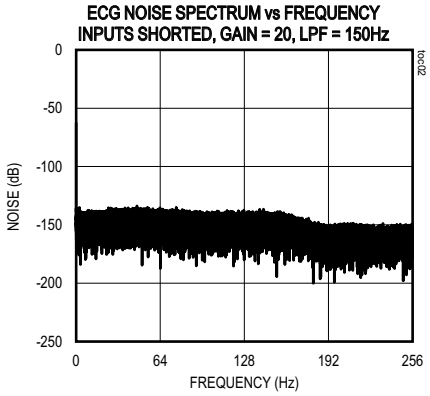


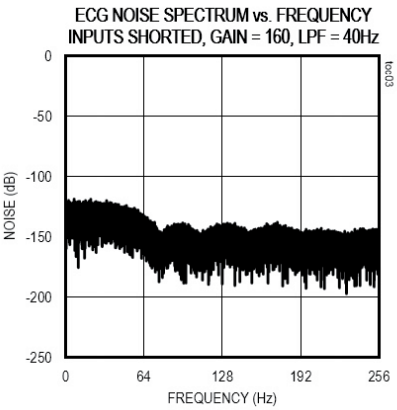
Figure 1b. FCLK Timing Diagram

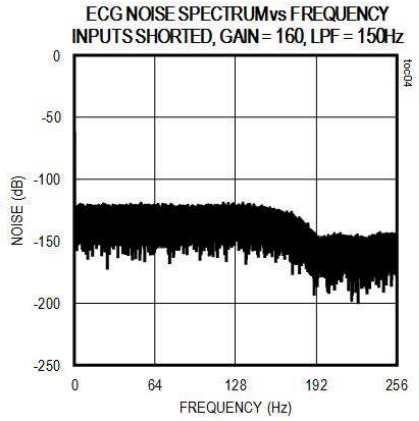
Typical Operating Characteristics

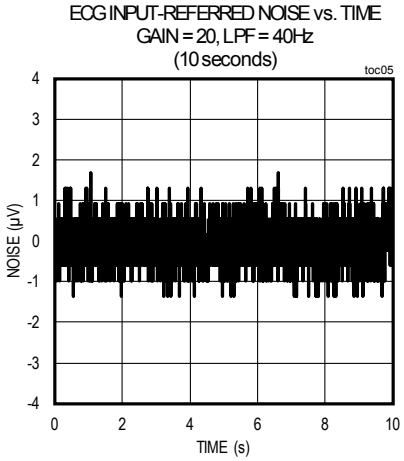
(V_{DVDD} = V_{AVDD} = +1.8V, V_{OVDD} = 2.5V, T_A = +25°C, unless otherwise noted.)

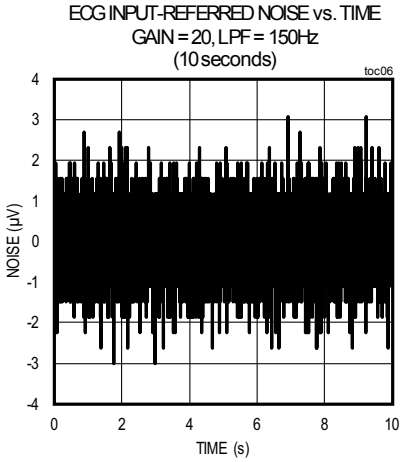


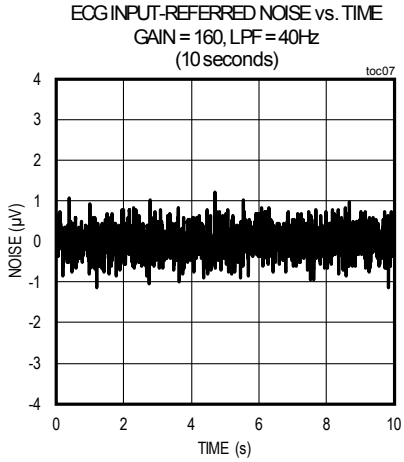






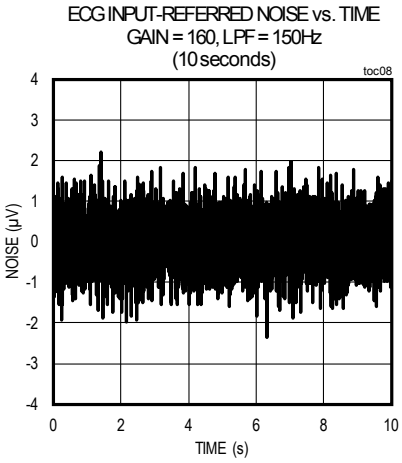


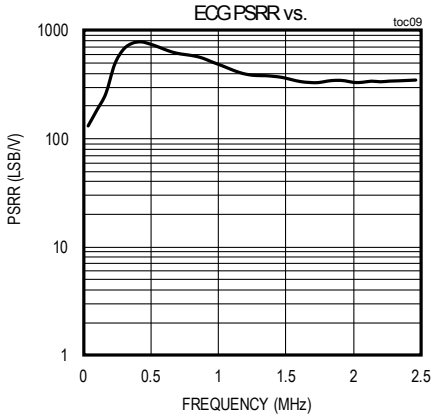


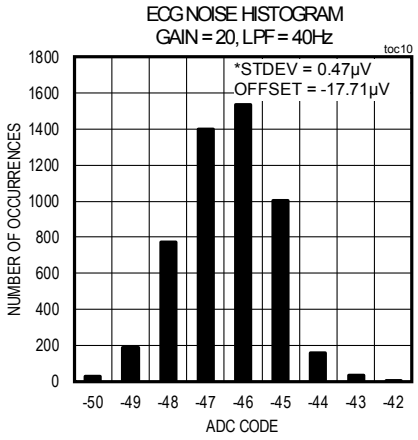


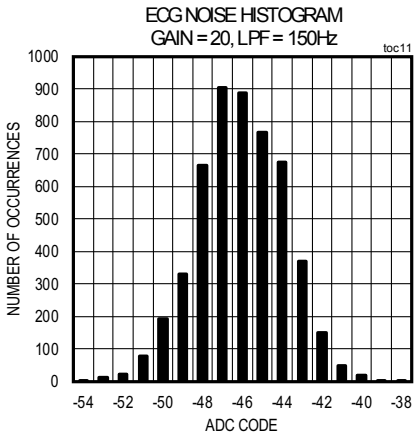
Typical Operating Characteristics (continued)

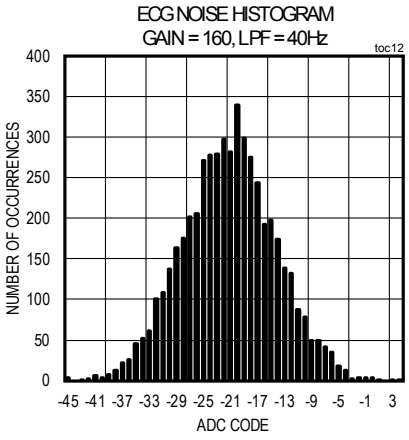
(V_{DVDD} = V_{AVDD} = +1.8V, V_{OVDD} = 2.5V, T_A = +25°C, unless otherwise noted.)

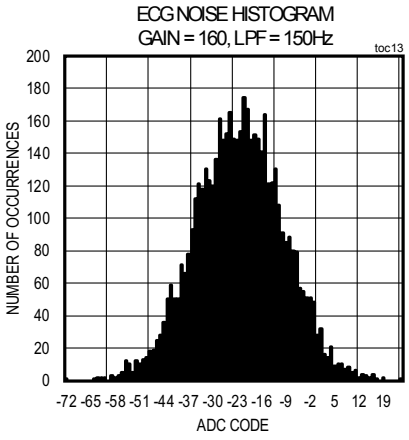








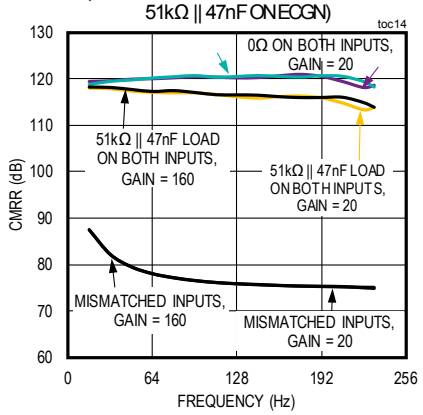




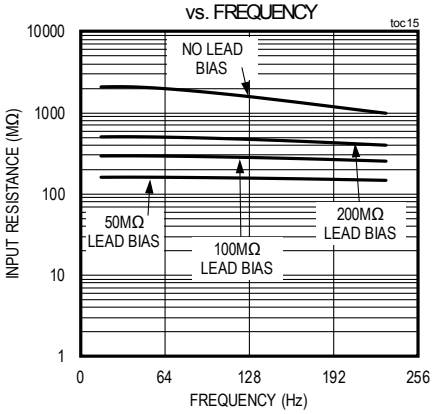
Typical Operating Characteristics (continued)

(V_{DVDD} = V_{AVDD} = +1.8V, V_{OVDD} = 2.5V, T_A = +25°C, unless otherwise noted.)

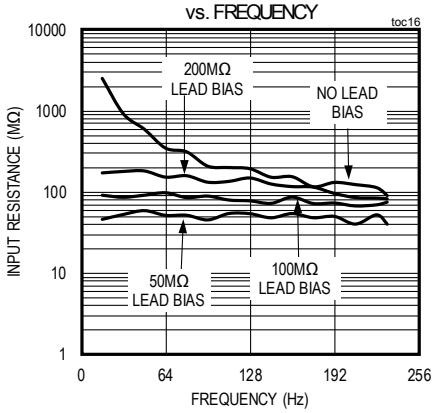
ECG CMRR vs. FREQUENCY
(MISMATCHED LOAD IS 0Ω ON ECGP, 51kΩ || 47nF ON ECGN)



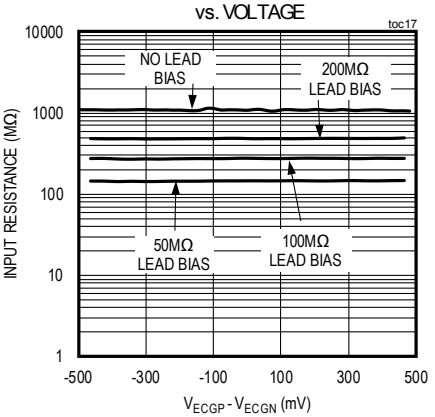
DIFFERENTIAL INPUT RESISTANCE vs. FREQUENCY



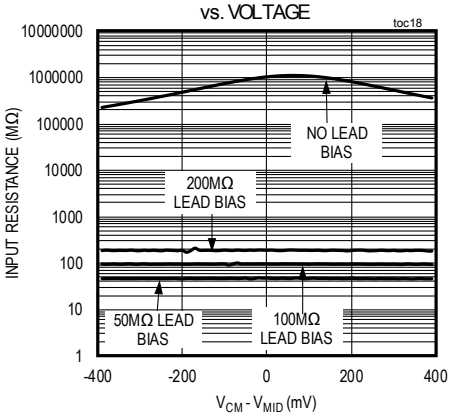
COMMON-MODE INPUT RESISTANCE vs. FREQUENCY



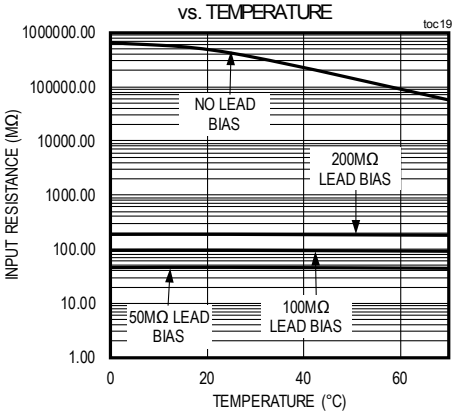
DIFFERENTIAL INPUT RESISTANCE vs. VOLTAGE



COMMON-MODE INPUT RESISTANCE vs. VOLTAGE

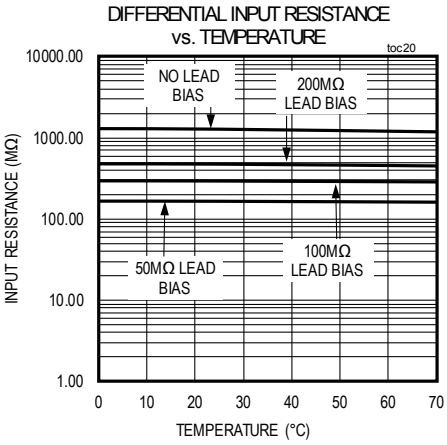


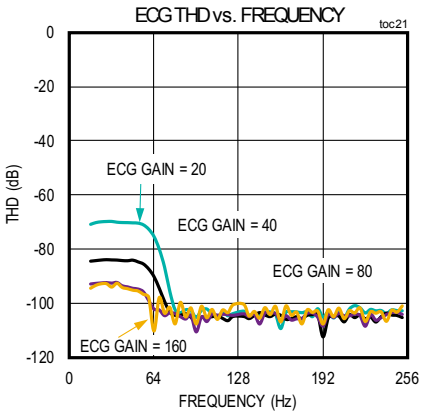
COMMON-MODE INPUT RESISTANCE vs. TEMPERATURE

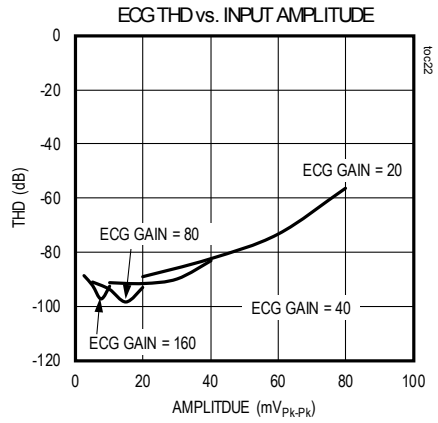


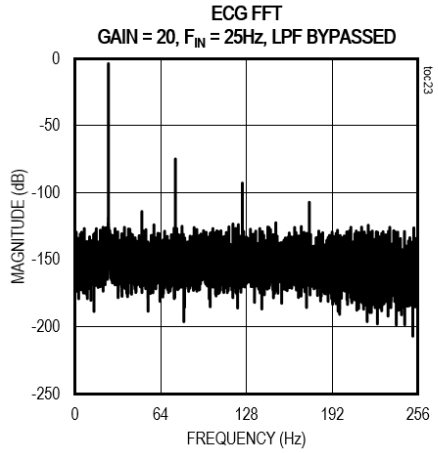
Typical Operating Characteristics (continued)

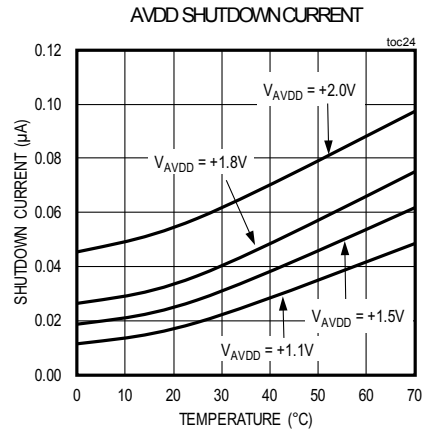
(V_{DVDD} = V_{AVDD} = +1.8V, V_{OVDD} = 2.5V, T_A = +25°C, unless otherwise noted.)

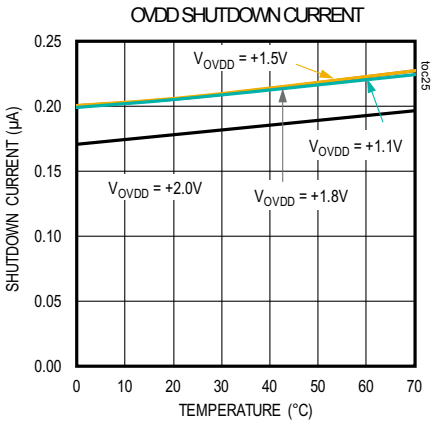




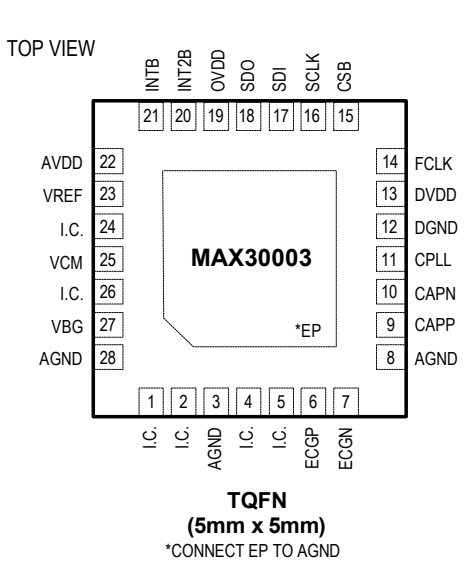




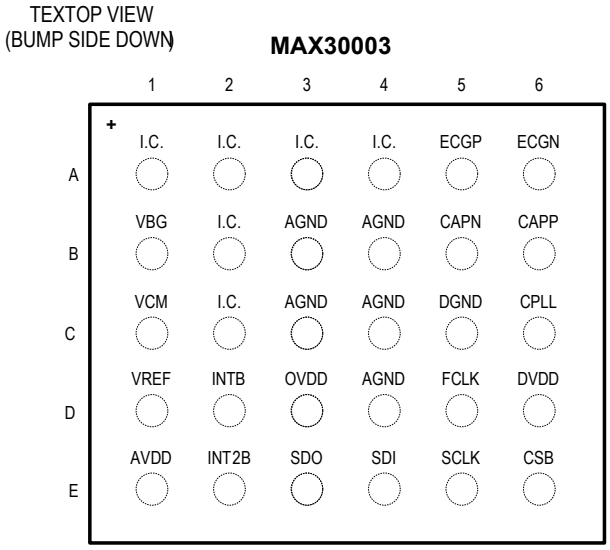




Pin Configurations



TQFN
(5mm x 5mm)
*CONNECT EP TO AGND



WLP
(2.74mm x 2.9mm)

Pin Description

PIN	BUMP	NAME	FUNCTION
TQFN	WLP		
1, 2, 4, 5, 24, 26	A1, A2, A3, A4, B2, C2	I.C.	Internally Connected. Connect to AGND.
3,8,28	B3, B4, C3, C4, D4	AGND	Analog Power and Reference Ground. Connect into the printed circuit board ground plane.
6	A5	ECGP	ECG Positive Input
7	A6	ECGN	ECG Negative Input
9	B6	CAPP	Analog High-Pass Filter Input. Connect a 1µF X7R capacitor (CHPF) between CAPP and CAPN to form a 0.5Hz high-pass response in the ECG channel.
10	B5	CAPN	Analog High-Pass Filter Input. Connect a 1µF X7R capacitor (CHPF) between CAPP and CAPN to form a 0.5Hz high-pass response in the ECG channel.
11	C6	CPLL	PLL Loop Filter Input. Connect 1nF COG cap between CPLL and AGND.
12	C5	DGND	Digital Ground for Both Digital Core and I/O Pad Drivers. Recommended to connect to AGND plane.
13	D6	DVDD	Digital Core Supply Voltage. Connect to AVDD

Pin Description (continued)

PIN	BUMP	NAME	FUNCTION
TQFN	WLP		
14	D5	FCLK	External 32.768kHz Clock that Controls the Sampling of the Internal Sigma-Delta Converters and Decimator.
15	E6	CSB	Active-Low Chip-Select Input. Enables the serial interface.
16	E5	SCLK	Serial Clock Input. Clocks data in and out of the serial interface when CSB is low.
17	E4	SDI	Serial Data Input. SDI is sampled into the device on the rising edge of SCLK when CSB is low.
18	E3	SDO	Serial Data Output. SDO will change state on the falling edge of SCLK when CSB is low. SDO is three-stated when CSB is high.
19	D3	OVDD	Logic Interface Supply Voltage
20	E2	INT2B	Interrupt 2 Output. INT2B is an active-low status output. It can be used to interrupt an external device.
21	D2	INTB	Interrupt Output. INTB is an active low status output. It can be used to interrupt an external device.
22	E1	AVDD	Analog Core Supply Voltage. Connect to DVDD.
23	D1	V_{REF}	ADC Reference Buffer Output. Connect a 10µF X5R ceramic capacitor between V_{REF} and AGND.
25	C1	V_{CM}	Common Mode Buffer Output. Connect a 10µF X5R ceramic capacitor between V_{CM} and AGND.
27	B1	V_{BG}	Bandgap Noise Filter Output. Connect a 1.0µF X7R ceramic capacitor between V_{BG} and AGND.
EP	—	—	Exposed Paddle. Connect to AGND.

Detailed Description

ECG Channel

Figure 2 illustrates the ECG channel block diagram, excluding the ADC. The channel comprises an input MUX, a fast-recovering instrumentation amplifier, an anti-alias filter, and a programmable gain amplifier. The MUX includes several features such as ESD protection, EMI filtering, lead biasing, leads off checking, and ultra-low power leads-on checking. The output of this analog channel drives a high-resolution ADC.

Input MUX

The ECG input MUX shown in Figure 3 contains integrated ESD and EMI protection, DC leads off detect current sources, lead-on detect, series isolation switches, lead biasing, and a programmable calibration voltage source to enable channel built in self-test.

EMI Filtering and ESD Protection

EMI filtering of the ECGP and ECGN inputs consists of a single pole, low pass, differential, and common mode filter with the pole located at approximately 2MHz. The ECGP and ECGN inputs also have input clamps that protect the inputs from ESD events.

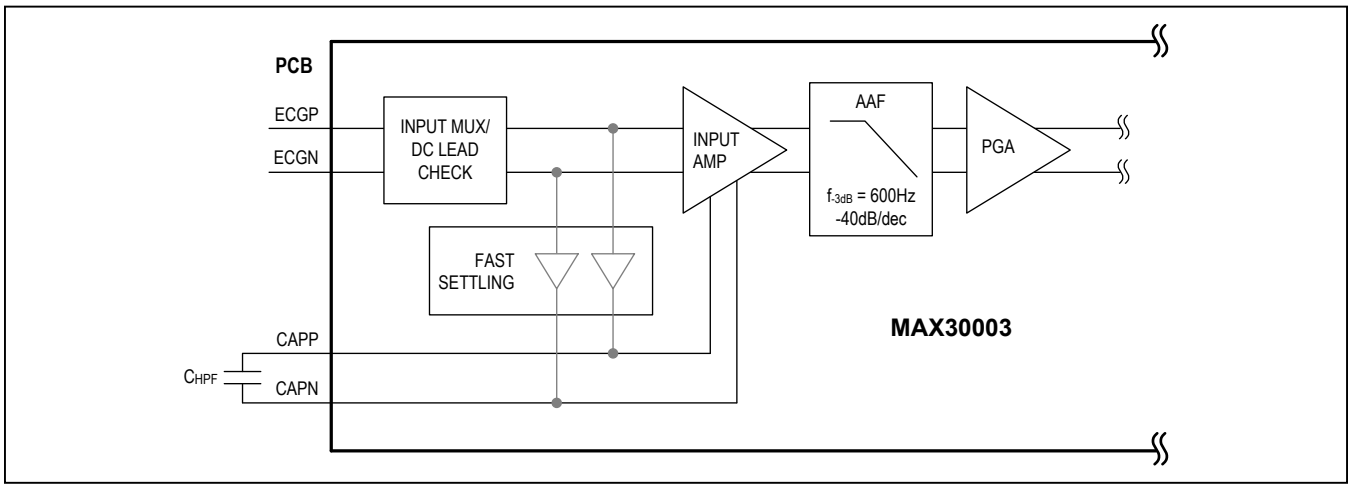


Figure 2. ECG Channel Input Amplifier and PGA Excluding the ADC

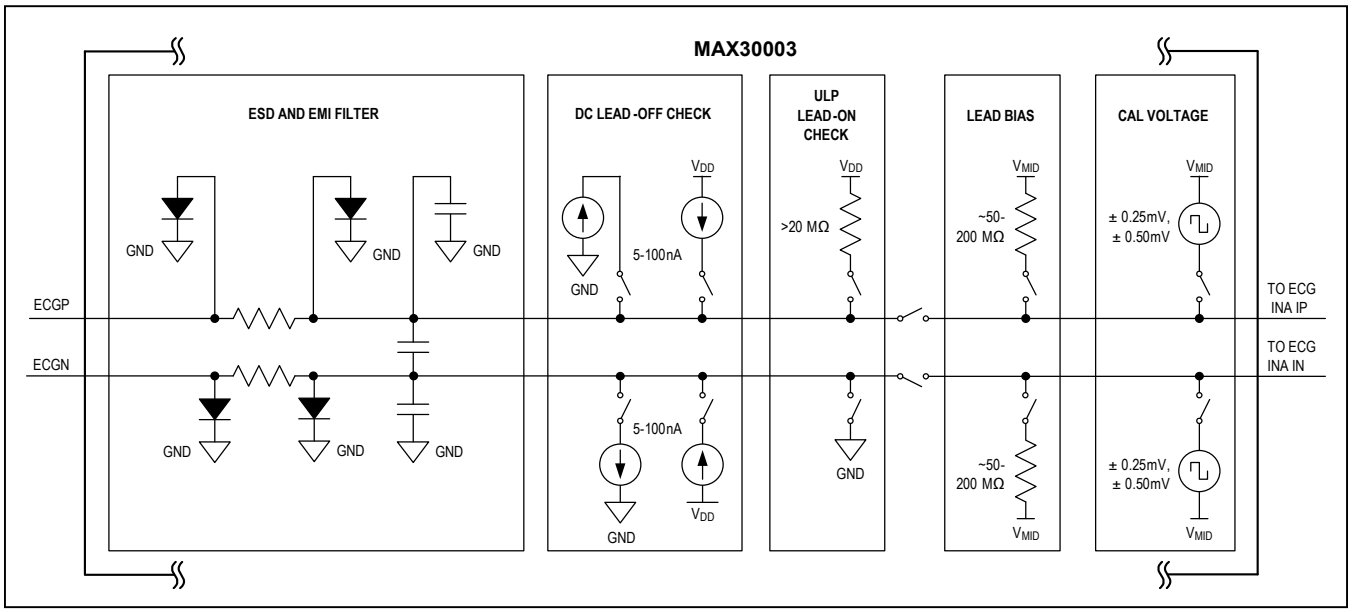


Figure 3. ECG Input MUX

- ±8kV using the Contact Discharge method specified in IEC61000-4-2 ESD
- ±15kV using the Air Gap Discharge method specified in IEC61000-4-2 ESD
- ±8kV HBM
- For IEC61000-4-2 ESD protection, use 1kΩ series resistors on ECGP and ECGN that is rated to withstand 8kV surge voltages.

DC Leads-Off Detection and ULP Leads-On Detection

The input MUX leads-off detect circuitry consists of programmable sink/source DC current sources that allow for DC leads-off detection, while the channel is powered up in normal operation and an ultra-low-power (ULP) leads-on detect while the channel is powered-down.

The MAX30003 accomplishes DC leads-off detection by applying a DC current to pull the ECG input voltage up to above V_{MID} + V_{TH} or down to below V_{MID} - V_{TH}. The current sources have user selectable values of 0nA, 5nA, 10nA, 20nA, 50nA, and 100nA that allow coverage of dry and wet electrode impedance ranges. Supported thresholds are V_{MID} ± 0.30V (recommended), V_{MID} ± 0.40V, V_{MID} ± 0.45V, and V_{MID} ± 0.50V. A threshold of 400mV, 450mV, and 500mV should only be used when V_{AVDD} ≥ 1.45V, 1.55V, and 1.65V, respectively. A dynamic comparator protects against false flags generated by the input amplifier and input chopping. The comparator checks for a minimum continuous violation (or threshold exceeded) of 115ms to 140ms depending on the setting of FMSTR[1:0] before asserting any one of the LDOFF_* interrupt flags (Figure 4). See registers CNFG_GEN (0x10) and CNFG_EMUX 0x14) for configuration settings and see Table 1 for recommended values given electrode type and supply voltage.

The ULP lead on detect operates by pulling ECGN low with a pulldown resistance larger than 5mΩ and pulling ECGP high with a pullup resistance larger than 15MΩ. A low-power comparator determines if ECGP is pulled below a predefined threshold that occurs when both electrodes make contact with the body. When the impedance between ECGP and ECGN is less than 20mΩ, an interrupt LONINT is asserted, alerting the µC to a leads-on condition.

A 0nA/V_{MID} ± 300mV selection is available allowing monitoring of the input compliance of the INA during non-DC lead-off checks.

Lead Bias

The MAX30003 limits the ECGP and ECGN DC input common mode range to V_{MID} ±150mV. This range can be maintained either through external/internal lead-biasing.

Internal DC lead-biasing consists of 50MΩ, 100MΩ, or 200MΩ selectable resistors to V_{MID} that drive the electrodes within the input common mode requirements of the ECG channel and can drive the connected body to the proper common mode voltage level. See register CNFG_GEN (0x10) to select a configuration.

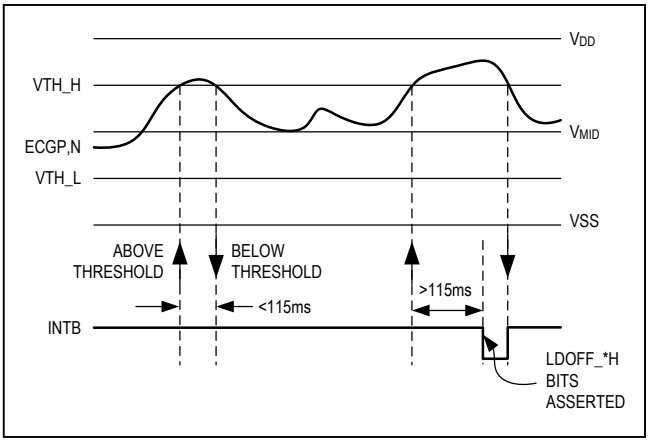


Figure 4. Lead-Off Detect Behavior

Isolation Switches

The series switches in the MAX30003 isolate ECGP and ECGN pins (subject) from the internal signal path. the series switches are disabled by default. They must be enabled to record ECG.

Calibration Voltage Sources

Calibration voltage sources are available to provide ±0.25mV (0.5mV_{P-P}) or ±0.5mV (1.0mV_{P-P}) inputs to the ECG channel with programmable frequency and duty cycle. The sources can be unipolar/bipolar relative to V_{MID}.

Figure 5 illustrates the possible calibration waveforms. Frequency selections are available in 4X increments from 15.625mHz to 256Hz with selected pulse widths varying from 30.5µs to 31.723ms and 50% duty cycle. Signals can be single-ended, differential, or common mode. This flexibility allows end-to-end channel-testing of the ECG signal path.

When applying calibration voltage sources with the device connected to a subject, the series input switches must be disconnected so as not to drive signals into the subject. See registers CNFG_CAL (0x12) and CNFG_EMUX (0x14) to select configuration.

Table 1. Recommended Lead Bias, Current Source Values, and Thresholds for Electrode Impedance

I_{DC} V_{TH}	ELECTRODES IMPEDANCE							
	<100kΩ	**100kΩ - 200kΩ**	**200kΩ - 400kΩ**	**400kΩ - 1MΩ**	**1MΩ - 2MΩ**	**2MΩ - 4 MΩ**	**4MΩ - 10MΩ**	**10MΩ - 20MΩ**
I_{DC} = 10nA	All settings of R_b $V_{TH} = V_{MID}$ ± 300mV, ± 400mV							
I_{DC} = 20nA	All settings of R_b All settings of V_{TH}							All settings of R_b $V_{TH} = V_{MID}$ ± 400mV, ± 450mV, ± 500mV
I_{DC} = 50nA	All settings of R_b All settings of V_{TH}						All settings of R_b $V_{TH} = V_{MID}$ ± 450mV, ± 500mV	
I_{DC} = 100nA	All settings of R_b All settings of V_{TH}					All settings of Rb $V_{TH} = V_{MID}$ ± 400mV, ± 450mV, ± 500mV		

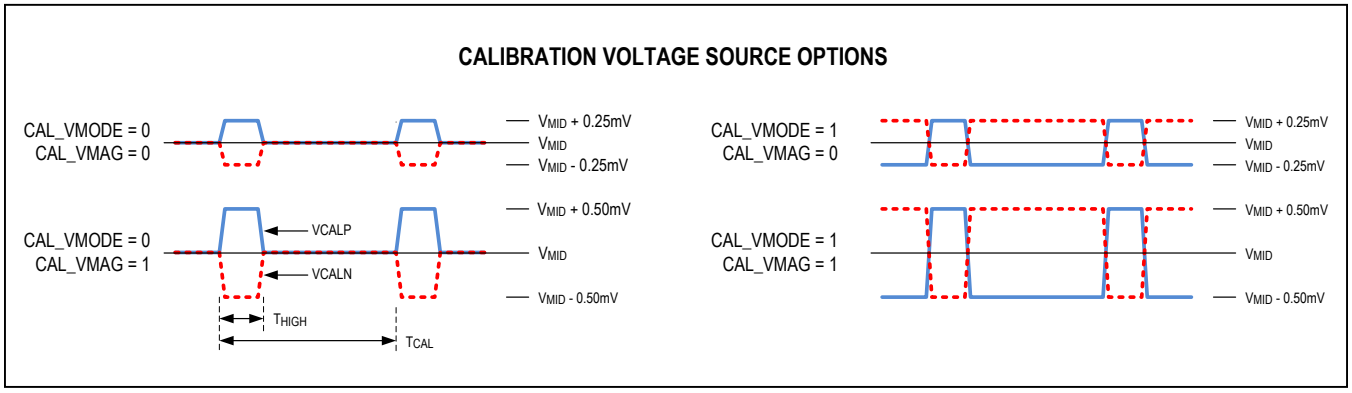


Figure 5. Calibration Voltage Source Options

Gain Settings and Input Range

The device's ECG channel contains an input instrumentation amplifier that provides low-noise, fixed-gain amplification of the differential signal, rejects differential DC voltage due to electrode polarization, rejects common-mode interference primarily due to AC mains interference, and provides high input impedance to guarantee high CMRR even in the presence of severe electrode impedance mismatch (see Figure 2). The differential DC rejection corner frequency is set by an external capacitor (C_{HPF}) placed between pins CAPP and CAPN, refer to Table 2 for appropriate value selection. There are three recommended options for the cutoff frequency: 4.4Hz, 0.4Hz, and 0.04Hz. Setting the cutoff frequency to 4.4Hz provides the most motion artifact rejection at the expense of ECG waveform quality, making it best suited for heart rate monitoring. For ambulatory applications requiring more robust ECG waveforms with moderate motion artifact rejection, 0.4Hz is recommended. Select 0.04Hz for patient monitoring applications in which ECG waveform quality is the primary concern and poor rejection of motion artifacts can be tolerated. The high-pass corner frequency is calculated by the following equation:

$1/(2r \times R_{HPF} \times C_{HPF})$

RHPF is specified in the Electrical Characteristics table.

Following the instrumentation amplifier is a 2-pole active anti-aliasing filter with a 600Hz -3dB frequency that provides 57dB of attenuation at half the modulator sampling rate (approximately 16kHz) and a PGA with programmable gains of 1, 2, 4, and 8V/V for an overall gain of 20, 40, 80, and 160V/V. The instrumentation amplifier and PGA are chopped to minimize offset and 1/f noise. Gain settings are configured via the CNFG_ECG (0x15) register. The useable common-mode range is V_{MID} ±150mV, internal lead biasing can be used to meet this requirement. The useable DC differential range is ±300mV to allow for electrode polarization voltages on each electrode. The input AC differential range is ±32.5mV or ±65mV_{P-P}.

Fast Recovery Mode

The input instrumentation amplifier has the ability to rapidly recover from an excessive overdrive event such as a defibrillation pulse, high-voltage external pacing, and electro-surgery interference. There are two modes of recovery that can be used: automatic or manual recovery. The mode is programmed by the FAST[1:0] bits in the MNGR_DYN (0x05) register.

Automatic mode engages once the saturation counter exceeds approximately 125ms (t_{SAT}). The counter is activated the first time the ADC output exceeds the symmetrical threshold defined by the FAST_TH[5:0] bits in the MNGR_DYN (0x05) register and accumulates the time that the ADC output exceeds either the positive or negative threshold. If the saturation counter exceeds 125ms, it triggers the fast settling mode (if enabled) and resets. The saturation counter can also be reset prior to triggering the fast settling mode if the ADC output falls below the threshold continuously for 125ms (t_{BLW}). This feature is designed to avoid false triggers due to the QRS complex. Once triggered, fast settling mode will be engaged for 500ms, see Figure 6. ECG samples are tagged if they were taken while fast settling mode was asserted.

In manual mode, a user algorithm running on the host microcontroller or an external stimulus input will generate the trigger to enter fast recovery mode. The host microcontroller then enables the manual fast recovery mode in the MNGR_DYN (0x05) register. The manual fast recovery mode can be of a much shorter duration than the automatic mode and allows for more rapid recovery. One such example is recovery from external high-voltage pacing signals in a few milliseconds to allow the observation of a subsequent p-wave.

Table 2. ECG Analog HPF Corner Frequency Selection

C_{HPF}	HPF CORNER FREQUENCY
0.1µ	≤ 5Hz
1.0µ	≤ 0.5Hz
10µ	≤ 0.05Hz

Table 3. Fast Recovery Mode Recovery Time vs. Number of Samples

SAMPLE RATE (sps)	NUMBER OF SAMPLES	RECOVERY TIME (APPROXIMATE) (ms)
512	255	498
256	127	496
128	63	492
500	249	498
250	124	496
125	64	512
200	99	495
199.8	99	495.5

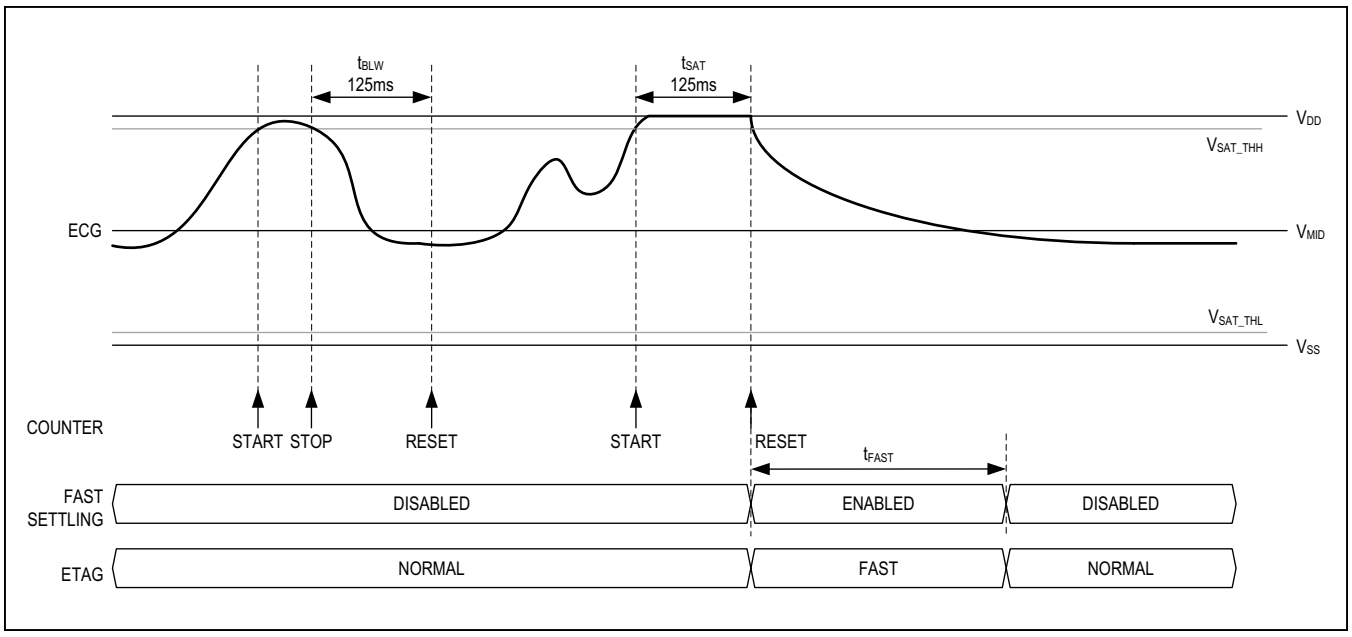


Figure 6. Automatic Fast Settling Behavior

Decimation Filter

The decimation filter consists of a Cascaded Integrator Comb (CIC) decimation filter to the data rate followed by a programmable FIR filter to implement HPF and LPF selections.

The high-pass filter options include a 1st-order IIR Butterworth filter with a 0.4Hz corner frequency along with a pass through setting for DC coupling. Low-pass filter options include a 12-tap linear phase (constant group delay) FIR filter with 40Hz, 100Hz, or 150Hz corner frequencies. See register CNFG_ECG (0x15) to configure the filters. Table 4 illustrates the ECG latency in samples and time for each ADC data rate.

Table 4. ECG Latency in Samples and Time as a Function of ECG Data Rate and Decimation

ECG CHANNEL SETTINGS			LATENCY			
INPUT SAMPLE RATE (Hz)	OUTPUT DATA RATE (sps)	DECIMATION RATIO	WITHOUT LFP (INPUT SAMPLES)	WITH LPF (INPUT SAMPLES)	WITHOUT LFP (ms)	WITH LPF (ms)
32,768	512	64	650	1,034	19.836	31.555
32,000	500	64	650	1,034	20.313	32.313
32,768	256	128	2,922	3,690	89.172	112.610
32,000	250	128	2,922	3,690	91.313	115.313
32,000	200	160	1,242	2,202	38.813	68.813
31,968	199.8	160	1,242	2,202	38.851	68.881
32,768	128	256	3,370	4,906	102.844	149.719
32,000	125	256	3,370	4,906	105.313	153.313

Noise Measurements

Table 5 shows the noise performance of the ECG channel of MAX30003 referred to the ECG inputs.

R-to-R Detection

The MAX30003 contains built-in hardware to detect R-R intervals using an adaptation of the Pan-Tompkins QRS detection algorithm[1]. The timing resolution of the R-R interval is approximately 8ms and depends on the setting of FMSTR [1:0] in CNFG_GEN (0x10) register. See Table 22 for the timing resolution of each setting.

When an R event is identified, the RRINT status bit is asserted and the RTOR_REG (0x25) register is updated with the count seen since the last R event. Figure 7 illustrates the R-R interval on a QRS complex. Refer to registers CNFG_RTOR1 (0x1D) and CNFG_RTOR2 (0x1E) for selection details.

Table 5. Biopotential (ECG) Channel Noise Performance

GAIN	BANDWIDTH	NOISE		SNR	ENOB
V/V	Hz	μV_{RMS}	μV_{PP}	dB	Bits
20	40	0.53	3.50	96.5	15.7
	100	0.64	4.20	94.9	15.5
	150	0.82	5.44	92.6	15.1
40	40	0.40	2.64	92.9	15.1
	100	0.54	3.56	90.3	14.7
	150	0.66	4.34	88.6	14.4
80	40	0.35	2.31	88.0	14.3
	100	0.50	3.33	84.9	13.8
	150	0.62	4.09	83.1	13.5
160	40	0.34	2.22	82.4	13.4
	100	0.49	3.24	79.1	12.8
	150	0.61	4.01	77.2	12.5

Note: $SNR = 20\log\left(\frac{\square_{\square N}(R\square S)}{\square_N(R\square S)}\right)$, $ENOB = (SNR - 1.76)/6.02$

Note: V_{INP-P} = 100mV, V_{INRMS} = 35.4mV for a gain of 20V/V. The input amplitude is reduced accordingly for high gain settings.

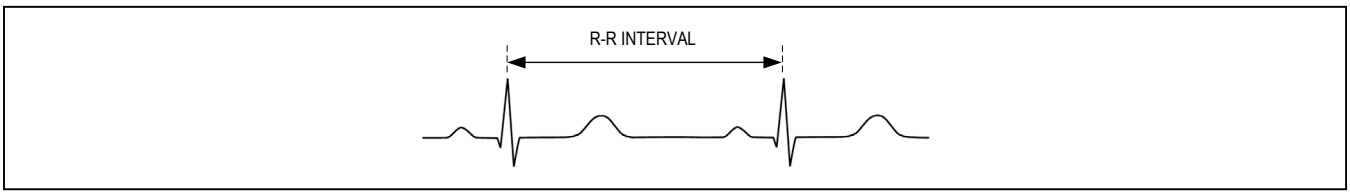


Figure 7. R-to-R Interval Illustration

[1] *J. Pan and W.J. Tompkins, "A Real-Time QRS Detection Algorithm," IEEE Trans. Biomed. Eng., vol. 32, pp. 230-236*

The latency of the R-to-R value written to the RTOR Interval Memory Register is the sum of the R-to-R decimation delay and the R-to-R detection delay blocks. The R-to-R decimation factor is fixed at 256 and the decimation delay (t_{R2R_DEC}) is always 3,370 FMSTR clocks, as shown in Table 6.

The detection circuit consists of several digital filters and signal processing delays. These depend on the WNDW[3:0] bits in the CNFG_RTOR (0x1D) register. The detection delay (t_{R2R_DET}) is described by the following equation:

t_{R2R_DET} = 5,376 + 256 x WNDW in FMSTR clocks where WNDW is an integer from 0 to 15 and the total latency (t_{R2R_DEL}) is the sum of the two delays and summarized in the equation below:

$t_{R2R\_DEL} = t_{R2R\_DEC} + t_{R2R\_DET}$ = 3,370 + 5,376 + 256 x WNDW in FMSTR clocks where WNDW is an integer from 0 to 15.

The total R-to-R latency minus the ECG latency is delay of the R-to-R value relative to the ECG data and can be used to place the first R-to-R value on the ECG data plot. The succeeding values in the R-to-R Interval Memory Register can be used as is to locate subsequent R-to-R values on the ECG data plot relative to the initial placement.

Reference and Common Mode Buffer

The MAX30003 features internally generated reference voltages. The bandgap output (V_{BG}) pin requires an external 1.0µF capacitor to AGND and the reference output (V_{REF}) pin requires a 10µF external capacitor to AGND for compensation and noise filtering.

A common-mode buffer is provided to buffer 650mV which is used to drive common mode voltages for internal blocks. Use a 10µF external capacitor between V_{CM} to AGND to provide compensation and noise filtering.

SPI Interface Description

32 Bit Normal Mode Read/Write Sequences

The MAX30003 interface is SPI/QSPI/Micro-wire/DSP compatible. The operation of the SPI interface is shown in Figure 1. Data is strobed into the MAX30003 on SCLK rising edges. The device is programmed and accessed by a 32 cycle SPI instruction framed by a CSB low interval. The content of the SPI operation consists of a one byte command word (comprised of a seven bit address and a Read/$\overline{\text{Write}}$ mode indicator, i.e., A[6:0] + R/$\overline{\text{W}}$) followed by a three-byte data word. The MAX30003 is compatible with CPOL = 0/CPHA = 0 and CPOL = 1/CPHA = 1 modes of operation.

Write mode operations will be executed on the 32nd SCLK rising edge using the first four bytes of data available. In write mode, any data supplied after the 32nd SCLK rising edge will be ignored. Subsequent writes require CSB to de-assert high and then assert low for the next write command. In order to abort a command sequence, the rise of CSB must precede the updating (32nd) rising-edge of SCLK, meeting the t_{CSA} requirement.

Read mode operations will access the requested data on the 8th SCLK rising edge, and present the MSB of the requested data on the following SCLK falling edge, allowing the µC to sample the data MSB on the 9th SCLK rising edge. Configuration, Status, and FIFO data are all available via normal mode read back sequences. If more than 32 SCLK rising edges are provided in a normal read sequence then the excess edges will be ignored and the device will read back zeros.

Table 6. R to R Decimation Delay in ms and FMSTR CLK vs. Register Settings, FCLK = 32.768Hz

FMSTR [1:0]	FMSTR FREQ IN FCLKs	FMSTR FREQ (Hz)	DECIMATION	RTOR TIME RESOLUTION (ms)	DELAY IN R TO R DECIMATION	
					IN FMSTR CLKs	IN ms
00	FCLK	32,768	256	7.8125	3370	102.844
01	FCLK x 625/640	32,000	256	8.0	3370	105.313
10	FCLK x 625/640	32,000	256	8.0	3370	105.313
11	FCLK x 640/656	31,968.78	256	8.0078	3370	105.415

If accessing the STATUS register or the ECG FIFO memories, all interrupt updates will be made and the internal FIFO read pointer will be incremented in response to the 30th SCLK rising edge, allowing for internal synchronization operations to occur. See the data tag structures used within each FIFO for means of detecting end-of-file (EOF) samples, invalid (empty samples) and other aides for efficiently using and managing normal mode read back operations.

Burst Mode Read Sequence

The MAX30003 provides commands to read back the ECG FIFO memory in a burst mode to increase data transfer efficiency. Burst mode uses different register addresses than the normal read sequence register addresses. The first 32 SCLK cycles operate exactly as described for the normal mode. If the µC continues to provide SCLK edges beyond the 32nd rising edge, the MSB of the next available FIFO word will be presented on the next falling SCLK edge, allowing the µC to sample the MSB of the next word on the 33rd SCLK rising edge. Any affected interrupts and/or FIFO read pointers will be incremented in response to the (30+n x 24)th SCLK rising edge where n is an integer starting at 0. (i.e., on the 30th, 54th, and 78th SCLK rising-edges for a three-word, burst-mode transfer).

This mode of operation will continue for every 24 cycle sub frame, as long as there is valid data in the FIFO. See the data tag structures used within each FIFO for means of detecting end-of-file (EOF) samples, invalid (empty samples) and other aides for efficiently using and managing burst mode read back operations.

There is no burst mode equivalent in write mode.

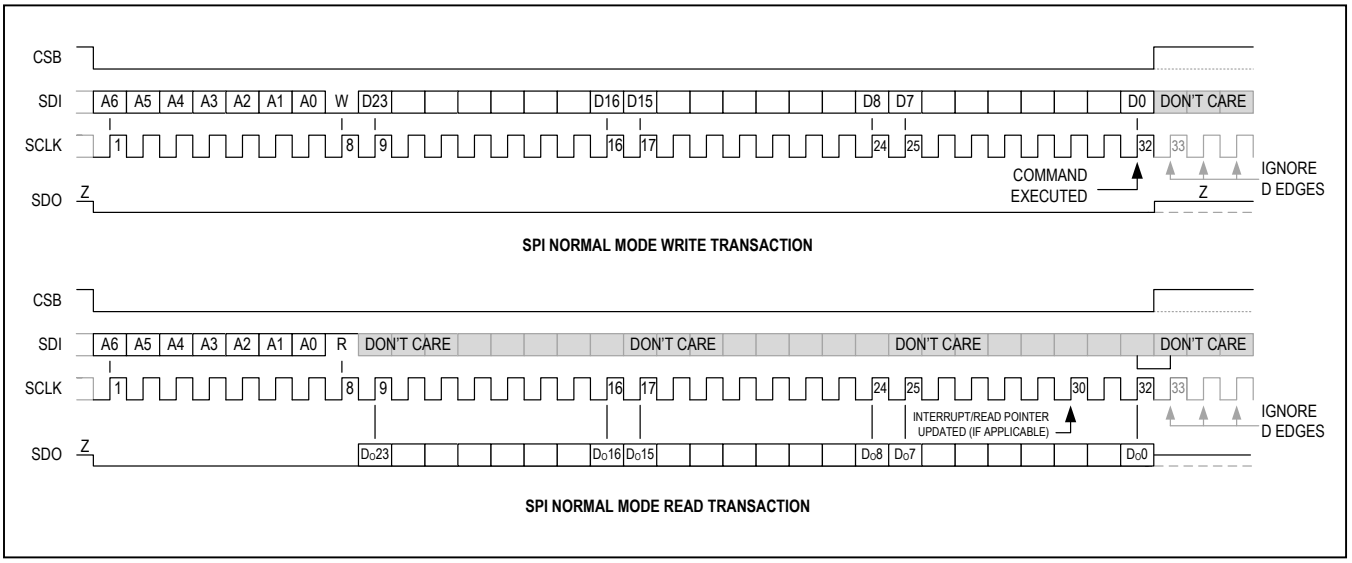


Figure 8. SPI Normal Mode Transaction Diagrams

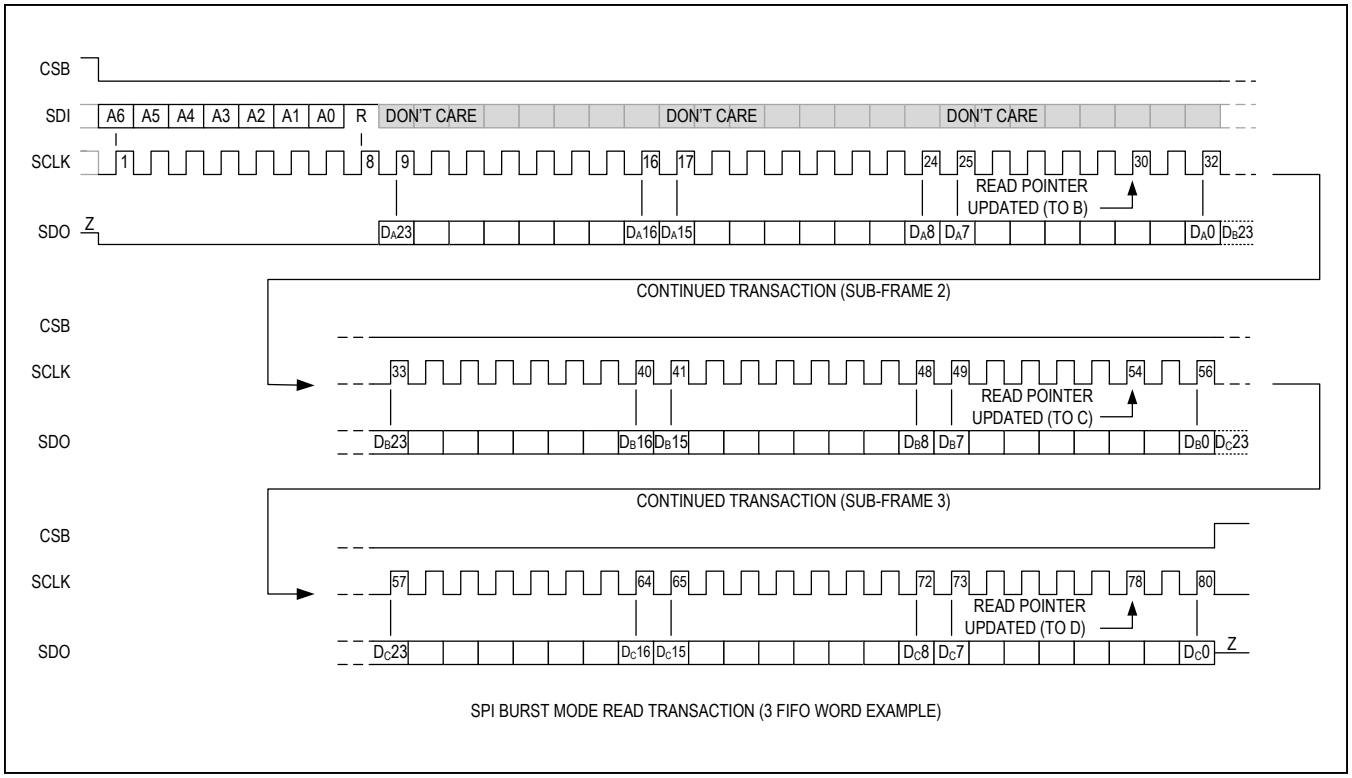


Figure 9. SPI Burst Mode Read Transactions Diagrams

User Command and Register Map

REG [6:0]	NAME	R/W MODE	DATA INDEX (D_{INDEX})							
			23 / 15 / 7	**22 / 14 / 6**	**21 / 13 / 5**	**20 / 12 / 4**	**19 / 11 / 3**	**18 / 10 / 2**	**17 / 9 / 1**	**16 / 8 / 0**
0x00	NO-OP	R/W	x / x / x	x / x / x	x / x / x	x / x / x	x / x / x	x / x / x	x / x / x	x / x / x
0x01	STATUS	R	EINT	EOVF	FSTINT	DCLOFFINT	x	x	x	x
			x	x	x	x	LONINT	RRINT	SAMP	PLLINT
			0	0	x	x	LOFF_PH	LOFF_PL	LOFF_NH	LOFF_NL
0x02 0x03	EN_INT EN_INT2	R/W	EN_EINT	EN_EOVF	EN_FSTINT	EN_DCLOFFINT	x	x	x	x
			x	x	x	x	EN_LONINT	EN_RRINT	EN_SAMP	EN_PLLINT
			x	x	x	x	x	x	INTB_TYPE[1:0]	
0x04	MNGR_INT	R/W	EFIT[4:0]					x	x	x
			x	x	x	x	x	x	x	x
			x	CLR_FAST	CLR_RRINT[1:0]		x	CLR_SAMP	SAMP_IT[3:0]	
0x05	MNGR_DYN	R/W	FAST[1:0]		FAST_TH[5:0]					
			x	x	x	x	x	x	x	x
			x	x	x	x	x	x	x	x
0x08	SW_RST	W	Data Required for Execution = 0x000000							
0x09	SYNCH	W	Data Required for Execution = 0x000000							
0x0A	FIFO_RST	W	Data Required for Execution = 0x000000							
0x0F	INFO	R	0	1	0	1	REV_ID[3:0]			
			x	x	1	1	x	x	x	x
			x	x	x	x	x	x	x	x
0x10	CNFG_GEN	R/W	EN_ULP_LON[1:0]		FMSTR[1:0]		EN_ECG	x	x	x
			x	x	EN_DCLOFF[1:0]		IPOL	IMAG[2:0]		
			VTH[1:0]		EN_RBIAS[1:0]		RBIASV[1:0]		RBIASP	RBIASN

User Command and Register Map (continued)

REG [6:0]	NAME	R/W MODE	DATA INDEX (D_{INDEX})							
			23 / 15 / 7	**22 / 14 / 6**	**21 / 13 / 5**	**20 / 12 / 4**	**19 / 11 / 3**	**18 / 10 / 2**	**17 / 9 / 1**	**16 / 8 / 0**
0x12	CNFG_CAL	R/W	x	EN_VCAL	VMODE	VMAG	x	x	x	x
			x	FCAL[2:0]			FIFTY	THIGH[10:8]		
			THIGH[7:0]							
0x14	CNFG_EMUX	R/W	POL	x	OPENP	OPENN	CALP_SEL[1:0]		CALN_SEL[1:0]	
			x	x	x	x	x	x	x	x
			x	x	x	x	x	x	x	x
0x15	CNFG_ECG	R/W	RATE[1:0]		x	x	x	x	GAIN[1:0]	
			x	DHPF	DLPF[1:0]		x	x	x	x
			x	x	x	x	x	x	x	x
0x1D	CNFG_RTOR1	R/W	WNDW[3:0]				RGAIN[3:0]			
			EN_RTOR	x	PAVG[1:0]		PTSF[3:0]			
			x	x	x	x	x	x	x	x
0x1E	CNFG_RTOR2	R/W	x	x	HOFF[5:0]					
			x	x	RAVG[1:0]		x	RHSF[2:0]		
			x	x	x	x	x	x	x	x
0x20	ECG_FIFO_BURST	R+	ECG FIFO Burst Mode Read Back				See FIFO Description for details			
0x21	ECG_FIFO	R	ECG FIFO Normal Mode Read Back				See FIFO Description for details			
0x25	RTOR	R	R to R Interval Register Read Back				See FIFO Description for details			
0x7F	NO-OP	R/W	x/x/x	x/x/x	x/x/x	x/x/x	x/x/x	x/x/x	x/x/x	x/x/x