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19-0330; Rev 0; 11/94

MAXIM

MAX100 Evaluation Kit

Evaluates: MAX100

General Description

The MAX100 evaluation kit (EV kit) allows high-speed digitizing of analog signals at 250Msps, using the MAX100 ADC. All circuitry required to support the ADC is supplied. Data output is available in three formats: divide-by-1, divide-by-2, or divide-by-5 mode. Clocking is provided by an external clock source input through an SMA connector.

The MAX100 EV kit main board comes complete with a MAX100 high-speed, 8-bit flash ADC with strobed comparators, latched outputs, and an internal track/hold. Analog input to the board is through two SMA coaxial connectors, for use with either differential or single-ended inputs.

Signals from the main board include dual-output data paths that allow easy interfacing to external circuitry. These two outputs can be configured either to provide two identical fast outputs (A and B), or an 8-to-16 demultiplexer mode that reduces the output data rates to one-half the sample clock rate. This demux is internal to the MAX100 ADC and is one of the key features of this device.

A termination board with 50Ω ECL pull-down resistors is also supplied, and is connected to the main board with a 3x32 pin EURO-card connector. It provides access to the converter output data and provides proper ECL data termination. In addition to the pull-down resistors, this board has two ranks of square pins, each providing eight differential data outputs plus clock outputs. Either AData or BData may be observed with a high-speed logic analyzer.

Standard power supplies of +5V and -5.2V are needed to operate the MAX100 EV kit board. Power can be supplied through the 3x32 EURO-card connector or through the pads on the edge of the board. Nominal power dissipation for both boards is 12W. The board set comes fully assembled and tested, with the MAX100 installed.

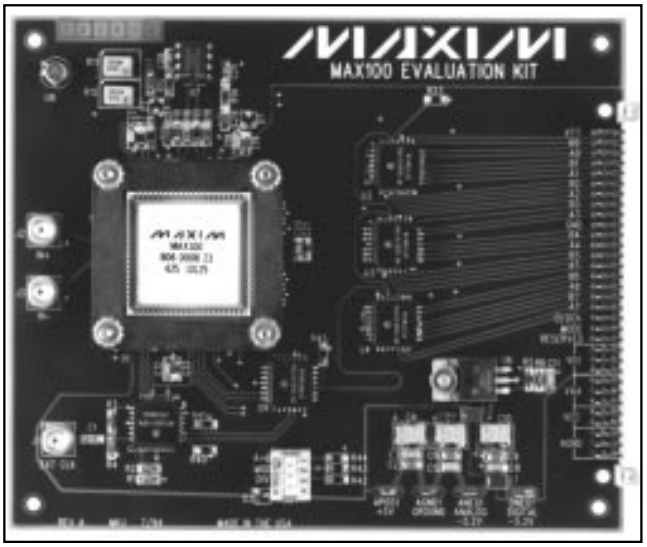
Features

- **6.8 Effective Bits at 125MHz**
- **On-Board Reference Generator/Buffer**
- **50Ω Input Through SMA Coaxial Connectors**
- **Dual Differential-Output Data Paths**
- **±270mV Input Signal Range**
- **Latched 100k ECL Outputs**
- **3x32 Pin EURO-Card Connector**

Ordering Information

PART	TEMP. RANGE	BOARD TYPE
MAX100EVKIT	0°C to +70°C	Multi-Layer

EV Kit



MAX100 Evaluation Kit

Component List

DESIGNATION	QTY	DESCRIPTION
U5	1	Motorola MC100E116 (quintuple line receiver)
U2, U3, U4	3	Motorola MC100E151 (Hex D flip-flop)
U9	1	Motorola MC100E157 (quadruple 2:1 multiplexer)
U6	1	LM337T negative voltage regulator
Install on back of board behind U6	1	Insulating washer
U7	1	Maxim MAX412CPA
U8	1	Maxim MX580KH
D1, D2	2	Central Semiconductor CMPSH-3
D3	1	Central Semiconductor CMPD4448
C25, C27	2	0.22µF ceramic SMD capacitors
C2, C6, C9	3	0.1µF ceramic SMD capacitors
C1, C3, C5, C8, C11, C12, C14, C16, C18, C20, C22–C24, C26, C28, C29	16	0.01µF ceramic SMD capacitors
C13, C15, C17, C19, C21, C30	6	100pF ceramic SMD capacitors
C4, C7, C10	3	10µF surface-mount tantalum capacitors
SW1	1	8-pin dip switch
L1, L2	2	Surface-mount ferrite bead
R14, R15	2	20Ω, 5% surface-mount resistors
R18, R19	2	27.4Ω, 1% surface-mount resistors
R7, R8, R13, R20–R45	29	51Ω, 5% surface-mount resistors
R1, R3, R6	3	82.5Ω, 1% surface-mount resistors
R5, R10	2	121Ω, 1% surface-mount resistors
R9	1	150Ω, 1% surface-mount resistor
R2, R4	2	221Ω, 1% surface-mount resistors
R16, R17	2	12.1kΩ, 1% surface-mount resistors
R11, R12	2	100Ω trim pots
J1, J2, J3	3	Female SMA connectors
J4	1	96-pin EURO-style plug
None	1	MAX100 clamp kit

Quick Start

1) Plug the termination board into the 96-pin connector of the MAX100 EV kit board.
2) Use a fan to provide at least 200 lineal feet per minute airflow to the MAX100's heatsink.
3) Connect the power supplies. The power-supply input pads are in the lower right corner of the MAX100 EV kit board. The board requires a 12W power supply that provides +5V and -5.2V with a common ground.
4) Turn on the -5.2V power supply, followed by the +5V power supply. The -5.2V power supply should be the first supply turned on and the last supply turned off.
5) Connect a low-phase-jitter RF source with an input range of -4dBm to +10dBm to the clock input.
6) Connect a test signal to the analog inputs. Use IN+ and IN- if the signal is differential, or use IN+ if the signal is single-ended.
7) Use a logic analyzer (such as the HP8000 or an equivalent data-acquisition system) to observe the digitized results on the termination board pins. The outputs are 100k ECL compatible.

Detailed Description

Board Set

The MAX100 EV kit is a two-board set. The first contains ECL-interface circuitry and the MAX100 ADC. The second (termination board) provides for high-speed signal termination and access to the data. For further signal processing, the board containing the MAX100 can be plugged into a larger customer system via the provided EURO-card connector.

Clock Input

The ADC clock is provided through an external clock input. The external clock supplied to the board must be very stable, with low phase jitter (-150dBc/Hz at 0.2kHz from fundamental) for best effective bits performance. Figure 2 in the MAX100 data sheet shows the input to output clock and data timing relationships.

The MAX100 will accurately operate with low-repetition-rate clocks (DC to 250MHz) as long as the proper t_{pwl} is observed (nominally 2ns to 5ns). Refer to Figures 1–4 in the MAX100 data sheet for further information.

Analog Input

Analog input to the ADC is made through one or both of the SMA coaxial connectors (IN+, IN-) provided. Each input is a direct connection to the ADC. 50Ω terminations are provided (at AIN+ and AIN- inputs) internal to the MAX100 ADC. Optimum performance is achieved

by using the converter in differential input mode. Single-ended drive is handled by choosing either input, and leaving open or terminating the other in the system characteristic impedance. In this mode, the unused input can provide a DC offset to the incoming signal. (See the *Electrical Characteristics* in the MAX100 data sheet for this DC voltage range.)

To obtain a digital output of all ones (11....1) with differential input drive, apply 270mV between AIN+ and AIN-. That is, AIN+ = +135mV and AIN- = -135mV (when no DC offset is applied). Mid-scale digital output code occurs when there is no voltage difference across the analog inputs. Zero-scale digital output code, with differential drive, occurs when AIN+ = -135mV and AIN- = +135mV. The converter's output stays at all ones (full scale) or all zeros (zero scale) when over-ranged or under-ranged, respectively. Table 1 shows these relationships.

Digital Outputs

The MAX100 EV kit provides complementary ECL digital outputs. Data output from the ADC is available in several selectable options (Table 2). Two 8-bit-wide data paths from the ADC are latched in D flip-flops (MC100E151), and are provided as unterminated differential outputs at the 3x32 pin EURO-card connector on the main board. Output timing clocks DCLK and $\overline{\text{DCLK}}$ are also available unterminated at the connector.

Clock Phasing

The MAX100 contains an internal track/hold (T/H) amplifier. The differential inputs, AIN+ and AIN-, are tracked continuously between data samples. When a negative CLK is applied, the T/H enters the hold mode. When CLK reaches the low state, the just-acquired sample is presented to the ADC's input comparators. After additional clock cycles required for internal processing, the sampled data is available at the AData or BData outputs. All output data is timed from the output clocks, DCLK and $\overline{\text{DCLK}}$. (See Figure 2 in the MAX100 data sheet.)

ADC Reference Resistors

An on-board reference supply and op-amp circuit drive the ADC reference-resistor string. Adjustments can be made through the two potentiometers provided. After the MAX100 ADC is installed, follow the *Calibration Procedure*.

Buffer amplifiers are used to drive the top and bottom inputs of the reference-resistor string. (The resistor string center-tap is not made available for adjustment on this board.) A 2.5V reference (MX580KH) is divided down and buffered through a MAX412 op amp. The relatively low 146Ω input impedance of this string will draw approximately 14mA. A reference voltage of nominally ±1.02V is set by trim pots R11 and R12 at the factory, and can be measured at the VA_{RTS} and VA_{RBS} sense input pins. This reference controls the comparator input windows, and can be adjusted between ±1.4V to accommodate other reference voltages (MAX100 accuracy specifications are based on a reference voltage of ±1.02V).

DIV, MOD, A=B

Three dip switches (SW1), DIV, MOD, and A=B, program converter operation and the characteristics of the two output data paths. Six options are available, but the normal operating configuration is set to 0 0 1 on the A=B, MOD, and DIV switches, respectively (Table 2). This gives the most current sample at AData, with the older data on BData. Both outputs are synchronous and are output at half the input clock rate. Figure 4 shows the location of these switches on the ADC board. Refer to Table 1 for mode-selection instructions.

Power Supplies

Two supplies are needed for normal operation of both boards with a device installed: +5V at 0.6A and -5.2V at 1.7A. The pads APOS1 and ANEG1 are located in the lower right corner of the ADC board, and are labeled accordingly. The ADC runs off both supplies.

Power may also be applied at the EURO-card connector pins, which are labeled as follows: VCC (+5V), VEE (-5.2V for digital DNEG1), VAA (-5.2V for analog ANEG1), and AGND (AGND1 ground). The ferrite beaded jumper (L1) in the lower right corner of the board connects VAA and VEE for a single -5.2V supply.

Board Layout

The MAX100 requires proper PC board layout for device operation. This section explains the layout requirements and demonstrates how the EV kit achieves these goals.

Use power and ground planes to deliver power to the devices, keeping the digital planes separate from the analog planes. The EV kit uses layers 3, 4, and 5 for power and ground planes. Tie digital ground and analog ground together at a single point, as close to the power supply as possible. On the EV kit, digital ground ties to analog ground at ferrite bead L1. Likewise, tie digital power (VEE) and analog power (VAA) together at a single point, as close to the power supply as possible. On the EV kit, digital power ties to analog -5.2V power at ferrite bead L2.

Use transmission lines for the analog input and for the high-speed digital outputs. The MAX100 EV kit uses 50Ω microstrip lines that occupy layers 1 and 2, and

FR4 epoxy dielectric material with a relative dielectric constant between 4.1 and 4.9. The nominal design has a foil thickness of 0.0014 inch (0.0355 mm) for layer 1 (the signal layer) and 0.0014 inch (0.0355 mm) for layer 2 (the ground return). Dieletric thickness between layers is nominally 0.011 inch (0.28 mm), with a signal trace width of 0.020 inch (0.50 mm). Refer to Motorola's MECL™ or ECLinPS™ data book for an introduction to microstrip design.

Due to the high-speed nature of this part, the propagation delay of the PC board traces becomes a significant design consideration. For the EV kit design, the propagation delay is approximately 145ps per inch (5.7ps/mm). For best results, try to match the lengths of the data traces to within 0.5 inch (12 mm). The EV kit board matches the data-bus lengths by using curved traces on layer 6. A computer-aided design system can be helpful in measuring the trace lengths accurately. The clock signal must be routed on one layer only, without using any through-hole vias. The MAX100 EV kit is a controlled-impedance board (50Ω) and has a total board thickness of 0.062 inches (1.57 mm) using six copper layers (Figure 3).

Testing

We recommend that a digital acquisition instrument like the HP8000 logic analyzer be used to acquire and process the output data. At Maxim, the data acquired from the converter is evaluated in an effective-bits software program developed in-house. The effective-bits measurement is a good tool to determine and compare ADC accuracy.

Calibration Procedure

The MAX100 EV kit comes ready to operate from the factory. If other devices are to be used in the same fixture, the EV kit should be recalibrated according to the following procedure:

1) With the ADC removed, adjust the +5V and -5.2V supplies.
2) Set the mode-select options (A=B, DIV, MOD) for the desired operation using the on-board DIP switches. See Table 1.
3) With the power off, insert the MAX100. The MAX100's heatsink fits down through the board with the device leads resting on top. Be sure to place the part in the board with pin 1 in the correct location. Provide at least 200 lineal feet per minute airflow whenever power is applied. Turn on the power supplies with -5.2V first, then the +5V. The -5.2V power supply should be the first supply turned on and the last supply turned off.

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Table 1. Input Voltage Range

INPUT	AIN+** (mV)	AIN-** (mV)	OUTPUT CODE	(MSB TO LSB)
Differential	+135 0 -135	-135 0 +135	11111111 10000000 00000000	Full scale Mid scale Zero scale
Single-Ended	+270 0 -270	0 0 0	11111111 10000000 00000000	Full scale Mid scale Zero scale

** An offset, V_{IO}, as specified in the *DC Electrical Characteristics,* is present at the input. Compensate for this offset either by adjusting the reference voltage VA_{RT}, VA_{RB}, or by introducing an offset voltage in one of the input terminals, AIN+ or AIN-.

Table 2. Output-Mode Control

DIV	MOD	A = B	DCLK*	DESCRIPTION
Divide-by-1 Mode				
0	X	0	250MHz	Data appears on AData only. BData port inactive (see Figure 3 of MAX100 data sheet).
0	X	1	250MHz	AData identical to BData (see Figure 3 of MAX100 data sheet).
Divide-by-2 Mode				
1	0	0	125MHz	8:16 demux mode. AData and BData ports are active. BData carries older sample and AData carries most recent sample (see Figure 4 of MAX100 data sheet).
1	0	1	125MHz	AData and BData ports are active. Both carry identical sampled data. Alternate samples are taken but discarded.
Divide-by-5 Mode				
1	1	0	50MHz	AData port updates data on 5th input CLK. BData port inactive. The other four sampled data points are discarded.
1	1	1	50MHz	AData and BData ports are both active with identical data. Data is updated on output ports every fifth input clock (CLK). The other four samples are discarded.

* Input clocks (CLK, $\overline{CLK}$) = 250MHz for all above combinations. In divide-by-2 or divide-by-5 mode, the output clock DCLK is always a 50% duty-cycle signal. In divide-by-1 mode, DCLK has the same duty cycle as CLK.

4) After the part has warmed up for several minutes, adjust the reference voltages to ±1.02V nominally. The test points for these voltages are at the bottom of the sense resistors, R13 and R16, located just above the sense pins VA_{RTS} and VA_{RBS} (Figure 4).

5) Adjust mid-code level. With no analog input (AIN+ - (AIN-) = 0V) the output code should match that specified in Table 1. If there is an offset, adjust either the positive or negative reference until the expected code of 10 00 00 00 (MSB to LSB) is achieved. After adjusting to the proper level, the references need to be balanced to ±1.02V around any offset that was introduced. (If the negative reference was moved by +32mV, the positive reference must be moved by that same amount to ensure the correct LSB size.) It may be necessary to repeat the reference offset adjustment again after the correct 2.04V differential reference voltage is re-established around the common-mode offset.

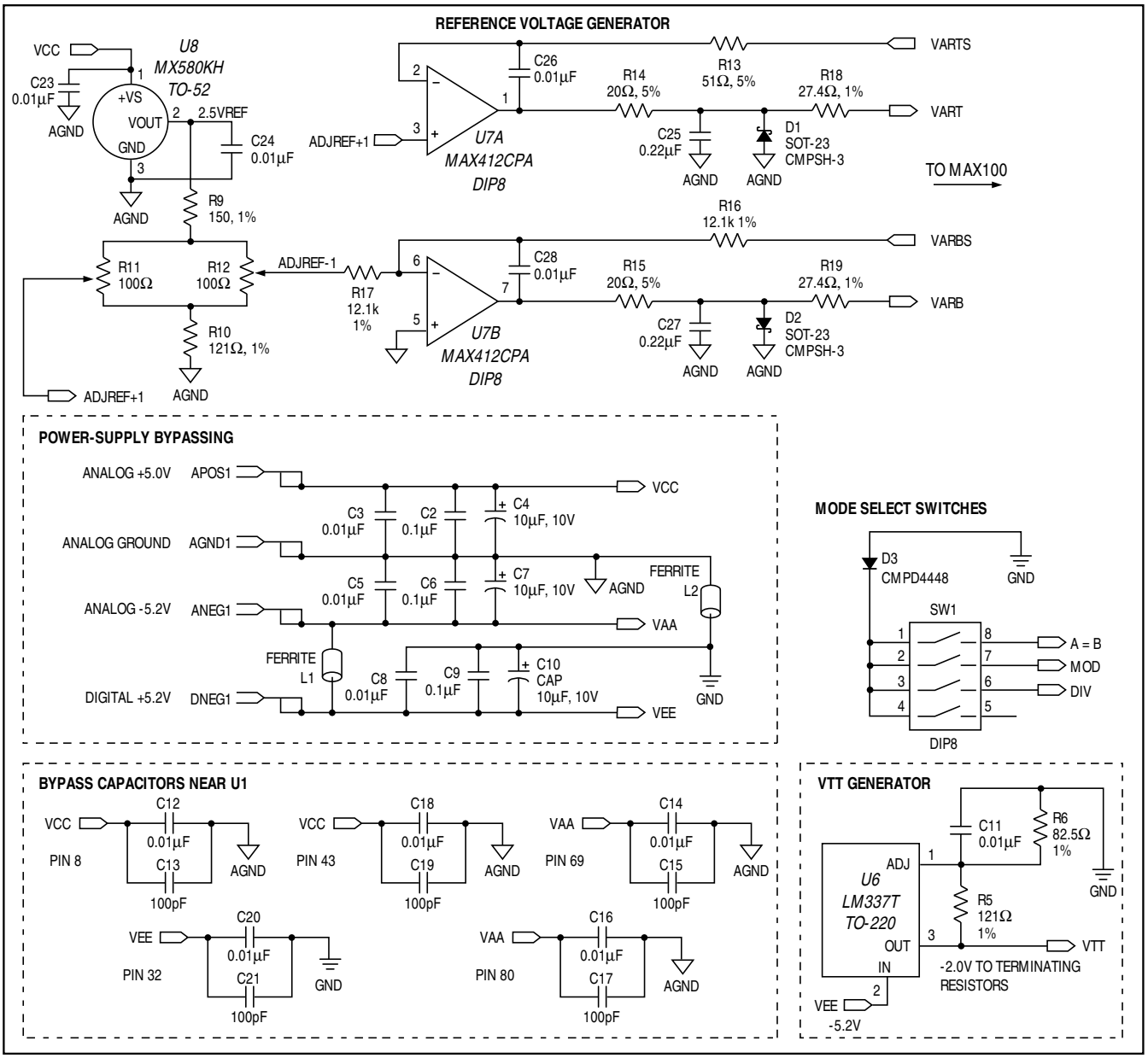


Figure 1. MAX100 EV Kit Schematic

MAX100 Evaluation Kit

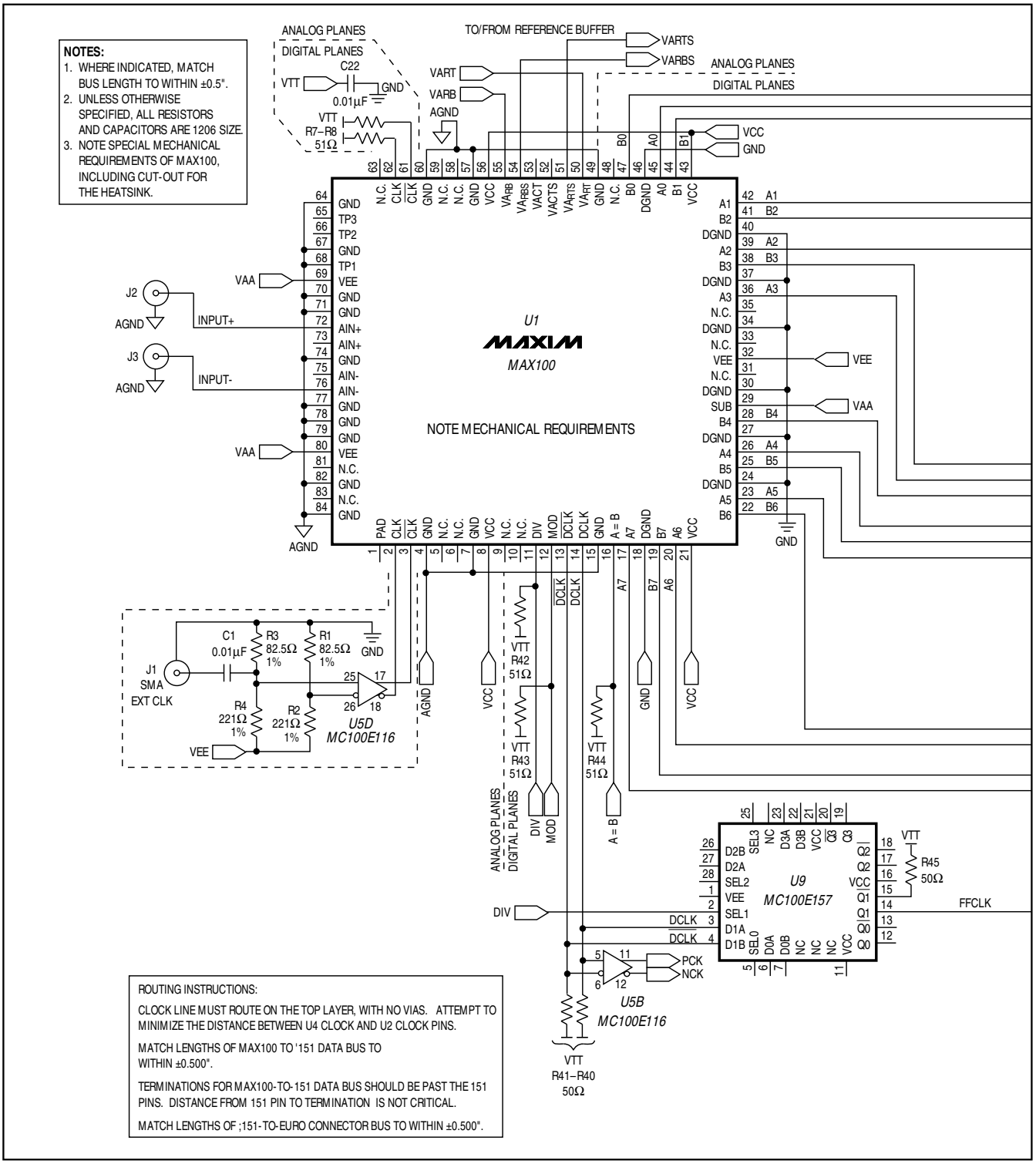
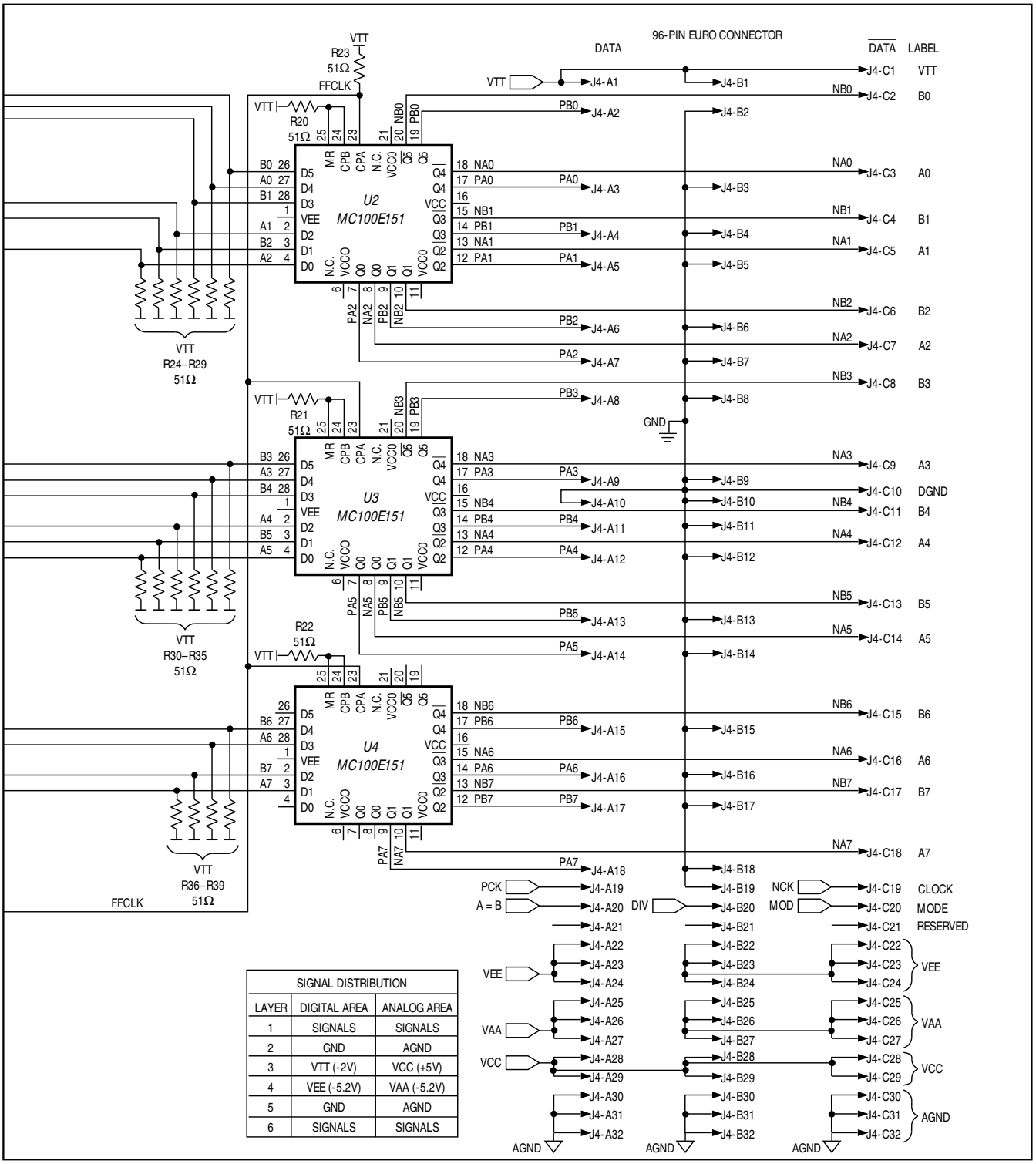


Figure 1. MAX100 EV Kit Schematic (continued)



SIGNAL DISTRIBUTION		
LAYER	DIGITAL AREA	ANALOG AREA
1	SIGNALS	SIGNALS
2	GND	AGND
3	VTT (-2V)	VCC (+5V)
4	VEE (-5.2V)	VAA (-5.2V)
5	GND	AGND
6	SIGNALS	SIGNALS

Figure 1. MAX100 EV Kit Schematic (continued)

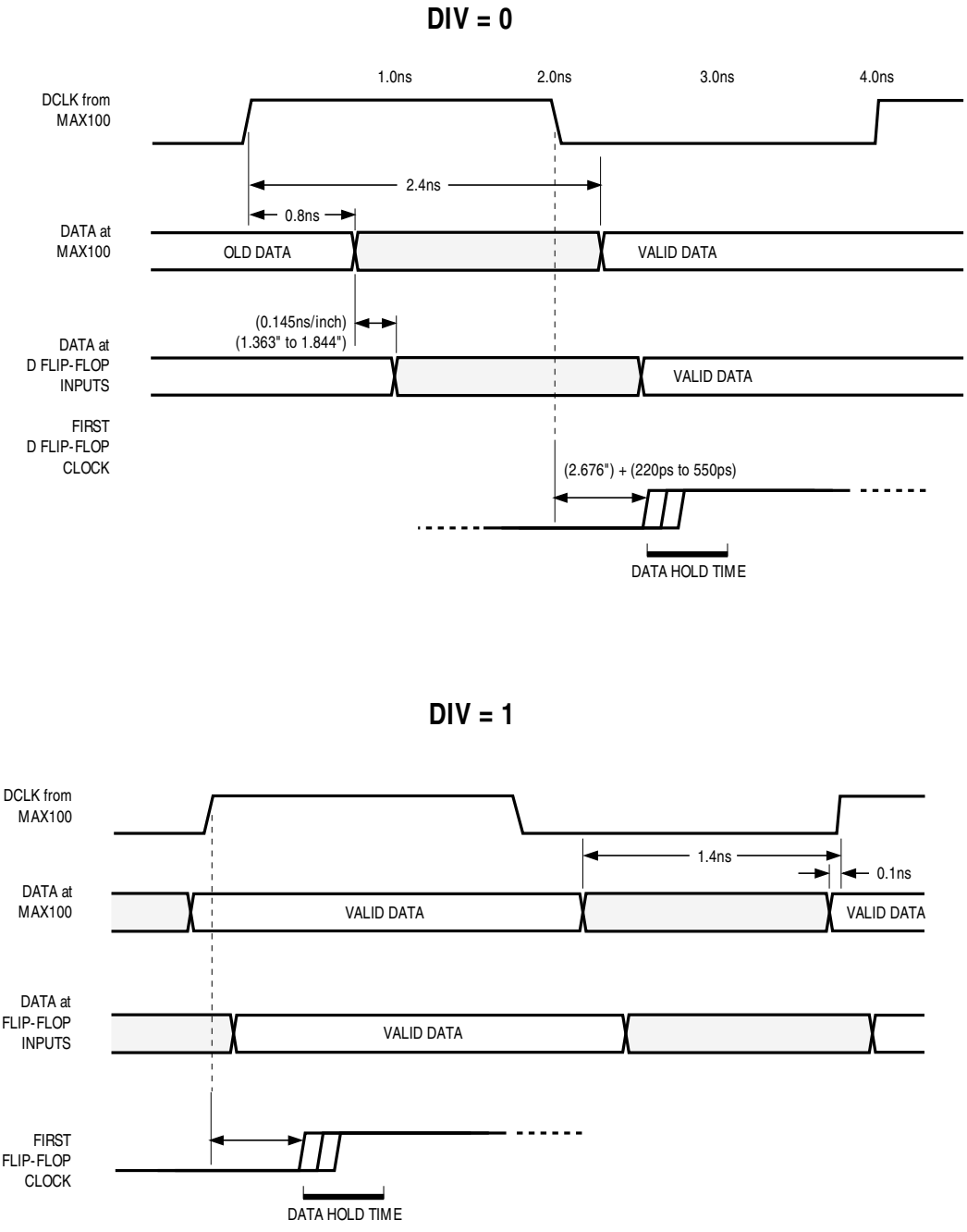


Figure 2. Evaluation Kit Timing

Copper Layer 1	Copper thickness = 0.0014” (1 oz copper)
Epoxy FR4	Dielectric layer thickness = 0.01072”
Copper Layer 2	Copper thickness = 0.0014” (1 oz copper)
Epoxy FR4	Dielectric layer thickness = 0.01072”
Copper Layer 3	Copper thickness = 0.0014” (1 oz copper)
Epoxy FR4	Dielectric layer thickness = 0.01072”
Copper Layer 4	Copper thickness = 0.0014” (1 oz copper)
Epoxy FR4	Dielectric layer thickness = 0.01072”
Copper Layer 5	Copper thickness = 0.0014” (1 oz copper)
Epoxy FR4	Dielectric layer thickness = 0.01072”
Copper Layer 6	Copper thickness = 0.0014” (1 oz copper)

Microstrip traces are 20 mils wide for 50Ω impedance.

Figure 3. Layer Profile

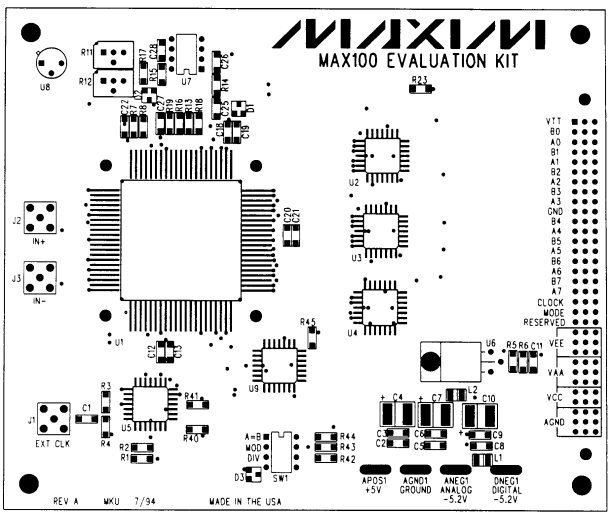


Figure 4. Main Board Component Placement Guide—Component Side

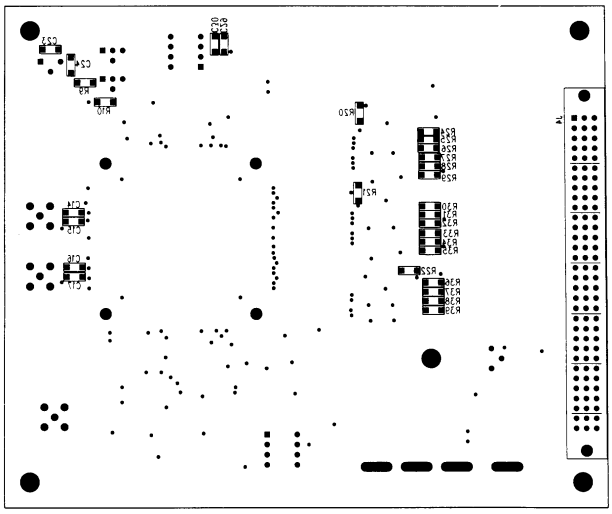


Figure 5. Main Board Component Placement Guide—Solder Side

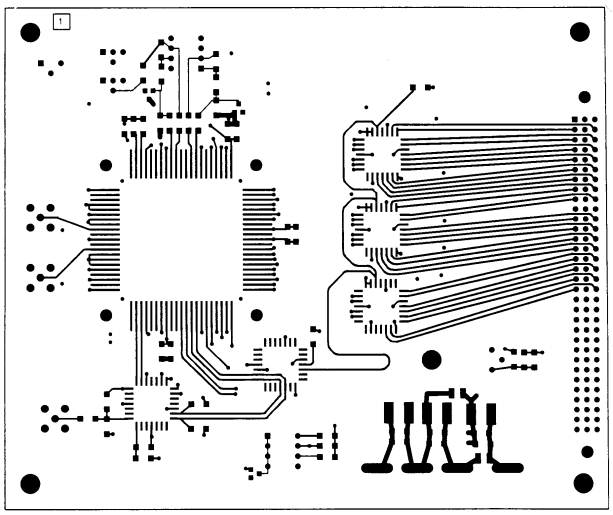


Figure 6. Main Board Layout—Copper Layer 1 (Top)

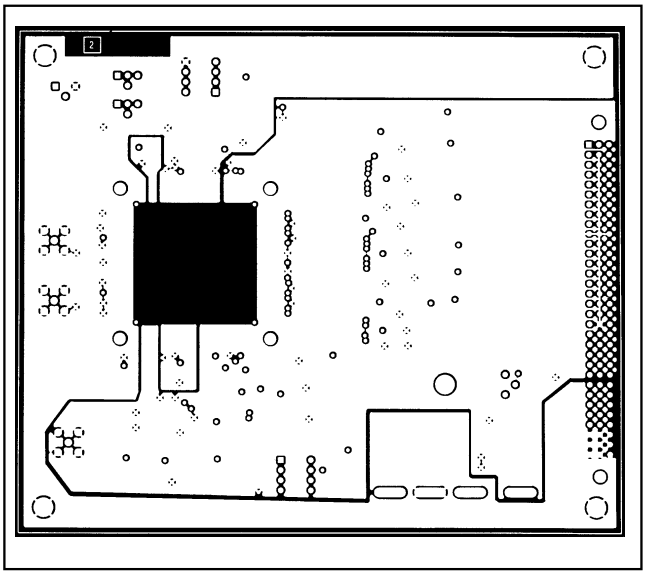


Figure 7. Main Board Layout—Copper Layer 2 (negative image)

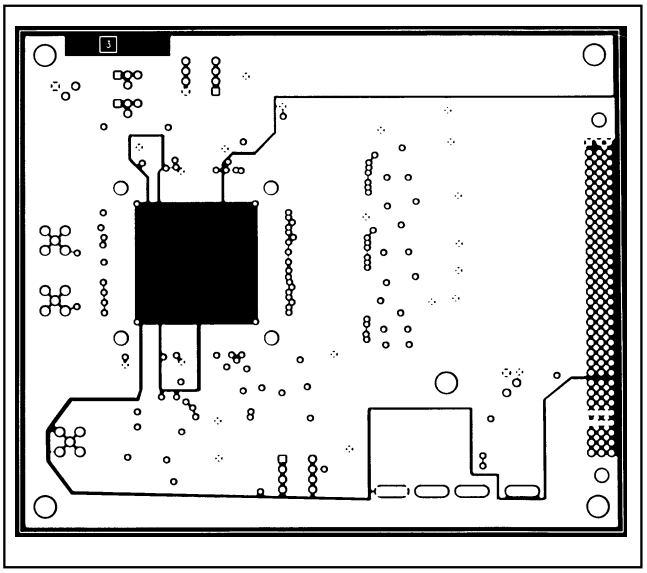


Figure 8. Main Board Layout—Copper Layer 3 (negative image)

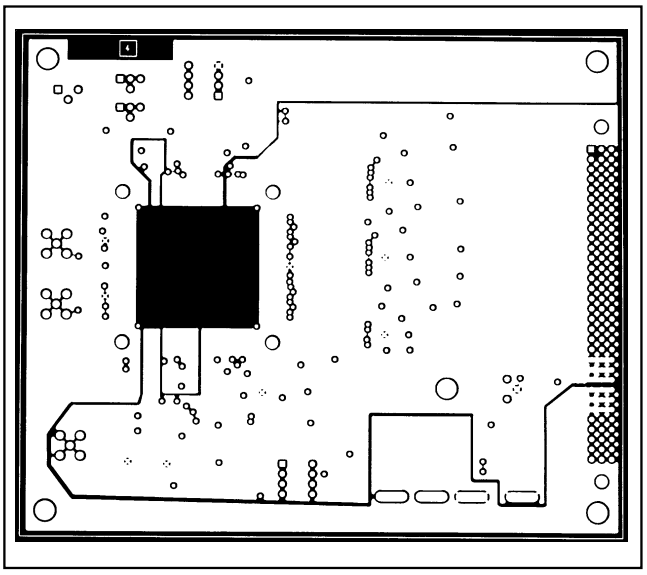


Figure 9. Main Board Layout—Copper Layer 4 (negative image)

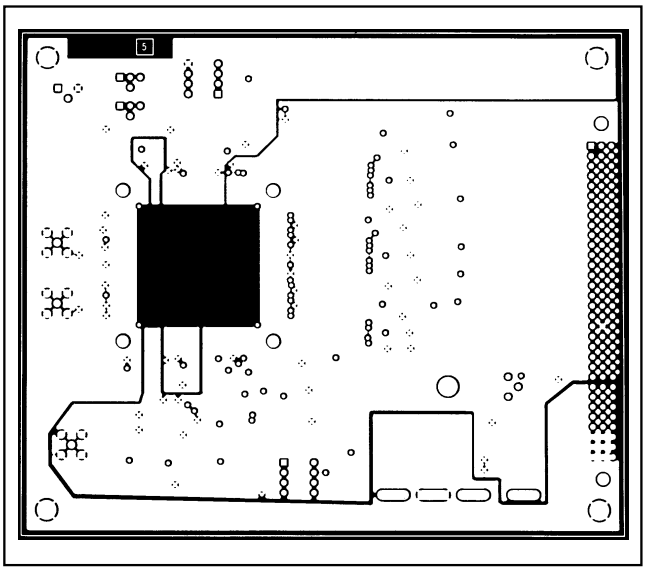


Figure 10. Main Board Layout—Copper Layer 5 (negative image)

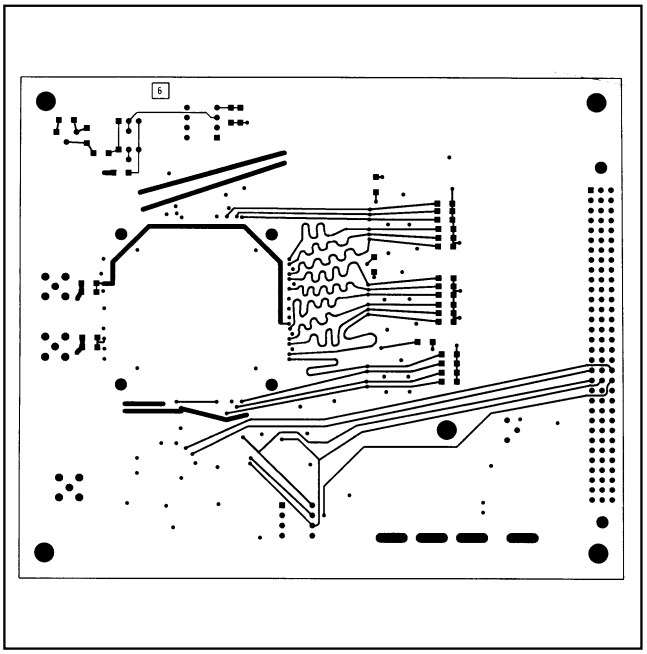
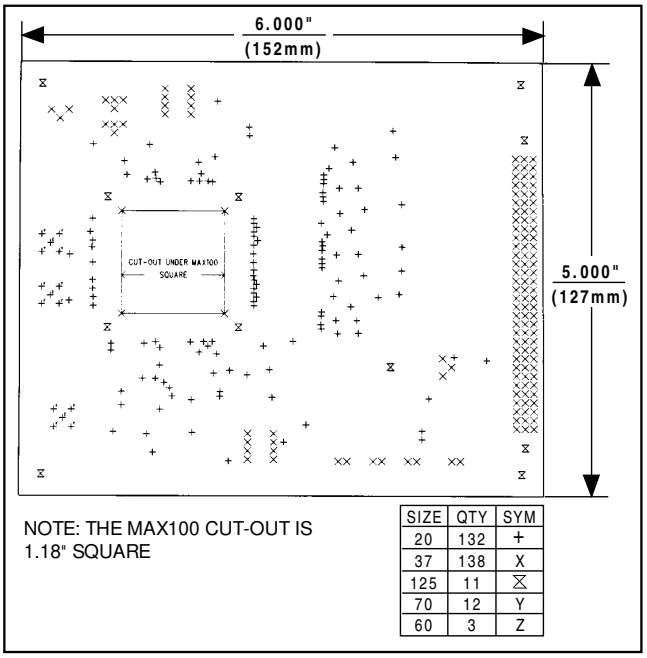
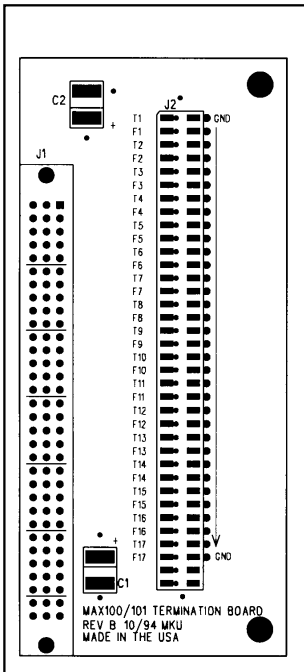


Figure 11. Main Board Layout—Copper Layer 6 (Bottom)



SIZE	QTY	SYM
20	132	+
37	138	X
125	11	⧖
70	12	Y
60	3	Z

Figure 12. Main Board Mechanical Outline



TERM BOARD SIGNAL	MAX100EVKIT SIGNAL	MAX101EVKIT SIGNAL
T1	B0	A0
F1	$\overline{B0}$	$\overline{A0}$
T2	A0	A1
F2	$\overline{A0}$	$\overline{A1}$
T3	B1	A2
F3	$\overline{B1}$	$\overline{A2}$
T4	A1	A3
F4	$\overline{A1}$	$\overline{A3}$
T5	B2	A4
F5	$\overline{B2}$	$\overline{A4}$
T6	A2	A5
F6	$\overline{A2}$	$\overline{A5}$
T7	B3	A6
F7	$\overline{B3}$	$\overline{A6}$
T8	A3	DCLK
F8	$\overline{A3}$	DCLK
T9	B4	A7
F9	$\overline{B4}$	$\overline{A7}$
T10	A4	B7
F10	$\overline{A4}$	$\overline{B7}$
T11	B5	B6
F11	$\overline{B5}$	$\overline{B6}$
T12	A5	B5
F12	$\overline{A5}$	$\overline{B5}$
T13	B6	B4
F13	$\overline{B6}$	$\overline{B4}$
T14	A6	B3
F14	$\overline{A6}$	$\overline{B3}$
T15	B7	B2
F15	$\overline{B7}$	$\overline{B2}$
T16	A7	B1
F16	$\overline{A7}$	$\overline{B1}$
T17	DCLK	B0
F17	$\overline{DCLK}$	$\overline{B0}$

Figure 13. Termination Board Component Placement Guide and Signal Connections—Component Side

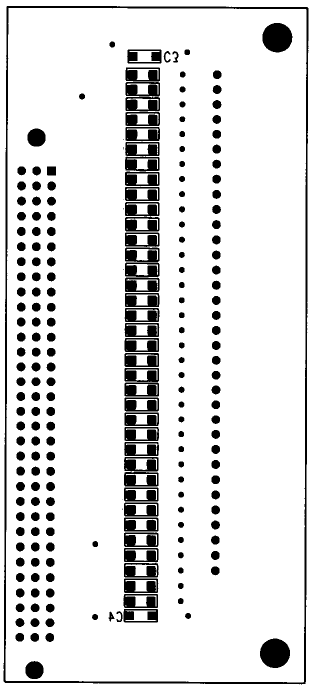


Figure 14. Termination Board Component Placement Guide—Solder Side

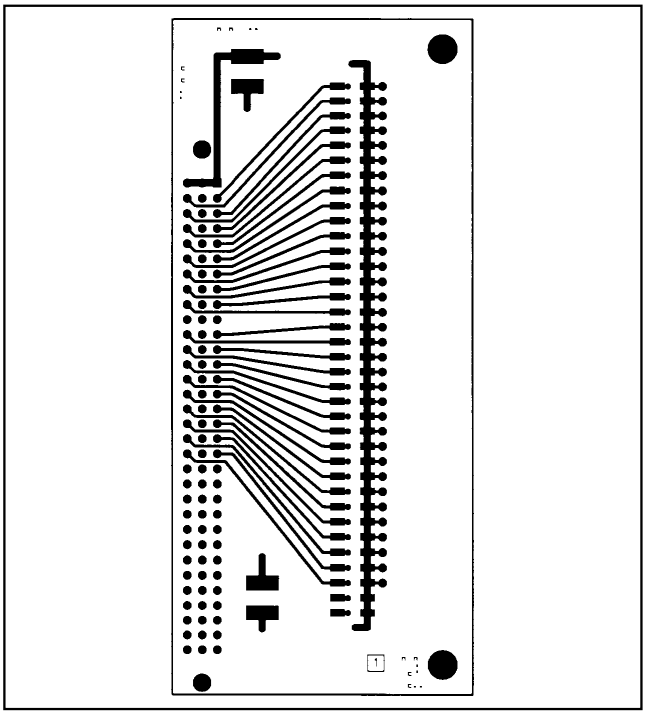


Figure 15. Termination Board Layout—Layer 1

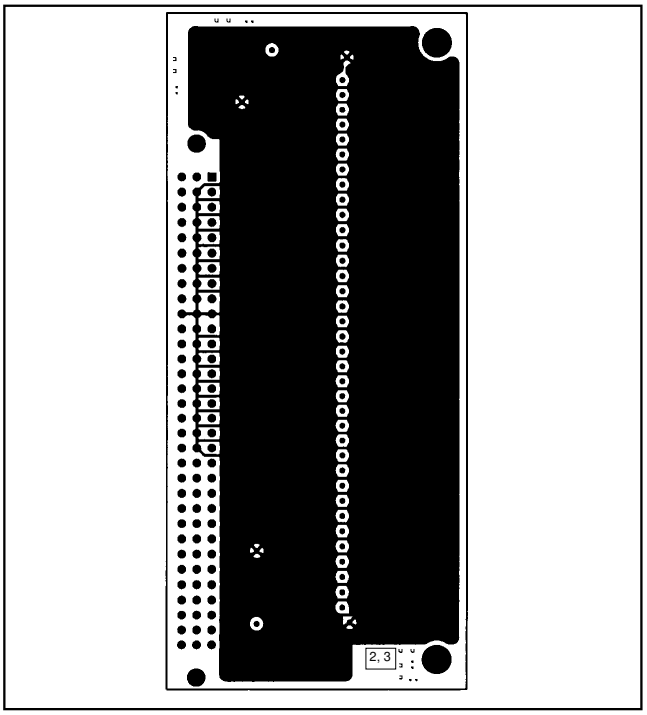


Figure 16. Termination Board Layout—Layers 2, 3

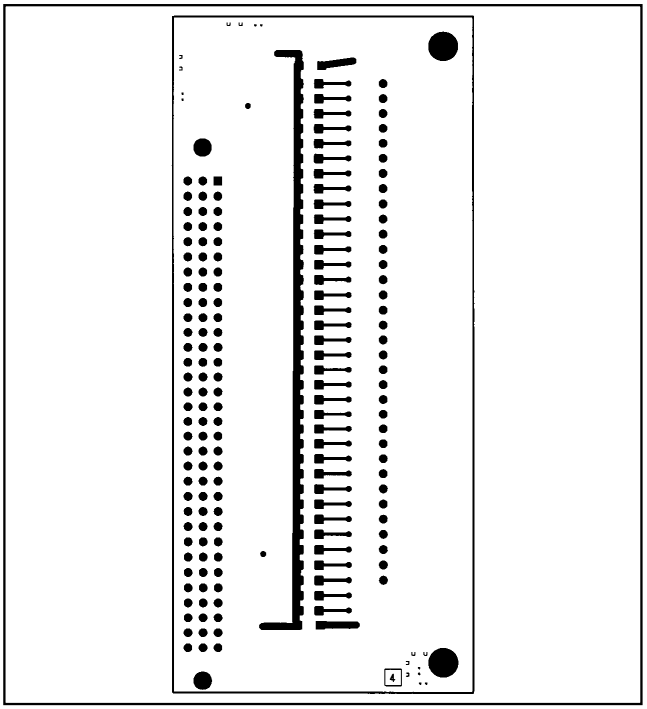


Figure 17. Termination Board Layout—Layer 4 (Bottom)

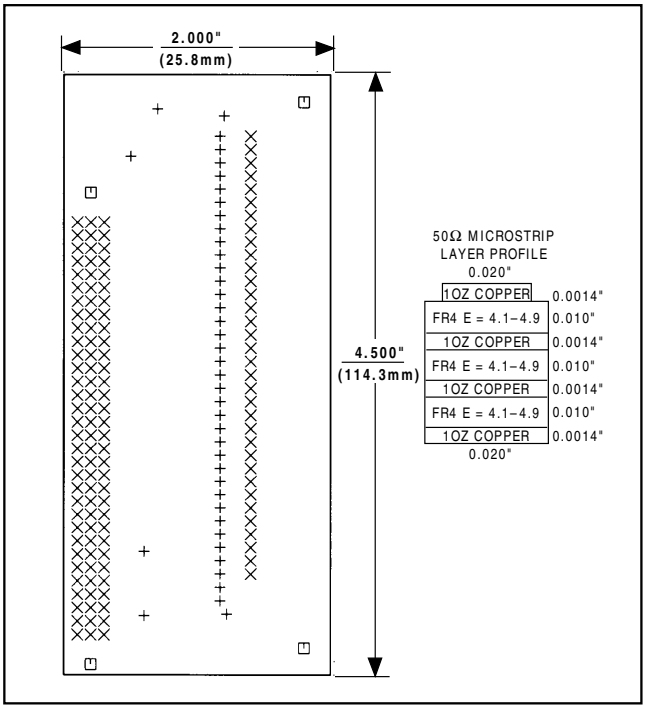


Figure 18. Termination Board Mechanical Guide