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## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email \& Skype: info@chipsmall.com Web: www.chipsmall.com Address: A1208, Overseas Decoration Building, \#122 Zhenhua RD., Futian, Shenzhen, China

## MAX101A Evaluation Kit

> General Description

The MAX101A evaluation kit (EV kit) was developed to assist in the initial evaluation of the MAX101A highspeed analog-to-digital converters (ADCs). The EV kit is a two-board set comprised of a main board and a termination board.
The main board contains all the circuitry needed to evaluate the initial performance of this flash converter, which combines high-speed analog and digital circuitry and requires special attention to circuit layout. In conjunction with the MAX101A, the main board allows digitizing of analog signals at up to 500 Msps . It has provisions for an external clock source, which is supplied through an SMA connector. The analog inputs to the converter are through two SMA connectors (AIN+ and AIN-). There are 16 data outputs (two 8 -bit words) plus the data clock output.
A separate termination board with $50 \Omega$ ECL pull-down resistors is provided with the kit and is connected to the main board with a $3 \times 32$ pin EURO-card connector. It provides access to the converter output data, as well as proper ECL termination. The termination board also has two ranks of square pins, each providing eight data outputs, plus data clock outputs. Either AData or BData can be observed with a high-speed logic analyzer.
Standard power supplies of +5 V and -5.2 V are needed to operate the MAX101A main board. Power can be supplied through the $3 \times 32$ EURO-card connector or through the pads on the edge of the board. Nominal power dissipation for both boards is 17W. The board set comes fully assembled and tested, with the MAX101A installed.
The MAX101A EV kit comes with a MAX101A installed on the board, but it can also be used to evaluate the MAX101. Refer to instructions for setting references and input conditions for the appropriate device version throughout this document.

| Features |
| :--- |
| 7.0 Effective Bits at 250MHz |
| On-Board Reference Generator/Buffer |
| $50 \Omega$ Input through SMA Coaxial Connectors |
| Dual Differential-Output Data Paths |
| $\pm 270 \mathrm{mV}$ Input Signal Range (MAX101) |
| $\pm 250 \mathrm{mV}$ Input Signal Range (MAX101A) |
| Buffered Differential 100k ECL Outputs |
| 3x32 Pin EURO-Card Connector |
| PART   TEMP. RANGE BOARD TYPE <br> MAX101AEVKIT-CFR $0^{\circ} \mathrm{C}$ to $+70^{\circ} \mathrm{C}$    |

Component List

| DESIGNATION | QTY | DESCRIPTION |
| :---: | :---: | :--- |
| C1, C2, C4, C6, C7, <br> C9, C10, C12, C14, <br> C15, C18, C20, C23, <br> C2, C27, C29, C31, <br> C32, C34, C36, <br> C38, C40, C42 | 23 | $0.01 \mu$ F capacitors |
| C3, C5, C11, C13 | 4 | $0.22 \mu$ F capacitors |
| C8, C16, C30, C33, <br> C35, C37, C39, <br> C41, C43 | 9 | $100 p$ F capacitors |
| C17, C21, C24 | 3 | $0.1 \mu$ F capacitors |
| C19, C22, C25 | 3 | $10 \mu$ F capacitors, <br> AVX "D" tantalum |
| D1-D4 | 4 | 100 mA Schottky diodes, <br> Central Semiconductor <br> CMPSH-3 |
| DIV 10 | 1 | $3-p i n$ jumper block |
| J1, J2, J3 | 3 | Female SMA connectors |
| J5 | 1 | $96-$ pin EURO-style plug |
| L1, L2 | 2 | Ferrite beads |
| R1, R12 | 2 | $180 \Omega, 1 \%$ resistors |
| R2, R13, R23 | 3 | $121 \Omega, 1 \%$ resistors |
| R3, R4, R14, R15 | 4 | $100 \Omega$ trim pots |
| R5, R16, R38, R39 | 4 | $51 \Omega, 5 \%$ resistors |

Component List continued on next page.

## MAX101A Evaluation Kit

Evaluates: MAX101/MAX101A

| Component List (continued) |  |  |
| :---: | :---: | :--- |
| DESIGNATION QTY DESCRIPTION <br> R6, R7, R17, R18 4 $20 \Omega, 5 \%$ resistors <br> R8, R9, R19, R20 4 $12.1 \mathrm{k} \Omega, 1 \%$ resistors <br> R10, R11, R21, R22 4 $27.4 \Omega, 1 \%$ resistors <br> R24, R34, R36 3 $82.5 \Omega, 1 \%$ resistors <br> R25 1 $1 \mathrm{k} \Omega, 1 \%$ resistor <br> R26 1 $2 \mathrm{k} \Omega$ trim pot <br> R27 1 $3.16 \mathrm{k} \Omega, 1 \%$ resistor <br> R28, R29, R40-R55 18 $100 \Omega, 5 \%$ resistors <br> R35, R37 2 $221 \Omega, 1 \%$ resistors <br> U1 1 Maxim MAX101ACFR <br> U2, U4 2 Maxim MAX412CPA high- <br> speed dual op amps <br> U3, U5 2 Maxim MX580KH 2.5V <br> references <br> U6 1 LM337T negative voltage <br> regulator <br> U8, U21-U24 5 MC100E116 quintuple line <br> receivers |  |  |

Quick Start

1) Plug the termination board into the 96 -pin connector of the MAX101A main board.
2) Use a fan to provide at least 200 lineal feet $/ \mathrm{min}$ airflow to the heatsink of the MAX101A.
3) Connect the power supplies. The power-supply input pads are in the lower right-hand corner of the MAX101A main board. The board requires a 20 W power supply that provides +5 V and -5.2 V with a common ground.
4) Turn on the -5.2 V power supply first, followed by the +5 V power supply. The -5.2 V power supply should be the first supply turned on and the last supply turned off.
5) Connect a low-phase-jitter RF source with a level range of -4 dBm to +10 dBm to the clock input.
6) Connect a test signal to the analog inputs. Use $\mathrm{IN}+$ and IN - if the signal is differential, or $\mathrm{IN}+$ if the signal is single-ended ( $\pm 270 \mathrm{mV}$ (MAX101), $\pm 250 \mathrm{mV}$ (MAX101A) differential; see the MAX101 or MAX101A data sheet).
7) Observe the digitized results on the termination board pins by using a logic analyzer, such as the HP16500 series or an equivalent data-acquisition system. The outputs are 100k ECL compatible.

## Detailed Description

Board Set
The MAX101A EV kit is a two-board set. The main board contains ECL-interface circuitry and the MAX101A ADC. The termination board provides high-speed signal termination and access to the digital data. For further signal processing, the main board can be plugged into a larger system board via the provided EURO-card connector.

Clock Input
The external clock input is capacitively coupled to an onboard bias network. Take care to ensure that the pulse width is within the specified requirements: clock input levels should be -4 dBm to +10 dBm , and clock frequency can range from 250 MHz to 500 MHz . Figure 1 in the MAX101A data sheet shows the necessary timing requirements for the clock input, as well as the expected output clock waveforms. The clock input should be driven by a low-jitter RF signal source. Refer to Figures 1, 2, and 3 of the MAX101A data sheet for more information.

## Analog Input

Analog input to the MAX101A is made through one or both of the two SMA coaxial connectors provided (AIN+ and AIN- inputs). Each input is a direct connection to the ADC, with internal $50 \Omega$ terminations provided by the MAX101A.

Outputs
The MAX101A main board has two 8-bit-wide digital outputs that are 100k ECL compatible. Each data output is buffered by 100E116 line receivers. There is also a data clock output (DCLK) provided for timing. All 17 outputs provided to the EURO-card connector are differential and unterminated.
The termination board provides a termination for each data line, through $50 \Omega$ to -2 V .

## ADC Reference Resistor String

An on-board reference supply and op-amp circuit drive the ADC reference resistor string. The reference supplies can be adjusted using the four potentiometers on the board (see the Calibration Procedure). It is important to ensure that a reverse bias condition never occurs on the reference inputs. Schottky diode clamps on the reference amp outputs help protect the MAX101A.

DIV 10
The jumper DIV 10 selects the operating mode of the MAX101A, which can output data either at full speed or at $1 / 10$ the clock rate. This feature is valuable during initial testing. DIV 10 is usually left open for normal (full-

# MAX101A Evaluation Kit 

speed) operation.
Power Supplies The following supplies are required for normal operation of the main board:

$$
\begin{aligned}
& \mathrm{V}_{\mathrm{CC}}=+5 \mathrm{~V} \text { at } 0.8 \mathrm{~A} \\
& \mathrm{~V}_{\mathrm{EE}} \text { and } \mathrm{V}_{\mathrm{AA}}=-5.2 \mathrm{~V} \text { at } 2.5 \mathrm{~A}
\end{aligned}
$$

These voltages should be supplied to the connector pins for $\mathrm{V}_{\mathrm{CC}}$, $\mathrm{V}_{\mathrm{EE}}$, and $\mathrm{V}_{\mathrm{AA}}$, respectively. $\mathrm{V}_{\mathrm{EE}}$ and $\mathrm{V}_{\mathrm{AA}}$ are connected on the board with a ferrite bead. If system noise must be reduced, you may remove this bead and then provide the analog supply, $\mathrm{V}_{\mathrm{AA}}$, separately from the digital supply, VEE. The -5.2 V power supply should be the first supply turned on and the last supply turned off.

## Board Layout

The MAX101A requires proper PC board layout for device operation. This section explains the layout requirements and demonstrates how the EV kit achieves these goals.
Use power and ground planes to deliver power to the device, keeping the digital planes separate from the analog planes. The EV kit uses layers 3,4 , and 5 for power and ground planes. Tie digital ground and analog ground to a single point, as close to the power supply as possible. On the EV kit, digital ground ties to analog ground at ferrite bead L1. Likewise, tie digital power ( $\mathrm{V}_{\mathrm{EE}}$ ) and analog power ( $\mathrm{V}_{\mathrm{AA}}$ ) to a single point, as close to the power supply as possible. On the EV kit, digital power ties to analog -5.2 V power at ferrite bead L 2 .
Use transmission lines for the analog input, clocks, and high-speed digital outputs. The MAX101A EV kit uses microstrip lines of two different impedances. The MAX101A data outputs drive differential line drivers through $100 \Omega$ microstrip lines. The $50 \Omega$ microstrip lines occupy layers 1 and 2 . The $100 \Omega$ microstrip lines occupy layers 1 and 3, with layer 2 void. The kit uses FR4 epoxy dielectric material, whose relative dielectric constant is between 4.1 and 4.9. The nominal design is 0.0014 inch $(0.0355 \mathrm{~mm})$ foil thickness for each copper layer, and 0.011 inch ( 0.28 mm ) dielectric thickness between layers. The $50 \Omega$ microstrip lines have a signal trace width of $0.020 \mathrm{inch}(0.50 \mathrm{~mm})$, and the $100 \Omega$
microstrip lines have a signal trace width of 0.010 inch ( 0.25 mm ). Refer to Motorola's MECL or ECLinPS data book for an introduction to interconnect design.
Due to the high-speed nature of this part, the propagation delay of the PC board traces becomes a significant design consideration. For the EV kit design, the propagation delay is approximately 145 ps per inch $(5.7 \mathrm{ps} / \mathrm{mm})$. For best results, try to match the lengths of the data traces to within 0.5 inch ( 12 mm ). The clock signal must be routed on one layer only, without using any through-hole vias. The MAX101A EV kit is a controlled impedance board ( $50 \Omega$ and $100 \Omega$ ) and has a total board thickness of 0.062 inches ( 1.57 mm ) using six copper layers (see Figure 1, the Layer Profile).

Evaluating the MAX101
The MAX101A EV kit also can be used to evaluate the MAX101.
To use the MAX101, refer to specific instructions in the Quick Start, Applications Information, and Calibration Procedure sections.

| Copper Layer 1 | Copper thickness = 0.0007" (1/2 oz <br> copper) (microstrip signals) |
| :--- | :--- |
| Epoxy FR4 | Dielectric layer thickness = 0.011" |
| Copper Layer 2 | Copper thickness = 0.0014" (1 oz copper) <br> (50 $\Omega$ microstrip return; ground plane) |
| Epoxy FR4 | Dielectric layer thickness = 0.011" |
| Copper Layer 3 | Copper thickness = 0.0014" (1 oz copper) <br> (100 2 microstrip return; ground plane) |
| Epoxy FR4 | Dielectric layer thickness = 0.011" |
| Copper Layer 4 | Copper thickness = 0.0014" (1 oz copper) <br> (VCc/VTT power plane) |
| Epoxy FR4 | Dielectric layer thickness = 0.011" |
| Copper Layer 5 | Copper thickness = 0.0014" (1 oz copper) <br> (VEE/VAA power plane) |
| Epoxy FR4 | Dielectric layer thickness = 0.011" |
| Copper Layer 6 | Copper thickness $=0.0014 " ~(1 ~ o z ~ c o p p e r) ~$ <br> (DC signal layer) |

Figure 1. MAX101A Evaluation Board Layer Thickness Profile

## MAX101A Evaluation Kit

## Applications Information

Analog Input
The main board digitizes single-ended signals by choosing either input and leaving the other input either open or terminated in the system characteristic impedance. In this mode the unused input can provide a DC offset to the incoming signal. (See the Electrical Characteristics in the MAX101A data sheet for this DC voltage range.)
To obtain a digital output of all ones (11....1) with differential input drive for the MAX101, 270 mV must be applied between AIN+ and AIN-. That is, AIN+ $=+135 \mathrm{mV}$ and AIN- $=-135 \mathrm{mV}$ (when no DC offset is applied). Mid-scale digital output code occurs when there is no voltage difference across the analog inputs. Zero-scale digital output code, with differential drive for the MAX101, occurs when AIN $+=-135 \mathrm{mV}$ and AIN- $=+135 \mathrm{mV}$. The output of the converter stays at all ones (full scale) or all zeros (zero scale) when overranged or underranged, respectively. - Tables 1a and 1b show these relationships for both the MAX101 and the MAX101A.

Digital Outputs
Data from the ADC is interleaved and is output on alternate clock phases. One 8 -bit word is output during one clock phase and the other is output on the alternate clock

Table 1a. MAX101 Input Voltage Range

| INPUT | AIN+ ${ }^{\star}$ | AIN-* | $\begin{array}{c}\text { OUTPUT } \\ \text { CODE }\end{array}$ | $\begin{array}{c}\text { MSB TO } \\ \text { LSB }\end{array}$ |
| :--- | :---: | :---: | :---: | :---: |
| Differential | $\begin{array}{c}+135 \mathrm{mV} \\ 0 \\ -135 \mathrm{mV}\end{array}$ | $\begin{array}{c}-135 \mathrm{mV} \\ 0 \\ +135 \mathrm{mV}\end{array}$ | $\begin{array}{c}11111111 \\ 10000000 \\ 00000000\end{array}$ | $\begin{array}{c}\text { full scale } \\ \text { mid scale } \\ \text { zero scale }\end{array}$ |
| $\begin{array}{l}\text { Single } \\ \text { Ended }\end{array}$ | +270 mV | 0 | 11111111 | full scale |
| 0 |  |  |  |  |$)$

Table 1b. MAX101A Input Voltage Range

| INPUT | AIN+* | AIN-* | OUTPUT <br> CODE | MSB TO <br> LSB |
| :--- | :---: | :---: | :---: | :---: |
| Differential | +125 mV <br> 0 <br> -125 mV | -125 mV <br> +125 mV | 11111111 | full scale <br> 00000000 <br> mid scale <br> zero scale |
| Single | +250 mV | 0 | 11111111 | full scale |
| Ended | 0 | 0 | 10000000 | mid scale |
| -250 mV | 0 | 00000000 | zero scale |  |

*An offset $\mathrm{V}_{\mathrm{IO}}$, as specified in the DC Electrical Characteristics, will be present at the input. Compensate for this offset by either adjusting the reference voltages $\mathrm{VA}_{R T}$, $\mathrm{VA}_{R B}$, VBRT, $\mathrm{VB} B_{R B}$, or introduce an offset voltage in one of the input terminals, $\mathrm{AIN}+$ or AIN-.
phase. The two 8-bit-wide data paths are buffered by 100E116 line receivers, which provide a differential output, available at the connector. If the termination board is not used, the user must provide proper ECL termination at the EURO-card connector.

## Input Reference-Resistor Strings

Operational amplifiers are used to drive the top and bottom inputs of each of the ADC reference resistor chains. A 2.5 V reference is resistor-divided down and buffered through two MAX412CPA op amps. (The relatively low input impedance of each string, $120 \Omega$, will draw approximately 17 mA .) The reference voltage is set at the factory for either the MAX101 or MAX101A. This reference controls the comparator input windows, and can be adjusted between $\pm 1.20 \mathrm{~V}$ to accommodate input requirements. (Accuracy specifications are guaranteed with a reference of $\pm 1.02 \mathrm{~V}$ (MAX101) or $\pm 0.95 \mathrm{~V}$ (MAX101A).)

Testing
We recommend that a digital acquisition instrument like the HP16500 series of logic analyzers be used to acquire and process the output data. At Maxim, the data acquired from the converter is evaluated in an effective-bits software program developed in-house. The effective-bits measurement is a good tool to determine and compare ADC accuracy. See the MAX101A data sheet for more details on effective-bits testing.

## Calibration Procedure

The MAX101 EV kit comes calibrated and ready to operate from the factory. If other MAX101A devices are to be used in the same fixture, the EV kit should be recalibrated according to the following procedure:

1) With the ADC removed, adjust the +5 V and -5.2 V power supplies.
2) Adjust the PHASE potentiometer (R26) to a nominal voltage of 0 V . A test point (TP1) for this voltage measurement is located near the potentiometer.
3) With the power off, insert the MAX101A into the board. The device's heatsink fits down through the board, and its leads rest on top of the board. Take care to place the part in the board with Pin 1 in the correct location. Pin 1 is indicated by a small dot near the U1 device designation.
4) Turn the power on, observing proper sequencing, and let the part warm up for several minutes. Use a fan to ensure 200 lineal feet/min airflow. Repeat Step 2.

## MAX101A Evaluation Kit

5) After the part has warmed up for several minutes, adjust the reference voltages to the values shown in Tables 2 a and 2 b . These tables list the reference voltages, the trim pots that control the reference voltages, and the measurement points.
6) Adjust the A converter mid-code level. With no analog input (AIN+ - (AIN-) $=0 \mathrm{~V}$ ), the output code should match that specified in Table 1. If there is an offset, adjust either the positive or negative reference (R3 or R4) until the expected code of 10000000 (MSB to LSB) is achieved. After adjusting to the proper level, the references need to be balanced to the proper values shown in Tables $2 a$ and $2 b$, around any offset that was introduced. (If the negative reference was moved by +32 mV , the positive reference must be moved by that same amount to ensure the correct LSB size.) It may be necessary to repeat the reference offset adjustment again after the correct differential reference voltage is re-established around a common-mode offset.
7) Repeat Step 6 for the $B$ converter reference voltages. (The adjustment pots of the B converter are R14 and R15.)
8) Adjust the phase potentiometer (R26) for best effective bits performance (optional). While digitizing a pure sine-wave input, compute the effectivebits performance of the interleaved output data. Good performance can be achieved with the PHADJ voltage set to OV (Step 2); however, maximum performance can be achieved by adjusting the sampling delay with R26 as required.

Table 2a. MAX101 Reference Adjustments

| REFERENCE <br> VOLTAGE | CONVERTER | TRIM <br> POT | MEASURE AT <br> DEVICE SIDE OF: |
| :---: | :---: | :---: | :---: |
| +1.02 V | A | R 3 | R 5 |
| -1.02 V | A | R 4 | R 8 |
| +1.02 V | B | R 14 | R 16 |
| -1.02 V | B | R 15 | R 19 |

Table 2b. MAX101A Reference Adjustments

| REFERENCE <br> VOLTAGE | CONVERTER | TRIM <br> POT | MEASURE AT <br> DEVICE SIDE OF: |
| :---: | :---: | :---: | :---: |
| +0.95 V | A | R 3 | R 5 |
| -0.95 V | A | R 4 | R 8 |
| +0.95 V | B | R 14 | R 16 |
| -0.95 V | B | R 15 | R 19 |

## MAX101A Evaluation Kit



Figure 2. MAX101A EV Kit Schematic
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## MAX101A Evaluation Kit



VLOLXVW/LOLXVW :səlenןe^ヨ

Figure 2. MAX101A EV Kit Schematic (continued)
MノXIAV

## MAX101A Evaluation Kit



Figure 2. MAX101A EV Kit Schematic (continued)
8

## MAX101A Evaluation Kit



Figure 2. MAX101A EV Kit Schematic (continued)
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## MAX101A Evaluation Kit



Figure 2. MAX101A EV Kit Schematic (continued)

## MAX101A Evaluation Kit




Figure 2. MAX101A EV Kit Schematic (continued)

## MAX101A Evaluation Kit



Figure 2. MAX101A EV Kit Schematic (continued)
12

## MAX101A Evaluation Kit



Figure 3. MAX101A EV Kit Main Board Component Placement Guide-Component Side


Figure 5. MAX101A EV Kit Main Board Layout—Layer 1


Figure 4. MAX101A EV Kit Main Board Component Placement Guide-Solder Side


Figure 6. MAX101A EV Kit Main Board Layout-Layer 2 (Negative Image)

MAX101A Evaluation Kit
Evaluates: MAX101/MAX101A


Figure 7. MAX101A EV Kit Main Board Layout-Layer 3 (Negative Image)


Figure 9. MAX101A EV Kit Main Board Layout-Layer 5 (Negative Image)


Figure 8. MAX101A EV Kit Main Board Layout-Layer 4 (Negative Image)


Figure 10. MAX101A EV Kit Main Board Layout-Layer 6

## MAX101A Evaluation Kit



Figure 11. MAX101A EV Kit Main Board Mechanical Guide


Figure 13. MAX101A EV Kit Termination Board Component Placement Guide-Solder Side

|  | TERM BOARD SIGNAL | M AXI00EVKIT | MAX101EVKIT |
| :---: | :---: | :---: | :---: |
|  | T1 | B0 | A0 |
|  | F1 | $\overline{\text { B0 }}$ | $\overline{A 0}$ |
|  | T2 | A0 | A1 |
|  | F2 | A0 | $\overline{\text { A1 }}$ |
|  | т3 | B1 | A2 |
|  | F3 | $\overline{B 1}$ | $\overline{\text { A2 }}$ |
|  | T4 | A1 | ${ }^{\text {A3 }}$ |
|  | F4 | AT | ${ }^{\text {A }}$ |
|  | T5 | $\frac{B 2}{82}$ | A4 |
|  | F5 | $\overline{\text { B2 }}$ | $\overline{\text { A4 }}$ |
|  | ${ }^{\text {T6 }}$ | ${ }^{\text {A2 }}$ | A5 |
|  | F6 | $\overline{\text { A2 }}$ | $\overline{\text { A5 }}$ |
|  | F7 | ${ }^{\text {B3 }}$ | ${ }^{\text {A }}$ G |
|  | F7 | $\overline{\text { B3 }}$ | $\overline{\text { A6 }}$ |
|  | T8 | ${ }^{\text {A3 }}$ | DCLK |
|  | F8 | $\overline{\text { A3 }}$ | $\overline{\text { DCLK }}$ |
|  | T9 | B4 | A7 |
|  | F9 | $\overline{84}$ | $\overline{\text { A7 }}$ |
|  | T10 | A4 | $\frac{B 7}{87}$ |
|  | F10 | $\overline{\text { A4 }}$ | $\overline{B 7}$ |
|  | T11 | B5 | ${ }^{\text {B6 }}$ |
|  | F11 | $\overline{\text { B5 }}$ | $\overline{\text { B6 }}$ |
|  | T12 | A5 | ${ }^{\text {B5 }}$ |
|  | F12 | $\overline{\text { A5 }}$ | $\overline{85}$ |
|  | T13 | ${ }^{\text {B6 }}$ | ${ }^{\text {B4 }}$ |
|  | F13 | $\overline{\text { B6 }}$ | $\overline{84}$ |
|  | T14 | ${ }^{\text {A } 6}$ | $\frac{B 3}{\square 3}$ |
|  | F14 | $\overline{\text { A6 }}$ | $\overline{\text { B3 }}$ |
|  | T15 | ${ }^{\text {B7 }}$ | B2 |
|  | F15 | $\overline{B 7}$ | $\overline{B 2}$ |
|  | T16 | A7 | B1 |
|  | F16 | $\overline{\text { A }}$ | $\overline{B 1}$ |
|  | T17 | DCLK | B0 |
|  | F17 | DCLK | $\overline{B 0}$ |

Figure 12. MAX101A EV Kit Termination Board Component Placement Guide-Component Side


Figure 14. MAX101A EV Kit Termination Board Layout-Layer 1

## MAX101A Evaluation Kit

## Evaluates: MAX101/MAX101A



Figure 15. MAX101A EV Kit Termination Board Layout-Layer 2


Figure 17. MAX101A EV Kit Termination Board Layout-Layer 4


Figure 16. MAX101A EV Kit Termination Board Layout—Layer 3


Figure 18. MAX101A EV Kit Termination Board Mechanical Guide

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