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Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

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EVALUATION KIT AVAILABLE

Dual RF LDMOS Bias Controller with Nonvolatile Memory

General Description

The MAX11008 controller biases RF LDMOS power devices found in cellular base stations and other wireless infrastructure equipment. Each controller includes a high-side current-sense amplifier with programmable gains of 2, 10, and 25 to monitor the LDMOS drain current over a range of 20mA to 5A. The MAX11008 supports up to two external diode-connected transistors to monitor the LDMOS temperatures while an internal temperature sensor measures the local die temperature. A 12-bit successive-approximation register (SAR) analog-to-digital converter (ADC) converts the analog signals from the programmable-gain amplifiers (PGAs), external temperature sensors, internal temperature measurement, and two additional auxiliary inputs. The MAX11008 automatically adjusts the LDMOS bias voltages by applying temperature, AIN, and/or drain current samples to data stored in lookup tables (LUTs).

The MAX11008 includes two gate-drive channels, each consisting of a 12-bit DAC to generate the positive gate voltage for biasing the LDMOS devices. Each gate-drive output supplies up to ±2mA of gate current. The gate-drive amplifier is current-limited to ±25mA and features a fast clamp to AGND.

The MAX11008 contains 4Kb of on-chip, nonvolatile EEPROM organized as 256 bits x 16 bits to store LUTs and register information. The device operates from either a 4-wire 16MHz SPI™-/MICROWIRE™-compatible or an I²C-compatible serial interface.

The MAX11008 operates from a +4.75V to +5.25V analog supply with a typical supply current of 2mA, and a +2.7V to +5.25V digital supply with a typical supply of 3mA. The device is packaged in a 48-pin, 7mm x 7mm, thin QFN package and operates over the extended (-40°C to +85°C) temperature range.

Applications

Cellular Base Stations

Microwave Radio Links

Feed-Forward Power Amps

Transmitters

Industrial Process Control

Features

- **On-Chip 4Kb EEPROM for Storing LDMOS Bias Characteristics**
- **Integrated High-Side Current-Sense PGA with Gain of 2, 10, or 25**
- **±0.75% Accuracy for Sense Voltage Between +75mV and +1250mV**
- **Full-Scale Sense Voltage**
  - **+100mV with a Gain of 25**
  - **+250mV with a Gain of 10**
  - **+1250mV with a Gain of 2**
- **Common-Mode Range, LDMOS Drain Voltage: +5V to +32V**
- **Adjustable Low-Noise 0 to AV_{DD} Output Gate Bias Voltage Range**
- **Fast Clamp to AGND for LDMOS Protection**
- **12-Bit DAC Control of Gate with Temperature**
- **Internal Die Temperature Measurement**
- **2-Channel External Temperature Measurement through Remote Diodes**
- **Internal 12-Bit ADC Measurement for Temperature, Current, and Voltage Monitoring**
- **User-Selectable Serial Interface**
  - **400kHz/1.7MHz/3.4MHz I²C-Compatible Interface**
  - **16MHz SPI-/MICROWIRE-Compatible Interface**

Ordering Information

PART	PIN-PACKAGE	TEMP ERROR (°C)
MAX11008BETM+	48 TQFN-EP*	±3

+Denotes a lead-free/RoHS-compliant package.
**EP = Exposed pad.*

Note: *The device is specified over the -40°C to +85°C operating temperature range.*

SPI is a trademark of Motorola, Inc.

MICROWIRE is a trademark of National Semiconductor Corp.

Dual RF LDMOS Bias Controller with Nonvolatile Memory

ABSOLUTE MAXIMUM RATINGS

AV_{DD} to AGND .....-0.3V to +6V
DV_{DD} to DGND.....-0.3V to +6V
AGND to DGND.....-0.3V to +0.3V
CS_+, CS_- to AGND .....-0.3V to +34V
CS_+ to CS_-
If CS_+ > 6V .....-0.3V to +6V
If CS_+ ≤ 6V .....-0.3V to V_{CS_-}
Analog Inputs/Outputs to AGND.....
.....-0.3V to the lower of (AV_{DD} + 0.3V) and +6V
Digital Inputs/Outputs to DGND
(except SDA/DIN and SCL/SCLK).....
.....-0.3V to the lower of (DV_{DD}+ 0.3V) and +6V
SDA/DIN and SCL/SCLK to DGND .....-0.3V to +6V
Continuous Input Current (all terminals).....±50mA
Continuous Power Dissipation (T_A = +70°C)
48-Pin, 7mm x 7mm, TQFN (derate 27.8mW/°C above +70°C).....2222.2mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CS_+} = +32V, AV_{DD} = DV_{DD} = +5V ±5%, external V_{REFADC} = +2.5V, external V_{REFDAC} = +2.5V, C_{REF} = 0.1µF, $C_{GATE\_}$ = 0.1nF, V_{SENSE} = V_{CS_+} - V_{CS_-}, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
HIGH-SIDE CURRENT-SENSE PGA						
Common-Mode Input Voltage Range	V_{CS1+}, V_{CS2+}		5		32	V
Common-Mode Rejection Ratio	CMRR	5V < V_{CS_+} < 32V		110		dB
CS_+ Input Bias Current	I_{CS_+}	V_{SENSE} < 100mV over the common-mode range		135	195	µA
CS_- Input Bias Current	I_{CS_-}	V_{SENSE} < 100mV over the common-mode range			±1	µA
Full-Scale Sense Voltage Range	V_{SENSE}	Gain = 25	0		100	mV
		Gain = 10	0		250	
		Gain = 2	0		1250	
Minimum Sense Voltage Range for ±0.75% V_{SENSE} Accuracy		Gain = 25	75		100	mV
		Gain = 10	75		250	
		Gain = 2	75		1250	
Minimum Sense Voltage Range for ±2.5% V_{SENSE} Accuracy		Gain = 25	20		100	mV
		Gain = 10	20		250	
		Gain = 2	20		1250	
Total PGAOUT Voltage Error		V_{SENSE} = 75mV		±0.1	±0.75	%
PGAOUT Capacitive Load	C_{PGAOUT}				50	pF
PGAOUT Settling Time	t_{HSCS}	(Note 1)		< 25		µs
Saturation Recovery Time		Settles to within ±0.5% accuracy from V_{SENSE} = 3 x full scale		< 45		µs

ELECTRICAL CHARACTERISTICS (continued)

(V_{CS_+} = +32V, AV_{DD} = DV_{DD} = +5V ±5%, external V_{REFADC} = +2.5V, external V_{REFDAC} = +2.5V, C_{REF} = 0.1µF, $C_{GATE\_}$ = 0.1nF, V_{SENSE} = V_{CS_+} - V_{CS_-}, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LDMOS GATE DRIVER (Gain = 2)						
Output Gate-Drive Voltage Range	$V_{GATE\_}$	$I_{GATE\_}$ = ±0.1mA	0.1		AV_{DD} - 0.1	V
		$I_{GATE\_}$ = ±2mA	0.75		AV_{DD} - 0.75	
Output Impedance	$R_{GATE\_}$	Measured at DC		0.1		Ω
GATE_ Settling Time	$t_{GATE\_}$	R_S = 500Ω, $C_{GATE\_}$ = 15µF, $V_{GATE\_}$ = 0.5V to 4.5V (Note 1)		45		ms
Output Capacitive Load	$C_{GATE\_}$	R_{SERIES} = 0Ω	0		0.5	nF
		R_{SERIES} = 500Ω	0	15,000		
GATE_ Noise		1kHz to 1MHz		1000		$µV_{P-P}$
Maximum Power-On Transient				±100		mV
Output Short-Circuit Current Limit	I_{SC}	1s, sinking or sourcing		±25		mA
Total Unadjusted Error	TUE	Worst case at CODE = 4063, use external reference (Note 2)		±7	±25	mV
Total Unadjusted Error without Offset	TUE_{NO_OFFSET}	CalCODE = 2457, MaxCODE = 2867, use external reference, T_A = +25°C (Note 2)			±8	mV
Drift		Gain = 2, MaxCODE = 2867 (Note 2)		±15		µV/°C
Clamp to Zero Delay		$C_{GATE\_}$ = 0.5nF (Note 3)		1		µs
Output-Safe Switch On-Resistance	R_{OPSW}	$V_{GATE\_}$ clamped to AGND (Note 4)		300		Ω
MONITOR ADC (DC characteristics)						
Resolution	N_{ADC}		12			Bits
Differential Nonlinearity	DNL_{ADC}	(Note 5)	-2		+2	LSB
Integral Nonlinearity	INL_{ADC}				±2	LSB
Offset Error				±2	±4	LSB
Gain Error		(Note 6)		±2	±4	LSB
Gain Temperature Coefficient				±0.4		ppm/°C
Offset Temperature Coefficient				±0.4		ppm/°C
MONITOR ADC DYNAMIC CHARACTERISTICS (1kHz sine-wave input, $2.5V_{P-P}$, up to 94.4ksps)						
Signal-to-Noise Plus Distortion	SINAD			70		dB
Total Harmonic Distortion	THD	Up to 5th harmonic		-82		dBc
Spurious-Free Dynamic Range	SFDR			86		dBc
Intermodulation Distortion	IMD	f_{IN1} = 0.99kHz, f_{IN2} = 1.02kHz		76		dBc
Full-Power Bandwidth		-3dB		1		MHz
Full-Linear Bandwidth		SINAD > 68dB		100		kHz

Dual RF LDMOS Bias Controller with Nonvolatile Memory

ELECTRICAL CHARACTERISTICS (continued)

(V_{CS_+} = +32V, AV_{DD} = DV_{DD} = +5V ±5%, external V_{REFADC} = +2.5V, external V_{REFDAC} = +2.5V, C_{REF} = 0.1µF, $C_{GATE\_}$ = 0.1nF, V_{SENSE} = V_{CS_+} - V_{CS_-}, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
MONITOR ADC CONVERSION RATE						
Power-Up Time (External Reference)	t_{PUEXT}			1.1		µs
Power-Up Time (Internal Reference)	t_{PUINT}			70		µs
Acquisition Time	t_{ACQ}			0.5		µs
Conversion Time	t_{CONV}	Internally clocked, T_A = +25°C			10	µs
Aperture Delay	t_{AD}			20		ns
MONITOR ADC ANALOG INPUT (ADCIN1, ADCIN2)						
Input Voltage Range	V_{ADCIN}	Relative to AGND (Note 7)	0		V_{REFADC}	V
Input Leakage Current		V_{IN} = 0 and V_{IN} = V_{AVDD}		±0.01		µA
Input Capacitance	C_{ADCIN}			34		pF
TEMPERATURE MEASUREMENTS						
Internal Sensor Measurement Error		T_A = +25°C		±0.25		°C
		T_A = T_{MIN} to T_{MAX} (Note 8)		±1.5	±3	
External Sensor Measurement Error (Note 9)		T_A = +25°C		±1		°C
		T_A = T_{MIN} to T_{MAX}		±3		
Relative Temperature Accuracy		T_A = T_{MIN} to T_{MAX} (Note 9)		±0.4		°C
Temperature Resolution				1/8		°C/LSB
External Diode Drive Current (Low)			3.25	4		µA
External Diode Drive Current (High)				68	75	µA
INTERNAL REFERENCE						
REFADC/REFDAC Output Voltage	V_{REFADC}, V_{REFDAC}	T_A = +25°C	2.49	2.50	2.51	V
REFADC/REFDAC Temperature Coefficient	TC_{REFADC}, TC_{REFDAC}			±15		ppm/°C
REFADC/REFDAC Output Impedance				6.5		kΩ
Capacitive Bypass at REFADC/REFDAC			270			pF
Power-Supply Rejection Ratio	PSRR	AV_{DD} = 5V ± 5%		64		dB
EXTERNAL REFERENCE						
REFADC Input Voltage Range	V_{REFADC}		1.0		AV_{DD}	V
REFADC Input Current	I_{REFADC}	V_{REFADC} = 2.5V, f_{SAMPLE} = 100ksps		60	80	µA
		Acquisition/between conversions		±0.01		
REFDAC Input Voltage Range	V_{REFDAC}		0.7		2.5	V
REFDAC Input Current		Static current when the DAC is not calibrated		0.1		µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{CS_+} = +32V, AV_{DD} = DV_{DD} = +5V ±5%, external V_{REFADC} = +2.5V, external V_{REFDAC} = +2.5V, C_{REF} = 0.1µF, $C_{GATE\_}$ = 0.1nF, V_{SENSE} = V_{CS_+} - V_{CS_-}, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
GATE-DRIVER DAC DC ACCURACY						
Resolution	N_{DAC}		12			Bits
Integral Nonlinearity	INL_{DAC}	Measured at GATE_		±2	±4	LSB
Differential Nonlinearity	DNL_{DAC}	Guaranteed monotonic (Note 10)			±1	LSB
DIGITAL INPUTS (SCL/SCLK, SDA/DIN, A0/$\overline{CS}$, A1/DOUT, A2/N.C., $\overline{CNVST}$, OPSAFE1, OPSAFE2)						
Input High Voltage	V_{IH}	SDA/DIN and SCL/SCLK only	0.7 x DV_{DD}			V
		A0/$\overline{CS}$, A1/DOUT, A2/N.C., $\overline{CNVST}$, OPSAFE1, OPSAFE2 only	2.3			
Input Low Voltage	V_{IL}	SDA/DIN and SCL/SCLK only			0.3 x DV_{DD}	V
		A0/$\overline{CS}$, A1/DOUT, A2/N.C., $\overline{CNVST}$, OPSAFE1, OPSAFE2 only			0.7	
Input Hysteresis	V_{HYS}	SDA/DIN and SCL/SCLK only	0.08 x DV_{DD}			V
Input Leakage Current		Digital inputs at 0 or V_{DVDD}		±0.1	±1	µA
Input Capacitance	C_{IN}			5		pF
DIGITAL OUTPUTS (SDA/DIN, ALARM, BUSY, DOUT)						
Output High Voltage	V_{OH}	ALARM and BUSY only, I_{SOURCE} = 0.2mA	DV_{DD} - 0.4V			V
Output Low Voltage	V_{OL}	SDA/DIN and A1/DOUT, I_{SINK} = 3mA, (Note 11)			0.4	V
		ALARM and BUSY only, I_{SINK} = 0.3mA			0.3	
Three-State Leakage	I_{IL}	Digital inputs at 0 or DV_{DD}		±0.1	±1	µA
Three-State Capacitance				5		pF
POWER SUPPLIES (Note 12)						
Analog Supply Voltage Range	AV_{DD}		4.75		5.25	V
Digital Supply Voltage Range	DV_{DD}		2.7		AV_{DD} + 0.3	V
Analog Supply Current	I_{AVDD}	AV_{DD} = 5V		2	4	mA
		Shutdown (Note 13)		0.4	2	µA
Digital Supply Current	I_{DVDD}	DV_{DD} = 5V		3	6	mA
		Shutdown		2	32	µA

Dual RF LDMOS Bias Controller with Nonvolatile Memory

SPI TIMING CHARACTERISTICS (Notes 14, 15, Figure 1)

(DV_{DD} = +2.7V to +5.25V, AV_{DD} = +4.75V to +5.25V, V_{DGND} = V_{AGND} = 0, external V_{REFADC} = +2.5V, external V_{REFDAC} = +2.5V, C_{REF} = 0.1µF, T_A = -40°C to +85°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLK Clock Period	t_{CP}		62.5			ns
SCLK High Time	t_{CH}		25			ns
SCLK Low Time	t_{CL}		25			ns
DIN to SCLK Rise Setup Time	t_{DS}		15			ns
DIN to SCLK Rise Hold Time	t_{DH}		0			ns
SCLK Fall to DOUT Transition	t_{DO}	C_L = 30pF			20	ns
$\overline{CS}$ Fall to DOUT Enable	t_{DV}	C_L = 30pF			50	ns
$\overline{CS}$ Rise to DOUT Disable	t_{TR}	C_L = 30pF (Note 16)			50	ns
$\overline{CS}$ Rise or Fall to SCLK Rise	t_{CSS}		12.5			ns
$\overline{CS}$ Pulse-Width High	t_{CSW}		50			ns
Last SCLK Rise to $\overline{CS}$ Rise	t_{CSH}		0			ns

I²C SLOW-/FAST-MODE TIMING CHARACTERISTICS (Notes 14, 15, Figure 4)

(DV_{DD} = +2.7V to +5.25V, AV_{DD} = +4.75V to +5.25V, V_{DGND} = V_{AGND} = 0, external V_{REFADC} = +2.5V, external V_{REFDAC} = +2.5V, C_{REF} = 0.1µF, T_A = -40°C to +85°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}		0		400	kHz
Bus Free Time Between a STOP and START Condition	t_{BUF}		1.3			µs
Hold Time (Repeated) for START Condition	$t_{HD:STA}$	After this period, the first clock pulse is generated	0.6			µs
Setup Time for a Repeated START Condition	$t_{SU:STA}$		0.6			µs
SCL Pulse-Width Low	t_{LOW}		1.3			µs
SCL Pulse-Width High	t_{HIGH}		0.6			µs
Data Setup Time	$t_{SU:DAT}$		100			ns
Data Hold Time	$t_{HD:DAT}$	(Note 17)	0.004		0.9	µs
SDA, SCL Rise Time	t_R	Receiving (Note 18)	0		300	ns
SDA, SCL Fall Time	t_F	Receiving (Note 18)	0		300	ns
SDA Fall Time	t_F	Transmitting (Notes 18, 19)	20 + 0.1 x C_B		250	ns
Setup Time for STOP Condition	$t_{SU:STO}$		0.6			µs
Capacitive Load for Each Bus Line	C_B	(Note 20)			400	pF
Pulse Width of Spikes Suppressed by the Input Filter	t_{SP}	(Note 21)			50	ns

I²C HIGH-SPEED-MODE TIMING CHARACTERISTICS (Notes 14, 15, Figure 4)

(DV_{DD} = +2.7V to +5.25V, AV_{DD} = +4.75V to +5.25V, V_{DGND} = V_{AGND} = 0, external V_{REFADC} = +2.5V, external V_{REFDAC} = +2.5V, C_{REF} = 0.1µF, T_A = -40°C to +85°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	C_B = 100pF max		C_B = 400pF		UNITS
			MIN	MAX	MIN	MAX	
Serial Clock Frequency	f_{SCL}		0	3.4	0	1.7	MHz
Setup Time (Repeated) START Condition	$t_{SU:STA}$		160		160		ns
Hold Time (Repeated) START Condition	$t_{HD:STA}$		160		160		ns
SCL Pulse-Width Low	t_{LOW}		160		320		ns
SCL Pulse-Width High	t_{HIGH}		80		120		ns
Data Setup Time	$t_{SU:DAT}$		10		10		ns
Data Hold Time	$t_{HD:DAT}$	(Note 17)	4	70	4	150	ns
SCL Rise Time	t_{RCL}		10	40	20	80	ns
SCL Rise Time	t_{RCL1}	After a repeated START condition and after an acknowledge bit	10	80	20	160	ns
SCL Fall Time	t_{FCL}		10	40	20	80	ns
SDA Rise Time	t_{RDA}		10	80	20	160	ns
SDA Fall Time	t_{FDA}		10	80	20	160	ns
Setup Time for STOP Condition	$t_{SU:STO}$		160		160		ns
Capacitive Load for Each Bus Line	C_B	(Note 20)		100		400	ns
Pulse Width of Spikes Suppressed by the Input Filter	t_{SP}	(Note 21)	0	10	0	10	ns

MISCELLANEOUS TIMING CHARACTERISTICS (Note 15)

(DV_{DD} = +2.7V to +5.25V, AV_{DD} = +4.75V to +5.25V, V_{DGND} = V_{AGND} = 0, external V_{REFADC} = +2.5V, external V_{REFDAC} = +2.5V, C_{REF} = 0.1µF, T_A = -40°C to +85°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Minimum Time to Wait After a Write Command Before Reading Back Data from the Same Location	t_{RDBK}	(Note 22)		1		µs
$\overline{CNVST}$ Active-Low Pulse Width in ADC Clock Mode 01	t_{CNV01}		20			ns
$\overline{CNVST}$ Active-Low Pulse Width in ADC Clock Mode 11 to Initiate a Temperature Conversion	t_{CNV11}		20			ns
$\overline{CNVST}$ Active-Low Pulse Width in ADC Clock Mode 11 for ADCIN1/2 Acquisition	t_{ACQ11A}		1.5			µs
ADC Power-Up Time (External Reference)	t_{APUEXT}			1.1		µs
ADC Power-Up Time (Internal Reference)	t_{APUINT}			70		µs

Dual RF LDMOS Bias Controller with Nonvolatile Memory

MISCELLANEOUS TIMING CHARACTERISTICS (Note 15) (continued)

(DV_{DD} = +2.7V to +5.25V, AV_{DD} = +4.75V to +5.25V, V_{DGND} = V_{AGND} = 0, external V_{REFADC} = +2.5V, external V_{REFDAC} = +2.5V, C_{REF} = 0.1µF, T_A = -40°C to +85°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DAC Power-Up Time (External Reference)	t_{DPUEXT}			2		µs
DAC Power-Up Time (Internal Reference)	t_{DPUINT}			70		µs
Acquisition Time (Internally Timed in ADC Clock Modes 00 or 01)	t_{ACQ}				0.6	µs
Conversion Time (Internally Clocked)	t_{CONV}	Internally clocked, T_A = +25°C			10	µs
Delay to Start of Conversion Time	t_{CONVW}	(Note 23)		1.3		µs
Temperature Conversion Time (Internally Clocked)	t_{CONVT}			70		µs

Note 1: Output settles to within ±0.5% of final value.

Note 2: Total unadjusted errors are for the entire gate-drive channel including the 12-bit DAC, and the gate driver is measured at the GATE1 and GATE2 outputs.

Note 3: $V_{GATE\_}$ = V_{DD} - 0.1. Measured from when OPSAFE1 or OPSAFE2 is set high.

Note 4: During power-on-reset, the output safe switch is closed. The output safe switch is opened under user software control.

Note 5: Guaranteed to be 11 bits linearly accurate.

Note 6: Offset nulled.

Note 7: The absolute range for analog inputs is from 0 to V_{AVDD}.

Note 8: Internal temperature-sensor performance is guaranteed by design.

Note 9: The MAX11008 and the external sensor are at the same ambient temperature. External sensor measurement error is tested with a diode-connected 2N3904.

Note 10: Guaranteed monotonicity. Accuracy is degraded at lower V_{REFDAC}.

Note 11: SDA/DIN is an open-drain output only when in I^2C mode. A1/DOUT is an open-drain output only when in SPI mode.

Note 12: Supply-current limits are valid only when digital inputs are set to DGND or supply voltage. Timing specifications are only guaranteed when inputs are driven rail-to-rail.

Note 13: Shutdown supply currents are typically 0.4µA for AV_{DD}; maximum specification is limited by automated test equipment.

Note 14: All times are referred to the 50% point between V_{IH} and V_{IL} levels.

Note 15: Guaranteed by design. Not production tested.

Note 16: DOUT will go into three-state mode after the $\overline{CS}$ rising edge. Keep $\overline{CS}$ low long enough for the DOUT value to be sampled before it goes to three-state.

Note 17: A master device must provide a hold time of at least 300ns for the SDA signal (referred to V_{IL} of the SCL signal) to bridge the undefined region of SCL's falling edge.

Note 18: t_R and t_F measured between 0.3 x DV_{DD} and 0.7 x DV_{DD}.

Note 19: C_B = total capacitance of one bus line in pF. For bus loads between 100pF and 400pF, the timing parameters should be linearly interpolated.

Note 20: An appropriate bus pullup resistance must be selected depending on board capacitance.

Note 21: Input filters on the SDA and SCL inputs suppress noise spikes less than 50ns.

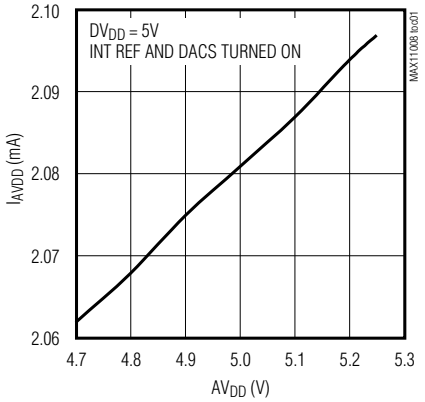
Note 22: When a command is written to the serial interface, the command is passed by the internal oscillator clock and executed. There is a small synchronization delay before the new value is written to the appropriate register. If the serial interface attempts to read the new value back before t_{RDBK}, the new data is not corrupted; however, the result of the read command may not reflect the new value.

Note 23: This is the minimum time from the end of a command before $\overline{CNVST}$ should be asserted. The time allows for the data from the preceding write to arrive and set up the chip in preparation for the $\overline{CNVST}$. The time need only be observed when the write affects the ADC controls. Failure to observe this time may lead to incorrect conversions (for example, conversion of the wrong ADC channel).

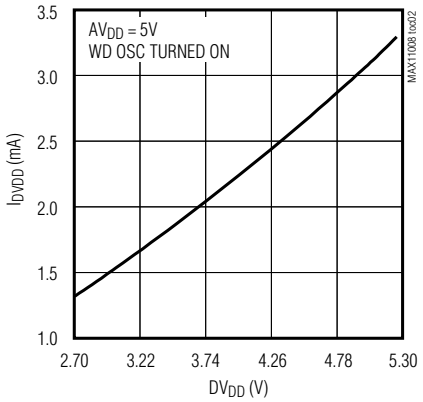
Typical Operating Characteristics

(AV_{DD} = DV_{DD} = 5V, external V_{REFADC} = 2.5V, external V_{REFDAC} = 2.5V, V_{CS_-} = V_{CS_+} = 32V, C_{REF} = 0.1µF, T_A = +25°C, unless otherwise noted.)

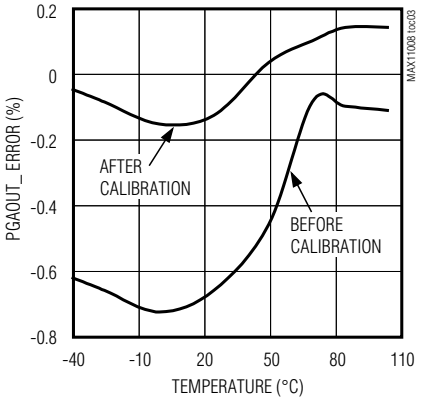
ANALOG SUPPLY CURRENT vs. SUPPLY VOLTAGE



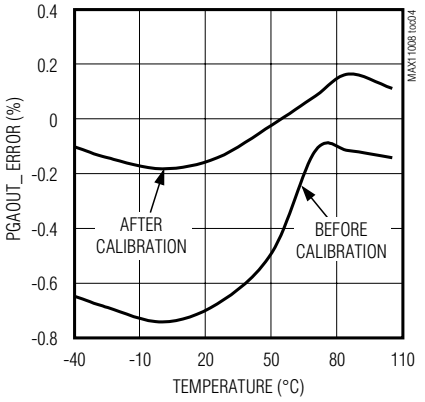
DIGITAL SUPPLY CURRENT vs. SUPPLY VOLTAGE



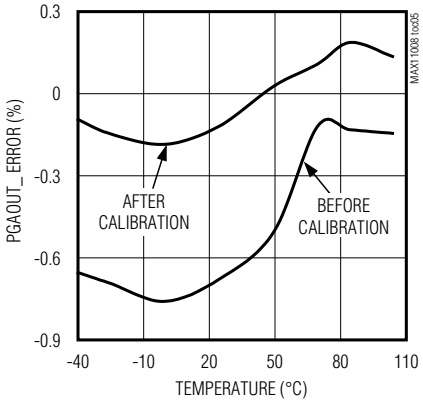
CURRENT-SENSE AMPLIFIER OUTPUT ERROR vs. TEMPERATURE (G = 2)



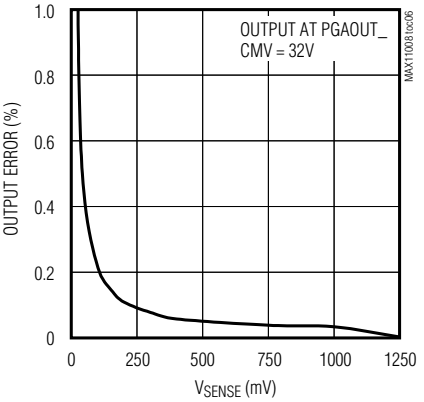
CURRENT-SENSE AMPLIFIER OUTPUT ERROR vs. TEMPERATURE (G = 10)



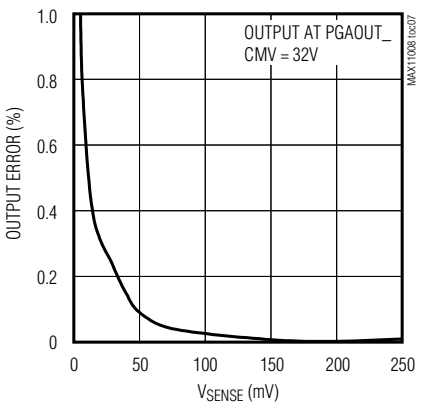
CURRENT-SENSE AMPLIFIER OUTPUT ERROR vs. TEMPERATURE (G = 25)



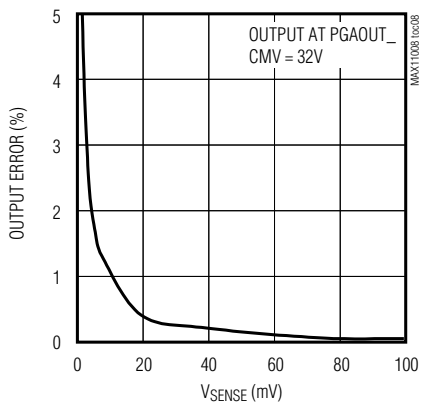
CURRENT-SENSE AMPLIFIER OUTPUT ERROR vs. SENSE VOLTAGE (G = 2)



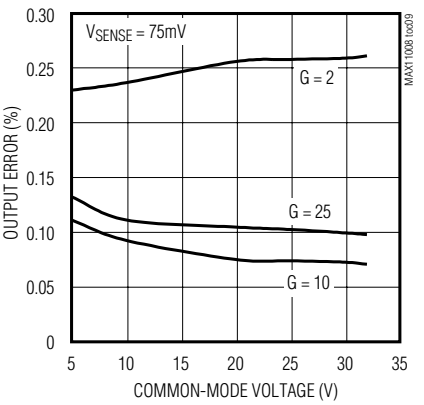
CURRENT-SENSE AMPLIFIER OUTPUT ERROR vs. SENSE VOLTAGE (G = 10)



CURRENT-SENSE AMPLIFIER OUTPUT ERROR vs. SENSE VOLTAGE (G = 25)



CURRENT-SENSE AMPLIFIER OUTPUT ERROR vs. CMV

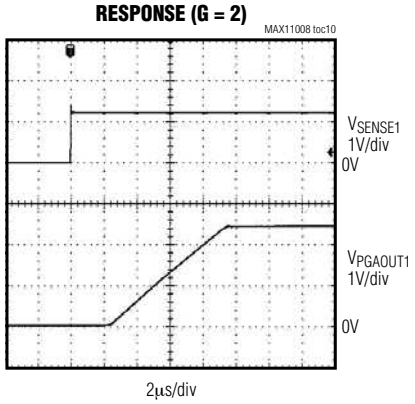


Dual RF LDMOS Bias Controller with Nonvolatile Memory

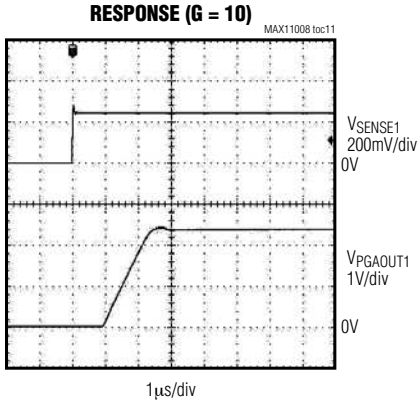
Typical Operating Characteristics (continued)

(AV_{DD} = DV_{DD} = 5V, external V_{REFADC} = 2.5V, external V_{REFDAC} = 2.5V, V_{CS_-} = V_{CS_+} = 32V, C_{REF} = 0.1µF, T_A = +25°C, unless otherwise noted.)

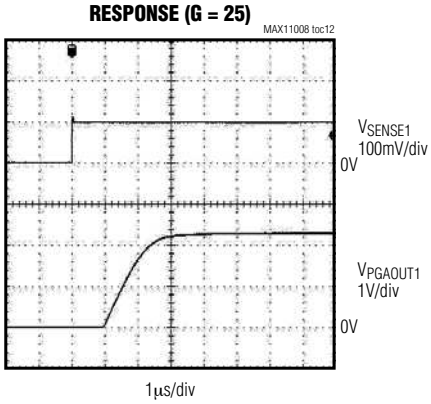
CURRENT-SENSE TRANSIENT RESPONSE (G = 2)



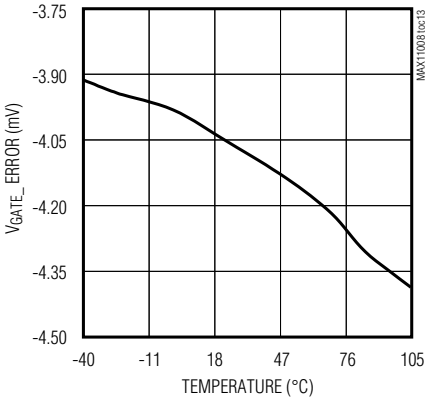
CURRENT-SENSE TRANSIENT RESPONSE (G = 10)



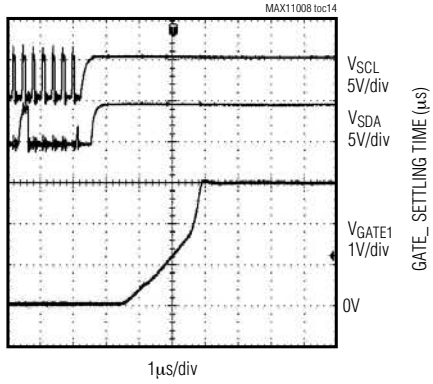
CURRENT-SENSE TRANSIENT RESPONSE (G = 25)



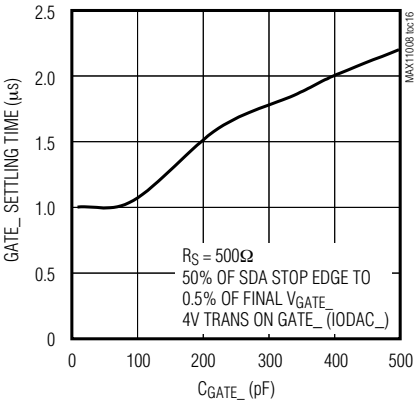
GATE VOLTAGE TOTAL UNADJUSTED ERROR vs. TEMPERATURE



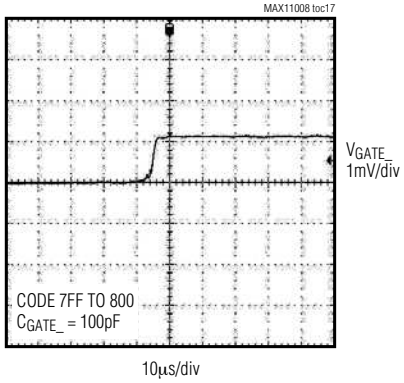
GATE POWER-UP TIME



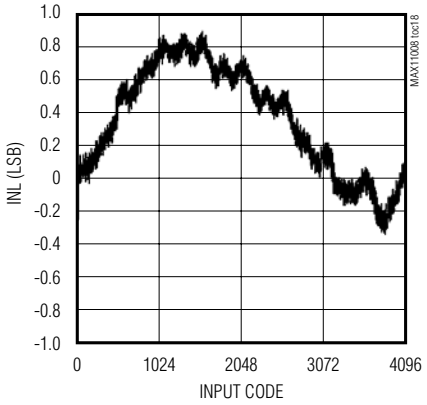
GATE_ SETTLING TIME vs. C_{GATE}



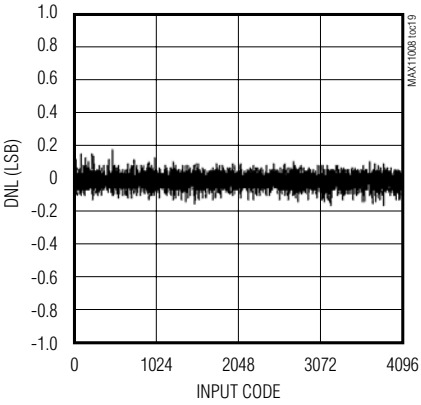
MAJOR CARRY TRANSITION GLITCH



DAC INTEGRAL NONLINEARITY vs. INPUT CODE



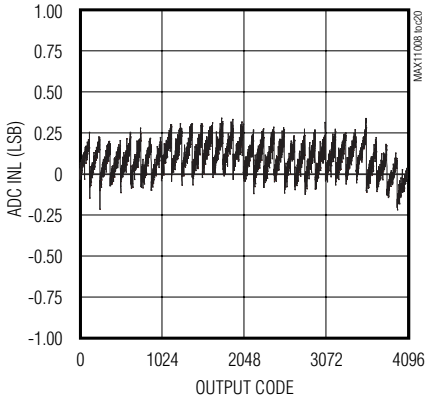
DAC DIFFERENTIAL NONLINEARITY vs. INPUT CODE



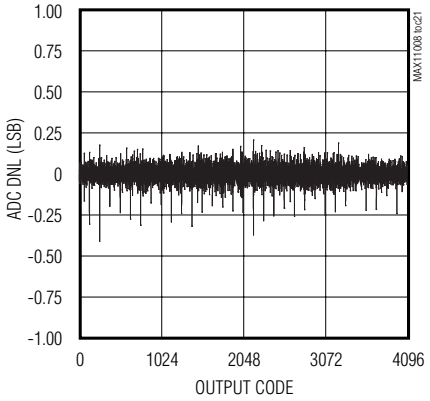
Typical Operating Characteristics (continued)

(AV_{DD} = DV_{DD} = 5V, external V_{REFADC} = 2.5V, external V_{REFDAC} = 2.5V, V_{CS_-} = V_{CS_+} = 32V, C_{REF} = 0.1µF, T_A = +25°C, unless otherwise noted.)

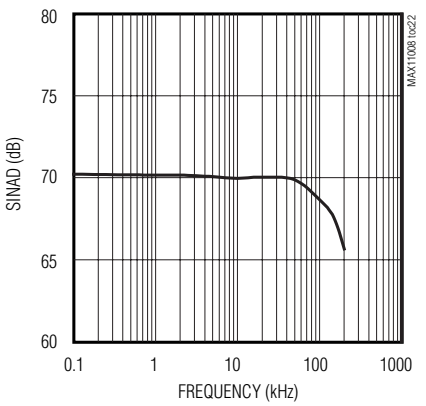
ADC INTEGRAL NONLINEARITY vs. OUTPUT CODE



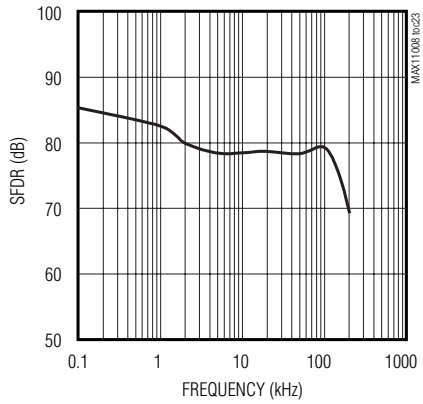
ADC DIFFERENTIAL NONLINEARITY vs. OUTPUT CODE



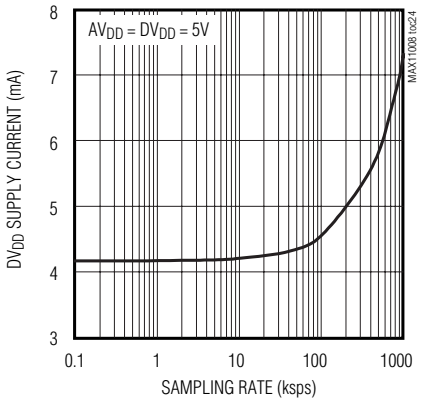
ADC SINAD vs. FREQUENCY



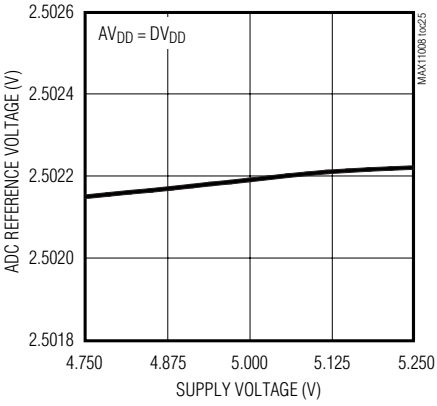
ADC SFDR vs. FREQUENCY



DIGITAL SUPPLY CURRENT vs. SAMPLING RATE



ADC INTERNAL REFERENCE VOLTAGE vs. SUPPLY VOLTAGE

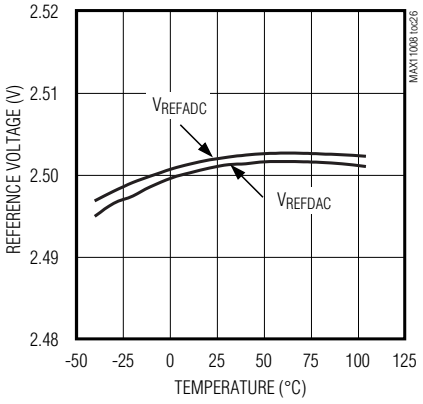


Dual RF LDMOS Bias Controller with Nonvolatile Memory

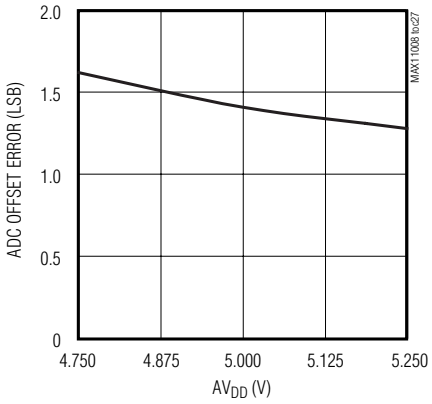
Typical Operating Characteristics (continued)

(AV_{DD} = DV_{DD} = 5V, external V_{REFADC} = 2.5V, external V_{REFDAC} = 2.5V, V_{CS_-} = V_{CS_+} = 32V, C_{REF} = 0.1µF, T_A = +25°C, unless otherwise noted.)

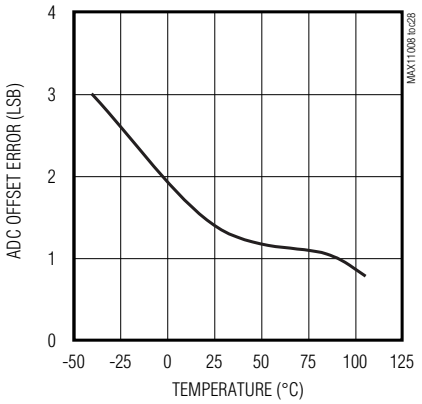
INTERNAL REFERENCE VOLTAGE vs. TEMPERATURE



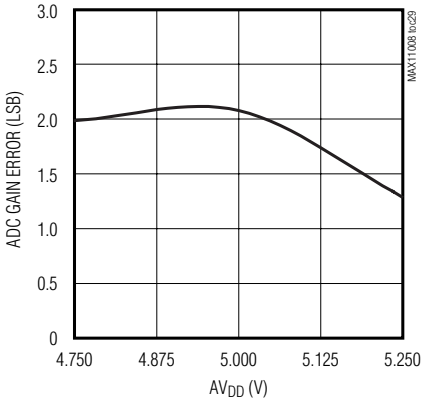
ADC OFFSET ERROR vs. ANALOG SUPPLY VOLTAGE



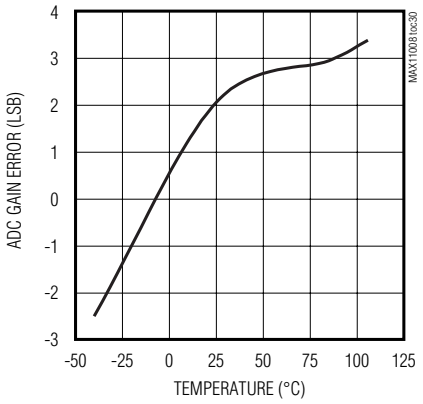
ADC OFFSET ERROR vs. TEMPERATURE



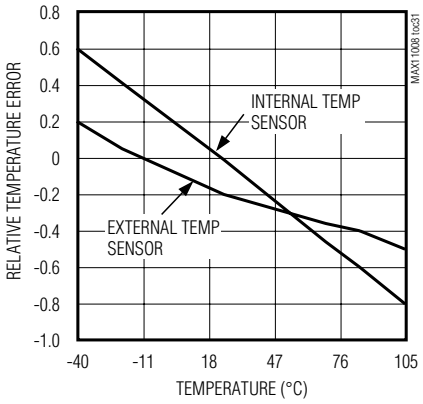
ADC GAIN ERROR vs. ANALOG SUPPLY VOLTAGE



ADC GAIN EROR vs. TEMPERATURE



RELATIVE TEMPERATURE ERROR vs. TEMPERATURE

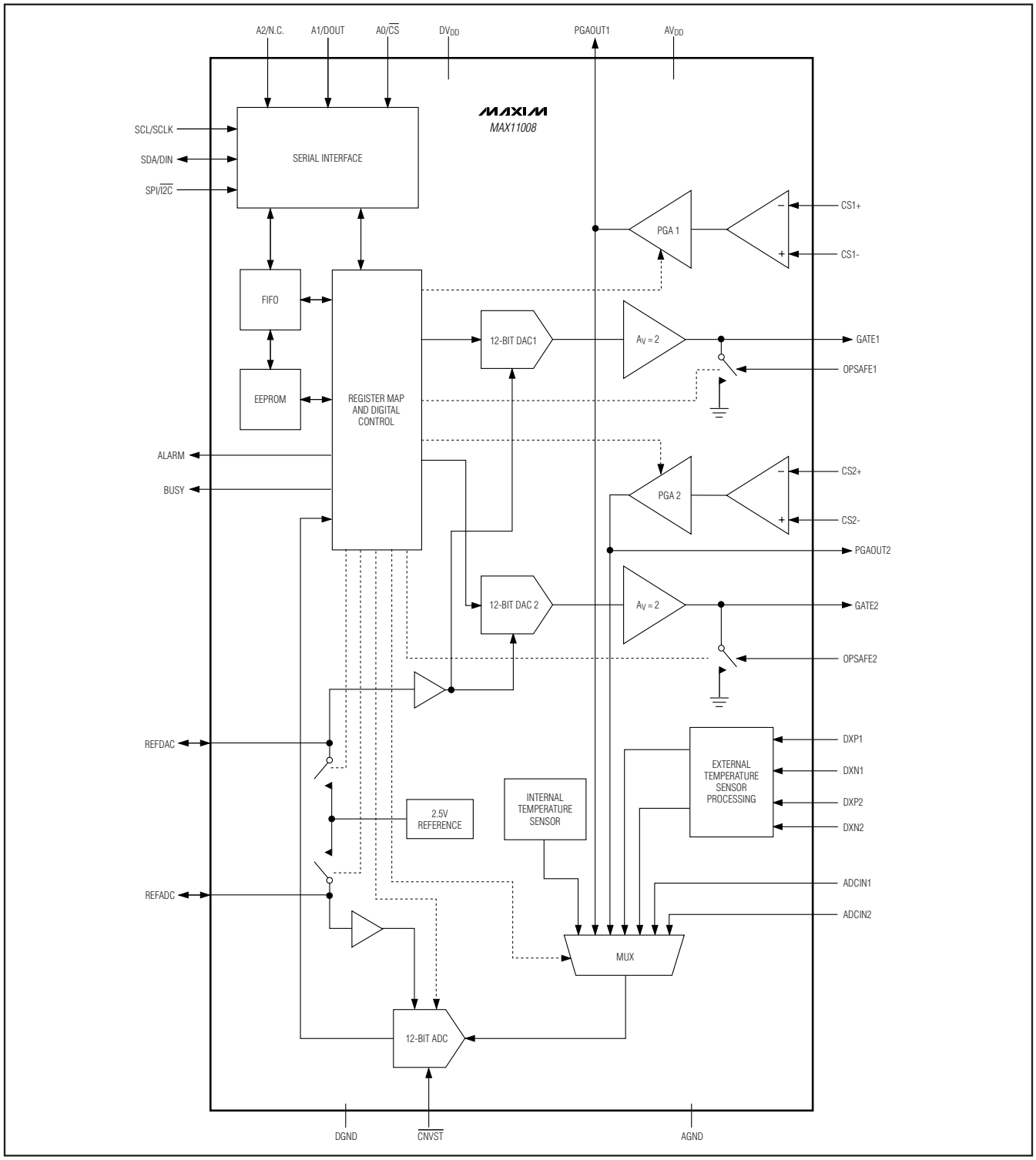


Pin Description

PIN	NAME	FUNCTION
1, 31	DGND	Digital Ground. Connect both DGND inputs to the same potential.
2	OPSAFE1	Output Safe Switch Logic Input 1. Drive OPSAFE1 high to close the output safe switch and clamp GATE1 to AGND. Drive OPSAFE1 low to open the switch.
3	A0/$\overline{CS}$	Address-Select Input 0/Chip-Select Input. In I²C mode, this is the address-select input 0. See Table 1. In SPI mode, this is the chip-select input.
4	$\overline{CNVST}$	Active-Low Conversion Start Input. Drive $\overline{CNVST}$ low to begin a conversion when in clock modes 01 and 11.
5	SPI/$\overline{I2C}$	Interface-Select Input. Connect to DGND for I²C interface. Connect to DV_{DD} for SPI interface.
6	ALARM	Alarm Output
7	OPSAFE2	Output Safe Switch Logic Input 2. Drive OPSAFE2 high to close the output safe switch and clamp GATE2 to AGND. Drive OPSAFE2 low to open the switch.
8	REFDAC	DAC Reference Input/Output
9	REFADC	ADC Reference Input/Output
10	DXP1	Temperature Diode Positive Input 1. Connect DXP1 to the anode of the external diode.
11	DXN1	Temperature Diode Negative Input 1. Connect DXN1 to the cathode of the external diode.
12	DXP2	Temperature Diode Positive Input 2. Connect DXP2 to the anode of the external diode.
13	DXN2	Temperature Diode Negative Input 2. Connect DXN2 to the cathode of the external diode.
14	ADCIN1	ADC Auxiliary Input 1
15	ADCIN2	ADC Auxiliary Input 2
16	PGAOUT2	Programmable-Gain Amplifier Output 2
17	GATE2	Gate-Drive Amplifier Output 2
18	GATE1	Gate-Drive Amplifier Output 1
19, 25, 30, 34–39, 42, 48	N.C.	No Connection. Not internally connected. Leave unconnected.
20, 24	AV_{DD}	Analog-Supply Input. Connect both AV_{DD} inputs to the same potential.
21, 22, 23	AGND	Analog Ground. Connect all AGND inputs to the same potential.
26	CS2+	Current-Sense Positive Input 2. CS2+ is the external sense-resistor connection to the LDMOS 2 supply.
27	CS2-	Current-Sense Negative Input 2. CS2- is the external sense-resistor connection to the LDMOS 2 drain.
28	CS1-	Current-Sense Negative Input 1. CS1- is the external sense-resistor connection to the LDMOS 1 drain.
29	CS1+	Current-Sense Positive Input 1. CS1+ is the external sense-resistor connection to the LDMOS 1 supply.
32, 33, 47	DV_{DD}	Digital-Supply Input. Connect all DV_{DD} inputs to the same potential. Connect a 0.1µF capacitor to DV_{DD}.
40	PGAOUT1	Programmable-Gain Amplifier Output 1
41	A2/N.C.	Address-Select Input 2/N.C. In I²C mode, this pin is the address-select input 2. See Table 1. In SPI mode, this is a no connection pin.
43	SCL/SCLK	Serial-Clock Input. SCL is the I²C-compatible clock input. SCLK is the SPI-compatible clock input.
44	SDA/DIN	Serial-Data Input/Output. SDA is the I²C-compatible input/output. DIN is the SPI-compatible data input.
45	A1/DOUT	Address-Select Input 1/Data Out. In I²C mode, this is the address-select input 1. See Table 1. In SPI mode, this is the serial-data output. Data is clocked out on the falling edge of SCLK. DOUT is a high-impedance output when $\overline{CS}$ is driven high.
46	BUSY	Busy Output. BUSY goes high to indicate activity.
—	EP	Exposed Pad. Connect EP to AGND. Internally connected to AGND.

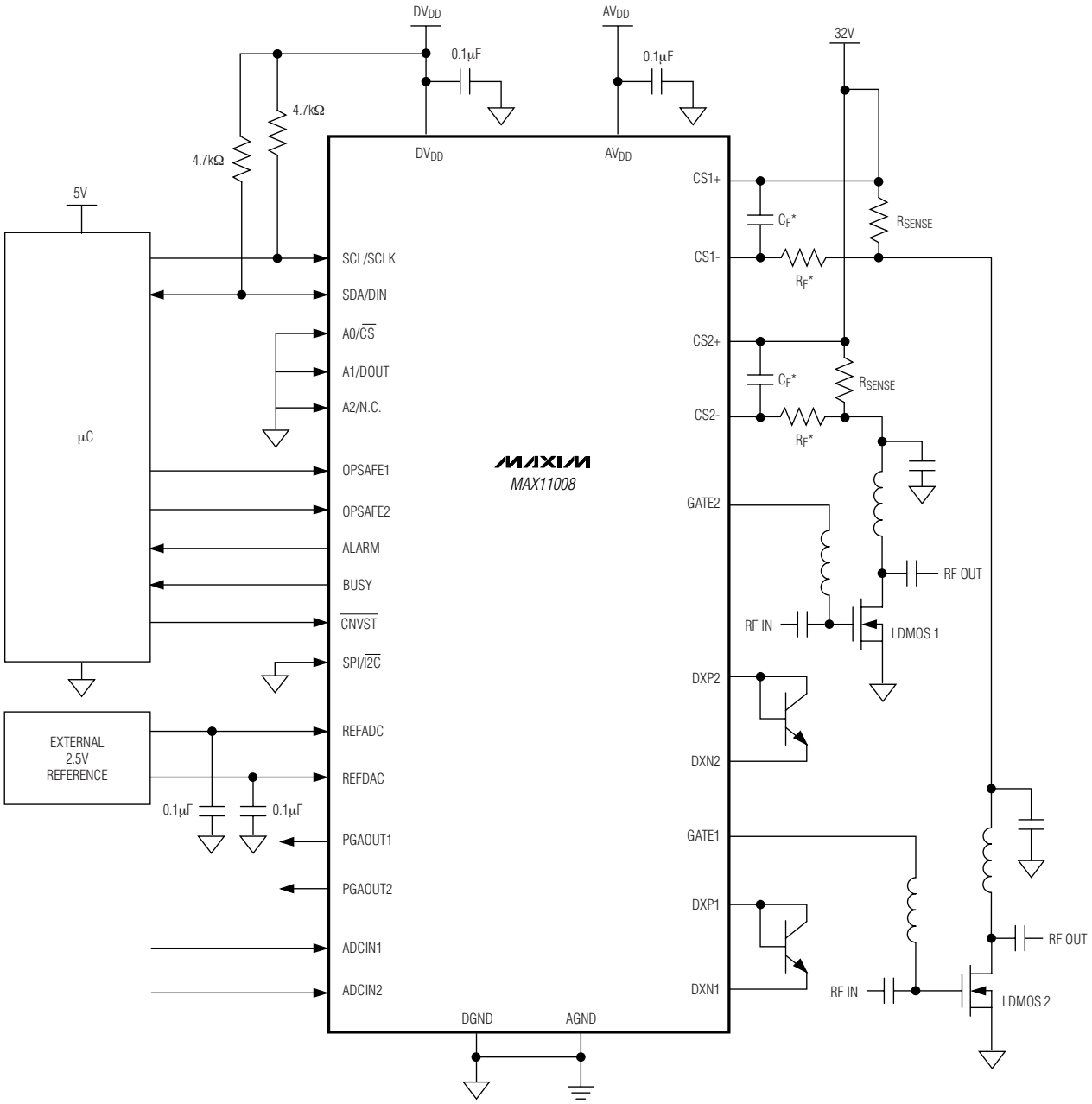
Dual RF LDMOS Bias Controller with Nonvolatile Memory

Functional Diagram



Dual RF LDMOS Bias Controller with Nonvolatile Memory

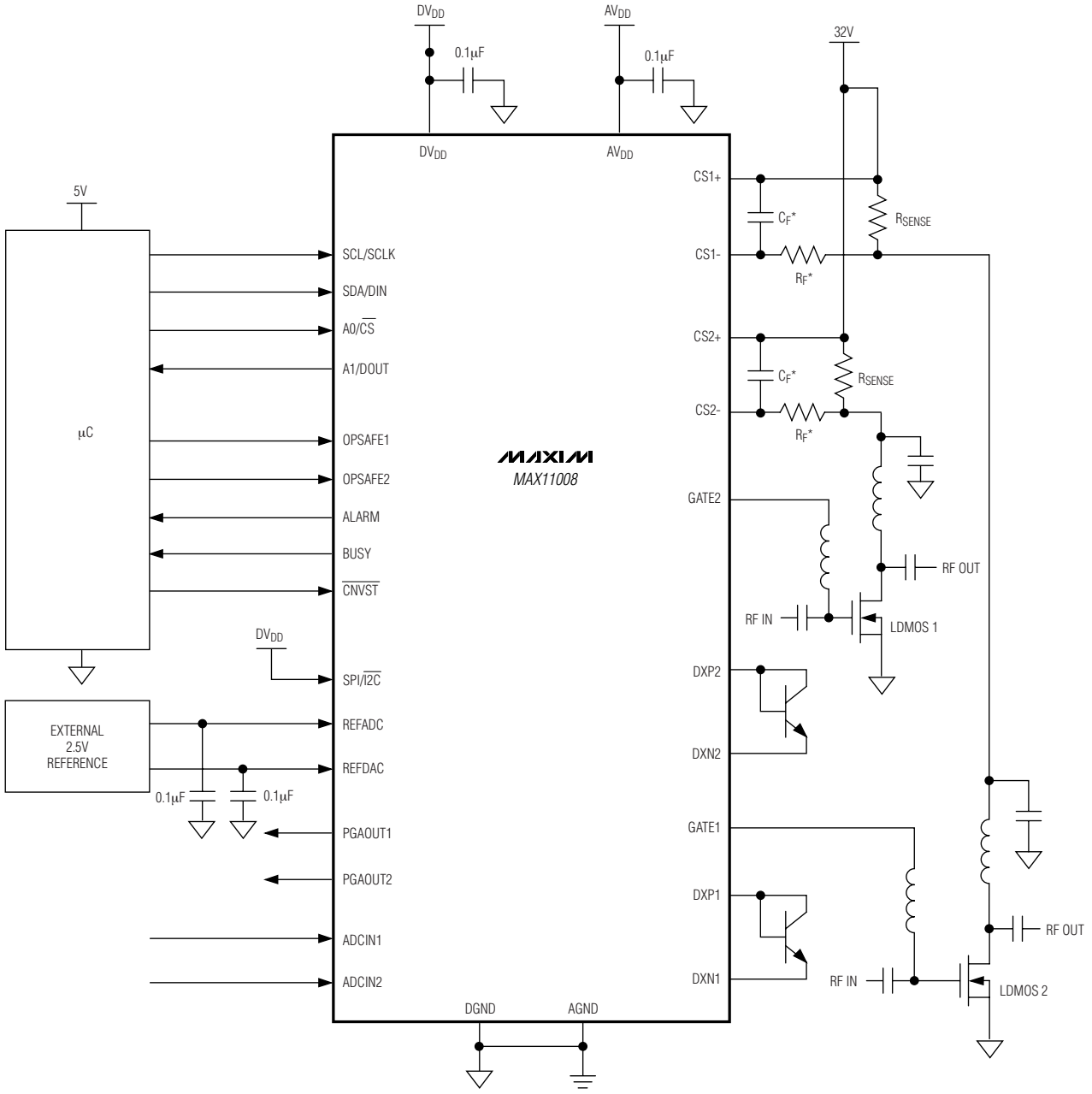
Typical Application Circuits—I²C Interface



*SDA RESISTOR VALUE VARIES WITH LOAD AND SCL FREQUENCY. SEE THE *I²C SERIAL INTERFACE* SECTION.
SELECT R_F AND C_F BASED ON DESIRED FILTER CUTOFF FREQUENCY WHERE $f_{CUTOFF} = 1/(2 \pi R_F C_F)$.
LIMIT R_F TO 100Ω TO MINIMIZE OFFSET ERRORS.

Dual RF LDMOS Bias Controller with Nonvolatile Memory

Typical Application Circuits—SPI Interface



*SELECT R_F AND C_F BASED ON DESIRED FILTER CUTOFF FREQUENCY WHERE $f_{CUTOFF} = 1/(2 \pi R_F C_F)$.
LIMIT R_F TO 100Ω TO MINIMIZE OFFSET ERRORS.

Detailed Description

The MAX11008 sets and controls the bias conditions for dual RF LDMOS power devices found in cellular base-station power amps. Each device includes two high-side current-sense amplifiers with programmable gains of 2, 10, and 25 to monitor the LDMOS transistor drain current over the 20mA to 5A range. Two external diode-connected transistors monitor the LDMOS transistor temperatures while an internal temperature sensor measures the local die temperature of the MAX11008. The 12-bit ADC is interfaced to a 7:1 multiplexer and converts the signals from the PGA outputs, internal and external temperature readings, or the two auxiliary analog inputs into digital data results that can be stored in the FIFO.

On the control side, two gate-drive channels, driven from two 12-bit DACs and a gain stage of 2, generate a positive gate voltage bias for the LDMOS. Each gate-drive output supports up to ±2mA of gate current. The gate-drive amplifier is current-limited to ±25mA and features a fast clamp to analog ground that operates independently of the serial interface.

The MAX11008 includes an on-chip, nonvolatile EEPROM that stores LUTs and register information. The LUTs are designed to store gate voltage vs. temperature curves for the LDMOS FET. The data is used for temperature compensation of the LDMOS FET's bias point. The LUTs can also contain compensation data for another independent parameter: either sense voltage or AIN voltage.

Digital Serial Interface

The MAX11008 features both an I²C and an SPI-compatible serial interface. Connect SPI/$\overline{I2C}$ to DGND to select the I²C serial-interface operation, or to DV_{DD} to select the SPI serial-interface operation. Do not alter interface mode during operation.

SPI Serial Interface

Connect SPI/$\overline{I2C}$ to DV_{DD} to select the SPI interface. The SPI serial interface consists of a serial data input (DIN), a serial clock line (SCLK), a chip select ($\overline{CS}$), and a serial data output (DOUT). The use of serial data output (DOUT) is optional and is only required when data is to be read back by the master device. The MAX11008 is SPI compatible within the range of V_{DD} = +2.7V to +5.25V. DIN, SCLK, $\overline{CS}$, and DOUT facilitate bidirectional communication between the MAX11008 and the master at rates up to 20MHz.

Figure 1 illustrates the 4-wire interface timing diagram. The MAX11008 is a transmit/receive slave-only device, relying upon a master to generate a clock signal. The master initiates data transfer on the bus and generates the SCLK signal to permit data transfer.

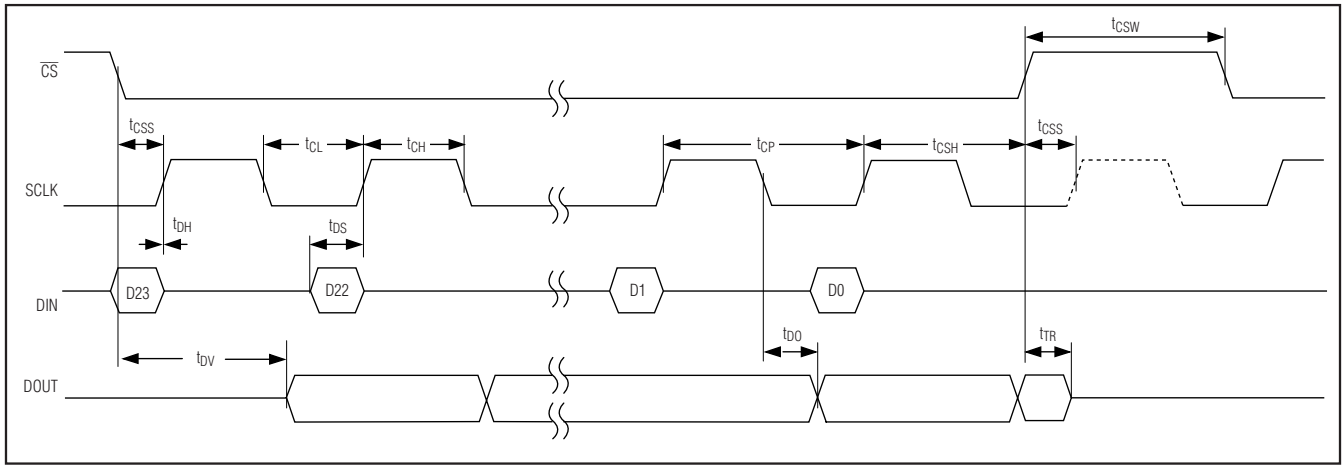


Figure 1. SPI Serial-Interface Timing

Dual RF LDMOS Bias Controller with Nonvolatile Memory

The SPI bus cycles are 24 bits long. Data can be supplied as three 8-bit bytes or as a continuous 24-bit stream. $\overline{CS}$ must remain low throughout the 24-bit sequence. The first 8-bit byte is a command byte C[7:0]. The next 16 bits are data bits D[15:0]. Clock signal SCLK can idle low or high, but data is always clocked in on the rising edge of SCLK (CPOL = CPHA).

SPI data transfers begin with the falling edge of $\overline{CS}$. Data is clocked into the device on the rising edges of SCLK and clocked out of the device on the falling edges of SCLK. For correct bus cycles, $\overline{CS}$ should frame the data and should not return to a 1 until after the last active rising clock edge. See Figure 2 for timing details. A rising edge of $\overline{CS}$ causes DOUT to three-state and data reads should be performed accordingly. See Figures 1 and 3.

When writing instructions to the MAX11008, 24 clock cycles must be completed before $\overline{CS}$ is driven high. The MAX11008 executes the instruction only after the 24th clock cycle has been received and $\overline{CS}$ is driven high. To abort unwanted instructions, $\overline{CS}$ can be driven high at any time before the 23rd rising clock edge.

When reading data from the MAX11008, 24 clock cycles must be completed before $\overline{CS}$ is driven high. If $\overline{CS}$ is driven high before the completion of the 24th falling edge, DOUT immediately three-states, the interface resets in preparation for the next command, and the data being read is lost.

Write Format

Use the following sequence to write 16 bits of data to a MAX11008 register (see Figure 2):

1) Drive $\overline{CS}$ low to select the device.
2) Send the appropriate write command byte (see Table 6 for the register address map). The command byte is clocked in on the rising edge of SCLK.
3) Send 16 bits of data D[15:0] starting with the most significant bit (MSB). Data is clocked in on the rising edges of SCLK.
4) Drive $\overline{CS}$ high to conclude the command.

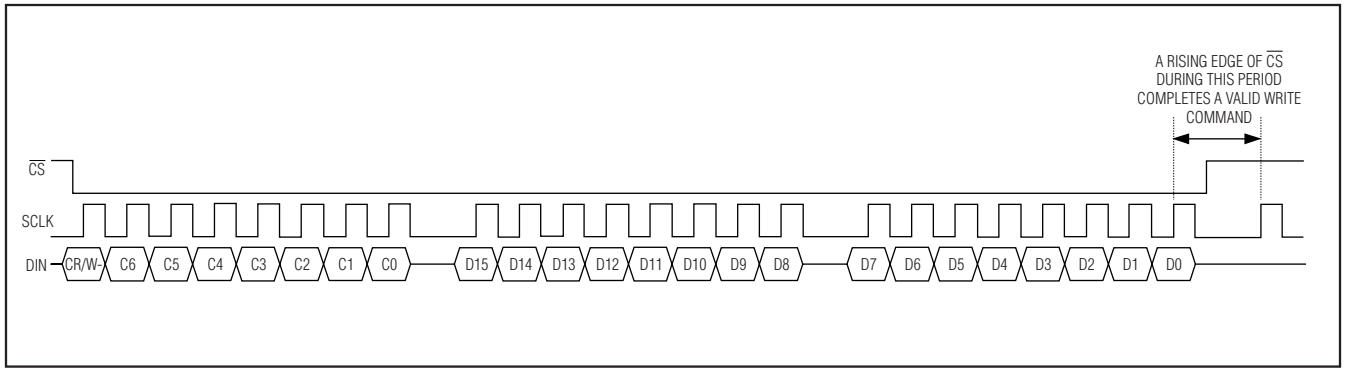


Figure 2. SPI Write Sequence

Read Format

Use the following sequence to read 16 bits of data from a MAX11008 register (see Figure 3):

1) Drive $\overline{CS}$ low to select the device.
2) Send the appropriate read command byte (see Table 6 for the register address map). The command byte is clocked in on the rising edges of SCLK.
3) Receive 16 bits of data. The first 4 bits of data are always high. Data is clocked out on the falling edges of SCLK.
4) Drive $\overline{CS}$ high.

I²C Serial Interface

Connect SPI/$\overline{I2C}$ to DGND to select the I²C interface. The I²C serial interface consists of a serial data line (SDA) and a serial clock line (SCL). The MAX11008 is I²C compatible within the DV_{DD} = 2.7V to 5.25V range. SDA and SCL facilitate bidirectional communication between the MAX11008 and the master at rates up to 400kHz for fast mode and up to 3.4MHz for high-speed mode (HS mode). See the *Bus Timing* and *HS I²C Mode* sections for more information on data-rate configurations.

Figure 4 shows the 2-wire interface timing diagram. The MAX11008 is a transmit/receive slave-only device, relying upon a master to generate a clock signal. The master (typically a microcontroller) initiates data transfers on the bus and generates the SCL signal to permit data transfer.

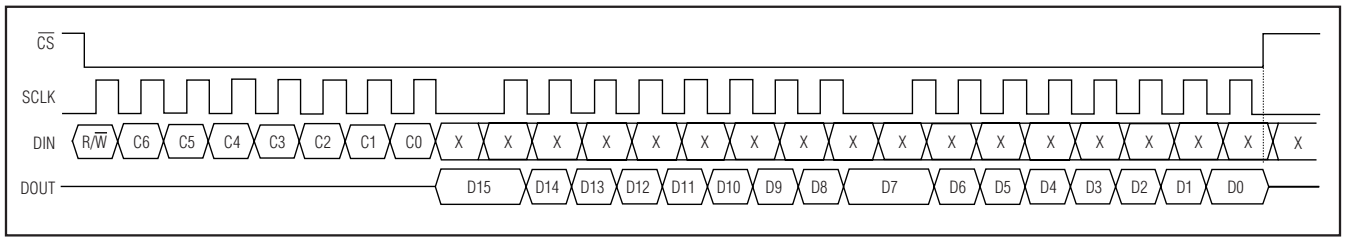


Figure 3. SPI Read Sequence

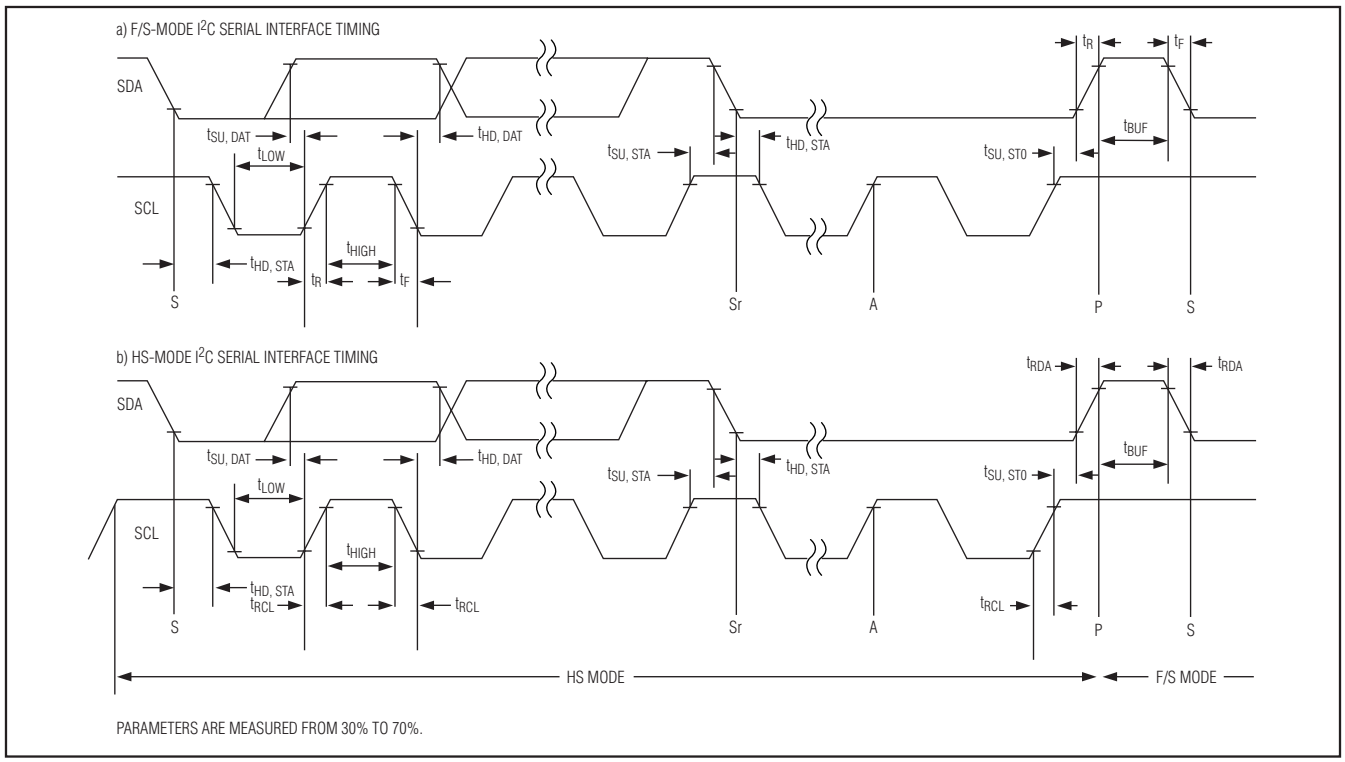


Figure 4. I²C Serial-Interface Timing Diagram

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A master device communicates to the MAX11008 by transmitting the proper slave address followed by a command and/or data words. Each transmit sequence is framed by a START (S) or repeated START (Sr) condition and a STOP (P) condition. Each word transmitted over the bus is 8 bits long and is always followed by an acknowledge clock pulse.

The MAX11008 SDA and SCL drivers are open-drain outputs, requiring a pullup resistor (750Ω or greater) to generate a logic-high voltage (see the *Typical Application Circuits*). Series resistors are optional for noise filtering. These series resistors protect the input stages of the MAX11008 from high-voltage spikes on the bus line, and minimize crosstalk and undershoot of the bus signals.

Bit Transfer

One data bit is transferred during each SCL clock cycle. The data on SDA must remain stable during the high period of the SCL clock pulse. Changes in SDA while SCL is high are control signals (see the *START and STOP Conditions* section). Both SDA and SCL idle high when the I²C bus is not busy.

START and STOP Conditions

The master initiates a transmission with a START condition (S), which is a high-to-low transition on SDA while SCL is high. The master terminates a transmission with a STOP condition (P), which is a low-to-high transition on SDA while SCL is high (see Figure 5). A repeated START condition (Sr) can be used in place of a STOP condition to leave the bus active and the mode unchanged (see the *HS I²C Mode* section).

Acknowledge Bits and Not-Acknowledge Conditions

Data transfers are framed with an acknowledge bit (ACK) or a not-acknowledge bit (NACK). Both the master and the MAX11008 (slave) generate acknowledge bits. To generate an acknowledge, the receiving device must pull SDA low before the rising edge of the acknowledge-related clock pulse (ninth clock pulse) and keep it low during the high period of the clock pulse (see Figure 6).

To generate a not-acknowledge condition, the receiver allows SDA to be pulled high before the rising edge of the acknowledge-related clock pulse, and leaves SDA high during the high period of the clock pulse. Monitoring the acknowledge bits allows for detection of unsuccessful data transfers. An unsuccessful data transfer happens if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master reattempts communication at a later time.

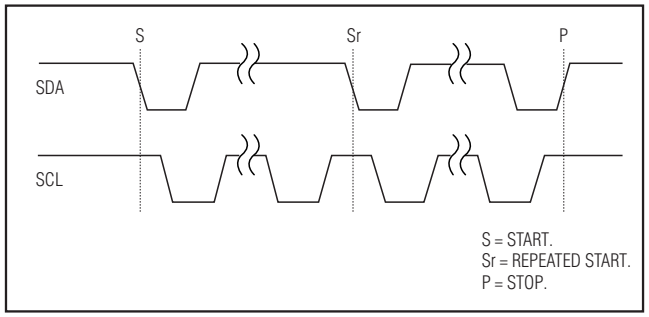

Figure 5. START and STOP Conditions

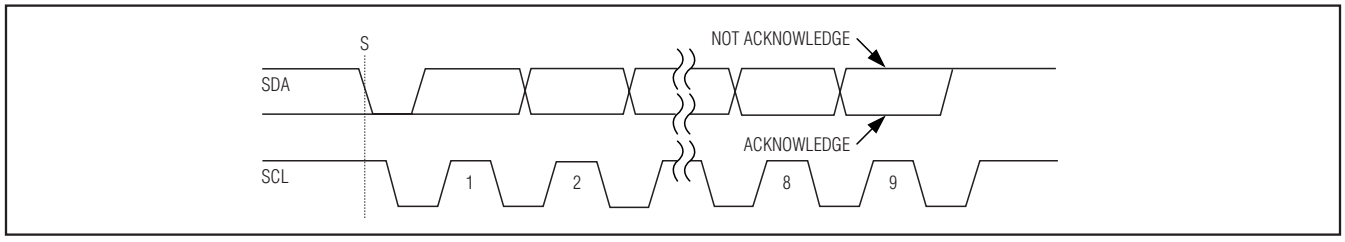

Figure 6. Acknowledge Bits

Slave Address

A bus master initiates communication with a slave device by issuing a START condition followed by the 7-bit slave address and a read/write (R/$\overline{W}$) bit (see Figure 7). When the device recognizes its slave address, it is ready to accept or send data depending on the R/$\overline{W}$ bit. When the MAX11008 recognizes its slave address, it issues an ACK by pulling SDA low for one clock cycle and is ready to accept or send data depending on the R/$\overline{W}$ bit that was sent.

The MAX11008 has eight user-selectable slave addresses, which are set through inputs A0, A1, and A2 (see Table 1). This feature allows up to eight MAX11008 devices to share the same bus inputs. The 4 MSBs D[7:4] are factory set, and the 3 LSBs are user-selectable.

Bus Timing

At power-up, the bus timing is set for I²C fast-mode (F/S mode), which allows I²C clock rates up to 400kHz. The MAX11008 can also operate in high-speed mode (HS mode) to achieve I²C clock rates up to 3.4MHz. See Figure 4 for I²C bus timing.

HS I²C Mode

Select HS mode by addressing all devices on the bus with the HS-mode master code 0000 1XXX (X = don't care). After successfully receiving the HS-mode master code, the MAX11008 issues a NACK, allowing SDA to be pulled high for one clock cycle (see Figure 8). After the NACK, the MAX11008 operates in HS mode. The master must then send a repeated START (Sr) followed by a slave address to initiate HS-mode communication. If the master generates a STOP condition, the

Table 1. Slave Address Select

A2	A1	A0	ADDRESS
0	0	0	0101000
0	0	1	0101001
0	1	0	0101010
0	1	1	0101011
1	0	0	0101100
1	0	1	0101101
1	1	0	0101110
1	1	1	0101111

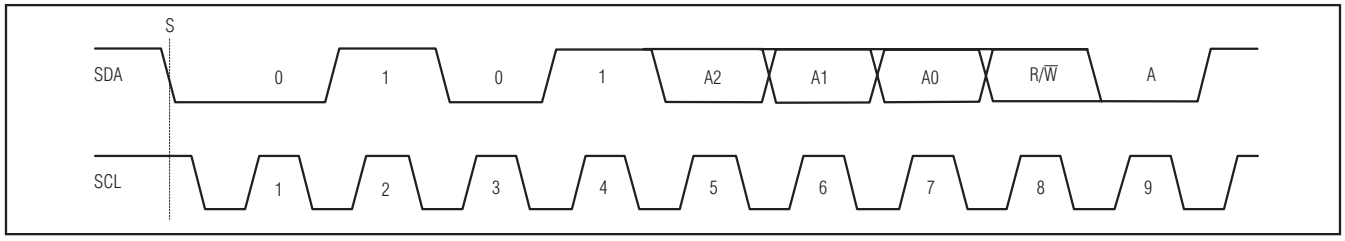

Figure 7. Slave Address Bits

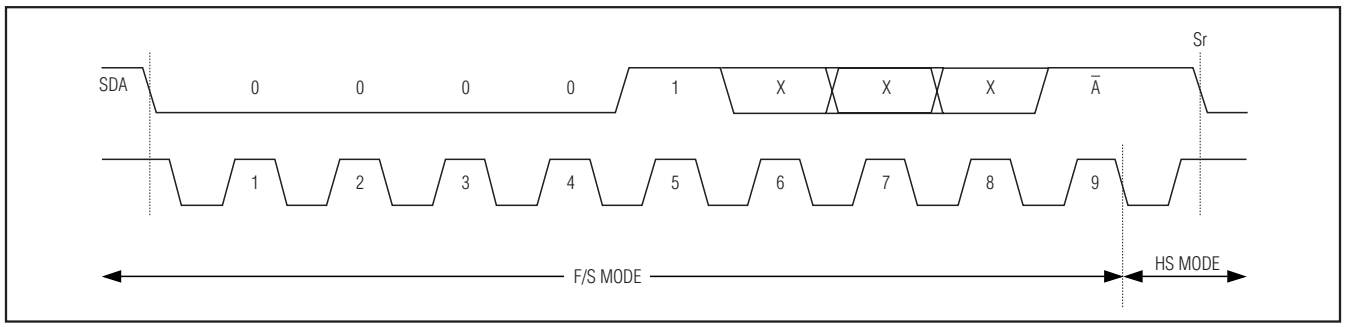

Figure 8. F/S-Mode to HS-Mode Transfer

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MAX11008 returns to F/S mode. Use a repeated START condition in place of a STOP condition to leave the bus active and the mode unchanged. Figure 9 summarizes the data bit transfer format for HS-mode communication.

Register Address/Data Bytes (Write Cycle)

A write cycle begins with the bus master issuing a START condition followed by 7 address bits (see Figure 5 and Table 1) and a write bit ($R/\overline{W}$ = 0). Once the slave address is recognized and the write bit is received, the MAX11008 (I^2C slave) issues an ACK by pulling SDA low for one clock cycle. The master then sends the register address byte (command byte) to the slave. The MSB of the register address byte is the read/write bit for the destination register address of the slave and must be set to 0 for a write cycle (see the *Register Address Map* section). After receiving the byte, the slave issues another acknowledge, pulling SDA low for one clock cycle. The master then writes two data bytes, receiving an ACK from the slave after each byte is sent. The master ends the write cycle by issuing a STOP condition. When operating in HS mode, a STOP condition returns the bus into F/S mode (see the *HS I^2C Mode* section). Figure 10 shows a complete write cycle.

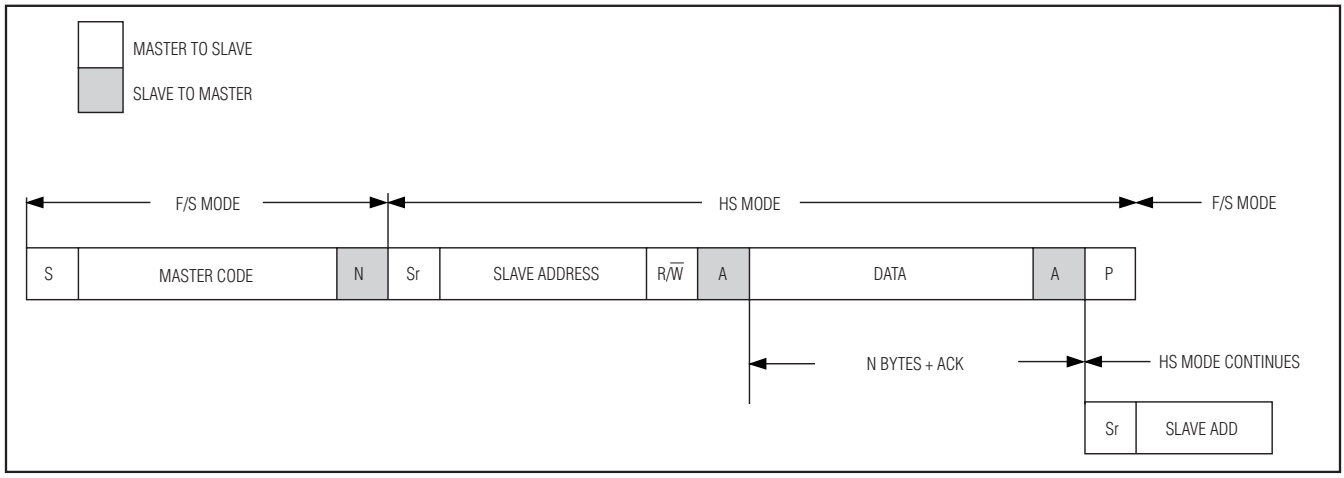

Figure 9. Data-Transfer Format in HS Mode

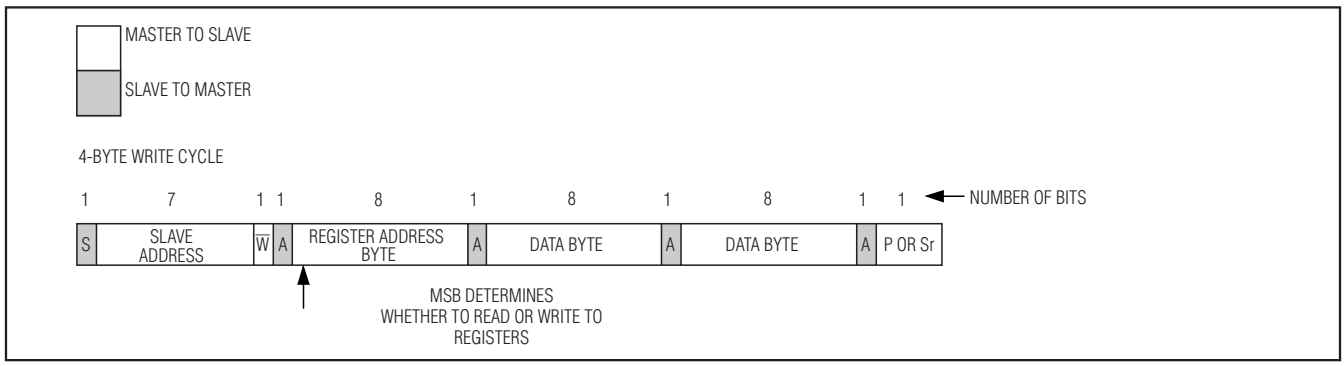

Figure 10. Write Cycle

Register Address/Data Bytes (5-Byte Read Cycle)

A read cycle begins with the master issuing a START condition followed by a 7-bit address, (see Figure 5 and Table 1) and a write bit (R/$\overline{W}$ = 0) to instruct the MAX11008 interface that it is about to receive data. Once the slave address is recognized and the write bit is received, the MAX11008 (I^2C slave) issues an ACK by pulling SDA low for one clock cycle. The master then sends the register address byte (command byte) to the slave. The MSB of the register address byte is the read/write bit for the destination register address of the slave and must be set to 1 for a read cycle (see the *Register Address Map* section). After this byte is received, another acknowledge bit is sent to the master from the slave. The master then issues a repeated START (Sr) condition. Following a repeated START (Sr), the master writes the slave address byte again with a read bit (R/$\overline{W}$ = 1). After a third acknowledge signal from the slave, the data direction on the SDA bus reverses and the slave writes the 2 data bytes (the contents of the register that was addressed in the previous command byte) to the master. Finally, the master issues a NACK followed by a STOP condition (P), ending the read cycle. Figure 11 shows a complete 5-byte read cycle.

Default Read Cycle (3-Byte Read Cycle)

The MAX11008 2-wire interface has a unique feature for read commands. To avoid the necessity of sending 2 slave address bytes in one read cycle (see the 5-byte read cycle in Figure 11), the MAX11008 2-wire interface recognizes a single slave address byte with a read bit (R/$\overline{W}$ = 1). In this case, the interface outputs the contents of the last read device register. This default read feature is useful when the master must perform multiple consecutive reads from the same device register. Figure 11 shows a complete 3-byte read cycle.

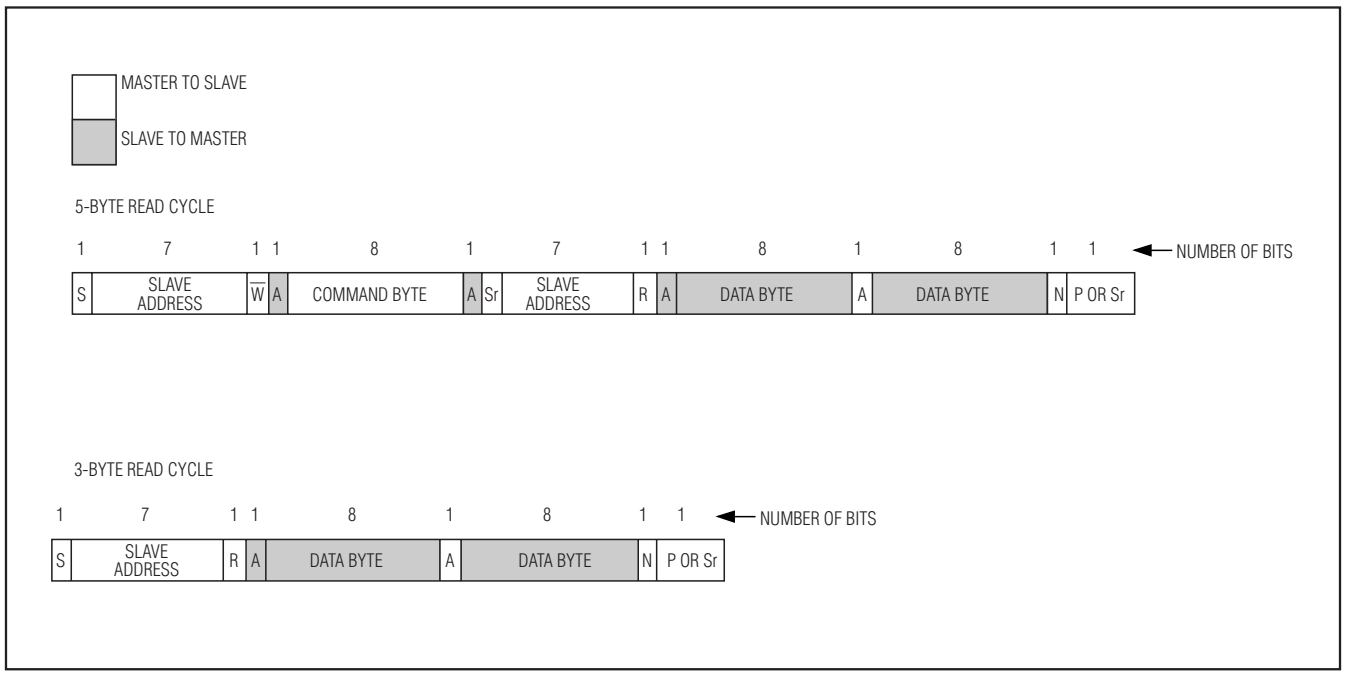

Figure 11. 5-Byte and 3-Byte Read Cycle

Dual RF LDMOS Bias Controller with Nonvolatile Memory

12-Bit ADC

The MAX11008 12-bit ADC uses a SAR conversion technique and on-chip track-and-hold (T/H) circuitry to convert the PGA outputs (PGAOUT1 and PGAOUT2), temperature measurements, and single-ended auxiliary input voltages (ADCIN1 and ADCIN2) into 12-bit digital data when in ADC monitor mode (see the *Hardware Configuration Register (HCFIG) (Read/Write)* section). All nontemperature measurements are converted using a unipolar transfer function (see Figure 13), and all temperature measurements are converted using a bipolar transfer function (see Figure 14).

Analog Input T/H

Figure 12 shows the equivalent circuit for the ADC input architecture of the MAX11008. In track mode, an input capacitor is connected to the input signal (ADCIN1, ADCIN2, PGAOUT1, PGAOUT2, or temperature sensor processor output). Another input capacitor is connected to AGND. After the T/H enters hold mode, the difference between the sampled positive and negative input voltages is converted. The charging rate of the input capacitance determines the time required for the T/H to acquire an input signal. If the input signal's source impedance is high, the required acquisition time lengthens accordingly.

Any source impedance below 300Ω does not affect the ADC's AC performance. A high-impedance source can be accommodated either by lengthening t_{ACQ} or by placing a 1µF capacitor between the positive and negative analog inputs. The combination of the analog-input source impedance and the capacitance at the analog input creates an RC filter that limits the analog input bandwidth.

Input Bandwidth

The ADC's input-tracking circuitry has a 1MHz small-signal bandwidth, to digitize high-speed transient events and measure periodic signals with bandwidths exceeding the ADC's sampling rate by using undersampling techniques. Anti-alias filtering of the input signals is necessary to prevent high-frequency components from aliasing into the frequency band of interest.

Analog Input Protection

Internal electrostatic-discharge (ESD) protection diodes clamp all analog inputs to AV_{DD} and AGND, allowing the inputs to swing from (AGND - 0.3V) to (AV_{DD} + 0.3V) without damage. However, for accurate conversions near full scale, the inputs must not exceed AV_{DD} by more than 50mV or be lower than AGND by 50mV. If an analog input voltage exceeds the supplies, limit the input current to 2mA.

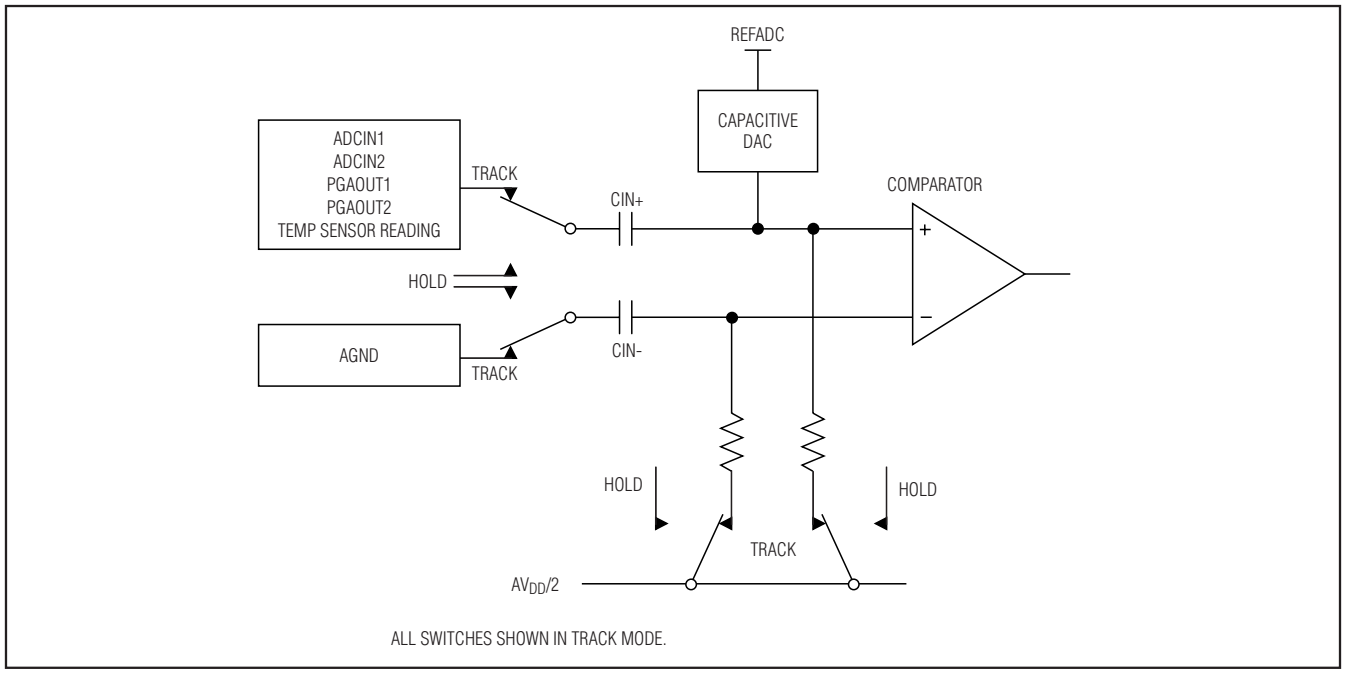

Figure 12. Analog Input Track and Hold

ADC Transfer Functions

Figure 13 shows the unipolar transfer function for nontemperature measurements, and Figure 14 shows the bipolar transfer function used for temperature measurements. Code transitions occur halfway between successive-integer LSB values. Output coding is binary, with 1 LSB = V_{REFADC}/4096 for nontemperature measurements, and 1 LSB = +0.125°C for temperature measurements. All signed binary results use two's complement format.

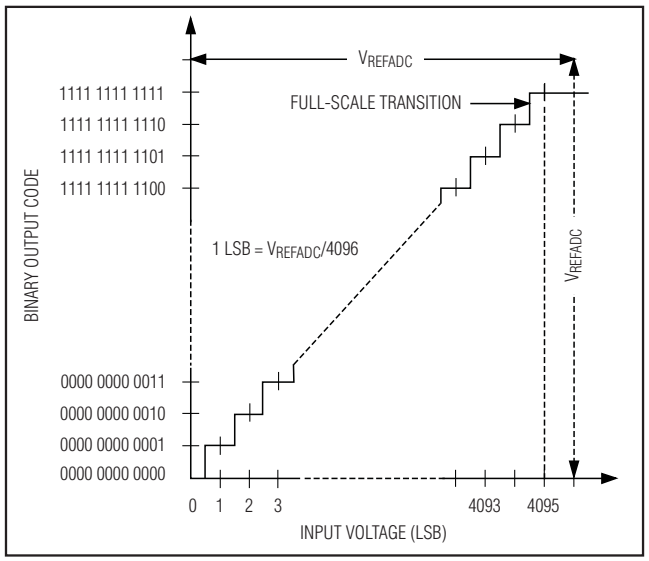

Figure 13. ADC Transfer Function

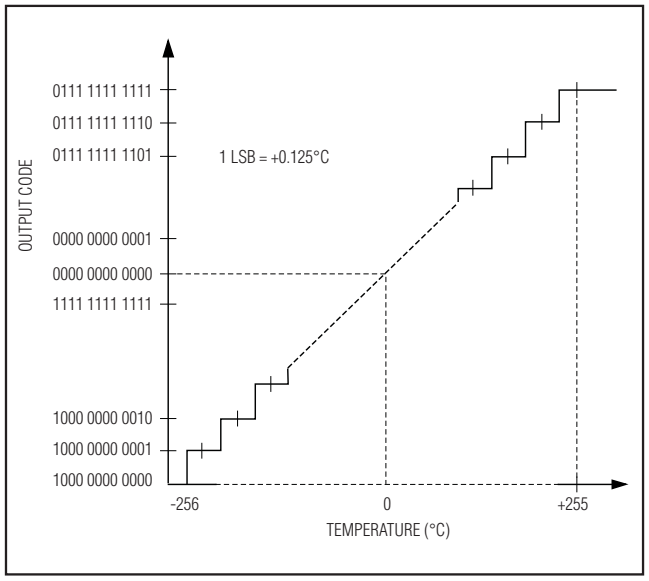

Figure 14. Temperature Transfer Function

ADC Conversion Scheduling

The MAX11008 ADC multiplexer scans and converts the selected inputs in the order shown in Table 2 (see the *ADC Conversion Register (ADCCON) (Write Only)* section) when more than one channel is selected. The results are stored in the FIFO when in ADC monitoring mode. The BUSY signal is set at the start and reset at the end of a scan except when the continuous convert bit is set at which time BUSY does not then respond to ADC conversions.

Writing a conversion command before a conversion is complete cancels the pending conversion. Avoid addressing the device using the serial interface while the ADC is converting.

Table 2. Order of ADC Conversion Scan

ORDER OF SCAN	DESCRIPTION OF CONVERSION
1	Internal device temperature
2	External diode 1 temperature
3	Output of PGA 1 for current sense
4	Auxiliary input 1 (ADCIN1)
5	External diode 2 temperature
6	Output of PGA 2 for current sense
7	Auxiliary input 2 (ADCIN2)

ADC Clock Modes

The MAX11008 offers three conversion/acquisition modes (known as clock modes) selectable through configuration register bits CKSEL1 and CKSEL0.

If the ADC conversion requires the internal reference (temperature measurement or voltage measurement with internal reference selected) and the reference has not been previously forced on (FBGON = 1), the device inserts a typical delay of 72µs, for the reference to settle, before commencing the ADC conversion. The reference remains powered up while there are pending conversions. If the reference is not forced on, it automatically powers down at the end of a scan or when CONCONV in the ADC Conversion register is set back to 0.

Internally Timed Acquisitions and Conversions

Clock Mode 00

In clock mode 00, power-up, acquisition, conversion, and power-down are all initiated by writing to the ADC Conversion register and performed automatically using the internal oscillator. This is the default clock mode. The ADC sets the BUSY output high, powers up, and scans all requested channels storing the results in the FIFO if the ADCMON bit has been set. After the scan is