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EVALUATION KIT AVAILABLE

Automatic RF MESFET Amplifier Drain-Current Controllers

General Description

The MAX11014/MAX11015 set and control bias conditions for dual MESFET power devices found in point-to-point communication and other microwave base stations. The MAX11014 integrates complete dual analog closed-loop drain-current controllers for Class A MESFET amplifier operation, while the MAX11015 targets Class AB operation. Both devices integrate SRAM lookup tables (LUTs) that can be used to store temperature and drain-current compensation data.

Each device includes dual high-side current-sense amplifiers to monitor the MESFET drain currents through the voltage drop across the sense resistors in the 0 to 625mV range. External diode-connected transistors monitor the MESFET temperatures while an internal temperature sensor measures the local die temperature of the MAX11014/MAX11015. The internal DAC sets the voltages across the current-sense resistors by controlling the GATE voltages. The internal 12-bit SAR ADC digitizes internal and external temperature, internal DAC voltages, current-sense amplifier voltages, and external GATE voltages. Two of the 11 ADC channels are available as general-purpose analog inputs for analog system monitoring.

The MAX11014's gate-drive amplifier functions as an integrator for the Class A drain-current control loop while the MAX11015's gate-drive amplifier functions with a gain of -2 for Class AB applications. The current-limited gate-drive amplifier can be fast clamped to an external voltage independent of the digital input from the serial interface. Both the MAX11014 and the MAX11015 include self-calibration modes to minimize error over time, temperature, and supply voltage.

The MAX11014/MAX11015 feature an internal reference and can operate from separate ADC and DAC external references. The internal reference provides a well-regulated, low-noise +2.5V reference for the ADC, DAC, and temperature sensors. These integrated circuits operate from a 4-wire 20MHz SPI™-/MICROWIRE™-compatible or 3.4MHz I²C-compatible serial interface (pin-selectable). Both devices operate from a +4.75V to +5.25V analog supply (2.8mA typical supply current), a +2.7V to +5.25V digital supply (1.5mA typical supply current), and a -4.5V to -5.5V negative supply (1.1mA supply current). The MAX11014/MAX11015 are available in a 48-pin thin QFN package specified over the -40°C to +105°C temperature range.

Features

- ♦ **Dual Drain-Current-Sense Gain Amplifier**
  - **Preset Gain of 4**
  - **±0.5% Accuracy for Sense Voltages Between 75mV and 625mV (MAX11014)**
- ♦ **Common-Mode Sense-Resistor Voltage Range**
  - **0.5V to 11V (MAX11014)**
  - **5V to 32V (MAX11015)**
- ♦ **Low-Noise Output GATE Bias with ±10mA GATE Drive**
- ♦ **Fast Clamp and Power-On Reset**
- ♦ **12-Bit DAC Controls MESFET GATE Voltage**
- ♦ **Internal Temperature Sensor/Dual Remote Diode Temperature Sensors**
- ♦ **Internal 12-Bit ADC Measures Temperature and Voltage**
- ♦ **Pin-Selectable Serial Interface**
  - **3.4MHz I²C-Compatible Interface**
  - **20MHz SPI-/MICROWIRE-Compatible Interface**

Ordering Information

PART	PIN-PACKAGE	AMPLIFIER
MAX11014BGTM+	48 Thin QFN-EP**	Class A
MAX11015BGTM+*	48 Thin QFN-EP**	Class AB

+ Denotes a lead-free package.
**Future product—contact factory for availability.*
***EP = Exposed pad.*
***Note:** All devices are specified over the -40°C to +105°C operating temperature range.*

Pin Configuration and Typical Operating Circuit appear at end of data sheet.

Applications

Cellular Base-Station RF MESFET Bias Controllers
Point-to-Point or Point-to-Multipoint Links
Industrial Process Control

SPI is a trademark of Motorola, Inc.
MICROWIRE is a trademark of National Semiconductor Corp.

Automatic RF MESFET Amplifier Drain-Current Controllers

ABSOLUTE MAXIMUM RATINGS

AV_{DD} to AGND .....-0.3V to +6V
DV_{DD} to DGND.....-0.3V to +6V
AGND to DGND.....-0.3V to +0.3V
AV_{SS} to AGND .....-0.3V to -6V
RCS1+, RCS1-, RCS2+, RCS2- to $GATEV_{SS}$ (MAX11014) .....-0.3V to +13V
RCS1+, RCS1-, RCS2+, RCS2- to AGND (MAX11015) .....-0.3V to +34V
RCS1- to RCS1+.....-6V to +0.3V
RCS2- to RCS2+.....-6V to +0.3V
$GATEV_{SS}$ to AGND.....+0.3V to -6V
GATE1, GATE2 to AGND .....($GATEV_{SS}$ - 0.3V) to (AV_{DD} + 0.3V)
DV_{DD} to AV_{DD}.....-0.3V to (AV_{DD} + 0.3V)
All Other Analog Inputs to AGND .....-0.3V to (AV_{DD} + 0.3V)
PGAOUT1, PGAOUT2 to AGND .....-0.3V to (AV_{DD} + 0.3V)
SCLK/SCL, DIN/SDA, $\overline{CS}$/A0, N.C./A2, $\overline{CNVST}$, OPSAFE1, OPSAFE2 to DGND.....-0.3V to (DV_{DD} + 0.3V)
DOUT/A1, SPI/$\overline{I2C}$, ALARM, BUSY to DGND .....-0.3V to (DV_{DD} + 0.3V)
Maximum Current into Any Pin.....50mA
Continuous Power Dissipation (T_A = +70°C) 48-Pin Thin QFN (derate 27.0mW/°C above +70°C).....2162.2mW
Operating Temperature Range .....-40°C to +105°C
Storage Temperature Range .....-60°C to 150°C
Junction Temperature.....+150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

($V_{GATEVSS}$ = V_{AVSS} = -5.5V to -4.75V, V_{AVDD} = +4.75V to +5.25V, V_{DVDD} = +2.7V to V_{AVDD}, external V_{REFADC} = +2.5V, external V_{REFDAC} = +2.5V, C_{REFADC} = C_{REFDAC} = 0.1µF, $V_{OPSAFE1}$ = $V_{OPSAFE2}$ = 0, V_{RCS1+} = V_{RCS2+} = +5V, C_{FILT1} = C_{FILT3} = 1nF, C_{FILT2} = C_{FILT4} = 1nF, V_{AGND} = V_{DGND} = 0, V_{ADCIN0} = V_{ADCIN1} = 0, $V_{ACLAMP1}$ = $V_{ACLAMP2}$ = -5V, T_J = T_{MIN} to T_{MAX}, unless otherwise noted. All typical values are at T_J = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CURRENT-SENSE AMPLIFIER (Note 1)						
Common-Mode Input Voltage Range	V_{RCS_+}	MAX11014	0.5		11.0	V
		MAX11015	5		32	
Common-Mode Rejection Ratio	CMRR	0.5V < V_{RCS_+} < 11V for the MAX11014		90		dB
		5V < V_{RCS_+} < 32V for the MAX11015		90		
Input-Bias Current	I_{RCS+}	V_{SENSE} < 100mV over the common-mode range			200	µA
	I_{RCS-}				±2	
Full-Scale Sense Voltage	V_{SENSE}	V_{SENSE} = V_{RCS_+} - V_{RCS_-}			625	mV
Sense Voltage Range		To within ±0.5% accuracy	75		625	mV
		To within ±2% accuracy	20		625	
		To within ±20% accuracy	2		625	
Total Current Set Error		V_{SENSE} = 75mV		±0.1	±0.5	%
Current-Sense Settling Time	t_{HSCS}	Settles to within ±0.5% of final value		< 25		µs
Saturation Recovery Time		Settles to within ±0.5% accuracy, from V_{SENSE} = 1.875V		< 45		µs
CLASS AB INPUT CHANNEL						
Untrimmed Offset				19		Bits
Offset Temperature Coefficient				0		Bits/°C
Gain				4		
Gain Error				0.1		%

ELECTRICAL CHARACTERISTICS (continued)

($V_{GATEVSS}$ = V_{AVSS} = -5.5V to -4.75V, V_{AVDD} = +4.75V to +5.25V, V_{DVDD} = +2.7V to V_{AVDD}, external V_{REFADC} = +2.5V, external V_{REFDAC} = +2.5V, C_{REFADC} = C_{REFDAC} = 0.1µF, $V_{OPSAFE1}$ = $V_{OPSAFE2}$ = 0, V_{RCS1+} = V_{RCS2+} = +5V, C_{FILT1} = C_{FILT3} = 1nF, C_{FILT2} = C_{FILT4} = 1nF, V_{AGND} = V_{DGND} = 0, V_{ADCIN0} = V_{ADCIN1} = 0, $V_{ACLAMP1}$ = $V_{ACLAMP2}$ = -5V, T_J = T_{MIN} to T_{MAX}, unless otherwise noted. All typical values are at T_J = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CLASS AB OUTPUT CHANNEL						
Untrimmed Offset		(Note 1)		50		µV
Offset Temperature Coefficient				0		mV/°C
Gain				-2		
Gain Error				0.1		%
GATE-DRIVE AMPLIFIER/INTEGRATOR						
Output Gate-Drive Voltage Range (Note 2)	V_{GATE}	I_{GATE} = -1mA	$V_{GATEVSS}$ + 1			V
		I_{GATE} = +1mA		-0.15	-4	mV
		I_{GATE} = -10mA	$V_{GATEVSS}$ + 1.2			V
		I_{GATE} = +10mA		-1	-20	mV
Gate Voltage Settling Time—MAX11015	t_{GATE}	Settles to within ±0.5% of final value, R_S = 50 , C_{GATE} = 15µF, see GATE Output Resistance vs. GATE Voltage in the *Typical Operating Characteristics*		1.1		ms
Output Capacitive Load (Note 3)	C_{GATE}	No series resistance, R_S = 0	0		0.5	nF
		R_S = 500	0	15,000		
Gate Voltage Noise		RMS noise, 1kHz to 1MHz		250		nV/√Hz
Maximum Power-On Transient		C_{LOAD} = 1nF		±100		mV
Output Short-Circuit Current Limit	I_{SC}	Sinking or sourcing		±25		mA
Output Safe Switch On-Resistance	R_{OPSW}	Clamp GATE1 to ACLAMP1, GATE2 to ACLAMP2 (Note 4)			3.6	k
ADC DC ACCURACY						
Resolution			12			Bits
Differential Nonlinearity	DNL_{ADC}				±2	LSB
Integral Nonlinearity	INL_{ADC}	(Note 5)			±2	LSB
Offset Error				±2	±4	LSB
Gain Error		(Note 6)		±2	±4	LSB
Gain Temperature Coefficient				±0.4		ppm/°C
Offset Temperature Coefficient				±0.4		ppm/°C
Channel-to-Channel Offset Matching				±0.1		LSB
Channel-to-Channel Gain Matching				±0.1		LSB

Automatic RF MESFET Amplifier Drain-Current Controllers

ELECTRICAL CHARACTERISTICS (continued)

($V_{GATEVSS}$ = V_{AVSS} = -5.5V to -4.75V, V_{AVDD} = +4.75V to +5.25V, V_{DVDD} = +2.7V to V_{AVDD}, external V_{REFADC} = +2.5V, external V_{REFDAC} = +2.5V, C_{REFADC} = C_{REFDAC} = 0.1µF, $V_{OPSAFE1}$ = $V_{OPSAFE2}$ = 0, V_{RCS1+} = V_{RCS2+} = +5V, C_{FILT1} = C_{FILT3} = 1nF, C_{FILT2} = C_{FILT4} = 1nF, V_{AGND} = V_{DGND} = 0, V_{ADCIN0} = V_{ADCIN1} = 0, $V_{ACLAMP1}$ = $V_{ACLAMP2}$ = -5V, T_J = T_{MIN} to T_{MAX}, unless otherwise noted. All typical values are at T_J = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ADC DYNAMIC ACCURACY (1kHz sine-wave input, -0.5dB from full scale, 94.4ksps)						
Signal-to-Noise Plus Distortion	SINAD			70		dB
Total Harmonic Distortion	THD	Up to the 5th harmonic		-84		dB
Spurious-Free Dynamic Range	SFDR			86		dB
Intermodulation Distortion	IMD	f_{IN1} = 9.9kHz, f_{IN2} = 10.2kHz		76		dB
Full-Power Bandwidth		-3dB point		1		MHz
Full-Linear Bandwidth		S / (N + D) > 68dB		100		kHz
ADC CONVERSION RATE						
Power-Up Time	t_{PU}	External reference		0.8		µs
		Internal reference		50		
Acquisition Time (Note 3)	t_{ACQ}	GATE_ and sense voltage measurements	40			µs
		All other measurements	1.5			
Conversion Time	t_{CONV}	Internally clocked			6.5	µs
Aperture Delay				30		ns
ADCIN1, ADCIN2 INPUTS						
Input Range	$V_{ADCIN\_}$	Relative to AGND (Note 7)	0		V_{REFADC}	V
Input Leakage Current		$V_{ADCIN\_}$ = 0V or V_{AVDD}		±0.01	±1	µA
Input Capacitance	$C_{ADCIN\_}$			34		pF
TEMPERATURE MEASUREMENTS						
Internal Sensor Measurement Error		T_J = +25°C		±0.25		°C
		T_J = -40°C to +85°C (Note 3)		±1.0	±2.5	
		T_J = -40°C to +105°C (Note 3)		±1.0	±3.5	
External Sensor Measurement Error (Note 8)		T_J = +25°C		±1.0		°C
		T_J = -40°C to +105°C		±3		
Temperature Resolution				0.125		°C/LSB
External Diode Drive			3.26		75.00	µA
External Temperature Sensor Drive Current Ratio				16.6		
INTERNAL REFERENCE						
Reference Output Voltage		V_{REFADC} = V_{REFDAC}, T_J = +25°C	+2.490	+2.500	+2.510	V
Reference Output Temperature Coefficient				±15		ppm/°C
Reference Output Impedance				6.5		kΩ
Power-Supply Rejection Ratio	PSRR	V_{AVDD} = +5V ±5%		-83		dB

ELECTRICAL CHARACTERISTICS (continued)

($V_{GATEVSS}$ = V_{AVSS} = -5.5V to -4.75V, V_{AVDD} = +4.75V to +5.25V, V_{DVDD} = +2.7V to V_{AVDD}, external V_{REFADC} = +2.5V, external V_{REFDAC} = +2.5V, C_{REFADC} = C_{REFDAC} = 0.1µF, $V_{OPSAFE1}$ = $V_{OPSAFE2}$ = 0, V_{RCS1+} = V_{RCS2+} = +5V, C_{FILT1} = C_{FILT3} = 1nF, C_{FILT2} = C_{FILT4} = 1nF, V_{AGND} = V_{DGND} = 0, V_{ADCIN0} = V_{ADCIN1} = 0, $V_{ACLAMP1}$ = $V_{ACLAMP2}$ = -5V, T_J = T_{MIN} to T_{MAX}, unless otherwise noted. All typical values are at T_J = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
EXTERNAL REFERENCES						
REFADC Input Voltage Range	V_{REFADC}		+1.0		V_{AVDD}	V
REFADC Input Current	I_{REFADC}	V_{REFADC} = +2.5V, f_{SAMPLE} = 178ksps		60		µA
		Acquisition/between conversions		±0.01		
REFDAC Input Voltage Range	V_{REFDAC}		+0.50		+2.52	V
REFDAC Input Current				26		µA
DAC DC ACCURACY						
Resolution			12			Bits
Integral Nonlinearity	INL_{DAC}	Measured at FILT_		±1		LSB
Differential Nonlinearity	DNL_{DAC}	Measured at FILT_, guaranteed monotonic		±0.4	±1	LSB
POWER SUPPLIES						
Analog Supply Voltage	V_{AVDD}		+4.75		+5.25	V
Digital Supply Voltage	V_{DVDD}		+2.7		AV_{DD}	V
Negative Supply Voltage	$V_{GATEVSS}$, V_{AVSS}	$V_{GATEVSS}$ = V_{AVSS}	-5.50		-4.75	V
Analog Supply Current	I_{AVDD}	V_{AVDD} = +5.25V		2.8	5	mA
Digital Supply Current	I_{DVDD}	V_{DVDD} = +5.25V		1.5	5	mA
Negative Supply Current	$I_{GATEVSS}$ + I_{AVSS}	$V_{GATEVSS}$ = V_{AVSS} = -5.5V		1.1	1.7	mA
Analog Shutdown Current		V_{AVDD} = +5.25V		0.8		µA
Digital Shutdown Current		V_{DVDD} = +5.25V		0.2		µA
Negative Shutdown Current		$V_{GATEVSS}$ = V_{AVSS} = -5.5V		0.6		µA
SERIAL-INTERFACE SUPPLIES						
Input Voltage	V_{IL}				0.3 x DV_{DD}	V
	V_{IH}		0.7 x DV_{DD}			
Input Hysteresis	V_{HYS}			0.05 x DV_{DD}		V
Output Low Voltage	V_{OL}	BUSY: I_{SINK} = 0.5mA; DOUT, ALARM: I_{SINK} = 3mA			0.4	V
Output High Voltage	V_{OH}	SPI/$\overline{I2C}$ = DV_{DD}; BUSY: I_{SOURCE} = 0.5mA; DOUT, ALARM: I_{SOURCE} = 2mA	DV_{DD} - 0.5V			V
Input Current	I_{IN}			±0.01	±10	µA
Input Capacitance	C_{IN}			5		pF

Automatic RF MESFET Amplifier Drain-Current Controllers

SPI-INTERFACE TIMING CHARACTERISTICS

(Note 9) (See Figure 1.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLK Clock Period	t_{CP}		40			ns
SCLK High Time	t_{CH}		16			ns
SCLK Low Time	t_{CL}		16			ns
DIN to SCLK Rise Setup Time	t_{DS}		10			ns
DIN to SCLK Rise Hold Time	t_{DH}		0			ns
SCLK Fall to DOUT Transition	t_{DO}	C_L = 30pF			20	ns
$\overline{CS}$ Fall to DOUT Enable	t_{DV}	C_L = 30pF (Note 3)			40	ns
$\overline{CS}$ Rise to DOUT Disable	t_{TR}	C_L = 30pF (Note 10)			40	ns
$\overline{CS}$ Rise or Fall to SCLK Rise	t_{CSS}		10			ns
$\overline{CS}$ Pulse-Width High	t_{CSW}	(Note 3)	40			ns
Last SCLK Rise to $\overline{CS}$ Rise	t_{CSH}	(Note 3)	0			ns

I²C-INTERFACE SLOW-/FAST-MODE TIMING CHARACTERISTICS

(Note 9) (See Figure 2.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}		0		400	kHz
Bus Free Time Between a STOP and START Condition	t_{BUF}		1.3			µs
Hold Time (Repeated) for START Condition	$t_{HD;STA}$	After this period, the first clock pulse is generated	0.6			µs
Setup Time for a Repeated START Condition	$t_{SU;STA}$		0.6			µs
SCL Pulse-Width Low	t_{LOW}		1.3			µs
SCL Pulse-Width High	t_{HIGH}		0.6			µs
Data Setup Time	$t_{SU;DAT}$		100			ns
Data Hold Time	$t_{HD;DAT}$	(Note 11)	0		0.9	µs
SDA, SCL Rise Time, Receiving	t_R	(Notes 3, 12)	0		300	ns
SDA, SCL Fall Time, Receiving	t_F	(Notes 3, 12)	0		300	ns
SDA Fall Time, Transmitting	t_F	(Notes 3, 12, 13)	20 + 0.1 x C_B		250	ns
Setup Time for STOP Condition	$t_{SU;STO}$		0.6			µs
Capacitive Load for Each Bus Line	C_B	(Notes 3, 14)			400	pF
Pulse Width of Spikes Suppressed By the Input Filter	t_{SP}	(Note 15)			50	ns

I²C-WIRE-INTERFACE HIGH-SPEED-MODE TIMING CHARACTERISTICS

(Note 9) (See Figure 3.)

PARAMETER	SYMBOL	CONDITIONS	C_B = 100pF max		C_B = 400pF		UNITS
			MIN	MAX	MIN	MAX	
Serial Clock Frequency	f_{SCL}		0	3.4	0	1.7	MHz
Setup Time (Repeated) START Condition	$t_{SU;STA}$		160		160		ns
Hold Time (Repeated) START Condition	$t_{HD;STA}$		160		160		ns
SCL Pulse-Width Low	t_{LOW}		160		320		ns
SCL Pulse-Width High	t_{HIGH}		60		120		ns
Data Setup Time	$t_{SU;DAT}$		10		10		ns
Data Hold Time	$t_{HD;DAT}$	(Note 11)	0	70	0	150	ns
SCL Rise Time	t_{RCL}	(Note 3)	10	40	20	80	ns
SCL Rise Time, After a Repeated START Condition and After an Acknowledge Bit	t_{RCL1}	(Note 3)	10	80	20	160	ns
SCL Fall Time	t_{FCL}	(Note 3)	10	40	20	80	ns
SDA Rise Time	t_{RDA}	(Note 3)	10	80	20	160	ns
SDA Fall Time	t_{FDA}	(Note 3)	10	80	20	160	ns
Setup Time for STOP Condition	$t_{SU;STO}$		160		160		ns
Capacitive Load for Each Bus Line	C_B	(Note 14)		100		400	pF
Pulse Width of Spikes Suppressed By the Input Filter	t_{SP}	(Note 15)	0	10	0	10	ns

Automatic RF MESFET Amplifier Drain-Current Controllers

MISCELLANEOUS TIMING CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Minimum Time to Wait After a Write Command Before Reading Back Data from the Same Location	t_{RDBK}	(Note 16)		1		µs
$\overline{CNVST}$ Active-Low Pulse Width in ADC Clock Mode 01	t_{CNV01}	(Note 3)	20			ns
$\overline{CNVST}$ Active-Low Pulse Width in ADC Clock Mode 11 to Initiate a Temperature Conversion	t_{CNV11}	(Note 3)	20			ns
$\overline{CNVST}$ Active-Low Pulse Width in ADC Clock Mode 11 for ADCIN1/2 Acquisition	t_{ACQ11A}	(Note 3)	1.5			µs
ADC Power-Up Time (External Reference)	t_{APUEXT}			0.8		µs
ADC Power-Up Time (Internal Reference)	t_{APUINT}			50		µs
DAC Power-Up Time (External Reference)	t_{DPUEXT}			2		µs
DAC Power-Up Time (Internal Reference)	t_{DPUINT}			50		µs
Acquisition Time (Internally Timed in ADC Clock Modes 00 or 01)	t_{ACQ}				0.6	µs
Conversion Time (Internally Clocked)	t_{CONV}				6.5	µs
Delay to Start of Conversion Time	t_{CONVW}	(Note 17)		1		µs
Temperature Conversion Time (Internally Clocked)	t_{CONVT}			30		µs

MISCELLANEOUS TIMING CHARACTERISTICS (continued)

Note 1: All current-sense amplifier specifications are tested after a current-sense calibration (valid when drain current = 0mA). See RCS Error vs. GATE Current in the *Typical Operating Characteristics*. The calibration is valid only at one temperature and supply voltage and must be repeated if either the temperature or supply voltage changes.

Note 2: The hardware configuration register's CH_OCM1 and CH_OCM0 bits are set to 0. See Table 10a. The max specification is limited by tester limitations.

Note 3: Guaranteed by design. Not production tested.

Note 4: At power-on reset, the output safe switch is closed. See the *ALMHCFG (Read/Write)* section.

Note 5: Integral nonlinearity is the deviation of the analog value at any code from its theoretical value after the gain and offset errors have been calibrated out.

Note 6: Offset nulled.

Note 7: Absolute range for analog inputs is from 0 to V_{AVDD}.

Note 8: Device and sensor at the same temperature. Verified by the current ratio (see the *Temperature Measurements* section).

Note 9: All timing specifications referred to V_{IH} or V_{IL} levels.

Note 10: D_{OUT} goes into tri-state mode after the $\overline{CS}$ rising edge. Keep $\overline{CS}$ low long enough for the DOUT value to be sampled before it goes to tri-state.

Note 11: A master device must provide a hold time of at least 300ns for the SDA signal (referred to V_{IL} of the SCL signal) to bridge the undefined region of SCL's falling edge.

Note 12: t_R and t_F measured between 0.3 x DV_{DD} and 0.7 x DV_{DD}.

Note 13: C_B = total capacitance of one bus line in pF. For bus loads between 100pF and 400pF, the timing parameters should be linearly interpolated.

Note 14: An appropriate bus pullup resistance must be selected depending on board capacitance. For more information, refer to the I^2C documentation on the Philips website.

Note 15: Input filters on the SDA and SCL inputs suppress noise spikes less than 50ns.

Note 16: When a command is written to the serial interface, it is passed to the internal oscillator clock to be executed. There is a small synchronization delay before the new value is written to the appropriate register. If the user attempts to read the new value back before t_{RDBK}, no harm will be caused to the data, but the read command may not yet show the new value.

Note 17: This is the minimum time from the end of a command before $\overline{CNVST}$ should be asserted. The time allows for the data from the preceding write to arrive and set up the chip in preparation for the $\overline{CNVST}$. The time need only be observed when the write affects the ADC controls. Failure to observe this time may lead to incorrect conversions (for example, conversion of the wrong ADC channel).

Automatic RF MESFET Amplifier Drain-Current Controllers

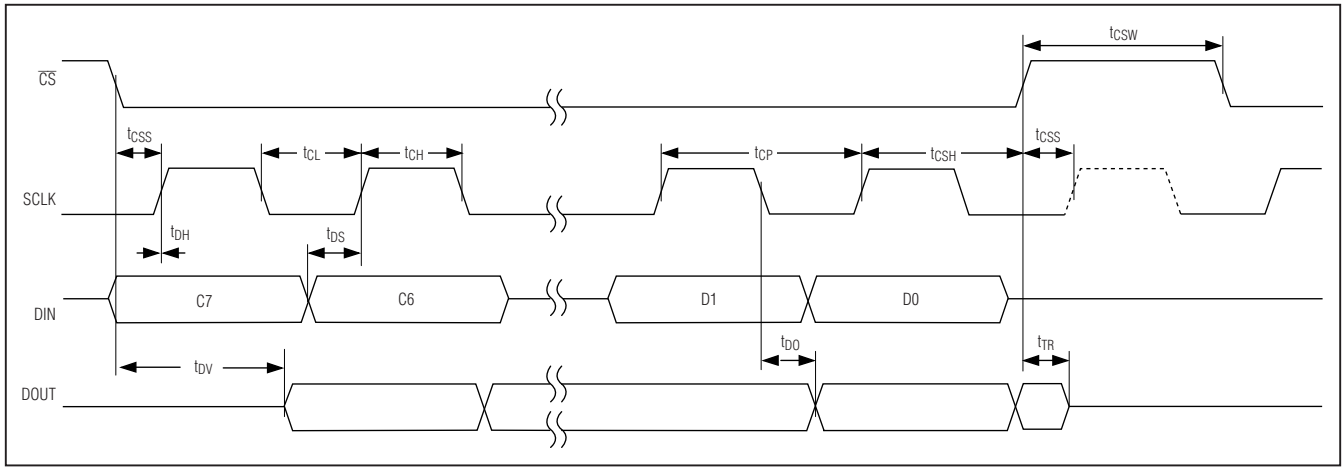


Figure 1. SPI Serial-Interface Timing Diagram

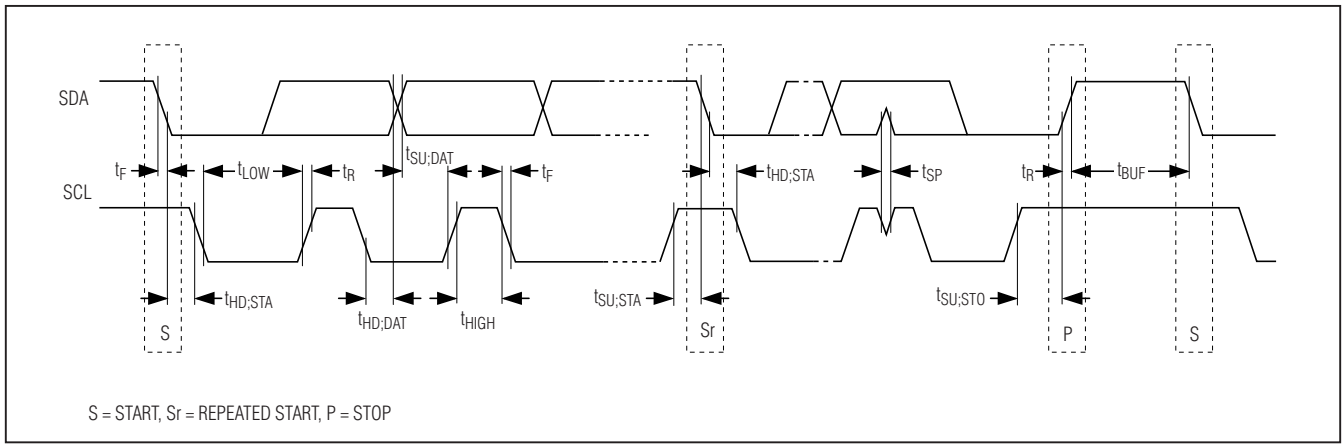


Figure 2. Slow-/Fast-Speed Timing Diagram

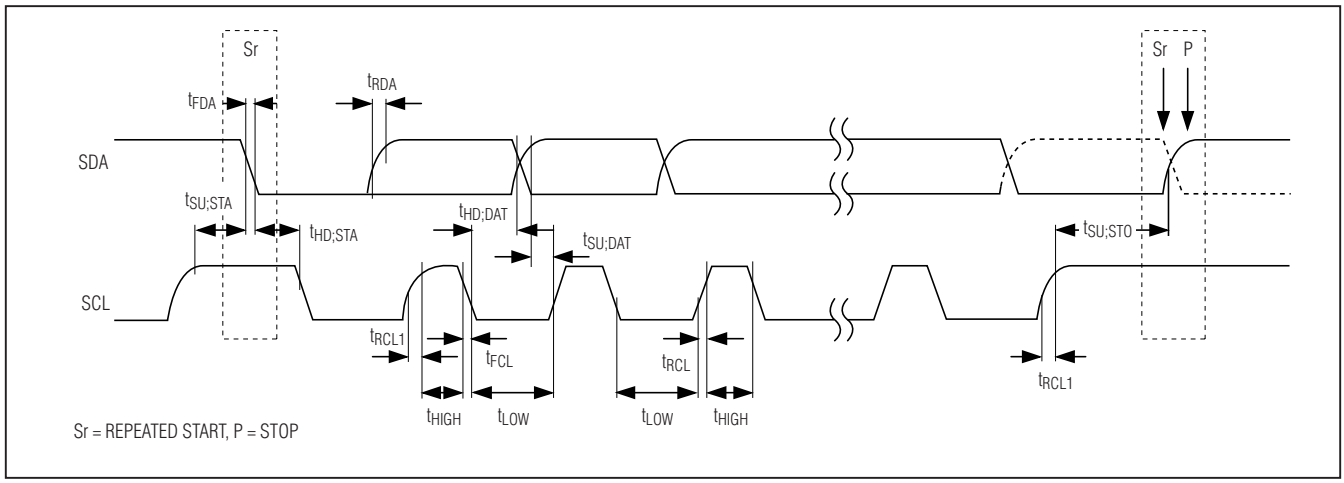
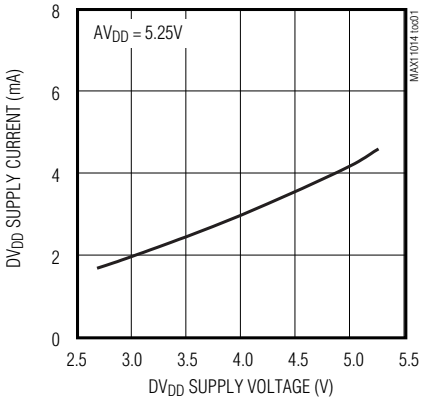


Figure 3. High-Speed Timing Diagram

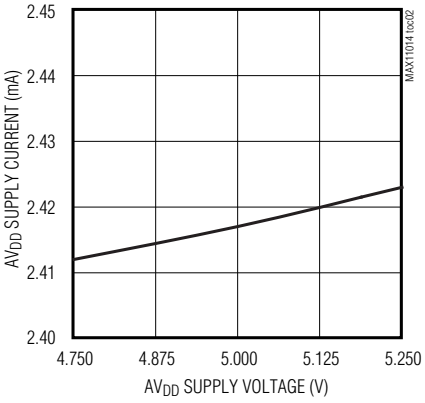
Typical Operating Characteristics

($V_{GATEVSS}$ = -5.5V; V_{AVDD} = V_{DVDD} = +5V, $GATEV_{SS}$ = AV_{SS} = -5V, external V_{REFADC} = +2.5V; external V_{REFDAC} = +2.5V; C_{REF} = 0.1µF; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

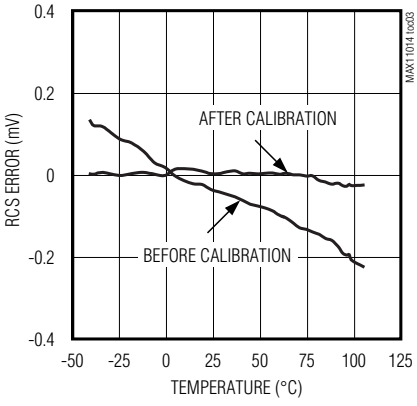
DIGITAL SUPPLY CURRENT vs. DIGITAL SUPPLY VOLTAGE



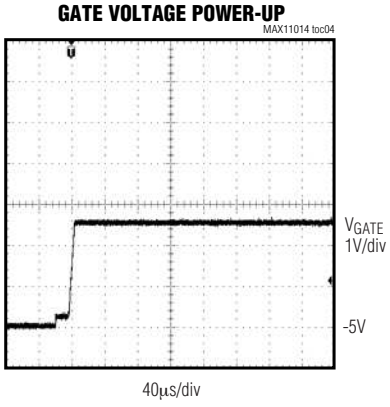
ANALOG SUPPLY CURRENT vs. ANALOG SUPPLY VOLTAGE



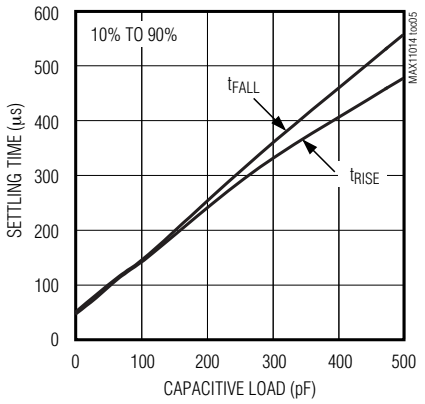
RCS ERROR vs. TEMPERATURE



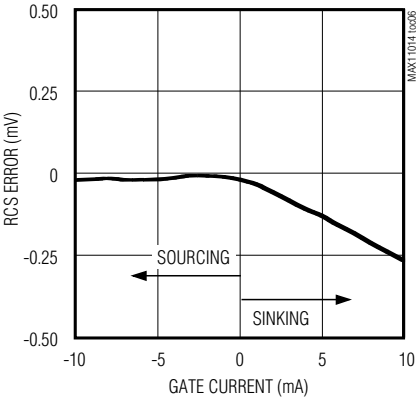
GATE VOLTAGE POWER-UP



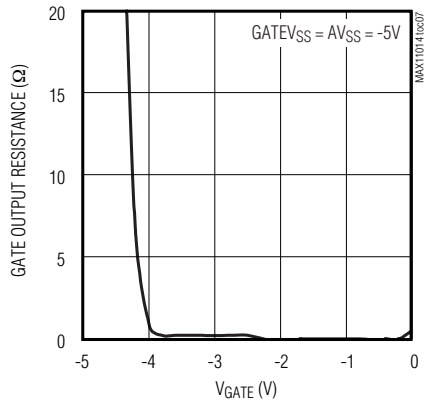
FILT1/FILT3 SETTLING TIME vs. FILT1/FILT3 CAPACITIVE LOAD



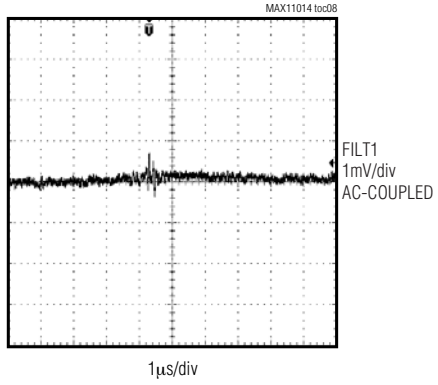
RCS ERROR vs. GATE CURRENT



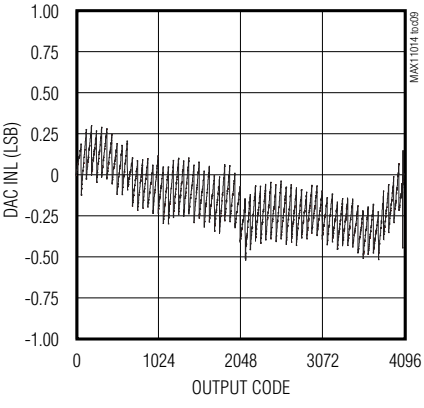
GATE OUTPUT RESISTANCE vs. GATE VOLTAGE



GLITCH IMPULSE



DAC INTEGRAL NONLINEARITY vs. OUPUT CODE

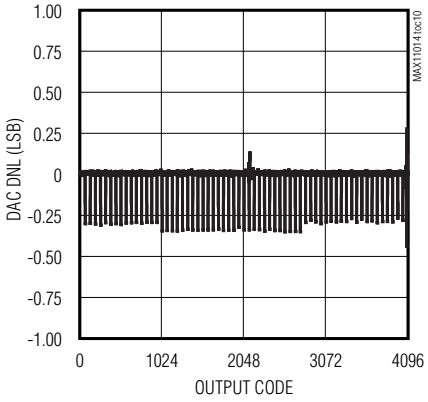


Automatic RF MESFET Amplifier Drain-Current Controllers

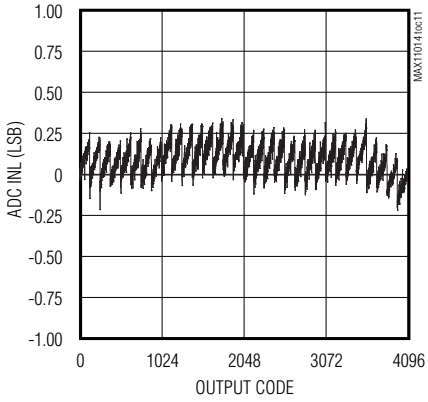
Typical Operating Characteristics (continued)

($V_{GATEVSS}$ = -5.5V; V_{AVDD} = V_{DVDD} = +5V, $GATEV_{SS}$ = AV_{SS} = -5V, external V_{REFADC} = +2.5V; external V_{REFDAC} = +2.5V; C_{REF} = 0.1µF; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

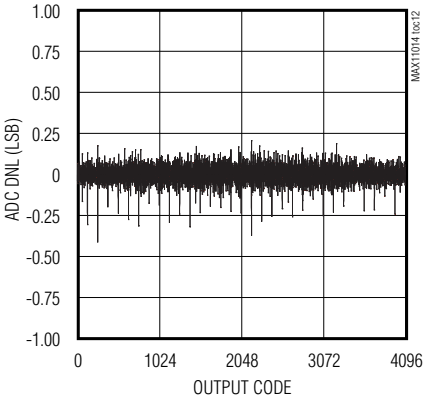
DAC DIFFERTIAL NONLINEARITY vs. OUTPUT CODE



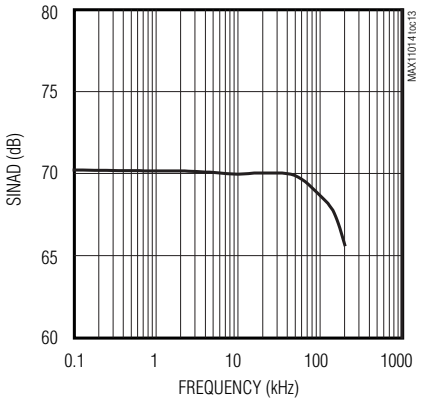
ADC INTEGRAL NONLINEARITY vs. OUTPUT CODE



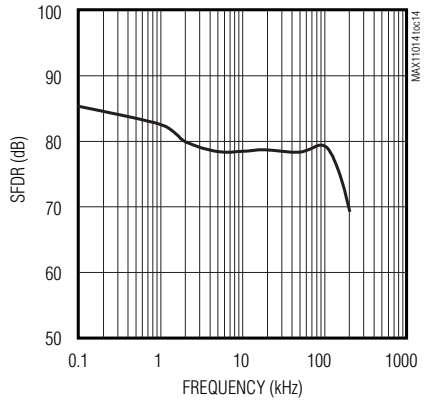
ADC DIFFERENTIAL NONLINEARITY vs. OUTPUT CODE



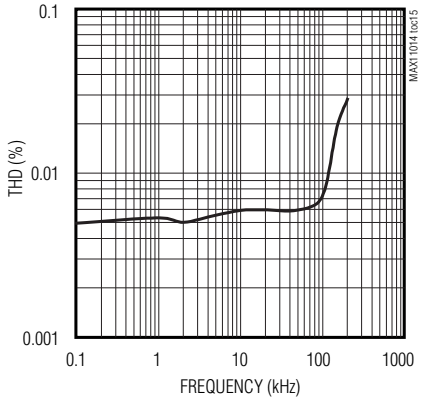
ADC SINAD vs. FREQUENCY



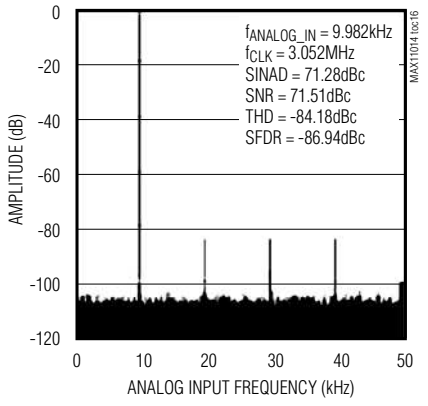
ADC SFDR vs. FREQUENCY



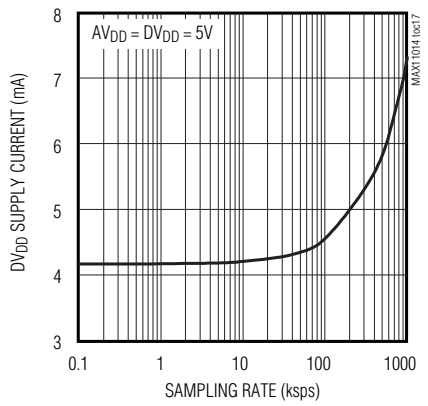
ADC TOTAL HARMONIC DISTORTION vs. FREQUENCY



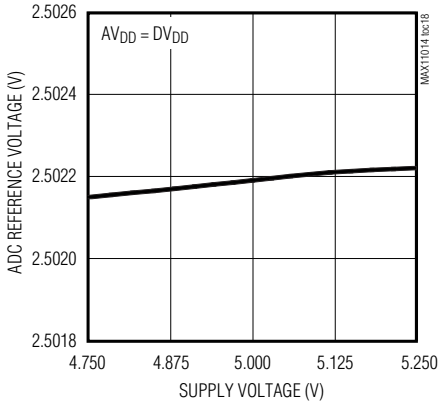
ADC FFT PLOT



DIGITAL SUPPLY CURRENT vs. SAMPLING RATE



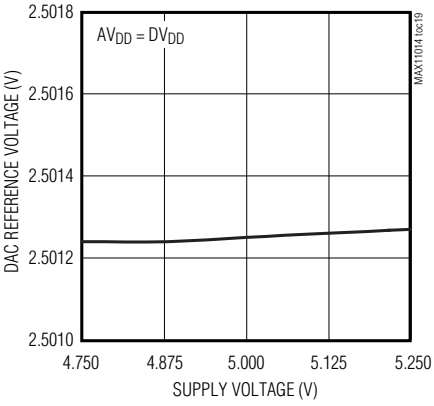
ADC INTERNAL REFERENCE VOLTAGE vs. SUPPLY VOLTAGE



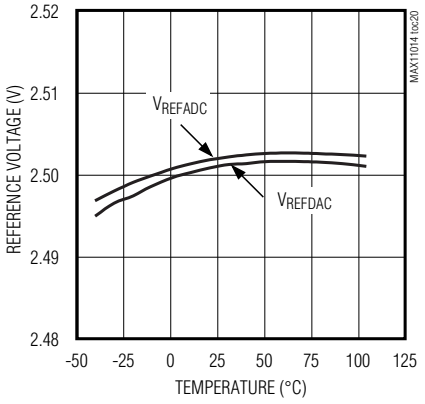
Typical Operating Characteristics (continued)

($V_{GATEVSS}$ = -5.5V; V_{AVDD} = V_{DVDD} = +5V, $GATEV_{SS}$ = AV_{SS} = -5V, external V_{REFADC} = +2.5V; external V_{REFDAC} = +2.5V; C_{REF} = 0.1µF; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

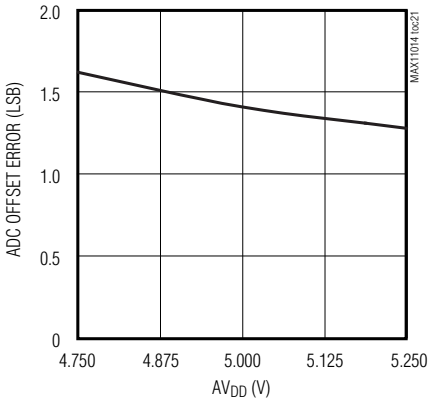
DAC INTERNAL REFERENCE VOLTAGE vs. SUPPLY VOLTAGE



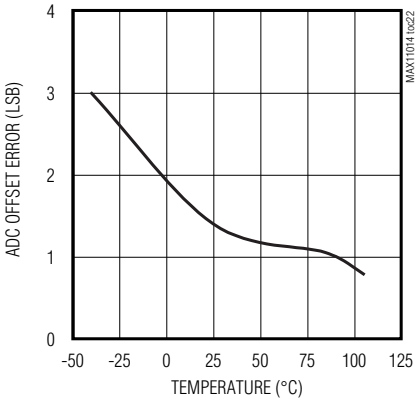
INTERNAL REFERENCE VOLTAGE vs. TEMPERATURE



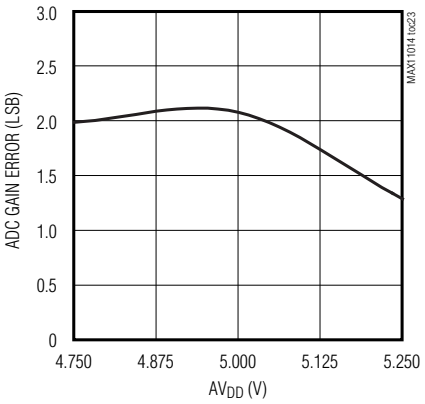
ADC OFFSET ERROR vs. ANALOG SUPPLY VOLTAGE



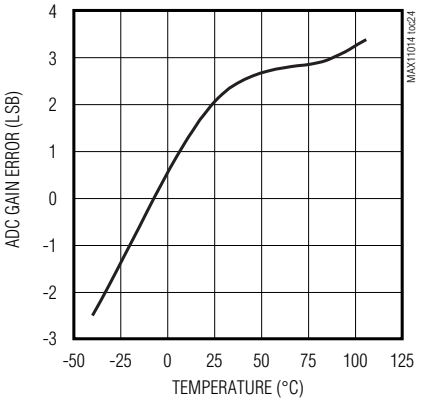
ADC OFFSET ERROR vs. TEMPERATURE



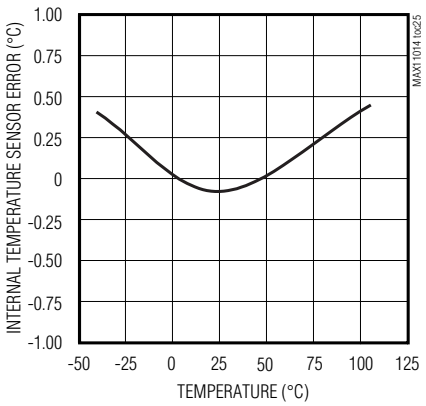
ADC GAIN ERROR vs. ANALOG SUPPLY VOLTAGE



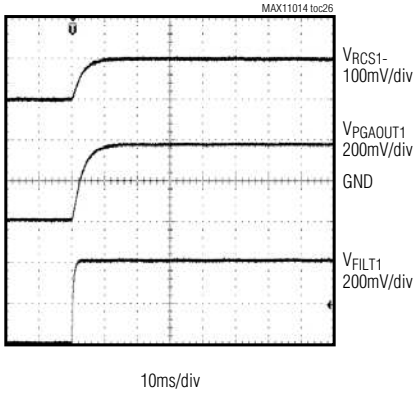
ADC GAIN EROR vs. TEMPERATURE



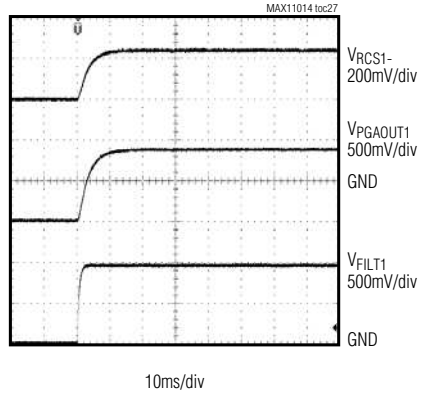
INTERNAL TEMPERATURE SENSOR ERROR vs. TEMPERATURE



0 TO 100mV V_{SENSE} TRANSIENT RESPONSE



0 TO 250mV V_{SENSE} TRANSIENT RESPONSE



Automatic RF MESFET Amplifier Drain-Current Controllers

Pin Description

PIN	NAME	FUNCTION
1	DIN/SDA	Serial Data Input. Data is latched into the serial interface on the rising edge of SCLK in SPI mode. Connect a pullup resistor to SDA in I^2C mode.
2	DOUT/A1	Serial Data Output in SPI Mode/Address Select 1 in I^2C Mode. Data transitions on the falling edge of SCLK. DOUT is high impedance when $\overline{CS}$ is high. Connect A1 to DV_{DD} or DGND to set the device address to I^2C mode.
3	ADCIN1	Analog Input 1
4	ADCIN2	Analog Input 2
5	DXN1	Remote-Diode Current Sink. Connect the emitter of a base-emitter junction remote npn transistor to DXN1.
6	DXP1	Remote-Diode Current Source. Connect DXP1 to the base/collector of a remote temperature-sensing npn transistor. **Do not leave DXP1 open**; connect to DXN1 if no remote diode is used.
7	DXN2	Remote-Diode Current Sink. Connect the emitter of a base-emitter junction remote npn transistor to DXN2.
8	DXP2	Remote-Diode Current Source. Connect DXP2 to the base/collector of a remote temperature-sensing npn transistor. **Do not leave DXP2 open**; connect to DXN2 if no remote diode is used.
9	REFDAC	DAC Reference Input/Output. Connect a 0.1µF capacitor to AGND in external reference mode. See the *HCFG (Read/Write)* section.
10	REFADC	ADC Reference Input/Output. Connect a 0.1µF capacitor to AGND in external reference mode. See the *HCFG (Read/Write)* section.
11, 27	AV_{DD}	Positive Analog Supply Voltage. Set AV_{DD} between +4.75V and +5.25V. Bypass with a 1µF and a 0.1µF capacitor in parallel to AGND.
12, 26	AGND	Analog Ground
13	ACLAMP2	MESFET2 External Clamping Voltage Input
14	GATE2	MESFET2 Gate Connection. See the *Gate-Drive Amplifiers* section.
15	$GATEV_{SS}$	Gate-Drive Amplifier Negative Power-Supply Input. Set $GATEV_{SS}$ between -4.75V and -5.5V. Connect externally to AV_{SS}. Bypass with a 1µF and a 0.1µF capacitor in parallel to AGND.
16, 28, 29, 34–37	N.C.	No Connection. Not internally connected.
17	ACLAMP1	MESFET1 External Clamping Voltage Input
18	GATE1	MESFET1 Gate Connection. See the *Gate-Drive Amplifiers* section.
19	FILT1	Channel 1 Filter 1 Input. See Figures 5 and 6.
20	FILT2	Channel 1 Filter 2 Input. See Figures 5 and 6.
21	FILT3	Channel 2 Filter 3 Input. See Figures 5 and 6.
22	FILT4	Channel 2 Filter 4 Input. See Figures 5 and 6.
23	PGAOUT1	Channel 1 Amplifier Voltage Output. See the *PGAOUT Outputs* section and Figures 5 and 6.
24	PGAOUT2	Channel 2 Amplifier Voltage Output. See the *PGAOUT Outputs* section and Figures 5 and 6.
25	AV_{SS}	Negative Analog Supply Voltage. Set AV_{SS} between -4.75V and -5.5V. Connect externally to $GATEV_{SS}$. Bypass with a 1µF and a 0.1µF capacitor in parallel to AGND.

Pin Description (continued)

PIN	NAME	FUNCTION
30	RCS2+	Channel 2 Current-Sense-Resistor Connection. Connect to the external supply powering channel 2's MESFET drain, in the range of +0.5V to +11V (MAX11014) or +5V to +32V (MAX11015). Bypass with a 1µF and a 0.1µF capacitor in parallel to AGND. If unused, connect to RCS1+.
31	RCS2-	Channel 2 Current-Sense-Resistor Connection. Connect to the channel 2 MESFET drain. Decouple as required by the application. If unused, connect to RCS2+.
32	RCS1-	Channel 1 Current-Sense-Resistor Connection. Connect to the channel 1 MESFET drain. Decouple as required by the application. If unused, connect to RCS1+.
33	RCS1+	Channel 1 Current-Sense-Resistor Connection. Connect to the external supply powering channel 1's MESFET drain, in the range of +0.5V to +11V (MAX11014) or +5V to +32V (MAX11015). Bypass with a 1µF and a 0.1µF capacitor in parallel to AGND. If unused, connect to RCS2+.
38	OPSAFE1	Operating Safe Channel 1 Input. Set OPSAFE1 high to clamp GATE1 to ACLAMP1 for fast protection of enhancement FET power transistors.
39	OPSAFE2	Operating Safe Channel 2 Input. Set OPSAFE2 high to clamp GATE2 to ACLAMP2 for fast protection of enhancement FET power transistors.
40	BUSY	BUSY Output. BUSY asserts high under certain conditions when the device is busy. See the *BUSY Output* section.
41	DV_{DD}	Digital Supply Voltage. Set DV_{DD} between +2.7V and AV_{DD}. Bypass with a 1µF and a 0.1µF capacitor in parallel to DGND.
42	DGND	Digital Ground
43	$\overline{CNVST}$	Active-Low Conversion Start Input. Set $\overline{CNVST}$ low to begin a conversion in clock modes 01 and 11. Connect $\overline{CNVST}$ to DV_{DD} when issuing conversion commands through the serial interface.
44	ALARM	ALARM Output. ALARM asserts when the temperature or voltage measurements exceed their preset high or low thresholds.
45	$\overline{CS}$/A0	Chip-Select Input in SPI Mode/Address Select 0 in I^2C Mode. $\overline{CS}$ is an active-low input. When $\overline{CS}$ is low, the serial interface is enabled. When $\overline{CS}$ is high, DOUT is high impedance. Connect A0 to DV_{DD} or DGND to set the device address in I^2C mode.
46	SPI/$\overline{I2C}$	SPI-/I^2C-Interface Select Input. Connect SPI/$\overline{I2C}$ to DV_{DD} to select SPI mode. Connect SPI/$\overline{I2C}$ to DGND to select I^2C mode.
47	N.C./A2	No Connection in SPI Mode/Address Select 2 in I^2C Mode. Connect A2 to DV_{DD} or DGND to set the device address in I^2C mode.
48	SCLK/SCL	Serial Clock Input. Clocks data in and out of the serial interface. (Duty cycle must be 40% to 60%.) Connect a pullup resistor to SCL in I^2C mode. See Table 10 for details on programming the clock mode.
—	EP	Exposed Pad. Connect to AGND and a large copper plane to meet power dissipation specifications. Do not use as a ground connection.

Automatic RF MESFET Amplifier Drain-Current Controllers

Detailed Description

The MAX11014/MAX11015 set and monitor the bias conditions for dual MESFET power devices found in cellular base stations and point-to-point microwave links. The internal DAC sets the voltage across the current-sense resistor by controlling the GATE voltage. These devices integrate a 12-bit ADC to measure voltage, internal and external temperature, and communicate through a 4-wire 20MHz SPI-/MICROWIRE-compatible serial interface or 2-wire 3.4MHz I^2C-compatible serial interface (pin-selectable).

The MAX11014/MAX11015 operate from an internal +2.5V reference or individual ADC and DAC external references. The external current-sense resistors monitor voltages over the 0 to (V_{DACREF} / 4) range. Two current-sense amplifiers with a preset gain of four monitor the voltage across the sense resistors. The MAX11014/MAX11015 accurately measure their internal die temperature and two external remote diode temperature sensors. The remote pn junctions are typically the base-emitter junction of an npn transistor, either discrete or integrated on a CPU, FPGA, or ASIC.

The MAX11014/MAX11015 also feature an ALARM output that can be triggered during an internal or external overtemperature condition, an excessive current-sense voltage, or an excessive GATE voltage. Figure 4 shows the MAX11014's functional diagram.

The MAX11014 integrates complete dual analog closed-loop drain-current controllers for Class A MESFET amplifier operation. See the *MAX11014 Class A Control Loop* section. The analog control loop sets the drain current through the current-sense resistors. The MESFET gate-drive amplifier can vary the DAC code accordingly if the temperature or other system variables change.

Implement Class A amplifier operation with the following three steps:

1) Characterization

   Characterize the MESFET over temperature to determine the amplifier's set of drain-current values, assuming the part-to-part calibration curve is consistent. There may be an offset shift, but no important change in the shape of the function. Load these values into the MAX11014 LUTs at power-up. In operation, there is a linear interpolation between the values stored in the LUTs.

   Adjust the drain current for other variables such as output power or drain voltage by loading values into the numerical KLUTs.

2) Calibration

   In production of the power amplifier, measure the quiescent drain current at a fixed calibration temperature (probably room) and adjust the $V_{SET(CODE)}$ value until the drain current is within the specified limits for that temperature. The $V_{SET(CODE)}$ value is stored for loading after power-up. Prior to operation, command a PGA calibration after powering up by writing to the PGA calibration control register, setting the TRACK bit to 0 and the DOCAL bit to 1 (see Table 18).

3) Operation

   Upon request, the MAX11014 measures the temperature of the MESFET and compares it with the previous reading. If the temperature reading has changed, the MAX11014 reads the LUTs with the characterization data and updates the DAC to correct the drain current. Setting the TRACK, DOCAL, and SELFTIME bits to 1 in the PGA calibration control register starts automatic monitoring and adjustment of drain current for variations in temperature.

Also, if the KLUTs are used, their values are monitored for changes. A DAC correction is then made if necessary.

For Class AB operation with the MAX11015, measure the MESFET temperature and set the GATE_ voltage through the LUTs and DAC to control the drain current. See the *MAX11015 Class AB Control* section. Implement Class AB amplifier operation with the same three steps as Class A operation, with the exception that the LUTs set the GATE_ voltage for constant drain current with varying temperature.

Power-On Reset

On power-up, the MAX11014/MAX11015 are in full power-down mode (see the *SHUT (Write)* section). To change to normal power mode, write two commands to the shutdown register. Set the FULLPD bit to 0 (other bits in the shutdown register are ignored) on the first command. A second command to this register then activates the internal blocks.

MAX11014 Class A Control Loop

The MAX11014 is designed to set and continuously control the drain current for MESFET power amplifiers configured to operate in Class A. Set the DAC code to control the voltage across the RCS_+ and RCS_- current-sense resistor connections. The MAX11014 internal control loop automatically keeps the voltage across the current-sense resistor to the value set by the DAC. See the *12-Bit DAC* section.

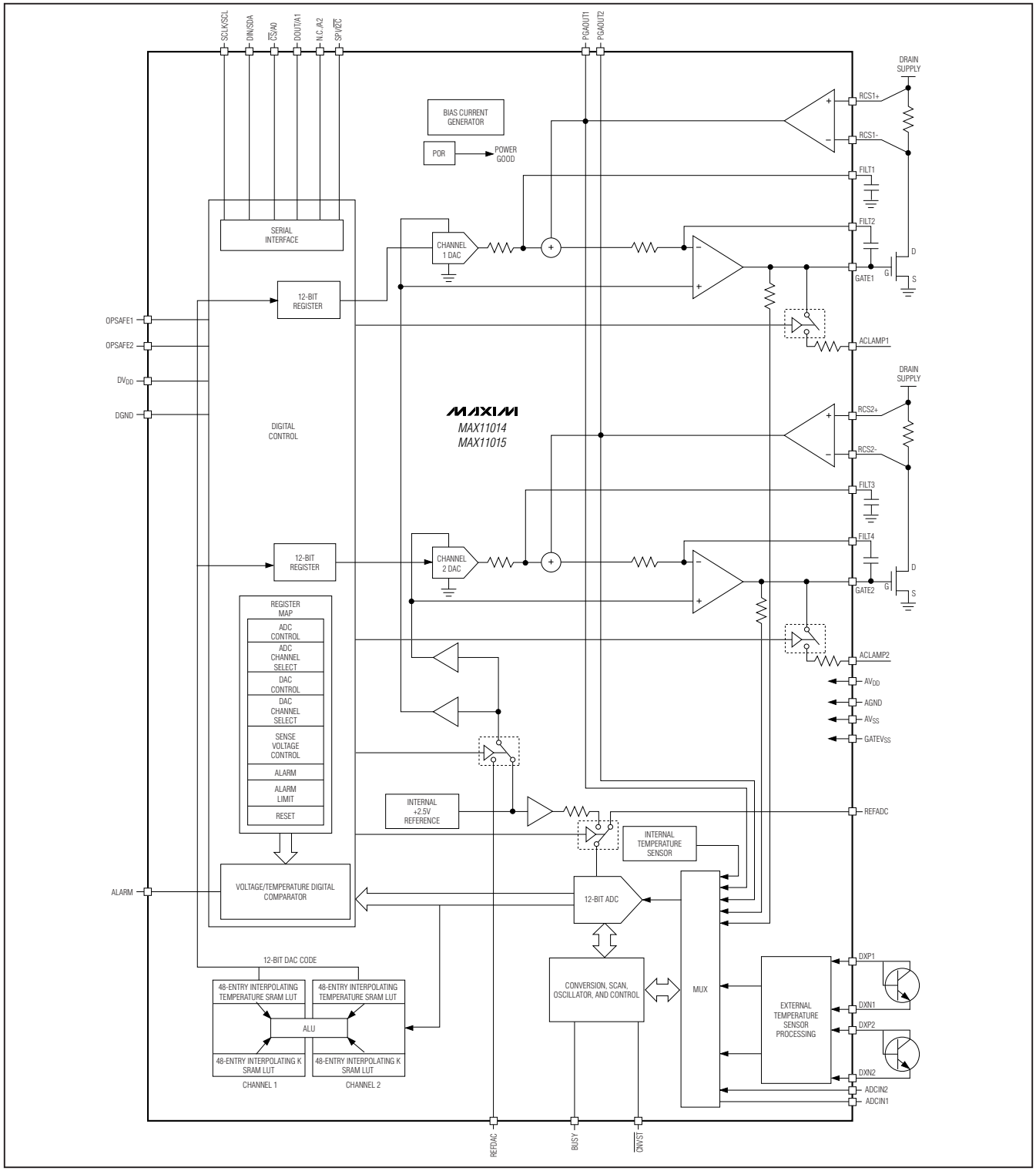


Figure 4. Functional Diagram

Automatic RF MESFET Amplifier Drain-Current Controllers

Once the control loop has been set, the MAX11014 automatically maintains the drain-current value. Figure 5 details the amplifiers that bias the channel 1 and channel 2 control loops.

The dual current-sense amplifiers amplify the voltage between RCS_+ and RCS_- by four and add an offset voltage (+12mV nominally). These current-sense amplifiers amplify sense voltages between 0 and 625mV when V_{REFDAC} = +2.5V. See the *Current-Sense Amplifiers* section.

The current-sense amplifier output injects a scaled-down replica of the MESFET drain current at the summing node to complete the internal analog feedback loop. The summing node drives the gate-drive amplifier through a 100kΩ series resistor. The gate-drive amplifier is configured as an integrator by the external capacitor connected between GATE1/GATE2 and FILT2/FILT4. The gate-drive amplifier includes automatic offset cancellation between 0 and 24mV to null the 12mV offset from the current-sense amplifier. See the *Register Descriptions* and *PGACAL (Write)* sections.

The MAX11014's analog control loop setpoint is described by the following equation:

$$V_{RCS\_+} - V_{RCS\_-} = \frac{V_{FILT}(CODE = 000h) - V_{FILT}}{4}$$

where:

$V_{FILT}(CODE = 000h) = V_{FILT1}$ (channel 1) and V_{FILT3} (channel 2) when the THRUDAC1/THRUDAC2 register code is set to 000h.

$V_{FILT} = V_{FILT1}$ (channel 1) and V_{FILT3} (channel 2).

V_{RCS_+} - V_{RCS_-} = the voltage drop across the current-sense resistor.

Connect a capacitor from FILT2 to GATE1 to form an integrator (setting the control-loop dominant pole) with the channel 1 internal 100kΩ resistor. Connect a capacitor from FILT4 to GATE2 to form an integrator (setting the control-loop dominant pole) with the channel 2 internal 100kΩ resistor. The gate-drive amplifier's output drives the MESFET gates. See the *Gate-Drive Amplifiers* section.

The channel 1 DAC voltage is output to FILT1 through a series 580kΩ resistor. The channel 2 DAC voltage is output to FILT3 through a series 580kΩ resistor. Connect a capacitor from FILT1 to AGND and FILT3 to AGND to set the filter's time constant for the respective channel.

MAX11015 Class AB Control

The MAX11015 is designed to be used with a Class AB amplifier configuration to independently measure the drain current and set the GATE_ output voltages through the serial interface. After sensing the drain current with no RF signal applied, set the DAC code to obtain the desired GATE_ voltage. Figure 6 details the amplifiers that bias the channel 1 and channel 2 control.

The MAX11015 internal 12-bit DAC voltage is applied to the gate-drive amplifier, which has a preset gain of -2. See the *Gate-Drive Amplifiers* section. Setting the DAC code between FFFh and 000h typically produces a GATE_ voltage between 0 and (-2 x V_{REFDAC}). See the *HCFG (Read/Write)* section for details on adjusting the GATE_ maximum voltage.

The channel 1 DAC voltage is output to FILT1 through a series 580kΩ resistor. The channel 2 DAC voltage is output to FILT3 through a series 580kΩ resistor. Connect a capacitor from FILT1 to AGND and FILT3 to AGND to set the filter's time constant for the respective channel. Connect FILT2 and FILT4 to AGND (MAX11015 only).

The dual current-sense amplifiers amplify the voltage between RCS_+ and RCS_- by four and add an offset voltage (+12mV nominally). The current-sense amplifiers amplify sense voltages between 0 and 625mV when V_{REFDAC} = +2.5V. See the *Current-Sense Amplifiers* section.

Current-Sense Amplifiers

The dual current-sense amplifiers amplify the voltage between RCS_+ and RCS_- and add an offset voltage. Connect a resistor between RCS_+ and RCS_- to sense the MESFET drain current. The current-sense amplifiers scale the sense voltage by four. These amplifiers also reject the drain supply voltage that appears as a DC common-mode level on the current signal.

The gate-drive amplifier includes automatic offset cancellation between 0 and 24mV to null the 12mV offset from the current-sense amplifier. See the *PGACAL (Write)* section.

Gate-Drive Amplifiers

The gate-drive amplifiers control the MESFET gate bias settings. The MAX11014's channel 1 and channel 2 DAC voltages are routed through a summing node and into the gate-drive amplifiers. The MAX11015's channel 1 and channel 2 DAC voltages are routed directly to the gate-drive amplifiers, which have a preset gain of -2. See the *12-Bit DAC* section for details on setting the DAC codes.

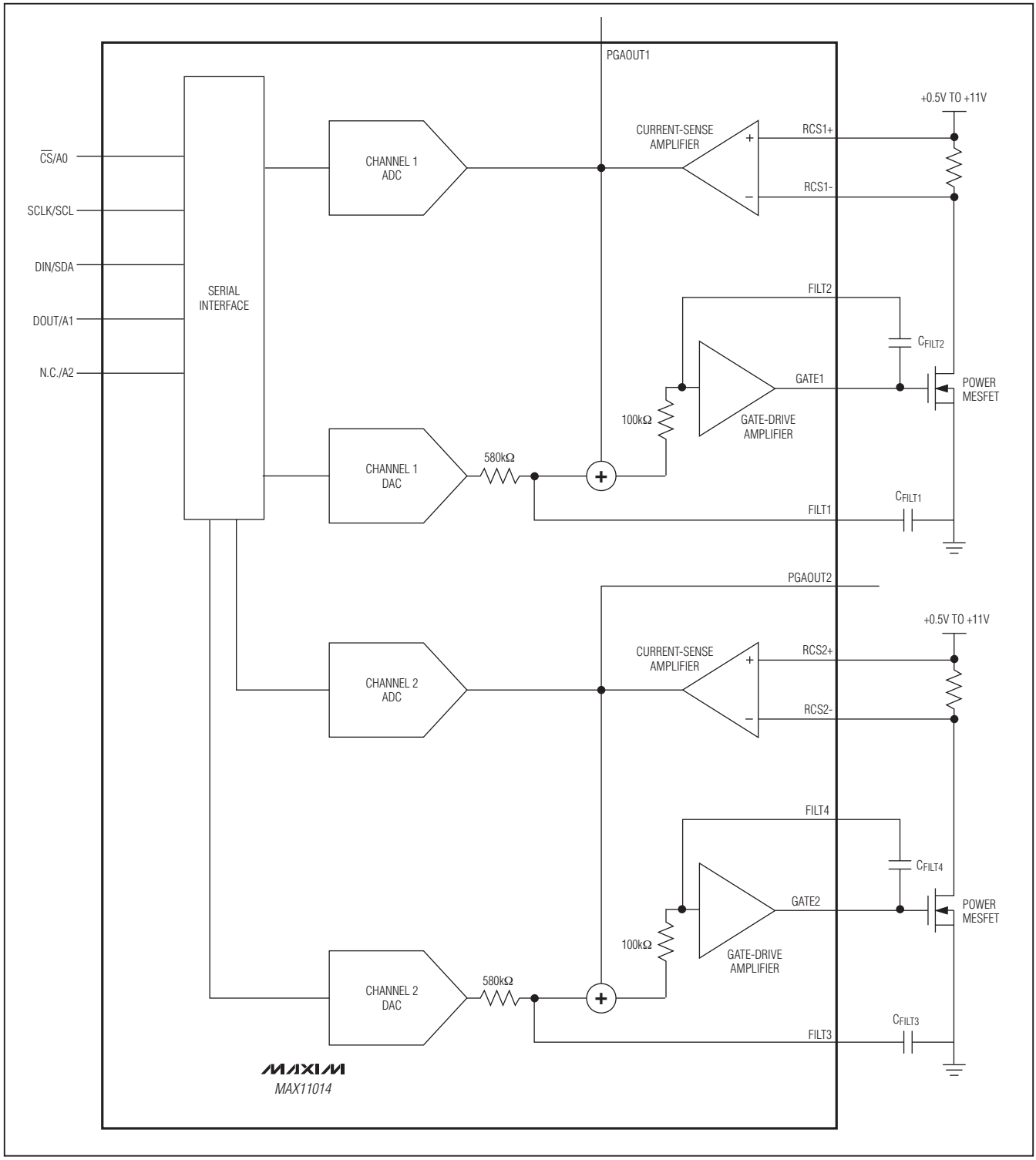


Figure 5. MAX11014 Class A Analog Control Loop

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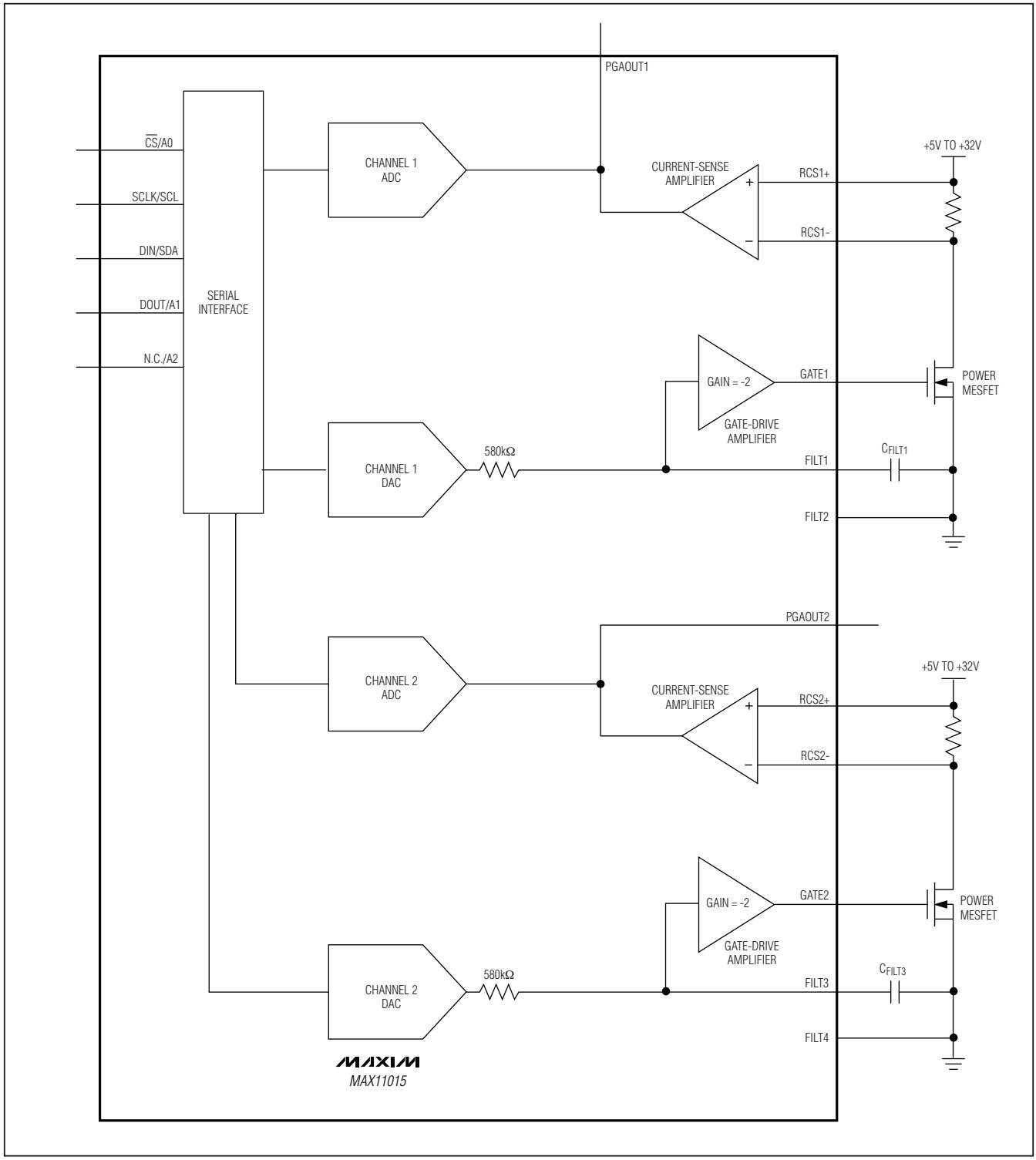

Figure 6. MAX11015 Class AB Analog Control

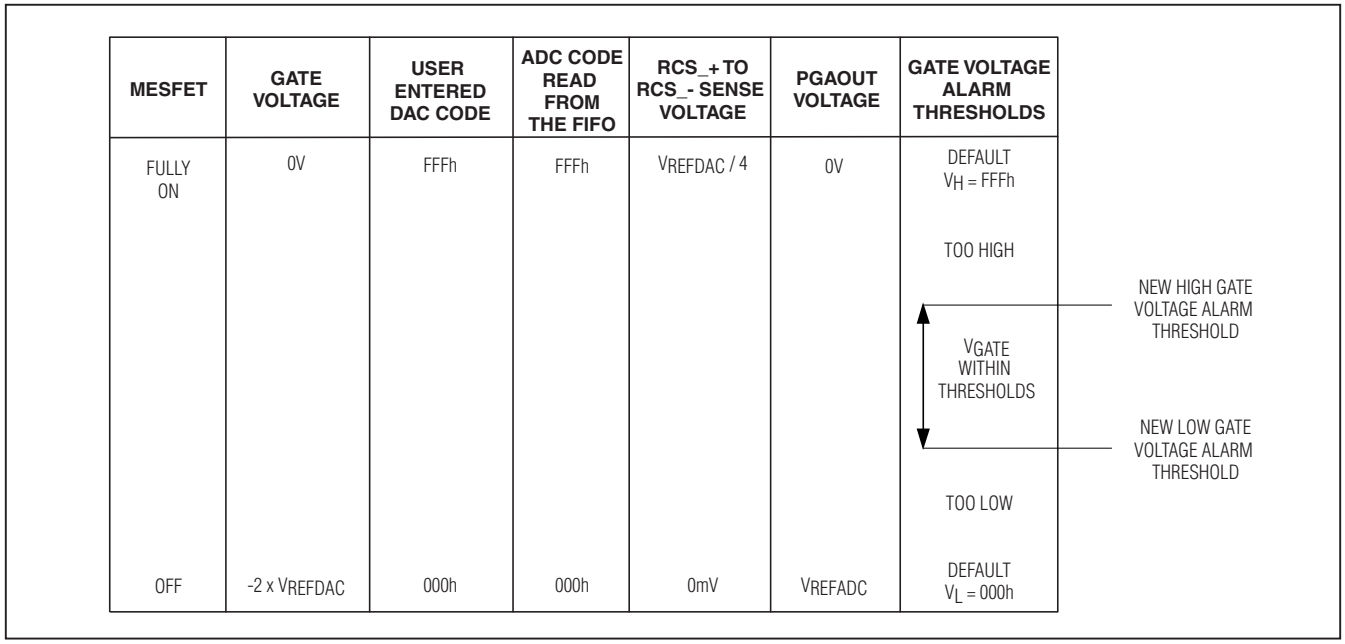

Figure 7. DAC Code Range

Connect the MESFET drain to the RCS_- input. Connect the MESFET's gate to the GATE_ output. Set the GATE_ voltage to -2 x V_{REFDAC} to turn the MESFET fully off. Set the GATE_ voltage to 0V to turn the MESFET fully on. See Figure 7.

The MAX11014/MAX11015 GATE_ output voltage can be clamped to the external voltage applied at ACLAMP_. Setting OPSAFE_ high clamps the GATE_ voltage unconditionally. The GATE_ can also be clamped by different commands issued through the serial interface. These devices can also monitor the alarms through the software to modify the clamping mechanism. See the *Automatic GATE Clamping* and *ALMHCFG (Read/Write)* sections.

12-Bit ADC Description

The MAX11014/MAX11015 ADCs use a fully differential successive-approximation register (SAR) conversion technique and on-chip track-and-hold (T/H) circuitry to convert temperature and voltage signals into 12-bit digital results. The analog inputs accept single-ended input signals. Single-ended signals are converted using a unipolar transfer function. See the *ADC Transfer Function* section for more details.

The internal ADC block converts the results of the internal die temperature, remote diode temperature readings, current-sense voltages, and ADCIN_ voltages. The ADC block also reads back the GATE_ analog output voltage and converts it to a 12-bit digital result. The conversion results are written to the FIFO memory. The FIFO holds up to 15 words (each word of 16 bits) with a leading 4-bit channel tag to indicate which channel the 12-bit data comes from. See Table 25. The FIFO reads back data words either one at a time or continuously. See the *ADCCON (Write)* section. The FIFO always stores the most recent conversion results and allows the oldest data to be overwritten. The FIFO indicates an overflow condition and underflow condition (read of an empty FIFO) through the flag register. See the *FLAG (Read)* section.

Analog Input Track and Hold

The equivalent circuit of Figure 8 details the MAX11014/MAX11015's ADCIN_ input architecture. In track mode, a positive input capacitor is connected to ADCIN1/ADCIN2. A negative input capacitor is connected to AGND. After the T/H enters hold mode, the difference between the sampled input voltages and AGND is converted. The input-capacitance charging rate determines the time required for the T/H to acquire an input signal. The required acquisition time lengthens with the increase of the input signal's source impedance. Any source impedance below 300Ω does not significantly affect the ADC's AC performance. A high-impedance source can be accommodated either by placing a 1µF capacitor between ADCIN_ and AGND. The combination of the analog-input source impedance and the capacitance at the analog input creates an RC

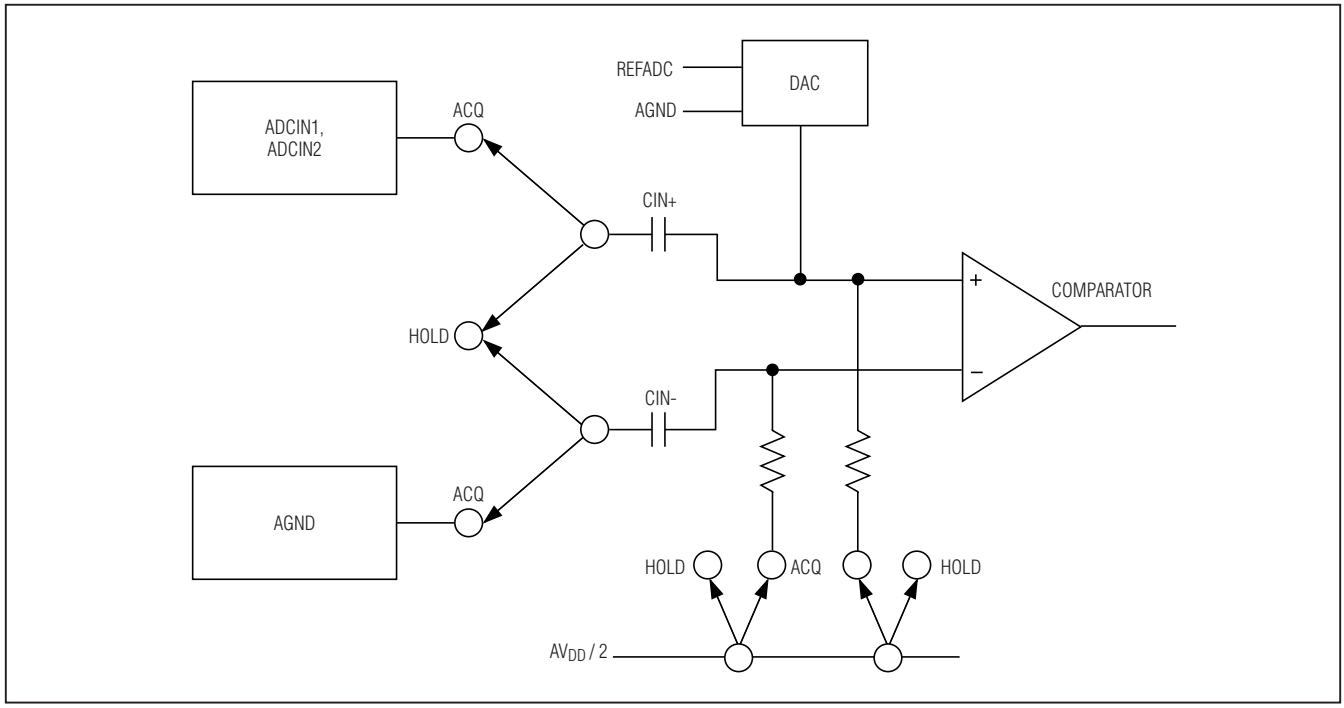

Figure 8. ADC Equivalent Input Circuit

filter that limits the analog-input bandwidth.

Analog Input Protection

Internal ESD protection diodes clamp ADCIN1/ADCIN2 to AV_{DD} and AGND, allowing them to swing from (AGND - 0.3V) to (AV_{DD} + 0.3V) without damage. However, for accurate conversions near full scale, the inputs must not exceed AV_{DD} by more than 50mV or be lower than AGND by 50mV. If an analog input voltage exceeds the supplies, limit the input current to 2mA.

Temperature Measurements

The MAX11014/MAX11015 measure their internal die temperature and two external remote-diode temperatures. Write to the ADC conversion register to command a temperature conversion. See Table 19. Set the CH6 bit to 1 to calculate the remote-diode DXP2/DXN2 temperature sensor reading and load the data into the FIFO. Set the CH1 bit to 1 to calculate the remote-diode DXP1/DXN1 temperature-sensor reading and load the data into the FIFO. Set the CH0 bit to 1 to calculate the internal die temperature-sensor reading and load the data into the FIFO. Temperature data is output in signed two's-complement format at DOUT in SPI mode and SDA in I^2C mode. See Figure 22 for the temperature transfer function.

The MAX11014/MAX11015 perform internal temperature measurements with a diode-connected transistor. The diode bias current changes from 66µA to 4µA to produce a temperature-dependent bias voltage difference. The second conversion result at 4µA is subtracted from the first at 66µA to calculate a digital value that is proportional to absolute temperature. The stored data result is the above digital code minus an offset to adjust from Kelvin to Celsius. The reference voltage for the temperature measurements is derived from the internal reference source to ensure the temperature calibration of 1 LSB corresponding to +0.125°C.

For external temperature readings, connect an npn transistor between DXP_ and DXN_. Connect the base and collector together as shown in Figure 4 to form a base-emitter pn junction. The MAX11014/MAX11015 feature an ALARM output that trips when the internal or external temperature rises above an upper threshold value or drops below a lower threshold value. Set the high and low temperature thresholds through the channel 1/channel 2 high/low temperature ALARM threshold registers. See Tables 3, 4, and 5.

The temperature-sensing circuits power up for the first temperature measurement in an ADC conversion scan. The temperature-sensing block remains on until the end of the scan to avoid an additional 50µs power-up delay for each individual temperature channel. See the

ADCCON (Write) section, Figure 31, and Figure 32. The temperature-sensor circuits remain powered up when the ADC conversion register's continuous convert bit (CONCONV) is set to 1 and the current ADC conversion includes a temperature channel. The temperature-sensor circuits remain powered up until the CONCONV bit is set low.

The external temperature sensor drive current ratio has been optimized for a 2N3904 npn transistor with an ideality factor of 1.0065. The nonideality offset is removed internally by a preset digital coefficient. Using a transistor with a different ideality factor produces a proportionate difference in the absolute measured temperature. For more details on this topic and others related to using an external temperature sensor, see Application Note 1057: *Compensating for Ideality Factor and Series Resistance Differences between Thermal Sense Diodes* and Application Note 1944: *Temperature Monitoring Using the MAX1253/54 and MAX1153/54* on Maxim's website: **www.maxim-ic.com**.

12-Bit DAC

The MAX11014/MAX11015 include two voltage-output, 12-bit monotonic DACs with ±1 LSB integral nonlinearity error and ±0.4 LSB differential nonlinearity error. The DAC operates from the internal +2.5V reference or an external reference voltage supplied at REFDAC. When using an external voltage reference, bypass REFDAC with a 0.1µF capacitor to AGND. The REFDAC external voltage range is +0.7V to +2.5V.

The MAX11014's channel 1/channel 2 DACs set the sense voltage between RCS_+ and RCS_- by controlling the GATE_ bias. See the *MAX11014 Class A Control Loop* section. The MAX11015's channel 1/channel 2 DACs drive the GATE_ outputs directly, independent of the current-sense voltages, through the gate-drive amplifier with a gain of -2. See the *MAX11015 Class AB Control* section.

Set the channel 1/channel 2 DAC code by writing to the respective channel's DAC input registers, DAC input and output registers, or V_{SET} registers. Write to the DAC input registers (Table 16) and use a subsequent write to the software load DAC register (Table 21) to control the timing of the update. Write to the DAC input and output registers (Table 17) to set the DAC output voltage code directly, independent of the software load DAC register bits. Write to the V_{SET} registers (Table 14) to include LUT data in the DAC code. Writing to the V_{SET} registers triggers a $V_{DAC(CODE)}$ calculation as shown in the following equation:

$$V_{DAC(CODE)} = V_{SET(CODE)} = (1 + LUT_K[K] \times LUT_{TEMP}[TEMP])$$

where

$V_{DAC(CODE)}$ = The modified channel 1/channel 2 12-bit DAC code.

$V_{SET(CODE)}$ = The 12-bit DAC code written to the channel 1 /channel 2 V_{SET} registers.

$LUT_K[K]$ = The interpolated, fractional 12-bit KLUT value. The KLUT data is derived from a variety of sources, including: the V_{SET} register value, the K parameter register value, or various ADC channels. See the *SRAM LUTs* section.

$LUT_{TEMP}[TEMP]$ = The interpolated, fractional 12-bit two's-complement temperature LUT value. The temperature LUT data is derived from either internal or external temperature values. See the *SRAM LUTs* section.

The $V_{DAC(CODE)}$ equation code is then loaded into the DAC input register or DAC output register, depending on the corresponding channel's LDAC bit in the software configuration register. See Table 11.

Self-Calibration

Calibrate channel 1 and channel 2 by writing to the PGA calibration control register. The MAX11014/MAX11015 function after power-up without a calibration. However, for best performance after powering up, command a calibration by setting the TRACK bit to 0 and the DOCAL bit to 1 (see Table 18). Subsequently, set the TRACK, DOCAL, and SELFTIME bits to 1 to minimize loss of performance over temperature and supply voltage.

The self-calibration algorithm cancels offsets at the gate-drive amplifier inputs in approximately 95µV increments to improve accuracy. The self-calibration routine can be commanded when the DACs are powered down, but the results will not be accurate. For best results, run the calibration after the DAC power-up time, t_{DPUEXT}. The ADC's operation is suspended during a self-calibration. The end of the self-calibration routine is indicated by the BUSY output returning low. See the *BUSY Output* section. Wait until the end of the self-calibration routine before requesting an ADC conversion.

Automatic RF MESFET Amplifier Drain-Current Controllers

ADC/DAC References

The MAX11014/MAX11015 provide an internal low-noise +2.5V reference for the ADCs, DACs, and temperature sensors. Set bits D3–D0 within the hardware configuration register to control the source of the DAC and ADC references. See Tables 10c and 10d.

Connect a voltage source to REFADC between +1.0V and AV_{DD} in external ADC reference mode. Connect a voltage source to REFDAC between +0.7V to +2.5V in external DAC reference mode. When using an external voltage reference, bypass REFADC and REFDAC with 0.1µF capacitors to AGND.

Power Supplies

The MAX11014/MAX11015 operate from separate analog and digital power supplies. Set the analog supply voltage, AV_{DD}, between +4.75V and +5.25V. Set the digital supply voltage, DV_{DD}, between +2.7V and AV_{DD}. Bypass AV_{DD} with a 0.1µF and 1µF capacitor to AGND and DV_{DD} with a 0.1µF and 1µF capacitor to DGND. The analog circuitry typically consumes 2.8mA of supply current and the digital circuitry 3.7mA.

Set the negative analog supply voltages, AV_{SS} and $GATEV_{SS}$, between -4.75V and -5.5V. Connect AV_{SS} and $GATEV_{SS}$ together externally. Bypass each of these negative supplies with a 0.1µF and 1µF capacitor to AGND.

The RCS_+ inputs supply the power to the input section of the current-sense amplifiers. Set RCS_+ between +0.5V and +11V on the MAX11014 and +5V to +32V on the MAX11015. Bypass RCS_+ with a 0.1µF and 1µF capacitor to AGND.

Serial Interface

The MAX11014/MAX11015 feature a pin-selectable I^2C/SPI serial interface. Connect SPI/$\overline{I2C}$ to DGND to select I^2C mode, or connect SPI/$\overline{I2C}$ to DV_{DD} to select SPI mode. SDA and SCL (I^2C mode) and DIN, SCLK, and $\overline{CS}$ (SPI mode) facilitate communication between the MAX11014/MAX11015 and the master.

SPI Compatibility (SPI/$\overline{I2C}$ = DV_{DD})

The MAX11014/MAX11015 communicate through a serial interface, compatible with SPI and MICROWIRE devices. For SPI, ensure that the SPI bus master (typically a µC) runs in master mode so it generates the serial clock signal. Set the SCLK frequency to 20MHz or less, and set the clock polarity (CPOL) and phase (CPHA) in the µC control registers to the same value. The MAX11014/MAX11015 operate with SCLK idling high or low, and thus operate with CPOL = CPHA = 0 or CPOL = CPHA = 1. Set $\overline{CS}$ low to latch input data at DIN on the rising edge of SCLK. Output data at DOUT is updated on the falling edge of SCLK. See Figure 1. Temperature values are available in signed two's-complement format, while all others are in straight binary.

A high-to-low transition on $\overline{CS}$ initiates the 24-bit data input cycle. Once $\overline{CS}$ is low, write an 8-bit command byte (MSB first) at DIN to indicate which internal register is being accessed. The command byte also identifies whether the data to follow is to be written into the serial interface or read out. See the *Register Descriptions* section. After writing the command byte, write two data bytes at DIN or read two data bytes at DOUT. Keep $\overline{CS}$ low throughout the entire 24-bit word write. The serial-interface circuitry is common to the ADC and DAC sections.

When writing data, write an 8-bit command word and 16 data bits at DIN. See Figure 9. Data is input to the serial interface on the rising edge of SCLK. When reading data, write an 8-bit command byte at DIN and read the following 16 data bits at DOUT. See Figure 10. Data transitions at DOUT on the falling edge of SCLK. DIN can be set high or low while data is being transferred out at DOUT.

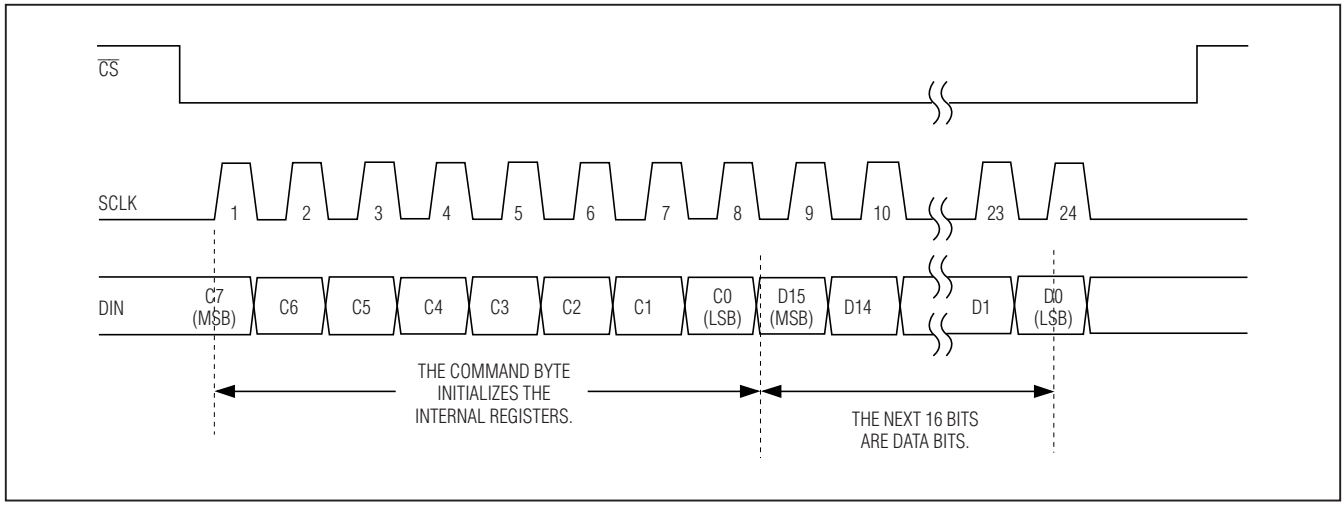

Figure 9. MAX11014/MAX11015 Write Timing

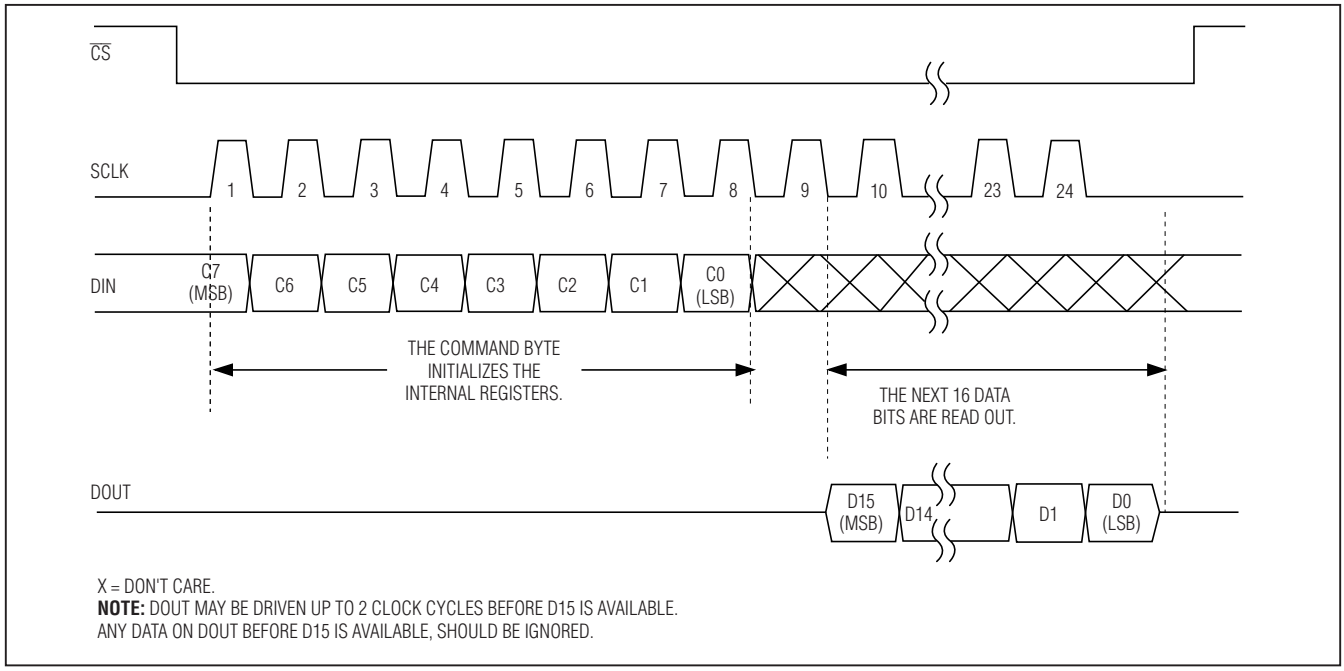

Figure 10. MAX11014/MAX11015 Read Timing