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EVALUATION KIT AVAILABLE

MAXIM

4-/6-/8-Channel, 16-/14-Bit, Simultaneous-Sampling ADCs

MAX11047–MAX11049/MAX11057–MAX11059

General Description

The MAX11047/MAX11048/MAX11049 and MAX11057/ MAX11058/MAX11059 16-bit/14-bit ADCs offer 4, 6, or 8 independent input channels. Featuring independent track and hold (T/H) and SAR circuitry, these parts provide simultaneous sampling at 250ksps for each channel.

The devices accept a 0 to +5V input. All inputs are overrange protected with internal ±20mA input clamps providing overrange protection with a simple external resistor. Other features include a 4MHz T/H input band-width, internal clock, and internal or external reference. A 20MHz, bidirectional, parallel interface provides the conversion results and accepts digital configuration inputs.

The devices operate with a 4.75V to 5.25V analog supply and a separate flexible 2.7V to 5.25V digital supply for interfacing with the host without a level shifter. The MAX11047/MAX11048/MAX11049 are available in a 56-pin TQFN and 64-pin TQFP packages while the MAX11057/ MAX11058/MAX11059 are available in TQFP only. All devices operate over the extended -40°C to +85°C temperature range.

Applications

Automatic Test Equipment

Power-Factor Monitoring and Correction

Power-Grid Protection

Multiphase Motor Control

Vibration and Waveform Analysis

Ordering Information

PART	PIN-PACKAGE	CHANNELS
MAX11047ETN+	56 TQFN-EP*	4
MAX11047ECB+	64 TQFP-EP*	4
MAX11048ETN+	56 TQFN-EP*	6
MAX11048ECB+	64 TQFP-EP*	6
MAX11049ETN+	56 TQFN-EP*	8
MAX11049ECB+	64 TQFP-EP*	8
MAX11057ECB+	64 TQFP-EP*	4
MAX11058ECB+	64 TQFP-EP*	6
MAX11059ECB+	64 TQFP-EP*	8

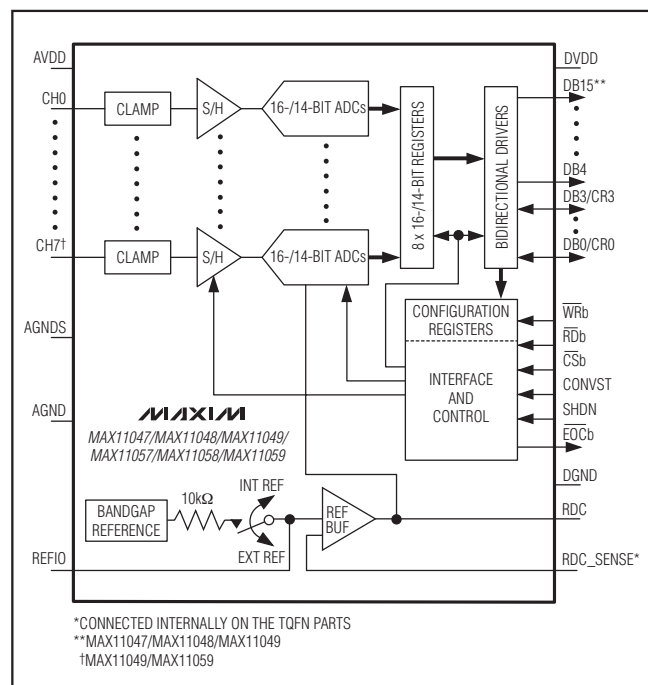**Note:** All devices are specified over the -40°C to +85°C operating temperature range.
+Denotes a lead(Pb)-free/RoHS-compliant package.
*EP = Exposed pad.

Features

♦ **16-Bit ADC (MAX11047/MAX11048/MAX11049)**

♦ **14-Bit ADC (MAX11057/MAX11058/MAX11059)**

♦ **4-Channel ADC (MAX11047/MAX11057)**

♦ **6-Channel ADC (MAX11048/MAX11058)**

♦ **8-Channel ADC (MAX11049/MAX11059)**

♦ **Single Analog and Digital Supply**

♦ **High-Impedance Inputs Up to 1GΩ**

♦ **On-Chip T/H Circuit for Each Channel**

♦ **Fast 3µs Conversion Time**

♦ **High Throughput: 250ksps for Each Channel**

♦ **16-/14-Bit, High-Speed, Parallel Interface**

♦ **Internal Clocked Conversions**

♦ **10ns Aperture Delay**

♦ **100ps Channel-to-Channel T/H Matching**

♦ **Low Drift, Accurate 4.096V Internal Reference Providing an Input Range of 0 to 5V**

♦ **External Reference Range of 3.0V to 4.25V, Allowing Full-Scale Input Ranges of +3.7V to +5.2V**

♦ **56-Pin TQFN (8mm x 8mm) and 64-Pin TQFP (10mm x 10mm) Packages**

♦ **Evaluation Kit Available (MAX11046EVKIT+)**

Functional Diagram

*CONNECTED INTERNALLY ON THE TQFN PARTS
**MAX11047/MAX11048/MAX11049
†MAX11049/MAX11059

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

4-/6-/8-Channel, 16-/14-Bit, Simultaneous-Sampling ADCs

ABSOLUTE MAXIMUM RATINGS

AVDD to AGND ....-0.3V to +6V
DVDD to AGND and DGND ....-0.3V to +6V
DGND to AGND..-0.3V to +0.3V
AGNDS to AGND..-0.3V to +0.3V
CH0–CH7 to AGND ....-2.5V to +7.5V
REFIO, RDC to AGND ....-0.3V to the lower of
                                                             (AVDD + 0.3V) and +6V
$\overline{EOC}$, $\overline{WR}$, $\overline{RD}$, $\overline{CS}$, CONVST to AGND.........-0.3V to the lower of
                                                             (DVDD + 0.3V) and +6V
DB0–DB15 to AGND ....-0.3V to the lower of
                                                             (DVDD + 0.3V) and +6V

Maximum Current into Any Pin Except AVDD, DVDD, AGND,
    DGND ....±50mA
Continuous Power Dissipation (T_A = +70°C)
    56-Pin TQFN (derated 47.6mW/°C above +70°C) ..3809.5mW
    64-Pin TQFP (derate 43.5mW/°C above +70°C 3478mW
Operating Temperature Range ....-40°C to +85°C
Junction Temperature...+150°C
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C
Soldering Temperature (reflow) ....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{AVDD} = 4.75V to 5.25V, V_{DVDD} = +2.7V to 5.25V, V_{AGNDS} = V_{AGND} = V_{DGND} = 0V, V_{REFIO} = internal reference, C_{RDC} = 4 x 33µF, C_{REFIO} = 0.1µF, C_{AVDD} = 4 x 0.1µF ll 10µF, C_{DVDD} = 3 x 0.1µF ll 10µF; all digital inputs at DVDD or DGND, unless otherwise noted. T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC PERFORMANCE (Note 1)						
Resolution	N	MAX11047/MAX11048/MAX11049	16			Bits
		MAX11057/MAX11058/MAX11059	14			
Integral Nonlinearity	INL	MAX11047/MAX11048/MAX11049	-2	±0.65	+2	LSB
		MAX11057/MAX11058/MAX11059	-0.9	±0.2	+0.9	
Differential Nonlinearity	DNL	MAX11047/MAX11048/MAX11049	> -1	±0.7	< +1.2	LSB
		MAX11057/MAX11058/MAX11059	-0.6	±0.2	+0.7	
No Missing Codes		MAX11047/MAX11048/MAX11049	16			Bits
		MAX11057/MAX11058/MAX11059	14			
Offset Error				±0.001	±0.012	%FSR
Offset Temperature Coefficient				±0.8		µV/°C
Channel Offset Matching					±0.01	%FSR
Gain Error					±0.012	%FSR
Positive Full-Scale Error					±0.017	%FSR
Positive Full-Scale Error Matching					±0.01	%FSR
Channel Gain-Error Matching		Between all channels			±0.01	%FSR
Gain Temperature Coefficient				±0.6		ppm/°C
DYNAMIC PERFORMANCE						
Signal-to-Noise Ratio	SNR	MAX11047/MAX11048/MAX11049, f_{IN} = 10kHz, full-scale input	90.7	92.3		dB
		MAX11057/MAX11058/MAX11059, f_{IN} = 10kHz, full-scale input	84.5	85.3		

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ELECTRICAL CHARACTERISTICS (continued)

V_{AVDD} = 4.75V to 5.25V, V_{DVDD} = +2.7V to 5.25V, V_{AGNDS} = V_{AGND} = V_{DGND} = 0V, V_{REFIO} = internal reference, C_{RDC} = 4 x 33µF, C_{REFIO} = 0.1µF, C_{AVDD} = 4 x 0.1µF ‖ 10µF, C_{DVDD} = 3 x 0.1µF ‖ 10µF; all digital inputs at DVDD or DGND, unless otherwise noted. T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Signal-to-Noise and Distortion Ratio	SINAD	MAX11047/MAX11048/MAX11049, f_{IN} = 10kHz, full-scale input		90.5	92		dB
		MAX11057/MAX11058/MAX11059, f_{IN} = 10kHz, full-scale input		84.5	85.2		
Spurious-Free Dynamic Range	SFDR	f_{IN} = 10kHz, full-scale input	MAX11047/MAX11048/ MAX11049	98	108		dB
			MAX11057/MAX11058/ MAX11059	95	108		
Total Harmonic Distortion	THD	f_{IN} = 10kHz, full-scale input	MAX11047/MAX11048/ MAX11049		-108	-98	dB
			MAX11057/MAX11058/ MAX11059)		-108	-95	
Channel-to-Channel Crosstalk		f_{IN} = 60Hz, full scale and ground on adjacent channel (Note 2)			-126	-100	dB
ANALOG INPUTS (CH0–CH7)							
Input Voltage Range		(Note 3)		0		1.22 x V_{REFIO}	V
Input Leakage Current				-1		+1	µA
Input Capacitance					15		pF
Input-Clamp Protection Current		Each input simultaneously		-20		+20	mA
TRACK AND HOLD							
Throughput Rate		Per channel				250	ksps
Acquisition Time	t_{ACQ}			1			µs
Full-Power Bandwidth		-3dB point			4		MHz
		-0.1dB point			> 0.2		
Aperture Delay					10		ns
Aperture-Delay Matching					100		ps
Aperture Jitter					50		ps_{RMS}
INTERNAL REFERENCE							
REFIO Voltage	V_{REF}			4.080	4.096	4.112	V
REFIO Temperature Coefficient					±4		ppm/°C
EXTERNAL REFERENCE							
Input Current				-10		+10	µA
REF Voltage Input Range	V_{REF}			3.00		4.25	V
REF Input Capacitance					15		pF
DIGITAL INPUTS (CR0–CR3, $\overline{RD}$, $\overline{WR}$, $\overline{CS}$, CONVST)							
Input-Voltage High	V_{IH}	V_{DVDD} = 2.7V to 5.25V		2			V
Input-Voltage Low	V_{IL}	V_{DVDD} = 2.7V to 5.25V				0.8	V
Input Capacitance	C_{IN}				10		pF
Input Current	I_{IN}	V_{IN} = 0 or V_{DVDD}				±10	µA

4-/6-/8-Channel, 16-/14-Bit, Simultaneous-Sampling ADCs

ELECTRICAL CHARACTERISTICS (continued)

V_{AVDD} = 4.75V to 5.25V, V_{DVDD} = +2.7V to 5.25V, V_{AGNDS} = V_{AGND} = V_{DGND} = 0V, V_{REFIO} = internal reference, C_{RDC} = 4 x 33µF, C_{REFIO} = 0.1µF, C_{AVDD} = 4 x 0.1µF ‖ 10µF, C_{DVDD} = 3 x 0.1µF ‖ 10µF; all digital inputs at DVDD or DGND, unless otherwise noted. T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DIGITAL OUTPUTS (DB0–DB15, $\overline{EOC}$)							
Output-Voltage High	V_{OH}	I_{SOURCE} = 1.2mA		V_{DVDD} - 0.4			V
Output-Voltage Low	V_{OL}	I_{SINK} = 1mA				0.4	V
Three-State Leakage Current		DB0–DB15, $V_{RD} \geq V_{IH}$ or $V_{\overline{CS}} \geq V_{IH}$				10	µA
Three-State Output Capacitance		DB0–DB15, $V_{RD} \geq V_{IH}$ or $V_{\overline{CS}} \geq V_{IH}$			15		pF
POWER SUPPLIES (MAX11047/MAX11057)							
Analog Supply Voltage	AVDD			4.75		5.25	V
Digital Supply Voltage	DVDD			2.70		5.25	V
Analog Supply Current	I_{AVDD}					25	mA
Digital Supply Current	I_{DVDD}	V_{DVDD} = 3.3V (Note 4)				5.5	mA
Shutdown Current		For DVDD				10	µA
Shutdown Current		For AVDD				10	µA
Power-Supply Rejection	PSR	V_{AVDD} = 4.9V to 5.1V (Note 5)	MAX11047		±1.2		LSB
			MAX11057		±0.3		
POWER SUPPLIES (MAX11048/MAX11058)							
Analog Supply Voltage	AVDD			4.75		5.25	V
Digital Supply Voltage	DVDD			2.70		5.25	V
Analog Supply Current	I_{AVDD}					32	mA
Digital Supply Current	I_{DVDD}	V_{DVDD} = 3.3V (Note 4)				6.5	mA
Shutdown Current		For DVDD				10	µA
Shutdown Current		For AVDD				10	µA
Power-Supply Rejection	PSR	V_{AVDD} = 4.9V to 5.1V (Note 5)	MAX11048		±1.2		LSB
			MAX11058		±0.3		
POWER SUPPLIES (MAX11049/MAX11059)							
Analog Supply Voltage	AVDD			4.75		5.25	V
Digital Supply Voltage	DVDD			2.70		5.25	V
Analog Supply Current	I_{AVDD}					39	mA
Digital Supply Current	I_{DVDD}	V_{DVDD} = 3.3V (Note 4)				7	mA
Shutdown Current		For DVDD				10	µA
Shutdown Current		For AVDD				10	µA
Power-Supply Rejection	PSR	V_{AVDD} = 4.9V to 5.1V (Note 5)	MAX11049		±1.2		LSB
			MAX11059		±0.3		
TIMING CHARACTERISTICS (Note 4)							
CONVST Rise to $\overline{EOC}$ Fall	t_{CON}	Conversion time (Note 6)				3	µs
Acquisition Time	t_{ACQ}			1			µs
$\overline{CS}$ Rise to CONVST Rise	t_Q	Sample quiet time (Note 6)		500			ns

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ELECTRICAL CHARACTERISTICS (continued)

V_{AVDD} = 4.75V to 5.25V, V_{DVDD} = +2.7V to 5.25V, V_{AGNDS} = V_{AGND} = V_{DGND} = 0V, V_{REFIO} = internal reference, C_{RDC} = 4 x 33µF, C_{REFIO} = 0.1µF, C_{AVDD} = 4 x 0.1µF ‖ 10µF, C_{DVDD} = 3 x 0.1µF ‖ 10µF; all digital inputs at DVDD or DGND, unless otherwise noted. T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CONVST Rise to $\overline{EOC}$ Rise	t_0			65	140	ns
$\overline{EOC}$ Fall to CONVST Fall	t_1	CONVST mode B0 = 0 only (Note 7)	0			ns
CONVST Low Time	t_2	CONVST mode B0 = 1 only	20			ns
$\overline{CS}$ Fall to $\overline{WR}$ Fall	t_3		0			ns
$\overline{WR}$ Low Time	t_4		20			ns
$\overline{CS}$ Rise to $\overline{WR}$ Rise	t_5		0			ns
Input Data Setup Time	t_6		10			ns
Input Data Hold Time	t_7		0			ns
$\overline{CS}$ Fall to $\overline{RD}$ Fall	t_8		0			ns
$\overline{RD}$ Low Time	t_9		30			ns
$\overline{RD}$ Rise to $\overline{CS}$ Rise	t_{10}		0			ns
$\overline{RD}$ High Time	t_{11}		10			ns
$\overline{RD}$ Fall to Data Valid	t_{12}				35	ns
$\overline{RD}$ Rise to Data Hold Time	t_{13}	(Note 7)	5			ns

Note 1: See the *Definitions* section at the end of the data sheet.
Note 2: Tested with alternating channels modulated at full scale and ground.
Note 3: See the *Input Range and Protection* section.
Note 4: C_{LOAD}= 30pF on DB0–DB15 and $\overline{EOC}$. Inputs (CH0–CH7) alternate between full scale and zero scale. f_{CONV} = 250ksps. All data is read out.
Note 5: Defined as the change in positive full scale caused by a ±2% variation in the nominal supply voltage.
Note 6: It is recommended that $\overline{RD}$, $\overline{WR}$, and $\overline{CS}$ are kept high for the quiet time (t_Q) and conversion time (t_{CON}).
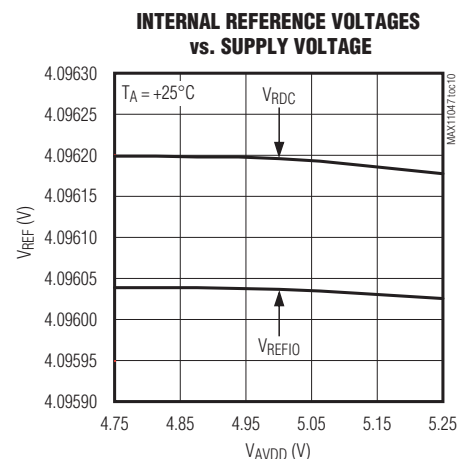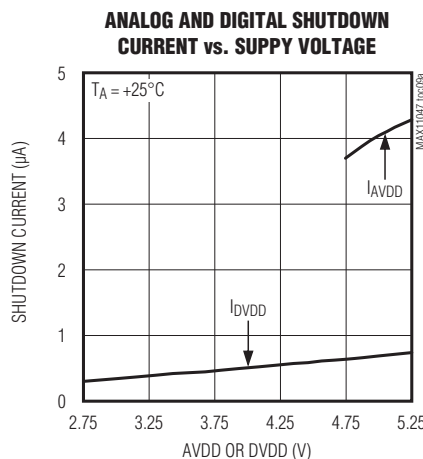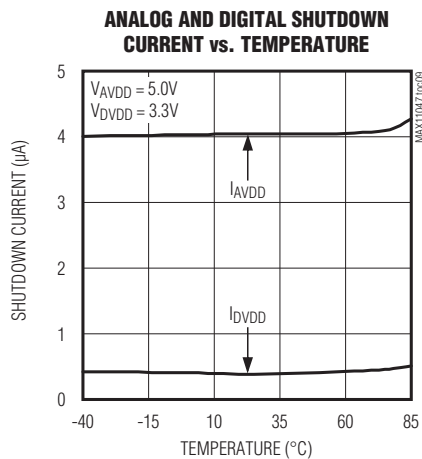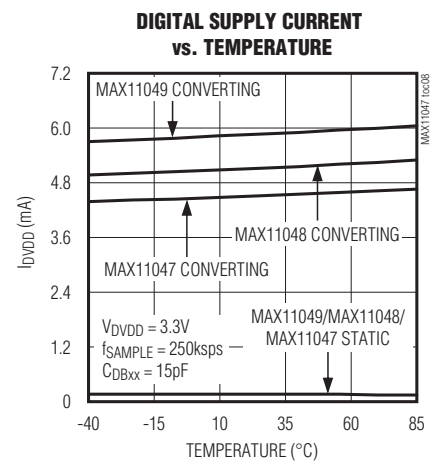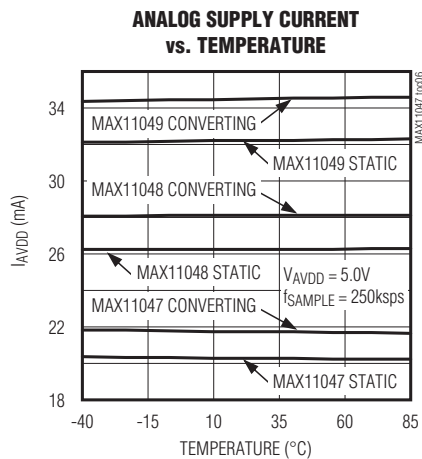**Note 7:** Guaranteed by design.

_____*Typical Operating Characteristics*
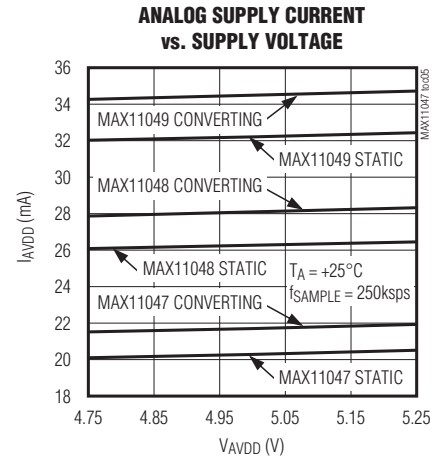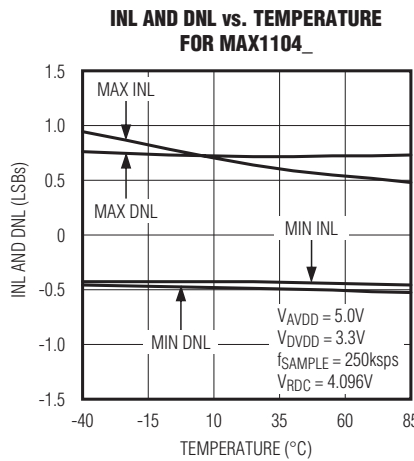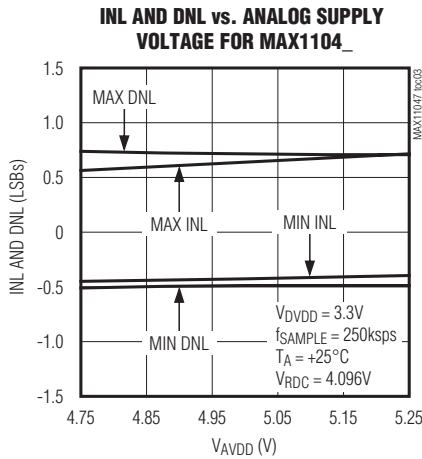
(V_{AVDD} = 5V, V_{DVDD} = 3.3V, T_A = +25°C, f_{SAMPLE} = 250ksps, internal reference, unless otherwise noted.)

INTEGRAL NONLINEARITY (INL) vs. CODE FOR MAX1104_

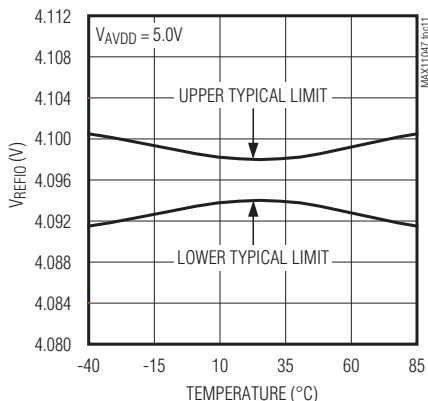DIFFERENTIAL NONLINEARITY (DNL) vs. CODE FOR MAX1104_
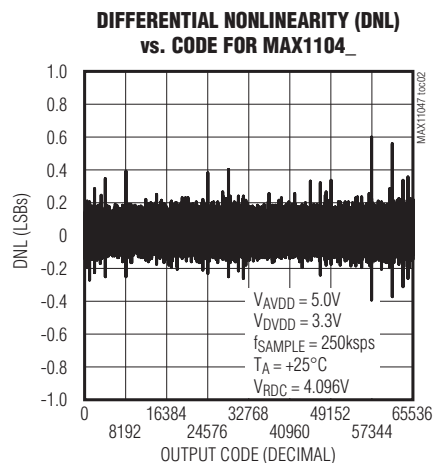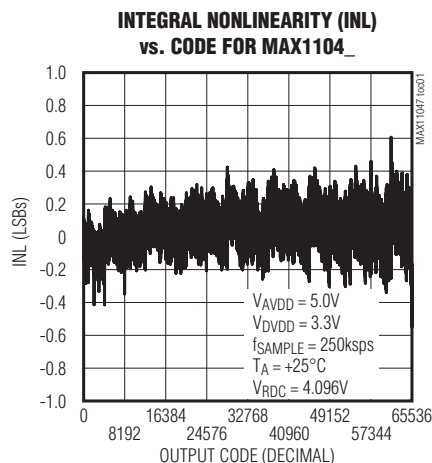
4-/6-/8-Channel, 16-/14-Bit, Simultaneous-Sampling ADCs

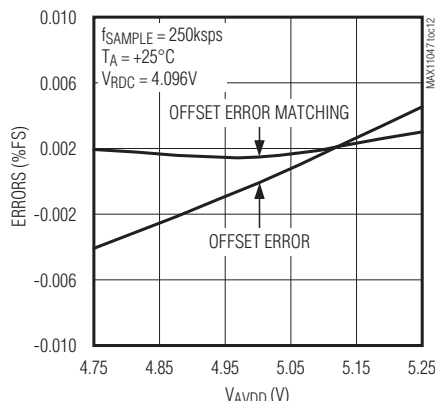## Typical Operating Characteristics (continued)

(V_{AVDD} = 5V, V_{DVDD} = 3.3V, T_A = +25°C, f_{SAMPLE} = 250ksps, internal reference, unless otherwise noted.)

INL AND DNL vs. ANALOG SUPPLY VOLTAGE FOR MAX1104_

MAX DNL
MAX INL   MIN INL
MIN DNL
V_{DVDD} = 3.3V
f_{SAMPLE} = 250ksps
T_A = +25°C
V_{RDC} = 4.096V

INL AND DNL (LSBs) vs. V_{AVDD} (V)

INL AND DNL vs. TEMPERATURE FOR MAX1104_

MAX INL
MAX DNL   MIN INL
MIN DNL
V_{AVDD} = 5.0V
V_{DVDD} = 3.3V
f_{SAMPLE} = 250ksps
V_{RDC} = 4.096V

INL AND DNL (LSBs) vs. TEMPERATURE (°C)

ANALOG SUPPLY CURRENT vs. SUPPLY VOLTAGE

MAX11049 CONVERTING
MAX11049 STATIC
MAX11048 CONVERTING
MAX11048 STATIC T_A = +25°C
f_{SAMPLE} = 250ksps
MAX11047 CONVERTING
MAX11047 STATIC

I_{AVDD} (mA) vs. V_{AVDD} (V)

ANALOG SUPPLY CURRENT vs. TEMPERATURE

MAX11049 CONVERTING
MAX11049 STATIC
MAX11048 CONVERTING
MAX11048 STATIC
MAX11047 CONVERTING
V_{AVDD} = 5.0V
f_{SAMPLE} = 250ksps
MAX11047 STATIC

I_{AVDD} (mA) vs. TEMPERATURE (°C)

DIGITAL SUPPLY CURRENT vs. SUPPLY VOLTAGE

T_A = +25°C
f_{SAMPLE} = 250ksps
C_{DBxx} = 15pF
MAX11049 CONVERTING
MAX11048 CONVERTING
MAX11049/MAX11048/
MAX11047 STATIC
MAX11047 CONVERTING

I_{DVDD} (mA) vs. V_{DVDD} (V)

DIGITAL SUPPLY CURRENT vs. TEMPERATURE

MAX11049 CONVERTING
MAX11048 CONVERTING
MAX11047 CONVERTING
MAX11049/MAX11048/
MAX11047 STATIC
V_{DVDD} = 3.3V
f_{SAMPLE} = 250ksps
C_{DBxx} = 15pF

I_{DVDD} (mA) vs. TEMPERATURE (°C)

ANALOG AND DIGITAL SHUTDOWN CURRENT vs. TEMPERATURE

V_{AVDD} = 5.0V
V_{DVDD} = 3.3V
I_{AVDD}
I_{DVDD}

SHUTDOWN CURRENT (μA) vs. TEMPERATURE (°C)

ANALOG AND DIGITAL SHUTDOWN CURRENT vs. SUPPY VOLTAGE

T_A = +25°C
I_{AVDD}
I_{DVDD}

SHUTDOWN CURRENT (μA) vs. AVDD OR DVDD (V)

INTERNAL REFERENCE VOLTAGES vs. SUPPLY VOLTAGE

T_A = +25°C V_{RDC}
V_{REFIO}

V_{REF} (V) vs. V_{AVDD} (V)

MAXIM

Typical Operating Characteristics (continued)

(V$_{AVDD}$ = 5V, V$_{DVDD}$ = 3.3V, T$_A$ = +25°C, f$_{SAMPLE}$ = 250ksps, internal reference, unless otherwise noted.)
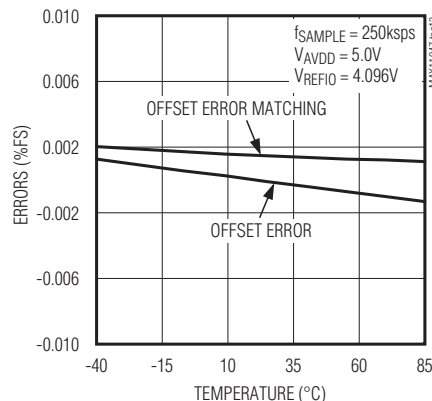
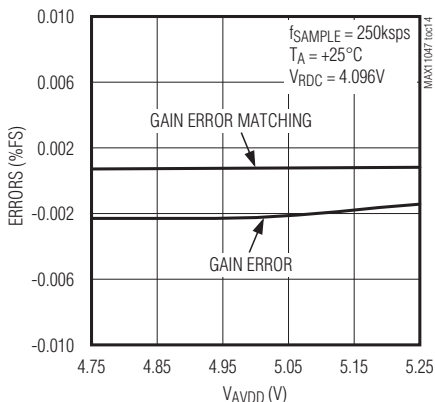**INTERNAL REFERENCE VOLTAGES vs. TEMPERATURE**

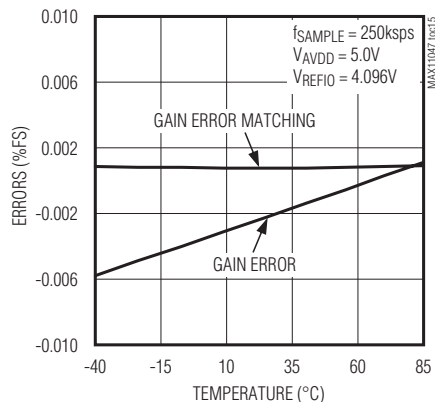**OFFSET ERROR AND OFFSET ERROR MATCHING vs. SUPPLY VOLTAGE**

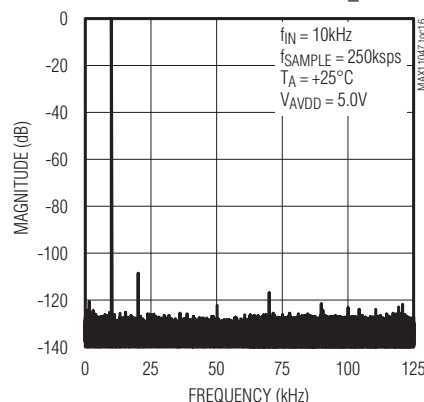**OFFSET ERROR AND OFFSET ERROR MATCHING vs. TEMPERATURE**

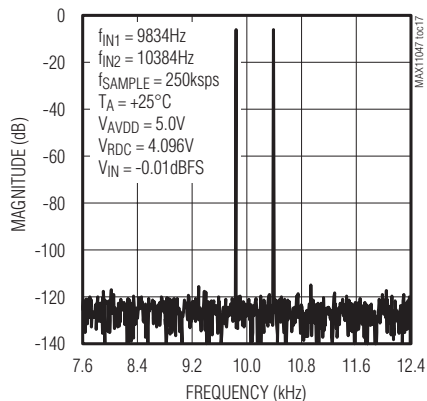**GAIN ERROR AND GAIN ERROR MATCHING vs. SUPPLY VOLTAGE**
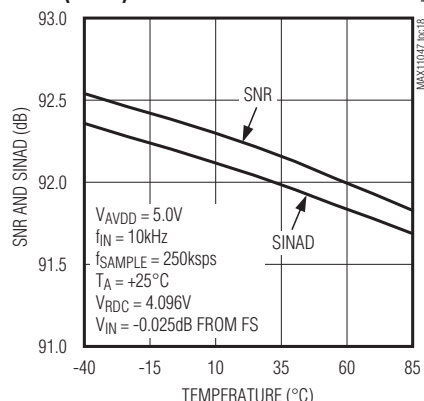
GAIN ERROR AND GAIN ERROR MATCHING vs. TEMPERATURE

FFT PLOT FOR MAX1104_

TWO-TONE IMD PLOT FOR MAX1104_

SIGNAL-TO-NOISE RATIO (SNR) AND SIGNAL-TO-NOISE AND DISTORTION RATIO (SINAD) vs. TEMPERATURE FOR MAX1104_

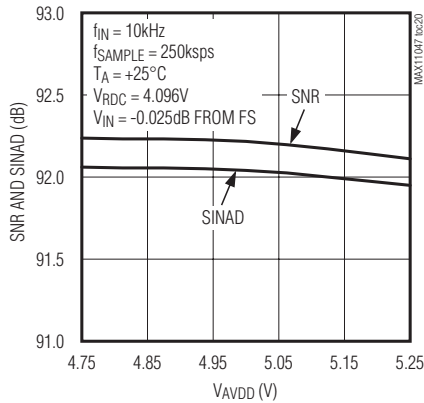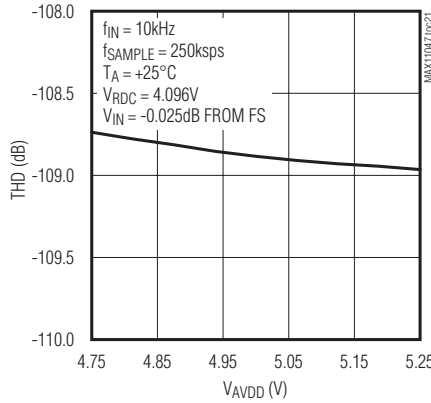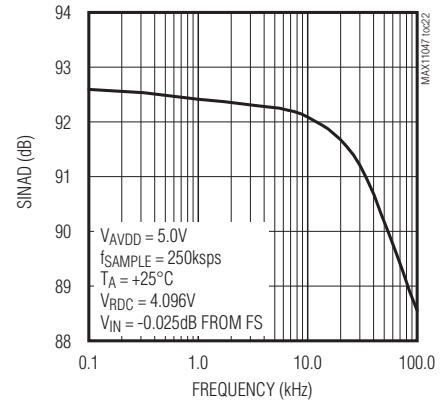**TOTAL HARMONIC DISTORTION (THD) vs. TEMPERATURE FOR MAX1104_**
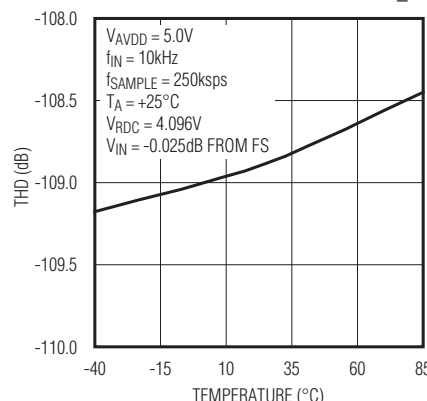
MAX11047–MAX11049/MAX11057–MAX11059

Typical Operating Characteristics (continued)

(V_{AVDD} = 5V, V_{DVDD} = 3.3V, T_A = +25°C, f_{SAMPLE} = 250ksps, internal reference, unless otherwise noted.)
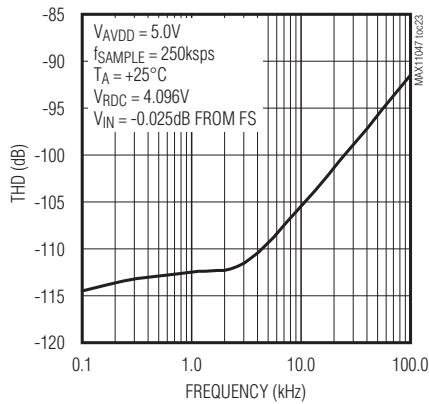
SNR AND SINAD vs. ANALOG SUPPLY VOLTAGE FOR MAX1104_

f_{IN} = 10kHz
f_{SAMPLE} = 250ksps
T_A = +25°C
V_{RDC} = 4.096V
V_{IN} = -0.025dB FROM FS

THD vs. ANALOG SUPPLY VOLTAGE FOR MAX1104_

f_{IN} = 10kHz
f_{SAMPLE} = 250ksps
T_A = +25°C
V_{RDC} = 4.096V
V_{IN} = -0.025dB FROM FS

SIGNAL-TO-NOISE AND DISTORTION RATIO (SINAD) vs. FREQUENCY FOR MAX1104_

V_{AVDD} = 5.0V
f_{SAMPLE} = 250ksps
T_A = +25°C
V_{RDC} = 4.096V
V_{IN} = -0.025dB FROM FS

THD vs. INPUT FREQUENCY FOR MAX1104_

V_{AVDD} = 5.0V
f_{SAMPLE} = 250ksps
T_A = +25°C
V_{RDC} = 4.096V
V_{IN} = -0.025dB FROM FS

CROSSTALK vs. FREQUENCY

f_{IN} = 60Hz
f_{SAMPLE} = 250ksps
T_A = +25°C
V_{AVDD} = 5.0V
V_{RDC} = 4.096V
V_{IN} = -0.025dB FROM FS
INACTIVE CHANNEL AT GND
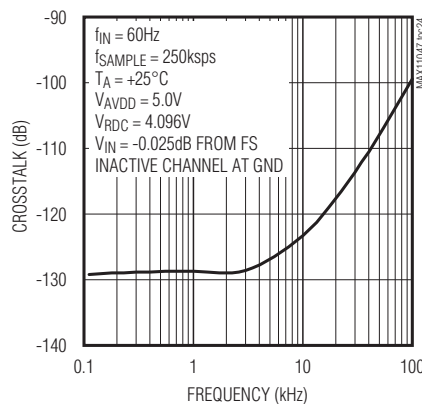
OUTPUT NOISE HISTOGRAM WITH INPUT CONNECTED TO 2.5V FOR MAX1104_

V_{CHX} = 2.500270V
V_{AVDD} = 5.0V
f_{SAMPLE} = 250ksps
T_A = +25°C
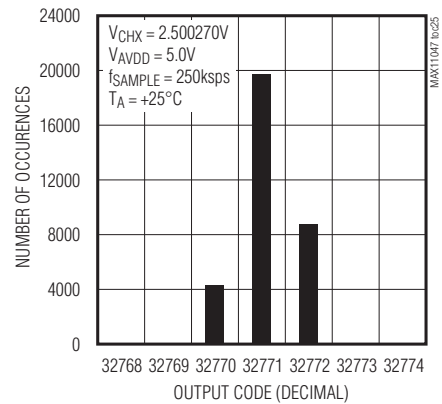
CONVERSION TIME vs. ANALOG SUPPLY VOLTAGE

T_A = +25°C
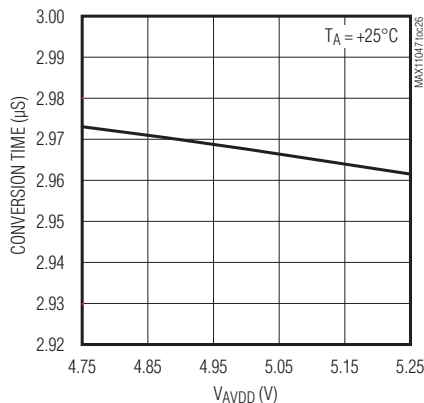
CONVERSION TIME vs. TEMPERATURE

V_{AVDD} = 5.0V

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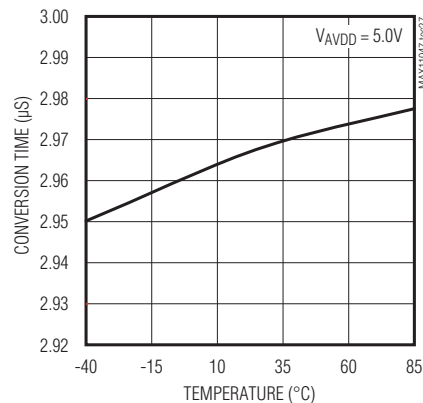
Pin Configurations

MAX11047–MAX11049/MAX11057–MAX11059

TOP VIEW

MAX11047 / MAX11048 / MAX11049

Top pins (left to right): CH6*/CH7†/I.C.‡ (42), AVDD (41), AGND (40), CH5*/CH4†/CH3‡ (39), AGNDS (38), CH4*/CH3†/CH2‡ (37), REFIO (36), RDC (35), CH3*/CH2†/CH1‡ (34), AGNDS (33), CH2*/CH1†/CH0‡ (32), AGND (31), AVDD (30), CH1*/CH0†/I.C.‡ (29)

Left side:
RDC	43
AGNDS	44
I.C.†‡/CH7*	45
AGND	46
AVDD	47
AGNDS	48
RDC	49
DGND	50
DVDD	51
W̄R̄	52
C̄S̄	53
R̄D̄	54
DB15	55
DB14	56

Right side:
28	RDC
27	AGNDS
26	CH0*/I.C.†‡
25	AGND
24	AVDD
23	AGNDS
22	RDC
21	DGND
20	DVDD
19	SHDN
18	CONVST
17	ĒŌC̄
16	DB0/CR0
15	DB1/CR1

Bottom pins: DB13 (1), DB12 (2), DB11 (3), DB10 (4), DB9 (5), DB8 (6), DGND (7), DVDD (8), DB7 (9), DB6 (10), DB5 (11), DB4 (12), DB3/CR3 (13), DB2/CR2 (14)

*EP

TQFN
8mm x 8mm

‡MAX11047
†MAX11048
*MAX11049

MAX11047 / MAX11048 / MAX11049

Top pins: RDC (48), CH6*/CH5†/I.C.‡ (47), AVDD (46), AGND (45), CH5*/CH4†/CH3‡ (44), AGNDS (43), CH4*/CH3†/CH2‡ (42), REFIO (41), RDC (40), CH3*/CH2†/CH1‡ (39), AGNDS (38), CH2*/CH1†/CH0‡ (37), AGND (36), AVDD (35), CH1*/CH0†/I.C.‡ (34), RDC (33)

Left side:
AGNDS	49
I.C.†‡/CH7*	50
AGND	51
AVDD	52
AGNDS	53
RDC	54
RDC_SENSE	55
AGND	56
AVDD	57
AGNDS	58
DGND	59
DVDD	60
W̄R̄	61
C̄S̄	62
R̄D̄	63
DB15	64

Right side:
32	AGNDS
31	CH0*/I.C.†‡
30	AGND
29	AVDD
28	AGNDS
27	RDC
26	RDC_SENSE
25	AGND
24	AVDD
23	AGNDS
22	DGND
21	DVDD
20	SHDN
19	CONVST
18	ĒŌC̄
17	DB0/CR0

Bottom pins: DB14 (1), DB13 (2), DB12 (3), DB11 (4), DB10 (5), DB9 (6), DB8 (7), DGND (8), DVDD (9), DB7 (10), DB6 (11), DB5 (12), DB4 (13), DB3/CR3 (14), DB2/CR2 (15), DB1/CR1 (16)

*EP

TQFP
10mm x 10mm

MAX11057 / MAX11058 / MAX11059

Top pins: RDC (48), CH6*/CH5†/I.C.‡ (47), AVDD (46), AGND (45), CH5*/CH4†/CH3‡ (44), AGNDS (43), CH4*/CH3†/CH2‡ (42), REFIO (41), RDC (40), CH3*/CH2†/CH1‡ (39), AGNDS (38), CH2*/CH1†/CH0‡ (37), AGND (36), AVDD (35), CH1*/CH0†/I.C.‡ (34), RDC (33)

Left side:
AGNDS	49
I.C.†‡/CH7*	50
AGND	51
AVDD	52
AGNDS	53
RDC	54
RDC_SENSE	55
AGND	56
AVDD	57
AGNDS	58
DGND	59
DVDD	60
W̄R̄	61
C̄S̄	62
R̄D̄	63
DB13	64

Right side:
32	AGNDS
31	CH0*/I.C.†‡
30	AGND
29	AVDD
28	AGNDS
27	RDC
26	RDC_SENSE
25	AGND
24	AVDD
23	AGNDS
22	DGND
21	DVDD
20	SHDN
19	CONVST
18	ĒŌC̄
17	CR0

Bottom pins: DB12 (1), DB11 (2), DB10 (3), DB9 (4), DB8 (5), DB7 (6), DB6 (7), DGND (8), DVDD (9), DB5 (10), DB4 (11), DB3 (12), DB2 (13), DB1/CR3 (14), DB0/CR2 (15), CR1 (16)

*EP

‡MAX11057
†MAX11058
*MAX11059

TQFP
10mm x 10mm

_____*Pin Description*

PIN			NAME	FUNCTION
MAX11047 (TQFN-EP)	MAX11048 (TQFN-EP)	MAX11049 (TQFN-EP)		
1	1	1	DB13	16-Bit Parallel Data Bus Digital Output Bit 13
2	2	2	DB12	16-Bit Parallel Data Bus Digital Output Bit 12
3	3	3	DB11	16-Bit Parallel Data Bus Digital Output Bit 11
4	4	4	DB10	16-Bit Parallel Data Bus Digital Output Bit 10
5	5	5	DB9	16-Bit Parallel Data Bus Digital Output Bit 9
6	6	6	DB8	16-Bit Parallel Data Bus Digital Output Bit 8
7, 21, 50	7, 21, 50	7, 21, 50	DGND	Digital Ground
8, 20, 51	8, 20, 51	8, 20, 51	DVDD	Digital Supply. Bypass to DGND with a 0.1µF capacitor at each DV$_{DD}$ input.
9	9	9	DB7	16-Bit Parallel Data Bus Digital Output Bit 7
10	10	10	DB6	16-Bit Parallel Data Bus Digital Output Bit 6
11	11	11	DB5	16-Bit Parallel Data Bus Digital Output Bit 5
12	12	12	DB4	16-Bit Parallel Data Bus Digital Output Bit 4
13	13	13	DB3/CR3	16-Bit Parallel Data Bus Digital Output Bit 3/Configuration Register Input Bit 3
14	14	14	DB2/CR2	16-Bit Parallel Data Bus Digital Output Bit 2/Configuration Register Input Bit 2
15	15	15	DB1/CR1	16-Bit Parallel Data Bus Digital Output Bit 1/Configuration Register Input Bit 1
16	16	16	DB0/CR0	16-Bit Parallel Data Bus Digital Output Bit 0/Configuration Register Input Bit 0
17	17	17	$\overline{EOC}$	Active-Low End of Conversion Output. $\overline{EOC}$ goes low when conversion is completed. $\overline{EOC}$ goes high when a conversion is initiated.
18	18	18	CONVST	Convert Start Input. Rising edge of CONVST ends sample and starts a conversion on the captured sample. The ADC is in acquisition mode when CONVST is low and CONVST mode = 0.
19	19	19	SHDN	Shutdown Input. If SHDN is held high, the entire device enters and stays in a low-current state. Contents of the Configuration register are not lost when in the shutdown state.
22, 28, 35, 43, 49	22, 28, 35, 43, 49	22, 28, 35, 43, 49	RDC	Reference Buffer Decoupling. Connect all RDC outputs together. Bypass to AGND with at least an 80µF total capacitance. See the *Layout, Grounding, and Bypassing* section.
23, 27, 33, 38, 44, 48	23, 27, 33, 38, 44, 48	23, 27, 33, 38, 44, 48	AGNDS	Signal Ground. Connect all AGND and AGNDS inputs together on PWB.
24, 30, 41, 47	24, 30, 41, 47	24, 30, 41, 47	AVDD	Analog Supply Input. Bypass AV$_{DD}$ to AGND with a 0.1µF capacitor at each AV$_{DD}$ input.
25, 31, 40, 46	25, 31, 40, 46	25, 31, 40, 46	AGND	Analog Ground. Connect all AGND inputs together.
26, 29, 42, 45	26, 45	—	I.C.	Internally Connected. Connect to AGND
32	29	26	CH0	Channel 0 Analog Input
34	32	29	CH1	Channel 1 Analog Input
36	36	36	REFIO	External Reference Input/Internal Reference Output. Place a 0.1µF capacitor from REFIO to AGND.

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MAX11047–MAX11049/MAX11057–MAX11059

Pin Description (continued)

PIN			NAME	FUNCTION
MAX11047 (TQFN-EP)	MAX11048 (TQFN-EP)	MAX11049 (TQFN-EP)		
37	34	32	CH2	Channel 2 Analog Input
39	37	34	CH3	Channel 3 Analog Input
—	39	37	CH4	Channel 4 Analog Input
—	42	39	CH5	Channel 5 Analog Input
—	—	42	CH6	Channel 6 Analog Input
—	—	45	CH7	Channel 7 Analog Input
52	52	52	$\overline{WR}$	Active-Low Write Input. Drive $\overline{WR}$ low to write to the ADC. Configuration registers are loaded on the rising edge of $\overline{WR}$.
53	53	53	$\overline{CS}$	Active Low-Chip Select Input. Drive $\overline{CS}$ low when reading from or writing to the ADC.
54	54	54	$\overline{RD}$	Active-Low Read Input. Drive $\overline{RD}$ low to read from the ADC. Each rising edge of $\overline{RD}$ advances the channel output on the data bus.
55	55	55	DB15	16-Bit Parallel Data Bus Digital Output Bit 15
56	56	56	DB14	16-Bit Parallel Data Bus Digital Output Bit 14
—	—	—	EP	Exposed Pad. Internally connected to AGND. Connect to a large ground plane to maximize thermal performance. Not intended as an electrical connection point.

PIN			NAME	FUNCTION
MAX11047 (TQFP-EP)	MAX11048 (TQFP-EP)	MAX11049 (TQFP-EP)		
1	1	1	DB14	16-Bit Parallel Data Bus Digital Output Bit 14
2	2	2	DB13	16-Bit Parallel Data Bus Digital Output Bit 13
3	3	3	DB12	16-Bit Parallel Data Bus Digital Output Bit 12
4	4	4	DB11	16-Bit Parallel Data Bus Digital Output Bit 11
5	5	5	DB10	16-Bit Parallel Data Bus Digital Output Bit 10
6	6	6	DB9	16-Bit Parallel Data Bus Digital Output Bit 9
7	7	7	DB8	16-Bit Parallel Data Bus Digital Output Bit 8
8, 22, 59	8, 22, 59	8, 22, 59	DGND	Digital Ground
9, 21, 60	9, 21, 60	9, 21, 60	DV_{DD}	Digital Supply. Bypass to DGND with a 0.µF capacitor at each DVDD input.
10	10	10	DB7	16-Bit Parallel Data Bus Digital Output Bit 7
11	11	11	DB6	16-Bit Parallel Data Bus Digital Output Bit 6
12	12	12	DB5	16-Bit Parallel Data Bus Digital Output Bit 5
13	13	13	DB4	16-Bit Parallel Data Bus Digital Output Bit 4
14	14	14	DB3/CR3	16-Bit Parallel Data Bus Digital Output Bit 3/Configuration Register Input Bit 3
15	15	15	DB2/CR2	16-Bit Parallel Data Bus Digital Output Bit 2/Configuration Register Input Bit 2
16	16	16	DB1/CR1	16-Bit Parallel Data Bus Digital Output Bit 1/Configuration Register Input Bit 1
17	17	17	DB0/CR0	16-Bit Parallel Data Bus Digital Output Bit 0/Configuration Register Input Bit 0

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MAX11047–MAX11049/MAX11057–MAX11059

PIN			NAME	FUNCTION
MAX11047 (TQFP-EP)	MAX11048 (TQFP-EP)	MAX11049 (TQFP-EP)		
18	18	18	$\overline{\text{EOC}}$	Active-Low, End-of-Conversion Output. EOC goes low when a conversion is completed. EOC goes high when a conversion is initiated.
19	19	19	CONVST	Convert Start Input. The rising edge of CONVST ends sample and starts a conversion on the captured sample. The ADC is in acquisition mode when CONVST is low and CONVST mode = 0.
20	20	20	SHDN	Shutdown Input. If SHDN is held high, the entire device enters and stays in a low-current state. Contents of the Configuration register are not lost when in the shutdown state.
23, 28, 32, 38, 43, 49, 53, 58	23, 28, 32, 38, 43, 49, 53, 58	23, 28, 32, 38, 43, 49, 53, 58	AGNDS	Signal Ground. Connect all AGND and AGNDS inputs together.
24, 29, 35, 46, 52, 57	24, 29, 35, 46, 52, 57	24, 29, 35, 46, 52, 57	AV$_{DD}$	Analog Supply Input. Bypass AVDD to AGND with a 0.1µF capacitor at each AVDD input.
25, 30, 36, 45, 51, 56	25, 30, 36, 45, 51, 56	25, 30, 36, 45, 51, 56	AGND	Analog Ground. Connect all AGND inputs together.
26, 55	26, 55	26, 55	RDC_SENSE	Reference Buffer Sense Feedback. Connect to RDC plane.
27, 33, 40, 48, 54	27, 33, 40, 48, 54	27, 33, 40, 48, 54	RDC	Reference Buffer Decoupling. Connect all RDC outputs together. Bypass to AGND with at least an 80µF total capacitance. See the *Layout, Grounding, and Bypassing* section.
31, 34, 47, 50	31, 50	—	I.C.	Internally Connected. Connect to AGND.
37	34	31	CH0	Channel 0 Analog Input
39	37	34	CH1	Channel 1 Analog Input
41	41	41	REFIO	External Reference Input/Internal Reference Output. Place a 0.1µF capacitor from REFIO to AGND.
42	39	37	CH2	Channel 2 Analog Input
44	42	39	CH3	Channel 3 Analog Input
—	44	42	CH4	Channel 4 Analog Input
—	47	44	CH5	Channel 5 Analog Input
—	—	47	CH6	Channel 6 Analog Input
—	—	50	CH7	Channel 7 Analog Input
61	61	61	$\overline{\text{WR}}$	Active-Low Write Input. Drive WR low to write to the ADC. Configuration registers are loaded on the rising edge of WR.
62	62	62	$\overline{\text{CS}}$	Active-Low Chip-Select Input. Drive CS low when reading from or writing to the ADC.
63	63	63	$\overline{\text{RD}}$	Active-Low Read Input. Drive RD low to read from the ADC. Each rising edge of RD advances the channel output on the data bus.
64	64	64	DB15	16-Bit Parallel Data Bus Digital Out Bit 15
—	—	—	EP	Exposed Pad. Internally connected to AGND. Connect to a large ground plane to maximize thermal performance. Not intended as an electrical connection point.

MAXIM

Pin Description (continued)

PIN			NAME	FUNCTION
MAX11057 (TQFP-EP)	MAX11058 (TQFP-EP)	MAX11059 (TQFP-EP)		
1	1	1	DB12	14-Bit Parallel Data Bus Digital Output Bit 12
2	2	2	DB11	14-Bit Parallel Data Bus Digital Output Bit 11
3	3	3	DB10	14-Bit Parallel Data Bus Digital Output Bit 10
4	4	4	DB9	14-Bit Parallel Data Bus Digital Output Bit 9
5	5	5	DB8	14-Bit Parallel Data Bus Digital Output Bit 8
6	6	6	DB7	14-Bit Parallel Data Bus Digital Output Bit 7
7	7	7	DB6	14-Bit Parallel Data Bus Digital Output Bit 6
8, 22, 59	8, 22, 59	8, 22, 59	DGND	Digital Ground
9, 21, 60	9, 21, 60	9, 21, 60	DV$_{DD}$	Digital Supply. Bypass to DGND with a 0.1µF capacitor at each DVDD input.
10	10	10	DB5	14-Bit Parallel Data Bus Digital Output Bit 5
11	11	11	DB4	14-Bit Parallel Data Bus Digital Output Bit 4
12	12	12	DB3	14-Bit Parallel Data Bus Digital Output Bit 3
13	13	13	DB2	14-Bit Parallel Data Bus Digital Output Bit 2
14	14	14	DB1/CR3	14-Bit Parallel Data Bus Digital Output Bit 1/Configuration Register Input Bit 3
15	15	15	DB0/CR2	14-Bit Parallel Data Bus Digital Output Bit 0/Configuration Register Input Bit 2
16	16	16	CR1	Configuration Register Input Bit 1
17	17	17	CR0	Configuration Register Input Bit 0
18	18	18	$\overline{EOC}$	Active-Low, End-of-Conversion Output. EOC goes low when a conversion is completed. EOC goes high when a conversion is initiated.
19	19	19	CONVST	Convert Start Input. The rising edge of CONVST ends sample and starts a conversion on the captured sample. The ADC is in acquisition mode when CONVST is low and CONVST mode = 0.
20	20	20	SHDN	Shutdown Input. If SHDN is held high, the entire device enters and stays in a low-current state. Contents of the Configuration register are not lost when in the shutdown state.
23, 28, 32, 38, 43, 49, 53, 58	23, 28, 32, 38, 43, 49, 53, 58	23, 28, 32, 38, 43, 49, 53, 58	AGNDS	Signal Ground. Connect all AGND and AGNDS inputs together.
24, 29, 35, 46, 52, 57	24, 29, 35, 46, 52, 57	24, 29, 35, 46, 52, 57	AV$_{DD}$	Analog Supply Input. Bypass AVDD to AGND with a 0.1µF capacitor at each AVDD input.
25, 30, 36, 45, 51, 56	25, 30, 36, 45, 51, 56	25, 30, 36, 45, 51, 56	AGND	Analog Ground. Connect all AGND inputs together.
26, 55	26, 55	26, 55	RDC_SENSE	Reference Buffer Sense Feedback. Connect to RDC plane.
27, 33, 40,48, 54	27, 33, 40,48, 54	27, 33, 40,48, 54	RDC	Reference Buffer Decoupling. Connect all RDC outputs together. Bypass to AGND with at least an 80µF total capacitance. See the *Layout, Grounding, and Bypassing* section.
31, 34, 47, 50	31, 50	—	I.C.	Internally Connected. Connect to AGND.
37	34	31	CH0	Channel 0 Analog Input
39	37	34	CH1	Channel 1 Analog Input

_____**Pin Description (continued)**

PIN			NAME	FUNCTION
MAX11057 (TQFP-EP)	MAX11058 (TQFP-EP)	MAX11059 (TQFP-EP)		
41	41	41	REFIO	External Reference Input/Internal Reference Output. Place a 0.1µF capacitor from REFIO to AGND.
42	39	37	CH2	Channel 2 Analog Input
44	42	39	CH3	Channel 3 Analog Input
—	44	42	CH4	Channel 4 Analog Input
—	47	44	CH5	Channel 5 Analog Input
—	—	47	CH6	Channel 6 Analog Input
—	—	50	CH7	Channel 7 Analog Input
61	61	61	$\overline{WR}$	Active-Low Write Input. Drive WR low to write to the ADC. Configuration registers are loaded on the rising edge of WR.
62	62	62	$\overline{CS}$	Active-Low Chip-Select Input. Drive CS low when reading from or writing to the ADC.
63	63	63	$\overline{RD}$	Active-Low Read Input. Drive RD low to read from the ADC. Each rising edge of RD advances the channel output on the data bus.
64	64	64	DB13	14-Bit Parallel Data Bus Digital Out Bit 13
—	—	—	EP	Exposed Pad. Internally connected to AGND. Connect to a large ground plane to maximize thermal performance. Not intended as an electrical connection point.

_____**Detailed Description**

The MAX11047/MAX11048/MAX11049 and MAX11057/MAX11058/MAX11059 are fast, low-power ADCs that combine 4, 6, or 8 independent ADC channels in a single IC. Each channel includes simultaneously sampling independent T/H circuitry that preserves relative phase information between inputs making the devices ideal for motor control and power monitoring. The devices are available with a 0 to 5V input range that features ±20mA overrange, fault-tolerant inputs. The devices operate with a single 4.75V to 5.25V supply. A separate 2.7V to 5.25V supply for digital circuitry makes the devices compatible with low-voltage processors.

The devices perform conversions for all channels in parallel by activating independent ADCs. Results are available through a high-speed, 20MHz, parallel data bus after a conversion time of 3µs following the end of a sample. The data bus is bidirectional and allows for easy programming of the configuration register. The devices feature a reference buffer, which is driven by an internal bandgap reference circuit (V_{REFIO} = 4.096V). Drive REFIO with an external reference or bypass with a 0.1µF capacitor to ground when using the internal reference.

Analog Inputs

Track and Hold (T/H)

To preserve phase information across all channels, each input includes a dedicated T/H circuitry. The input tracking circuitry provides a 4MHz small-signal bandwidth, enabling the device to digitize high-speed transient events and measure periodic signals with bandwidths exceeding the ADC's sampling rate by using undersampling techniques. Use anti-alias filtering to avoid high-frequency signals being aliased into the frequency band of interest.

MAXIM

Input Range and Protection

The full-scale analog input voltage is a product of the reference voltage. For the devices, the input is unipolar in the range of:

$$0 \text{ to } +V_{REFIO} \times \frac{5.0}{4.096}$$

In external reference mode, drive V_{REFIO} with a 3.0V to 4.25V source, resulting in a full-scale input range of 3.662V to 5.188V, respectively.

All analog inputs are fault-protected up to ±20mA. The devices include an input clamping circuit that activates when the input voltage at the analog input is above (V_{AVDD} + 300mV) or below -300mV. The clamp circuit remains high impedance while the input signal is within the range of 0V to +V_{AVDD} and draws little to no current. However, when the input signal exceeds the range of 0V to +V_{AVDD}, the clamps begin to turn on. Consequently, to obtain the highest accuracy, ensure that the input voltage does not exceed the range of 0V to +V_{AVDD}.

To make use of the input clamps, connect a resistor (R_S) between the analog input and the voltage source to limit the voltage at the analog input so that the fault current into the devices does not exceed ±20mA. Note that the voltage at the analog input pin limits to approximately 7V during a fault condition so the following equation can be used to calculate the value of R_S:

$$R_S = \frac{V_{FAULT\_MAX} - 7V}{20\text{mA}}$$

where V_{FAULT_MAX} is the maximum voltage that the source produces during a fault condition.
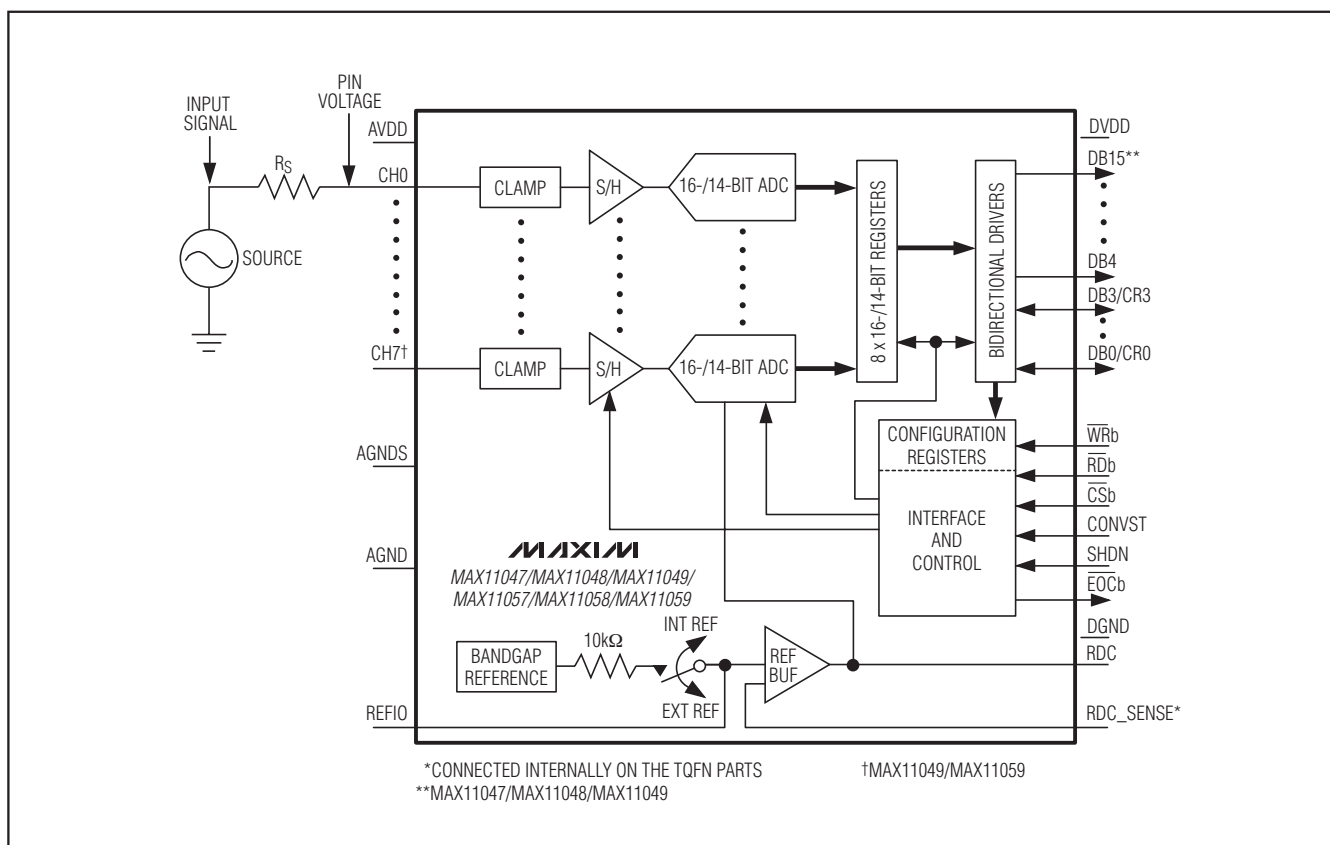
Figure 1. Required Setup for Clamp Circuit

MAX11047–MAX11049/MAX11057–MAX11059
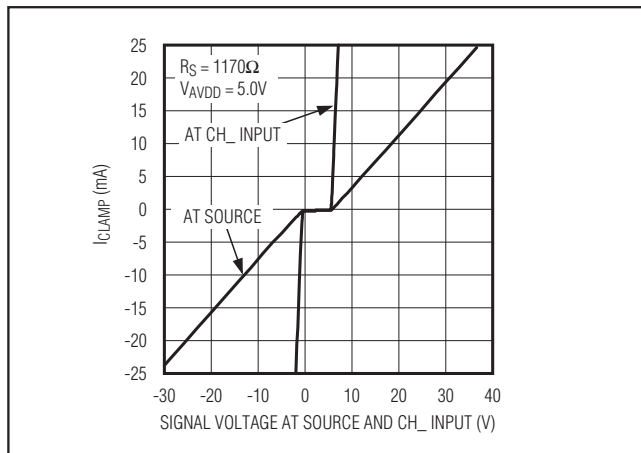
Figure 2. Input Clamp Characteristics
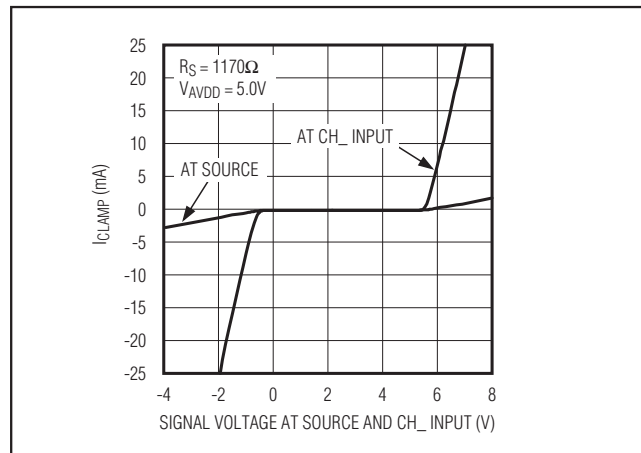
Figure 3. Input Clamp Characteristics (Zoom In)

Figures 2 and 3 illustrate the clamp circuit voltage-current characteristics for a source impedance RS = 1280Ω. While the input voltage is within the -300mV to +(V_AVDD + 300mV) range, no current flows in the input clamps. Once the input voltage goes beyond this voltage range, the clamps turn on and limit the voltage at the input pin.

Applications Information

Digital Interface

The bidirectional, parallel, digital interface, CR0–CR3, sets the 4-bit configuration register. This interface configures the following control signals: chip select ($\overline{CS}$), read ($\overline{RD}$), write ($\overline{WR}$), end of conversion ($\overline{EOC}$), and convert start (CONVST). Figures 6 and 7 and the Timing Characteristics in the *Electrical Characteristics* table show the operation of the interface.

DB0–DB15/13, output the 16-/14-bit conversion result. All bits are high impedance when $\overline{RD}$ = 1 or $\overline{CS}$ = 1.

CR3 (Int/Ext Reference)

CR3 selects the internal or external reference. The POR default = 0.

0 = internal reference, REFIO internally driven through a 10kΩ resistor, bypass with 0.1µF capacitor to AGND.

1 = external reference, drive REFIO with a high quality reference.

CR2 (Output Data Format)

CR2 selects the output data format. The POR default = 0.

0 = offset binary.

1 = two's complement.

CR1 (Reserved)

CR1 must be set to 0.

CR0 (CONVST Mode)

CR0 selects the acquisition mode. The POR default = 0.

0 = CONVST controls the acquisition and conversion. Drive CONVST low to start acquisition. The rising edge of CONVST begins the conversion.

1 = acquisition mode starts as soon as previous conversion is complete. The rising edge of CONVST begins the conversion.

Programming the Configuration Register

To program the configuration register, bring the $\overline{CS}$ and $\overline{WR}$ low and apply the required configuration data on CR3–CR0 of the bus and then raise $\overline{WR}$ once to save changes.

CAUTION: The host driving CR3–CR0 must relinquish the bus when the conversion results of the ADC are being read.

Starting a Conversion

CONVST initiates conversions. The devices provide two acquisition modes set through the configuration register. Allow a quiet time (t_Q) of 500ns prior to the start of conversion to avoid any noise interference during readout or write operations from corrupting a sample.

Table 1. Configuration Register

CR3	CR2	CR1	CR0
Int/Ext Reference	Output Data Format	Must be set to 0	CONVST Mode

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In default mode (CR0 = 0), drive CONVST low to place the devices into acquisition mode. All the input switches are closed and the internal T/H circuits track the respective input voltage. Keep the CONVST signal low for at least 1μs (t_{ACQ}) to enable proper settling of the sampled voltages. On the rising edge of CONVST, the switches are opened and the devices begin the conversion on all the samples in parallel. $\overline{EOC}$ remains high until the conversion is completed.

In the second mode (CR0 = 1), the devices enter acquisition mode as soon as the previous conversion is completed. CONVST rising edge initiates the next sample and conversion sequence. Drive CONVST low for at least 20ns to be valid.

Provide adequate time for acquisition and the requisite quiet time in both modes to achieve accurate sampling and maximum performance of the devices.

Reading Conversion Results
The $\overline{CS}$ and $\overline{RD}$ are active-low, digital inputs that control the readout through the 16-/14-bit, parallel, 20MHz data bus (D0–D15/13). After $\overline{EOC}$ transitions low, read the conversion data by driving $\overline{CS}$ and $\overline{RD}$ low. Each low period of $\overline{RD}$ presents the next channel's result. When $\overline{CS}$ or $\overline{RD}$ are high, the data bus is high impedance. $\overline{CS}$ may be driven high between individual channel readouts or left low during the entire 8-channel readout.

Reference
Internal Reference
The devices feature a precision, low-drift, internal bandgap reference. Bypass REFIO with a 0.1μF capacitor to AGND to reduce noise. The REFIO output voltage may be used as a reference for other circuits. The output impedance of REFIO is 10kΩ. Drive only high-impedance circuits or buffer externally when using REFIO to drive external circuitry.

External Reference
Set the configuration register to disable the internal reference and drive REFIO with a high-quality external reference. To avoid signal degradation, ensure that the integrated reference noise applied to REFIO is less than 10μV in the bandwidth of up to 50kHz.

Reference Buffer
The devices have a built-in reference buffer to provide a low-impedance reference source to the SAR converters. This buffer is used in both internal and external reference modes. The internal reference buffer output feeds five RDC outputs. Connect all RDC outputs together. The reference buffer is externally compensated and requires at least 10μF on the RDC node for stability. For best performance, provide a total of at least 80μF on the RDC outputs.

Transfer Functions
Figures 8 and 9 show the transfer functions for all the formats and devices. Code transitions occur halfway between successive-integer LSB values.

Layout, Grounding, and Bypassing
For best performance, use PCBs with ground planes. Ensure that digital and analog signal lines are separated from each other. Do not run analog and digital lines parallel to one another (especially clock lines), and avoid running digital lines underneath the ADC package. A single solid GND plane configuration with digital signals routed from one direction and analog signals from the other provides the best performance. Connect DGND, AGND, and AGNDS pins on the devices to this ground plane. Keep the ground return to the power supply for this ground low impedance and as short as possible for noise-free operation.

To achieve the highest performance, connect all the RDC pins 22, 28, 35, 43, and 49 for the TQFN package or pins 27, 33, 40, 48, and 54 for the TQFP package to a local RDC plane on the PCB. In addition, on the TQFP package, the RDC_SENSE pins 26 and 55 should be directly connected to this RDC plane as well. Bypass the RDC outputs with a total of at least 80μF of capacitance. For example, if two capacitors are used, place two 47μF, 10V X5R capacitors in 1210 case size as close as possible to pins 22 and 49 (TQFN), or pins 27 and 54 (TQFP). Alternatively, if four capacitors are used, place four 22μF, 10V X5R capacitors in 1210 case size as close as possible to pins 22, 28, 43, and 49 (TQFN), or pins 27, 33, 48, and 54 (TQFP). Ensure that each capacitor is connected directly into the GND plane with an independent via.

In cases where Y5U or Z5U ceramics are used, select higher voltage rating capacitors to compensate for the high-voltage coefficient of these ceramic capacitors, thus ensuring that at least 80μF of capacitance is on the RDC plane when the plane is driven to 4.096V by the internal reference buffer. For example, at 4.096V, a 22μF X5R ceramic capacitor with a 10V rating diminishes to only 20μF, whereas the same capacitor in Y5U ceramic at 4.096V decreases to about 13μF. However, a 22μF Y5U ceramic capacitor with a 25V rating capacitor is approximately 20μF at 4.096V.

Bypass AVDD and DVDD to the ground plane with 0.1μF ceramic chip capacitors on each pin as close as possible to the device to minimize parasitic inductance. Add at least one bulk 10μF decoupling capacitor to AVDD and DVDD per PCB. Interconnect all of the AVDD inputs and DVDD inputs using two solid power planes. For best performance, bring the AVDD power plane in on the analog interface side of the devices and the DVDD power plane from the digital interface side of the devices.

For sampling periods near minimum (1μs) use a 1nF C0G ceramic chip capacitor between each of the channel inputs to the ground plane as close as possible to the devices. This capacitor reduces the inductance seen by the sampling circuitry and reduces the voltage transient seen by the input source circuit.
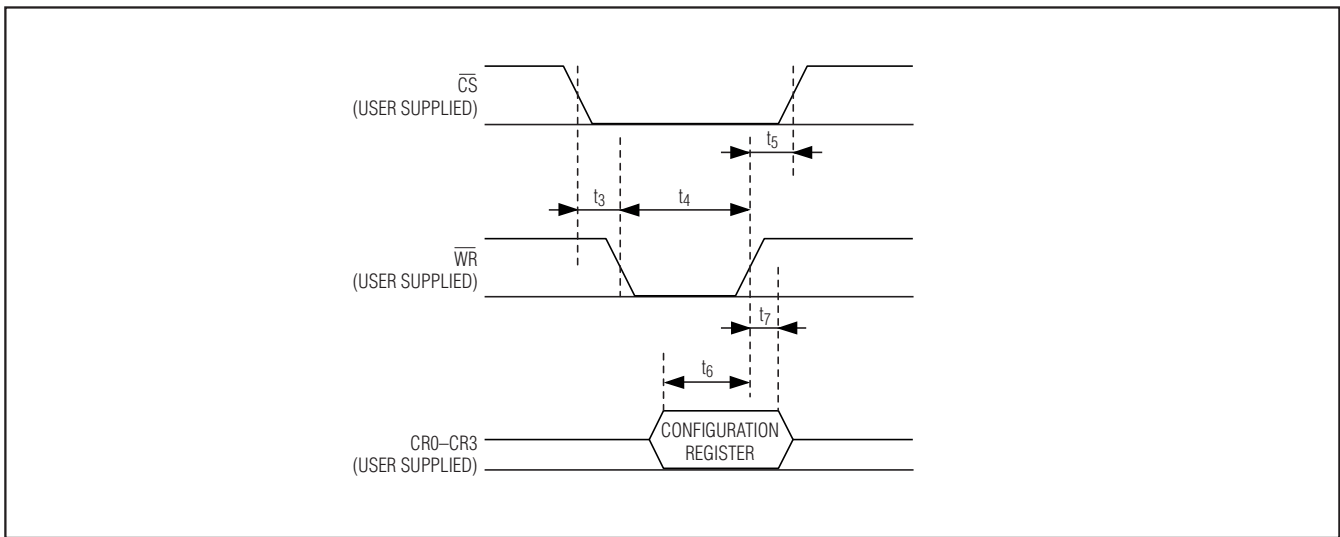
Figure 4. Programming Configuration-Register Timing Requirements
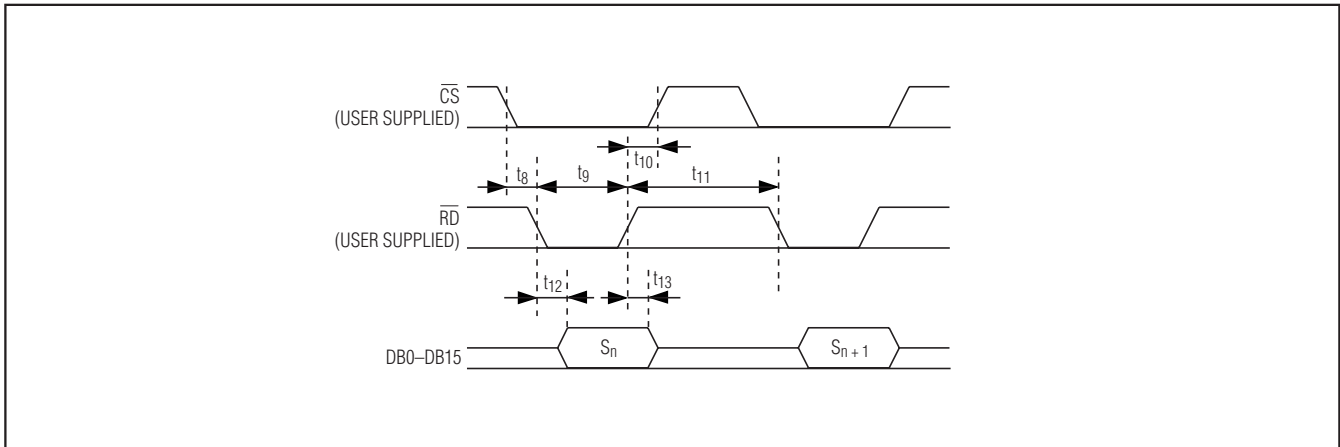
Figure 5. Readout Timing Requirements

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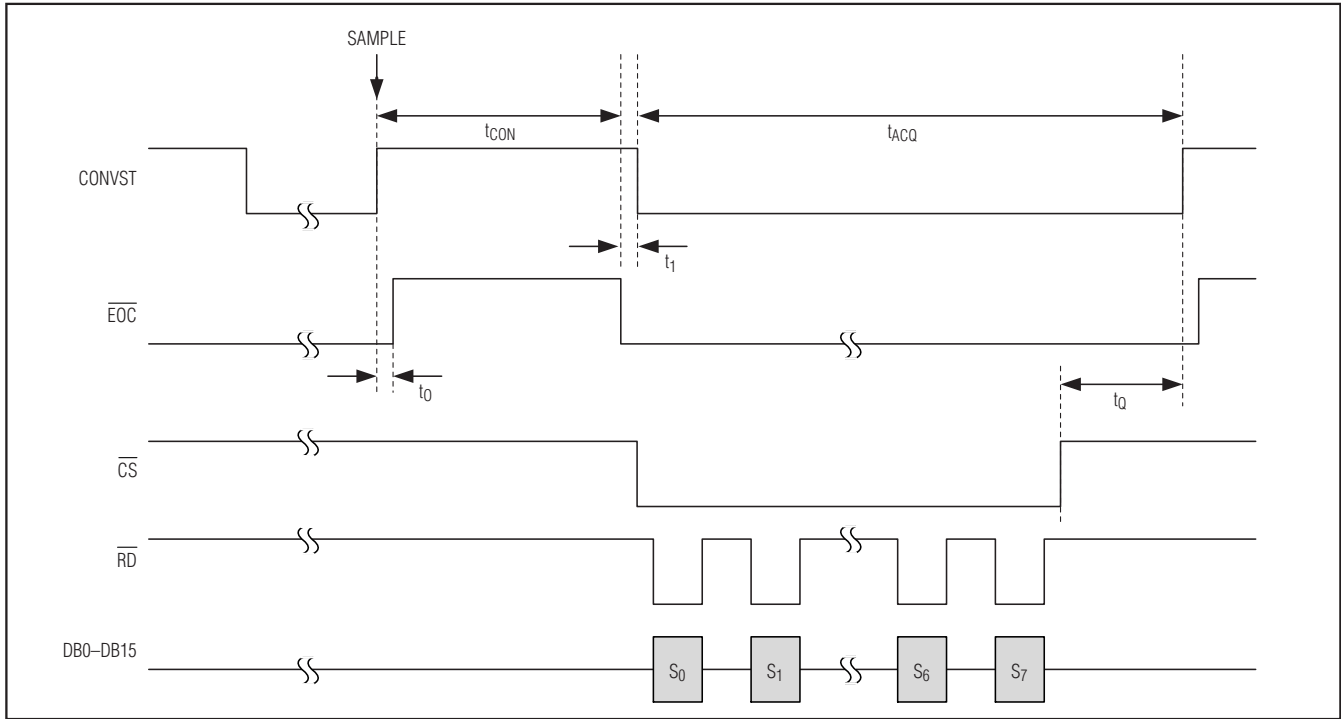
Figure 6. Conversion Timing Diagram (CR0 = 0)
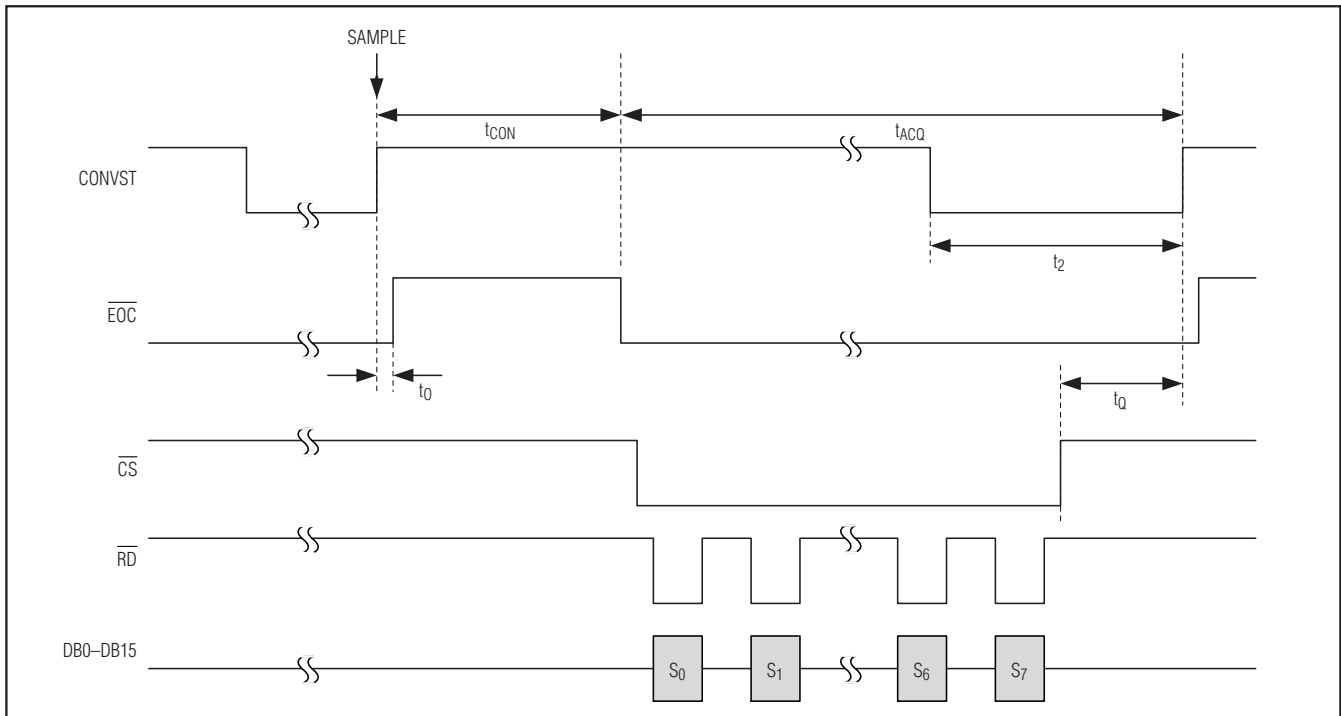
Figure 7. Conversion Timing Diagram (CR0 = 1)

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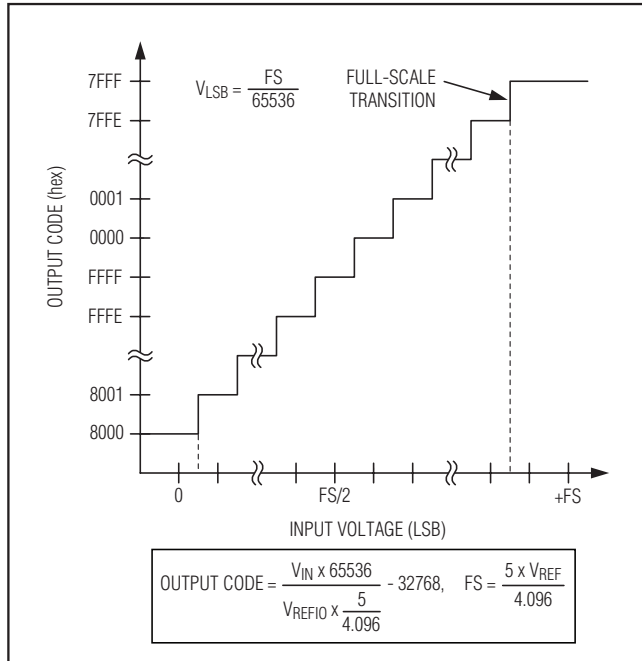
Figure 8a. Two's Complement Transfer Function for 16-Bit Devices
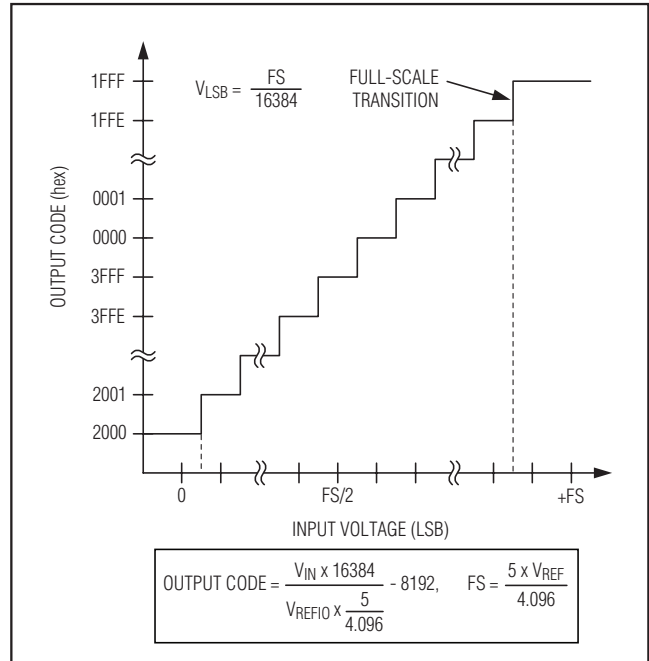
Figure 8b. Two's Complement Transfer Function for 14-Bit Devices
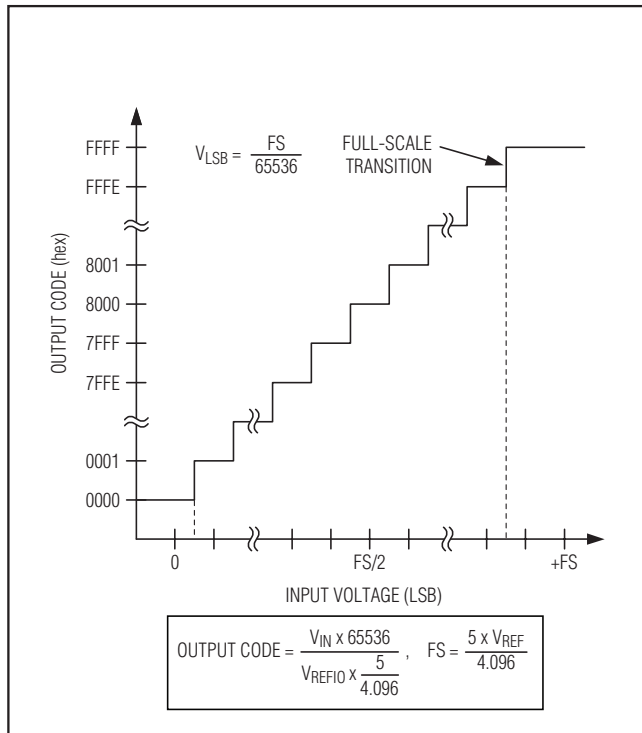
Figure 9a. Offset-Binary Transfer Function for 16-Bit Devices
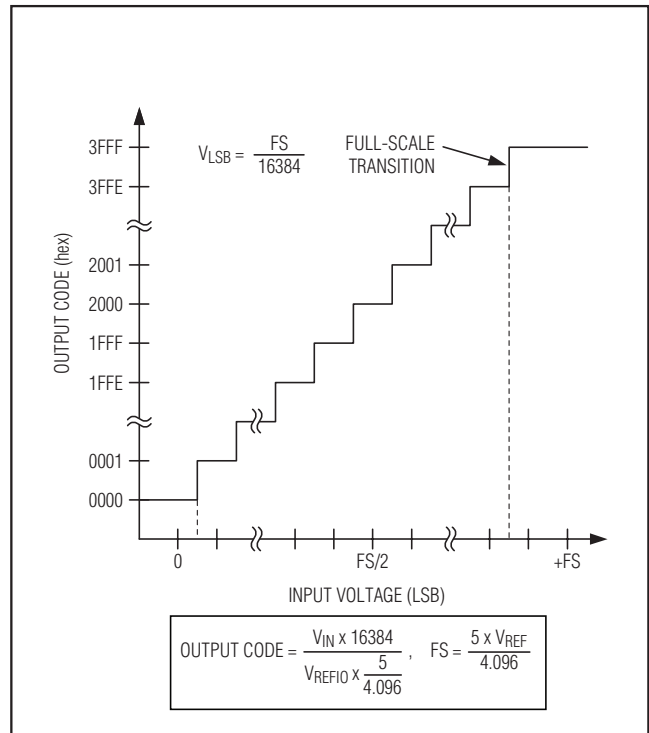
Figure 9b. Offset-Binary Transfer Function for 14-Bit Devices

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Typical Application Circuits

Power-Grid Protection

Figure 10 shows a typical power-grid protection application.

DSP Motor Control

Figure 11 shows a typical DSP motor control application.
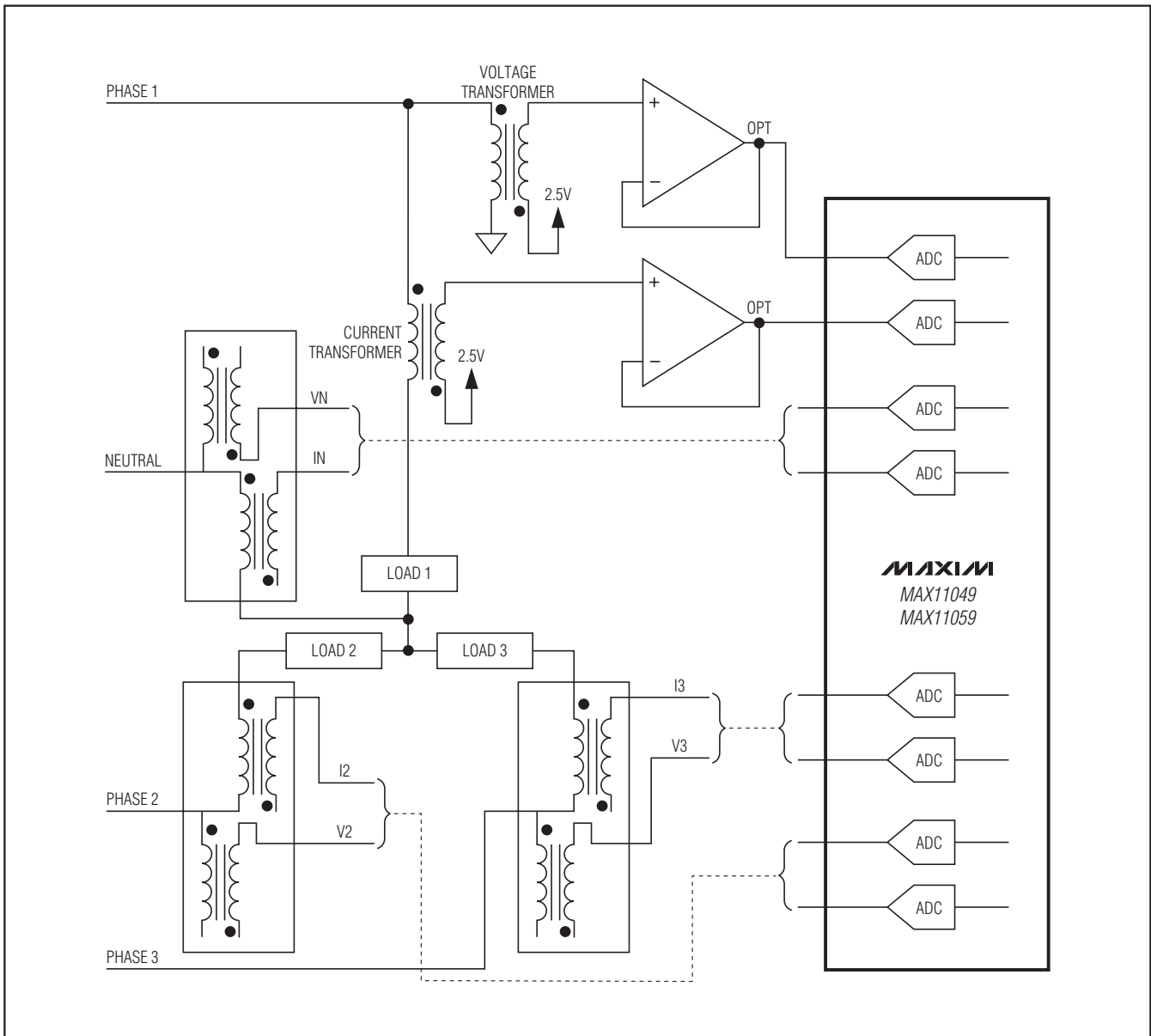
Figure 10. Power-Grid Protection

MAX11047–MAX11049/MAX11057–MAX11059
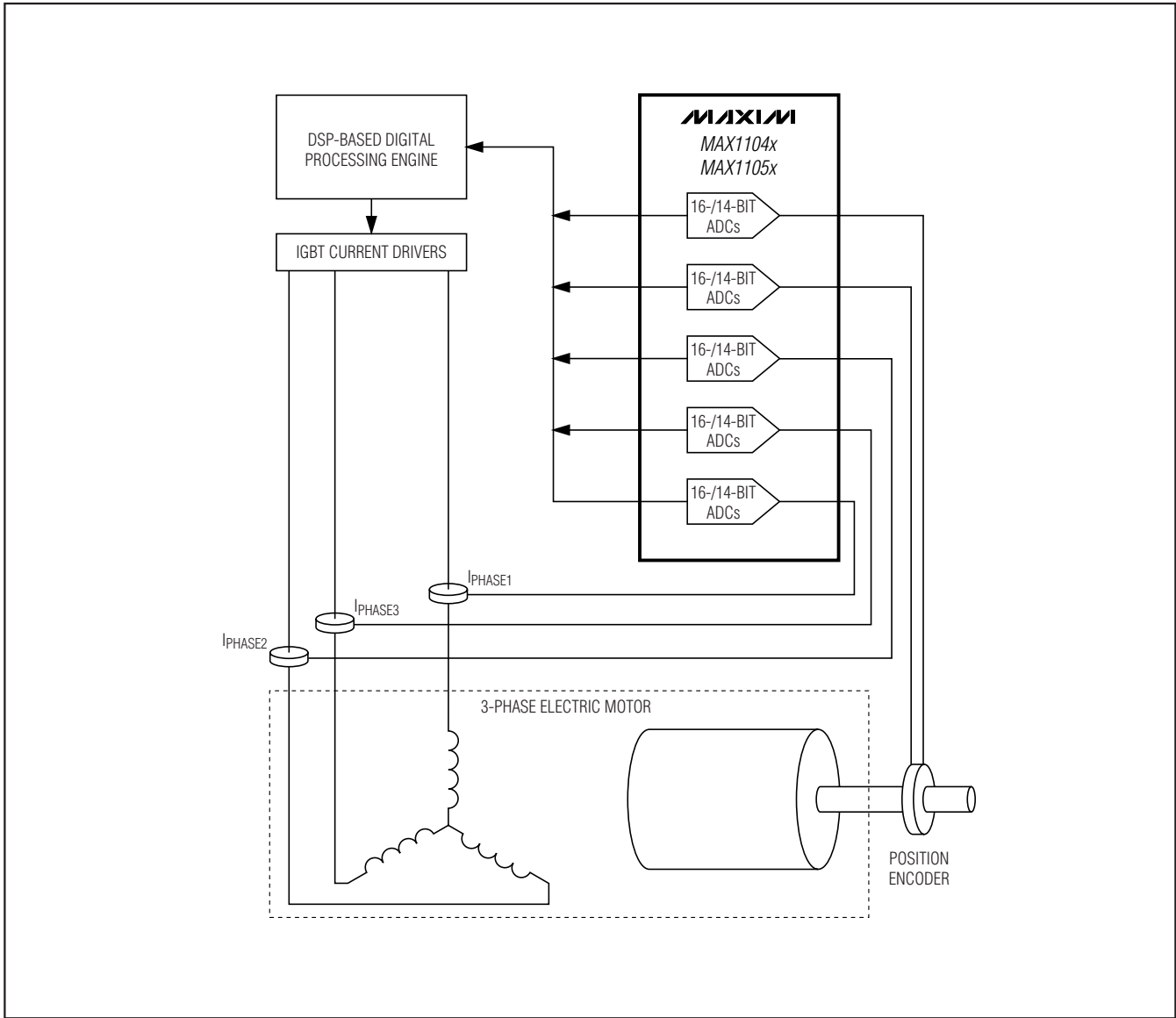
Figure 11. DSP Motor Control

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Definitions

Integral Nonlinearity (INL)

INL is the deviation of the values on an actual transfer function from a straight line. For these devices, this straight line is a line drawn between the end points of the transfer function, once offset and gain errors have been nullified.

Differential Nonlinearity (DNL)

DNL is the difference between an actual step width and the ideal value of 1 LSB. For these devices, the DNL of each digital output code is measured and the worst-case value is reported in the *Electrical Characteristics* table. A DNL error specification of greater than -1 LSB guarantees no missing codes and a monotonic transfer function for an SAR ADC. For example, -0.9 LSB guarantees no missing code while -1.1 LSB results in missing code.

Offset Error

For the MAX11047/MAX11048/MAX11049, the offset error is defined at code transition 0x0000 to 0x0001 in offset binary encoding and 0x8000 to 0x8001 for two's complement encoding. For the MAX11057/MAX11058/ MAX11059, the offset error is defined at code transition 0x0000 to 0x0001 in offset binary encoding and 0x2000 to 0x2001 for two's complement encoding. The offset code transitions should occur with an analog input voltage of exactly 0.5 x (5/4.096) x V_{REF}/65,536 above GND for 16-bit devices or 0.5 x (5/4.096) x V_{REF}/16384 above GND for 14-bit devices. The offset error is defined as the deviation between the actual analog input voltage required to produce the offset code transition and the ideal analog input of 0.5 x (5/4.096) x V_{REF}/65,536 above GND for 16-bit devices or 0.5 x (5/4.096) x V_{REF}/16384 above GND for 14-bit devices, expressed in LSBs.

Gain Error

Gain error is defined as the difference between the change in analog input voltage required to produce a top code transition minus a bottom code transition, subtracted from the ideal change in analog input voltage on (5/4.096) x V_{REF} x (65,534/65,536) for 16-bit or (5/4.096) x V_{REF} x (16382/16384) for 14-bit devices. For the devices, top code transition is 0x7FFE to 0x7FFF in two's complement mode and 0xFFFE to 0xFFFF in offset binary mode. The bottom code transition is 0x8000 and 0x8001 in two's complement mode and 0x0000 and 0x0001 in offset binary mode. For the MAX11057/MAX11058/MAX11059, top code transition is 0x1FFE to 0x1FFF in two's complement mode and 0x3FFE to 0x3FFF in offset binary mode. The bottom code transition is 0x2000 and 0x2001 in two's

complement mode and 0x0000 to 0x0001 in offset binary mode. For the devices, the analog input voltage to produce these code transitions is measured and the gain error is computed by subtracting (5/4.096) x V_{REF} x (65,534/65,536) or (5/4.096) x V_{REF} x (16382/16384), respectively, from this measurement.

Signal-to-Noise Ratio (SNR)

For a waveform perfectly reconstructed from digital samples, SNR is the ratio of the full-scale analog input (RMS value) to the RMS quantization error (residual error). The ideal, theoretical minimum analog-to-digital noise is caused by quantization noise error only and results directly from the ADC's resolution (N bits):

$$SNR = (6.02 \times N + 1.76)dB$$

where N = 16/14 bits. In reality, there are other noise sources besides quantization noise: thermal noise, reference noise, clock jitter, etc. SNR is computed by taking the ratio of the RMS signal to the RMS noise, which includes all spectral components not including the fundamental, the first five harmonics, and the DC offset.

Signal-to-Noise Plus Distortion (SINAD)

SINAD is the ratio of the fundamental input frequency's RMS amplitude to the RMS equivalent of all the other ADC output signals:

$$SINAD(dB) = 10 \times \log\left[\frac{Signal_{RMS}}{(Noise + Distortion)_{RMS}}\right]$$

Effective Number of Bits (ENOB)

The ENOB indicates the global accuracy of an ADC at a specific input frequency and sampling rate. An ideal ADC's error consists of quantization noise only. With an input range equal to the full-scale range of the ADC, calculate the ENOB as follows:

$$ENOB = \frac{SINAD - 1.76}{6.02}$$

Total Harmonic Distortion (THD)

THD is the ratio of the RMS of the first five harmonics of the input signal to the fundamental itself. This is expressed as:

$$THD = 20 \times \log\left[\frac{\sqrt{V2^2 + V3^2 + V4^2 + V5^2}}{V_1}\right]$$

where V_1 is the fundamental amplitude and V_2 through V_5 are the 2nd- through 5th-order harmonics.

Spurious-Free Dynamic Range (SFDR)

SFDR is the ratio of the RMS amplitude of the fundamental (maximum signal component) to the RMS value of the next-largest frequency component.

Aperture Delay

Aperture delay (t_{AD}) is the time delay from the sampling clock edge to the instant when an actual sample is taken.

Aperture Jitter

Aperture Jitter (t_{AJ}) is the sample-to-sample variation in aperture delay.

Channel-to-Channel Isolation

Channel-to-channel isolation indicates how well each analog input is isolated from the other channels. Channel-to-channel isolation is measured by applying DC to channels 1 to 7, while a -0.4dBFS sine wave at 60Hz is applied to channel 0. A 10ksps FFT is taken for channel 0 and channel 1. Channel-to-channel isolation is expressed in dB as the power ratio of the two 60Hz magnitudes.

Small-Signal Bandwidth

A small -20dBFS analog input signal is applied to an ADC in a manner that ensures that the signal's slew rate does not limit the ADC's performance. The input frequency is then swept up to the point where the amplitude of the digitized conversion result has decreased 3dB.

Full-Power Bandwidth

A large -0.5dBFS analog input signal is applied to an ADC, and the input frequency is swept up to the point where the amplitude of the digitized conversion result has decreased by 3dB. This point is defined as full-power input bandwidth frequency.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
56 TQFN-EP	T5688+2	**21-0135**	**90-0046**
64 TQFP-EP	C64E+6	**21-0084**	**90-0328**

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REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	12/09	Initial release	—
1	6/10	Released MAX11047, MAX11048, and MAX11049 in TQFP packages	1–20
2	1/11	Released MAX11057, MAX11058, and MAX11059. Updated *Electrical Characteristics* and *Typical Operating Characteristics*.	1–8

MAX11047–MAX11049/MAX11057–MAX11059