



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



# MAX11102/03/05/06/10/11/15/16/17

## 2Msps/3Msps, Low-Power, Serial 12-/10-/8-Bit ADCs

### General Description

The MAX11102/MAX11103/MAX11105/MAX11106/MAX11110/MAX11111/MAX11115/MAX11116/MAX11117 are 12-/10-/8-bit, compact, high-speed, low-power, successive approximation analog-to-digital converters (ADCs). These high-performance ADCs include a high-dynamic range sample-and-hold and a high-speed serial interface. These ADCs accept a full-scale input from 0V to the power supply or to the reference voltage.

The MAX11102/MAX11103/MAX11106/MAX11111 feature dual, single-ended analog inputs connected to the ADC core using a 2:1 MUX. The devices also include a separate supply input for data interface and a dedicated input for reference voltage. In contrast, the single-channel devices generate the reference voltage internally from the power supply.

These ADCs operate from a 2.2V to 3.6V supply and consume only 5.2mW at 3Msps and 3.7mW at 2Msps. The devices include full power-down mode and fast wake-up for optimal power management and a high-speed 3-wire serial interface. The 3-wire serial interface directly connects to SPI, QSPI™, and MICROWIRE® devices without external logic.

Excellent dynamic performance, low voltage, low power, ease of use, and small package size make these converters ideal for portable battery-powered data-acquisition applications, and for other applications that demand low-power consumption and minimal space.

These ADCs are available in a 10-pin TDFN package, 10-pin  $\mu$ MAX® package, and a 6-pin SOT23 package. These devices operate over the -40°C to +125°C temperature range.

### Features

- ◆ 2Msps/3Msps Conversion Rate, No Pipeline Delay
- ◆ 12-/10-/8-Bit Resolution
- ◆ 1-/2-Channel, Single-Ended Analog Inputs
- ◆ Low-Noise 73dB SNR
- ◆ Variable I/O: 1.5V to 3.6V (Dual-Channel Only)  
Allows the Serial Interface to Connect Directly to 1.5V, 1.8V, 2.5V, or 3V Digital Systems
- ◆ 2.2V to 3.6V Supply Voltage
- ◆ Low Power  
3.7mW at 2Msps  
5.2mW at 3Msps  
Very Low Power Consumption at 2.5 $\mu$ A/ksps
- ◆ External Reference Input (Dual-Channel Devices Only)
- ◆ 1.3 $\mu$ A Power-Down Current
- ◆ SPI-/QSPI-/MICROWIRE-Compatible Serial Interface
- ◆ 10-Pin, 3mm x 3mm TDFN Package
- ◆ 10-Pin, 3mm x 5mm  $\mu$ MAX Package
- ◆ 6-Pin, 2.8mm x 2.9mm SOT23 Package
- ◆ Wide -40°C to +125°C Operation

### Applications

Data Acquisition  
 Portable Data Logging  
 Medical Instrumentation  
 Battery-Operated Systems  
 Communication Systems  
 Automotive Systems

### Ordering Information

PART	PIN-PACKAGE	BITS	SPEED (Msps)	NO. OF CHANNELS	TOP MARK
MAX11102AUB+	10 $\mu$ MAX-EP*	12	2	2	+ABBA
MAX11102AUB/V+	10 $\mu$ MAX-EP*	12	2	2	+ABBR
MAX11102ATB+	10 TDFN-EP*	12	2	2	+AWI
MAX11103AUB+	10 $\mu$ MAX-EP*	12	3	2	+AAAU
MAX11103ATB+	10 TDFN-EP*	12	3	2	+AWV

Ordering Information continued at end of data sheet.

**Note:** All devices are specified over the -40°C to +125°C operating temperature range.

+Denotes a lead(Pb)-free/RoHS-compliant package.

\*EP = Exposed pad.

QSPI is a trademark of Motorola, Inc.

MICROWIRE is a registered trademark of National Semiconductor Corp.

$\mu$ MAX is a registered trademark of Maxim Integrated Products, Inc.

**For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at [www.maximintegrated.com](http://www.maximintegrated.com).**

# MAX11102/03/05/06/10/11/15/16/17

## 2Msps/3Msps, Low-Power, Serial 12-/10-/8-Bit ADCs

### ABSOLUTE MAXIMUM RATINGS

VDD to GND .....	-0.3V to +4V	10-Pin TDFN (derate 24.4mW/°C above +70°C).....	1951mW
REF, OVDD, AIN1, AIN2, AIN to GND .....	-0.3V to the lower of (VDD + 0.3V) and +4V	10-Pin μMAX (derate 8.8mW/°C above +70°C).....	707.3mW
CS, SCLK, CHSEL, DOUT TO GND.....	-0.3V to the lower of (VOVDD + 0.3V) and +4V	Operating Temperature Range .....	-40°C to +125°C
AGND to GND .....	-0.3V to +0.3V	Junction Temperature .....	+150°C
Input/Output Current (all pins) .....	50mA	Storage Temperature Range.....	-65°C to +150°C
Continuous Power Dissipation (TA = +70°C)		Lead Temperature (soldering, 10s) .....	+300°C
6-Pin SOT23 (derate 8.7mW/°C above +70°C) .....	696mW	Soldering Temperature (reflow) .....	+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### ELECTRICAL CHARACTERISTICS (MAX11102/MAX11103)

(VDD = 2.2V to 3.6V, VREF = VDD, VOVDD = VDD. MAX11102: fSCLK = 32MHz, 50% duty cycle, 2Msps. MAX11103: fSCLK = 48MHz, 50% duty cycle, 3Msps. CDOUT = 10pF, TA = -40°C to +125°C, unless otherwise noted. Typical values are at TA = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>DC ACCURACY</b>						
Resolution			12			Bits
Integral Nonlinearity	INL				±1	LSB
Differential Nonlinearity	DNL	No missing codes			±1	LSB
Offset Error	OE			±0.3	±3	LSB
Gain Error	GE	Excluding offset and reference errors		±1	±3	LSB
Total Unadjusted Error	TUE			±1.5		LSB
Channel-to-Channel Offset Matching				±0.4		LSB
Channel-to-Channel Gain Matching				±0.05		LSB
<b>DYNAMIC PERFORMANCE (MAX11103: fAIN = 1MHz, MAX11102: fAIN = 0.5MHz)</b>						
Signal-to-Noise and Distortion	SINAD	MAX11103	70	72		dB
		MAX11102	70	72.5		
Signal-to-Noise Ratio	SNR	MAX11103	70.5	72		dB
		MAX11102	70.5	73		
Total Harmonic Distortion	THD	MAX11103		-85	-75	dB
		MAX11102		-85	-76	
Spurious-Free Dynamic Range	SFDR	MAX11103	76	85		dB
		MAX11102	77	85		
Intermodulation Distortion	IMD	MAX11103: f1 = 1.0003MHz, f2 = 0.99955MHz MAX11102: f1 = 500.15kHz, f2 = 499.56kHz		-84		dB
Full-Power Bandwidth		-3dB point		40		MHz
Full-Linear Bandwidth		SINAD > 68dB		2.5		MHz
Small-Signal Bandwidth				45		MHz
Crosstalk				-90		dB

# MAX11102/03/05/06/10/11/15/16/17

## 2Msps/3Msps, Low-Power, Serial 12-/10-/8-Bit ADCs

### ELECTRICAL CHARACTERISTICS (MAX11102/MAX11103) (continued)

(V<sub>DD</sub> = 2.2V to 3.6V, V<sub>REF</sub> = V<sub>DD</sub>, V<sub>OVDD</sub> = V<sub>DD</sub>. MAX11102: f<sub>SCLK</sub> = 32MHz, 50% duty cycle, 2Msps. MAX11103: f<sub>SCLK</sub> = 48MHz, 50% duty cycle, 3Msps. C<sub>DOUT</sub> = 10pF, T<sub>A</sub> = -40°C to +125°C, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>CONVERSION RATE</b>						
Throughput		MAX11103	0.03		3	Msps
		MAX11102	0.02		2	
Conversion Time		MAX11103	260			ns
		MAX11102	391			
Acquisition Time	t <sub>ACQ</sub>		52			ns
Aperture Delay		From $\overline{CS}$ falling edge		4		ns
Aperture Jitter				15		ps
Serial-Clock Frequency	f <sub>CLK</sub>	MAX11103	0.48		48	MHz
		MAX11102	0.32		32	
<b>ANALOG INPUT (AIN1, AIN2)</b>						
Input Voltage Range	V <sub>AIN<sub>L</sub></sub>		0		V <sub>REF</sub>	V
Input Leakage Current	I <sub>ILA</sub>			0.002	±1	μA
Input Capacitance	C <sub>AIN<sub>L</sub></sub>	Track		20		pF
		Hold		4		
<b>EXTERNAL REFERENCE INPUT (REF)</b>						
Reference Input-Voltage Range	V <sub>REF</sub>		1		V <sub>DD</sub> + 0.05	V
Reference Input Leakage Current	I <sub>ILR</sub>	Conversion stopped		0.005	±1	μA
Reference Input Capacitance	C <sub>REF</sub>			5		pF
<b>DIGITAL INPUTS (SCLK, <math>\overline{CS}</math>, CHSEL)</b>						
Digital Input High Voltage	V <sub>IH</sub>		0.75 x			V
Digital Input Low Voltage	V <sub>IL</sub>				0.25 x	
Digital Input Hysteresis	V <sub>HYST</sub>			0.15 x		V
Digital Input Leakage Current	I <sub>IL</sub>	Inputs at GND or V <sub>DD</sub>		0.001	±1	μA
Digital Input Capacitance	C <sub>IN</sub>			2		pF
<b>DIGITAL OUTPUT (DOUT)</b>						
Output High Voltage	V <sub>OH</sub>	I <sub>SOURCE</sub> = 200μA	0.85 x			V
Output Low Voltage	V <sub>OL</sub>	I <sub>SINK</sub> = 200μA			0.15 x	
High-Impedance Leakage Current	I <sub>OL</sub>				±1.0	μA
High-Impedance Output Capacitance	C <sub>OUT</sub>			4		pF



# MAX11102/03/05/06/10/11/15/16/17

## 2Msps/3Msps, Low-Power, Serial 12-/10-/8-Bit ADCs

### ELECTRICAL CHARACTERISTICS (MAX11102/MAX11103) (continued)

(V<sub>DD</sub> = 2.2V to 3.6V, V<sub>REF</sub> = V<sub>DD</sub>, V<sub>OVDD</sub> = V<sub>DD</sub>. MAX11102: f<sub>SCLK</sub> = 32MHz, 50% duty cycle, 2Msps. MAX11103: f<sub>SCLK</sub> = 48MHz, 50% duty cycle, 3Msps. C<sub>DOUT</sub> = 10pF, T<sub>A</sub> = -40°C to +125°C, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>POWER SUPPLY</b>						
Positive Supply Voltage	V <sub>DD</sub>		2.2		3.6	V
Digital I/O Supply Voltage	V <sub>OVDD</sub>		1.5		V <sub>DD</sub>	V
Positive Supply Current (Full-Power Mode)	I <sub>VDD</sub>	MAX11103, V <sub>AIN_</sub> = V <sub>GND</sub>			3.3	mA
		MAX11102, V <sub>AIN_</sub> = V <sub>GND</sub>			2.6	
	I <sub>OVDD</sub>	MAX11103, V <sub>AIN_</sub> = V <sub>GND</sub>			0.33	
		MAX11102, V <sub>AIN_</sub> = V <sub>GND</sub>			0.22	
Positive Supply Current (Full-Power Mode), No Clock	I <sub>VDD</sub>	MAX11103		1.98		mA
		MAX11102		1.48		
Power-Down Current	I <sub>PD</sub>	Leakage only		1.3	10	μA
Line Rejection		V <sub>DD</sub> = +2.2V to +3.6V, V <sub>REF</sub> = 2.2V		0.7		LSB/V
<b>TIMING CHARACTERISTICS (Note 1)</b>						
Quiet Time	t <sub>Q</sub>	(Note 2)	4			ns
CS Pulse Width	t <sub>1</sub>	(Note 2)	10			ns
CS Fall to SCLK Setup	t <sub>2</sub>	(Note 2)	5			ns
CS Falling Until DOUT High-Impedance Disabled	t <sub>3</sub>	(Note 2)	1			ns
Data Access Time After SCLK Falling Edge	t <sub>4</sub>	Figure 2, V <sub>OVDD</sub> = 2.2V - 3.6V			15	ns
		Figure 2, V <sub>OVDD</sub> = 1.5V - 2.2V			16.5	
SCLK Pulse Width Low	t <sub>5</sub>	Percentage of clock period (Note 2)	40		60	%
SCLK Pulse Width High	t <sub>6</sub>	Percentage of clock period (Note 2)	40		60	%
Data Hold Time From SCLK Falling Edge	t <sub>7</sub>	Figure 3	5			ns
SCLK Falling Until DOUT High-Impedance	t <sub>8</sub>	Figure 4 (Note 2)	2.5		14	ns
Power-Up Time		Conversion cycle (Note 2)			1	Cycle

### ELECTRICAL CHARACTERISTICS (MAX11105)

(V<sub>DD</sub> = 2.2V to 3.6V, f<sub>SCLK</sub> = 32MHz, 50% duty cycle, 2Msps, C<sub>DOUT</sub> = 10pF, T<sub>A</sub> = -40°C to +125°C, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>DC ACCURACY</b>						
Resolution			12			Bits
Integral Nonlinearity	INL				±1	LSB
Differential Nonlinearity	DNL	No missing codes			±1	LSB
Offset Error	OE			±0.3	±3	LSB
Gain Error	GE	Excluding offset and reference errors		±1	±3	LSB
Total Unadjusted Error	TUE			±1.5		LSB
<b>DYNAMIC PERFORMANCE</b>						
Signal-to-Noise and Distortion	SINAD	f <sub>AIN</sub> = 500kHz	70	72.5		dB
Signal-to-Noise Ratio	SNR	f <sub>AIN</sub> = 500kHz	70.5	73		dB

# MAX11102/03/05/06/10/11/15/16/17

## 2Msps/3Msps, Low-Power, Serial 12-/10-/8-Bit ADCs

### ELECTRICAL CHARACTERISTICS (MAX11105) (continued)

(V<sub>DD</sub> = 2.2V to 3.6V, f<sub>SCLK</sub> = 32MHz, 50% duty cycle, 2Msps, C<sub>DOUT</sub> = 10pF, T<sub>A</sub> = -40°C to +125°C, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Total Harmonic Distortion	THD	f <sub>AIN</sub> = 500kHz		-85	-76	dB
Spurious-Free Dynamic Range	SFDR	f <sub>AIN</sub> = 500kHz	77	85		dB
Intermodulation Distortion	IMD	f <sub>1</sub> = 500.15 kHz, f <sub>2</sub> = 499.56 kHz		-84		dB
Full-Power Bandwidth		-3dB point		40		MHz
Full-Linear Bandwidth		SINAD > 68dB		2.5		MHz
Small-Signal Bandwidth				45		MHz
<b>CONVERSION RATE</b>						
Throughput			0.02		2	Msps
Conversion Time			391			ns
Acquisition Time	t <sub>ACQ</sub>		52			ns
Aperture Delay		From $\overline{\text{CS}}$ falling edge		4		ns
Aperture Jitter				15		ps
Serial Clock Frequency	f <sub>CLK</sub>		0.32		32	MHz
<b>ANALOG INPUT</b>						
Input Voltage Range	V <sub>AIN</sub>		0		V <sub>DD</sub>	V
Input Leakage Current	I <sub>ILA</sub>			0.002	±1	μA
Input Capacitance	C <sub>AIN</sub>	Track		20		pF
		Hold		4		
<b>DIGITAL INPUTS (SCLK, <math>\overline{\text{CS}}</math>, CHSEL)</b>						
Digital Input High Voltage	V <sub>IH</sub>		0.75 x V <sub>VDD</sub>			V
Digital Input Low Voltage	V <sub>IL</sub>				0.25 x V <sub>VDD</sub>	V
Digital Input Hysteresis	V <sub>HYST</sub>			0.15 x V <sub>VDD</sub>		V
Digital Input Leakage Current	I <sub>IL</sub>	Inputs at GND or V <sub>DD</sub>		0.001	±1	μA
Digital Input Capacitance	C <sub>IN</sub>			2		pF
<b>DIGITAL OUTPUT (DOUT)</b>						
Output High Voltage	V <sub>OH</sub>	I <sub>SOURCE</sub> = 200μA	0.85 x V <sub>VDD</sub>			V
Output Low Voltage	V <sub>OL</sub>	I <sub>SINK</sub> = 200μA			0.15 x V <sub>VDD</sub>	V
High-Impedance Leakage Current	I <sub>OL</sub>				±1.0	μA
High-Impedance Output Capacitance	C <sub>OUT</sub>			4		pF
<b>POWER SUPPLY</b>						
Positive Supply Voltage	V <sub>DD</sub>		2.2		3.6	V
Positive Supply Current (Full-Power Mode)	I <sub>VDD</sub>	V <sub>AIN</sub> = V <sub>GND</sub>			2.6	mA

# MAX11102/03/05/06/10/11/15/16/17

## 2Msps/3Msps, Low-Power, Serial 12-/10-/8-Bit ADCs

### ELECTRICAL CHARACTERISTICS (MAX11105) (continued)

( $V_{DD} = 2.2V$  to  $3.6V$ ,  $f_{SCLK} = 32MHz$ , 50% duty cycle, 2Msps,  $C_{DOUT} = 10pF$ ,  $T_A = -40^{\circ}C$  to  $+125^{\circ}C$ , unless otherwise noted. Typical values are at  $T_A = +25^{\circ}C$ .)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Positive Supply Current (Full-Power Mode), No Clock	$I_{VDD}$			1.48		mA
Power-Down Current	$I_{PD}$	Leakage only		1.3	10	$\mu A$
Line Rejection		$V_{DD} = +2.2V$ to $+3.6V$		0.7		LSB/V
<b>TIMING CHARACTERISTICS (Note 1)</b>						
Quiet Time	$t_Q$	(Note 2)	4			ns
$\overline{CS}$ Pulse Width	$t_1$	(Note 2)	10			ns
$\overline{CS}$ Fall to SCLK Setup	$t_2$	(Note 2)	5			ns
$\overline{CS}$ Falling Until DOUT High-Impedance Disabled	$t_3$	(Note 2)	1			ns
Data Access Time After SCLK Falling Edge	$t_4$	Figure 2, $V_{DD} = +2.2V$ to $+3.6V$			15	ns
SCLK Pulse Width Low	$t_5$	Percentage of clock period (Note 2)	40		60	%
SCLK Pulse Width High	$t_6$	Percentage of clock period (Note 2)	40		60	%
Data Hold Time From SCLK Falling Edge	$t_7$	Figure 3	5			ns
SCLK Falling Until DOUT High-Impedance	$t_8$	Figure 4 (Note 2)	2.5		14	ns
Power-Up Time		Conversion cycle (Note 2)			1	Cycle

### ELECTRICAL CHARACTERISTICS (MAX11106)

( $V_{DD} = 2.2V$  to  $3.6V$ ,  $V_{REF} = V_{DD}$ ,  $V_{OVDD} = V_{DD}$ ,  $f_{SCLK} = 48MHz$ , 50% duty cycle, 3Msps;  $C_{DOUT} = 10pF$ ,  $T_A = -40^{\circ}C$  to  $+125^{\circ}C$ , unless otherwise noted. Typical values are at  $T_A = +25^{\circ}C$ .)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>DC ACCURACY</b>						
Resolution			10			Bits
Integral Nonlinearity	INL				$\pm 0.4$	LSB
Differential Nonlinearity	DNL	No missing codes			$\pm 0.4$	LSB
Offset Error	OE			$\pm 0.5$	$\pm 1$	LSB
Gain Error	GE	Excluding offset and reference errors		0	$\pm 1$	LSB
Total Unadjusted Error	TUE			$\pm 0.5$		LSB
Channel-to-Channel Offset Matching				$\pm 0.05$		LSB
Channel-to-Channel Gain Matching				$\pm 0.05$		LSB
<b>DYNAMIC PERFORMANCE</b>						
Signal-to-Noise and Distortion	SINAD	$f_{AIN} = 1MHz$	61	61.8		dB
Signal-to-Noise Ratio	SNR	$f_{AIN} = 1MHz$	61	61.8		dB
Total Harmonic Distortion	THD	$f_{AIN} = 1MHz$		-83	-74	dB
Spurious-Free Dynamic Range	SFDR	$f_{AIN} = 1MHz$	75			dB

# MAX11102/03/05/06/10/11/15/16/17

## 2Msps/3Msps, Low-Power, Serial 12-/10-/8-Bit ADCs

### ELECTRICAL CHARACTERISTICS (MAX11106) (continued)

(V<sub>DD</sub> = 2.2V to 3.6V, V<sub>REF</sub> = V<sub>DD</sub>, V<sub>OVDD</sub> = V<sub>DD</sub>, f<sub>SCLK</sub> = 48MHz, 50% duty cycle, 3Msps; C<sub>DOUT</sub> = 10pF, T<sub>A</sub> = -40°C to +125°C, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Intermodulation Distortion	IMD	f <sub>1</sub> = 1.0003MHz, f <sub>2</sub> = 0.99955MHz		-82		dB
Full-Power Bandwidth		-3dB point		40		MHz
Full-Linear Bandwidth		SINAD > 60dB		2.5		MHz
Small-Signal Bandwidth				45		MHz
Crosstalk				-90		dB
<b>CONVERSION RATE</b>						
Throughput			0.03		3	Msps
Conversion Time			260			ns
Acquisition Time	t <sub>ACQ</sub>		52			ns
Aperture Delay		From $\overline{\text{CS}}$ falling edge		4		ns
Aperture Jitter				15		ps
Serial-Clock Frequency	f <sub>CLK</sub>		0.48		48	MHz
<b>ANALOG INPUT (AIN1, AIN2)</b>						
Input Voltage Range	V <sub>AIN_</sub>		0		V <sub>REF</sub>	V
Input Leakage Current	I <sub>ILA</sub>			0.002	±1	μA
Input Capacitance	C <sub>AIN_</sub>	Track		20		pF
		Hold		4		
<b>EXTERNAL REFERENCE INPUT (REF)</b>						
Reference Input-Voltage Range	V <sub>REF</sub>		1		V <sub>DD</sub> + 0.05	V
Reference Input Leakage Current	I <sub>ILR</sub>	Conversion stopped		0.005	±1	μA
Reference Input Capacitance	C <sub>REF</sub>			5		pF
<b>DIGITAL INPUTS (SCLK, <math>\overline{\text{CS}}</math>, CHSEL)</b>						
Digital Input-High Voltage	V <sub>IH</sub>		0.75 x			V
Digital Input-Low Voltage	V <sub>IL</sub>				0.25 x	V
Digital Input Hysteresis	V <sub>HYST</sub>			0.15 x		V
Digital Input Leakage Current	I <sub>IL</sub>	Inputs at GND or V <sub>DD</sub>		0.001	±1	μA
Digital Input Capacitance	C <sub>IN</sub>			2		pF
<b>DIGITAL OUTPUT (DOUT)</b>						
Output-High Voltage	V <sub>OH</sub>	I <sub>SOURCE</sub> = 200μA	0.85 x			V
Output-Low Voltage	V <sub>OL</sub>	I <sub>SINK</sub> = 200μA			0.15 x	V
High-Impedance Leakage Current	I <sub>OL</sub>				±1.0	μA
High-Impedance Output Capacitance	C <sub>OUT</sub>			4		pF



# MAX11102/03/05/06/10/11/15/16/17

## 2Msps/3Msps, Low-Power, Serial 12-/10-/8-Bit ADCs

### ELECTRICAL CHARACTERISTICS (MAX11106) (continued)

(V<sub>DD</sub> = 2.2V to 3.6V, V<sub>REF</sub> = V<sub>DD</sub>, V<sub>OVDD</sub> = V<sub>DD</sub>, f<sub>SCLK</sub> = 48MHz, 50% duty cycle, 3Msps; C<sub>DOUT</sub> = 10pF, T<sub>A</sub> = -40°C to +125°C, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>POWER SUPPLY</b>						
Positive Supply Voltage	V <sub>DD</sub>		2.2		3.6	V
Digital I/O Supply Voltage	V <sub>OVDD</sub>		1.5		V <sub>DD</sub>	V
Positive Supply Current (Full-Power Mode)	I <sub>VDD</sub>	V <sub>AIN</sub> = V <sub>GND</sub>			3.3	mA
	I <sub>OVDD</sub>	V <sub>AIN</sub> = V <sub>GND</sub>			0.33	
Positive Supply Current (Full-Power Mode), No Clock	I <sub>VDD</sub>			1.98		mA
Power-Down Current	I <sub>PD</sub>	Leakage only		1.3	10	μA
Line Rejection		V <sub>DD</sub> = +2.2V to +3.6V, V <sub>REF</sub> = 2.2V		0.17		LSB/V
<b>TIMING CHARACTERISTICS (Note 1)</b>						
Quiet Time	t <sub>Q</sub>	(Note 2)	4			ns
CS Pulse Width	t <sub>1</sub>	(Note 2)	10			ns
CS Fall to SCLK Setup	t <sub>2</sub>	(Note 2)	5			ns
CS Falling Until DOUT High-Impedance Disabled	t <sub>3</sub>	(Note 2)	1			ns
Data Access Time After SCLK Falling Edge (Figure 2)	t <sub>4</sub>	V <sub>OVDD</sub> = 2.2V - 3.6V			15	ns
		V <sub>OVDD</sub> = 1.5V - 2.2V			16.5	
SCLK Pulse Width Low	t <sub>5</sub>	Percentage of clock period (Note 2)	40		60	%
SCLK Pulse Width High	t <sub>6</sub>	Percentage of clock period (Note 2)	40		60	%
Data Hold Time From SCLK Falling Edge	t <sub>7</sub>	Figure 3	5			ns
SCLK Falling Until DOUT High-Impedance	t <sub>8</sub>	Figure 4 (Note 2)	2.5		14	ns
Power-Up Time		Conversion cycle (Note 2)			1	Cycle

### ELECTRICAL CHARACTERISTICS (MAX11110/MAX11117)

(V<sub>DD</sub> = 2.2V to 3.6V. MAX11110: f<sub>SCLK</sub> = 32MHz, 50% duty cycle, 2Msps. MAX11117: f<sub>SCLK</sub> = 48MHz, 50% duty cycle, 3Msps. C<sub>DOUT</sub> = 10pF, T<sub>A</sub> = -40°C to +125°C, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>DC ACCURACY</b>						
Resolution			10			Bits
Integral Nonlinearity	INL				±1	LSB
Differential Nonlinearity	DNL	No missing codes			±1	LSB
Offset Error	OE	MAX11117		±0.5	±1.65	LSB
		MAX11110		±0.3	±1.2	
Gain Error	GE	Excluding offset and reference errors, MAX11117		±0.7	±1.4	LSB
		Excluding offset and reference errors, MAX11110		±0.15	±1	
Total Unadjusted Error	TUE			±1		LSB

# MAX1102/03/05/06/10/11/15/16/17

## 2Msps/3Msps, Low-Power, Serial 12-/10-/8-Bit ADCs

### ELECTRICAL CHARACTERISTICS (MAX1110/MAX1117) (continued)

(V<sub>DD</sub> = 2.2V to 3.6V. MAX11110: f<sub>SCLK</sub> = 32MHz, 50% duty cycle, 2Msps. MAX11117: f<sub>SCLK</sub> = 48MHz, 50% duty cycle, 3Msps. C<sub>DOUT</sub> = 10pF, T<sub>A</sub> = -40°C to +125°C, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>DYNAMIC PERFORMANCE (MAX11117: f<sub>AIN</sub> = 1MHz, MAX11110: f<sub>AIN</sub> = 0.5MHz)</b>						
Signal-to-Noise and Distortion	SINAD	MAX11117	59	61.5		dB
		MAX11110	60.5	61.5		
Signal-to-Noise Ratio	SNR	MAX11117	59	61.5		dB
		MAX11110	60.5	61.5		
Total Harmonic Distortion	THD	MAX11117		-85	-74	dB
		MAX11110		-85	-73	
Spurious-Free Dynamic Range	SFDR	MAX11117	75			dB
		MAX11110	75			
Intermodulation Distortion	IMD	MAX11117: f <sub>1</sub> = 1.0003MHz, f <sub>2</sub> = 0.9995MHz MAX11110: f <sub>1</sub> = 500.15kHz, f <sub>2</sub> = 499.56kHz		-82		dB
Full-Power Bandwidth		-3dB point		40		MHz
Full-Linear Bandwidth		SINAD > 60dB		2.5		MHz
Small-Signal Bandwidth				45		MHz
<b>CONVERSION RATE</b>						
Throughput		MAX11117	0.03		3	Msps
		MAX11110	0.02		2	
Conversion Time		MAX11117	260			ns
		MAX11110	391			
Acquisition Time	t <sub>ACQ</sub>		52			ns
Aperture Delay		From $\overline{CS}$ falling edge		4		ns
Aperture Jitter				15		ps
Serial Clock Frequency	f <sub>CLK</sub>	MAX11117	0.48		48	MHz
		MAX11110	0.32		32	
<b>ANALOG INPUT (AIN)</b>						
Input Voltage Range	V <sub>AIN</sub>		0		V <sub>DD</sub>	V
Input Leakage Current	I <sub>ILA</sub>			0.002	±1	μA
Input Capacitance	C <sub>AIN</sub>	Track		20		pF
		Hold		4		
<b>DIGITAL INPUTS (SCLK, <math>\overline{CS}</math>, CHSEL)</b>						
Digital Input-High Voltage	V <sub>IH</sub>		0.75 x V <sub>DD</sub>			V
Digital Input-Low Voltage	V <sub>IL</sub>			0.25 x V <sub>DD</sub>		V
Digital Input Hysteresis	V <sub>HYST</sub>			0.15 x V <sub>DD</sub>		V
Digital Input Leakage Current	I <sub>IL</sub>	Inputs at GND or V <sub>DD</sub>		0.001	±1	μA
Digital Input Capacitance	C <sub>IN</sub>			2		pF

# MAX11102/03/05/06/10/11/15/16/17

## 2Msps/3Msps, Low-Power, Serial 12-/10-/8-Bit ADCs

### ELECTRICAL CHARACTERISTICS (MAX11110/MAX11117) (continued)

(V<sub>DD</sub> = 2.2V to 3.6V. MAX11110: f<sub>SCLK</sub> = 32MHz, 50% duty cycle, 2Msps. MAX11117: f<sub>SCLK</sub> = 48MHz, 50% duty cycle, 3Msps. C<sub>DOUT</sub> = 10pF, T<sub>A</sub> = -40°C to +125°C, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>DIGITAL OUTPUT (DOUT)</b>						
Output-High Voltage	V <sub>OH</sub>	I <sub>SOURCE</sub> = 200μA	0.85 x V <sub>DD</sub>			V
Output-Low Voltage	V <sub>OL</sub>	I <sub>SINK</sub> = 200μA			0.15 x V <sub>DD</sub>	V
High-Impedance Leakage Current	I <sub>OL</sub>				±1.0	μA
High-Impedance Output Capacitance	C <sub>OUT</sub>			4		pF
<b>POWER SUPPLY</b>						
Positive Supply Voltage	V <sub>DD</sub>		2.2		3.6	V
Positive Supply Current (Full-Power Mode)	I <sub>VDD</sub>	MAX11117, V <sub>AIN</sub> = V <sub>GND</sub>			3.55	mA
		MAX11110, V <sub>AIN</sub> = V <sub>GND</sub>			2.6	
Positive Supply Current (Full-Power Mode), No Clock	I <sub>VDD</sub>	MAX11117		1.98		mA
		MAX11110		1.48		
Power-Down Current	I <sub>PD</sub>	Leakage only		1.3	10	μA
Line Rejection		V <sub>DD</sub> = +2.2V to +3.6V		0.17		LSB/V
<b>TIMING CHARACTERISTICS (Note 1)</b>						
Quiet Time	t <sub>Q</sub>	(Note 2)	4			ns
$\overline{CS}$ Pulse Width	t <sub>1</sub>	(Note 2)	10			ns
$\overline{CS}$ Fall to SCLK Setup	t <sub>2</sub>	(Note 2)	5			ns
$\overline{CS}$ Falling Until DOUT High-Impedance Disabled	t <sub>3</sub>	(Note 2)	1			ns
Data Access Time After SCLK Falling Edge	t <sub>4</sub>	Figure 2, V <sub>DD</sub> = +2.2V to +3.6V			15	ns
SCLK Pulse Width Low	t <sub>5</sub>	Percentage of clock period (Note 2)	40		60	%
SCLK Pulse Width High	t <sub>6</sub>	Percentage of clock period (Note 2)	40		60	%
Data Hold Time From SCLK Falling Edge	t <sub>7</sub>	Figure 3	5			ns
SCLK Falling Until DOUT High-Impedance	t <sub>8</sub>	Figure 4 (Note 2)	2.5		14	ns
Power-Up Time		Conversion cycle (Note 2)			1	Cycle

# MAX11102/03/05/06/10/11/15/16/17

## 2Msps/3Msps, Low-Power, Serial 12-/10-/8-Bit ADCs

### ELECTRICAL CHARACTERISTICS (MAX11111)

( $V_{DD} = 2.2V$  to  $3.6V$ ,  $V_{REF} = V_{DD}$ ,  $V_{OVDD} = V_{DD}$ ,  $f_{SCLK} = 48MHz$ , 50% duty cycle, 3Msps,  $C_{DOUT} = 10pF$ ,  $T_A = -40^{\circ}C$  to  $+125^{\circ}C$ , unless otherwise noted. Typical values are at  $T_A = +25^{\circ}C$ .)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>DC ACCURACY</b>						
Resolution			8			Bits
Integral Nonlinearity	INL				$\pm 0.15$	LSB
Differential Nonlinearity	DNL	No missing codes			$\pm 0.15$	LSB
Offset Error	OE			0.45	$\pm 0.7$	LSB
Gain Error	GE	Excluding offset and reference errors		0	$\pm 0.2$	LSB
Total Unadjusted Error	TUE			0.5		LSB
Channel-to-Channel Offset Matching				0.01		LSB
Channel-to-Channel Gain Matching				0.01		LSB
<b>DYNAMIC PERFORMANCE</b>						
Signal-to-Noise and Distortion	SINAD	$f_{AIN\_} = 1MHz$	49	49.8		dB
Signal-to-Noise Ratio	SNR	$f_{AIN\_} = 1MHz$	49	49.8		dB
Total Harmonic Distortion	THD	$f_{AIN\_} = 1MHz$		-75	-67	dB
Spurious-Free Dynamic Range	SFDR	$f_{AIN\_} = 1MHz$	63	67		dB
Intermodulation Distortion	IMD	$f_1 = 1.0003MHz$ , $f_2 = 0.99955MHz$		-65		dB
Full-Power Bandwidth		-3dB point		40		MHz
Full-Linear Bandwidth		SINAD > 49dB		2.5		MHz
Small-Signal Bandwidth				45		MHz
Crosstalk				-90		dB
<b>CONVERSION RATE</b>						
Throughput			0.03		3	Msps
Conversion Time			260			ns
Acquisition Time	$t_{ACQ}$		52			ns
Aperture Delay		From CS falling edge		4		ns
Aperture Jitter				15		ps
Serial-Clock Frequency	$f_{CLK}$		0.48		48	MHz
<b>ANALOG INPUT (AIN1, AIN2)</b>						
Input Voltage Range	$V_{AIN\_}$		0		$V_{REF}$	V
Input Leakage Current	$I_{ILA}$			0.002	$\pm 1$	$\mu A$
Input Capacitance	$C_{AIN\_}$	Track		20		pF
		Hold		4		
<b>EXTERNAL REFERENCE INPUT (REF)</b>						
Reference Input Voltage Range	$V_{REF}$		1		$V_{DD} + 0.05$	V
Reference Input Leakage Current	$I_{ILR}$	Conversion stopped		0.005	$\pm 1$	$\mu A$
Reference Input Capacitance	$C_{REF}$			5		pF

# MAX11102/03/05/06/10/11/15/16/17

## 2Msps/3Msps, Low-Power, Serial 12-/10-/8-Bit ADCs

### ELECTRICAL CHARACTERISTICS (MAX11111) (continued)

( $V_{DD} = 2.2V$  to  $3.6V$ ,  $V_{REF} = V_{DD}$ ,  $V_{OVDD} = V_{DD}$ ,  $f_{SCLK} = 48MHz$ , 50% duty cycle, 3Msps,  $C_{DOUT} = 10pF$ ,  $T_A = -40^{\circ}C$  to  $+125^{\circ}C$ , unless otherwise noted. Typical values are at  $T_A = +25^{\circ}C$ .)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>DIGITAL INPUTS (SCLK, CS)</b>						
Digital Input High Voltage	$V_{IH}$		$0.75 \times V_{OVDD}$			V
Digital Input Low Voltage	$V_{IL}$				$0.25 \times V_{OVDD}$	V
Digital Input Hysteresis	$V_{HYST}$			$0.15 \times V_{OVDD}$		V
Digital Input Leakage Current	$I_{IL}$	Inputs at GND or $V_{DD}$		0.001	$\pm 1$	$\mu A$
Digital Input Capacitance	$C_{IN}$			2		pF
<b>DIGITAL OUTPUT (DOUT)</b>						
Output High Voltage	$V_{OH}$	$I_{SOURCE} = 200\mu A$ (Note 2)	$0.85 \times V_{OVDD}$			V
Output Low Voltage	$V_{OL}$	$I_{SINK} = 200\mu A$ (Note 2)			$0.15 \times V_{OVDD}$	V
High-Impedance Leakage Current	$I_{OL}$				$\pm 1.0$	$\mu A$
High-Impedance Output Capacitance	$C_{OUT}$			4		pF
<b>POWER SUPPLY</b>						
Positive Supply Voltage	$V_{DD}$		2.2		3.6	V
Digital I/O Supply Voltage	$V_{OVDD}$		1.5		$V_{DD}$	V
Positive Supply Current (Full-Power Mode)	$I_{VDD}$	$V_{AIN} = V_{GND}$			3.3	mA
	$I_{OVDD}$	$V_{AIN} = V_{GND}$			0.33	
Positive Supply Current (Full-Power Mode), No Clock	$I_{VDD}$			1.98		mA
Power-Down Current	$I_{PD}$	Leakage only		1.3	10	$\mu A$
Line Rejection		$V_{DD} = +2.2V$ to $+3.6V$ , $V_{REF} = 2.2V$		0.17		LSB/V
<b>TIMING CHARACTERISTICS (Note 1)</b>						
Quiet Time	$t_Q$	(Note 2)	4			ns
CS Pulse Width	$t_1$	(Note 2)	10			ns
CS Fall to SCLK Setup	$t_2$	(Note 2)	5			ns
CS Falling Until DOUT High-Impedance Disabled	$t_3$	(Note 2)	1			ns
Data Access Time After SCLK Falling Edge (Figure 2)	$t_4$	$V_{OVDD} = 2.2V - 3.6V$			15	ns
		$V_{OVDD} = 1.5V - 2.2V$			16.5	
SCLK Pulse Width Low	$t_5$	Percentage of clock period (Note 2)	40		60	%
SCLK Pulse Width High	$t_6$	Percentage of clock period (Note 2)	40		60	%
Data Hold Time From SCLK Falling Edge	$t_7$	Figure 3	5			ns
SCLK Falling Until DOUT High-Impedance	$t_8$	Figure 4 (Note 2)	2.5		14	ns
Power-Up Time		Conversion cycle (Note 2)			1	Cycle

# MAX11102/03/05/06/10/11/15/16/17

## 2Msps/3Msps, Low-Power, Serial 12-/10-/8-Bit ADCs

### ELECTRICAL CHARACTERISTICS (MAX11115/MAX11116)

(V<sub>DD</sub> = 2.2V to 3.6V. MAX11115: f<sub>SCLK</sub> = 32MHz, 50% duty cycle, 2Msps. MAX11116: f<sub>SCLK</sub> = 48MHz, 50% duty cycle, 3Msps. C<sub>DOUT</sub> = 10pF, T<sub>A</sub> = -40°C to +125°C, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>DC ACCURACY</b>						
Resolution			8			Bits
Integral Nonlinearity	INL				±0.25	LSB
Differential Nonlinearity	DNL	No missing codes			±0.25	LSB
Offset Error	OE			±0.45	±0.75	LSB
Gain Error	GE	Excluding offset and reference errors		±0.04	±0.5	LSB
Total Unadjusted Error	TUE			±0.75		LSB
<b>DYNAMIC PERFORMANCE (MAX11116: f<sub>AIN</sub> = 1MHz MAX11115: f<sub>AIN</sub> = 500kHz)</b>						
Signal-to-Noise and Distortion	SINAD	MAX11116	49	49.5		dB
		MAX11115	49	49.5		
Signal-to-Noise Ratio	SNR	MAX11116	49	49.5		dB
		MAX11115	49	49.5		
Total Harmonic Distortion	THD	MAX11116		-70	-66	dB
		MAX11115		-75	-67	
Spurious-Free Dynamic Range	SFDR	MAX11116	63	66		dB
		MAX11115	63	66		
Intermodulation Distortion	IMD	MAX11116: f <sub>1</sub> = 1.0003MHz, f <sub>2</sub> = 0.99955MHz MAX11115: f <sub>1</sub> = 500.15kHz, f <sub>2</sub> = 499.56kHz		-65		dB
Full-Power Bandwidth		-3dB point		40		MHz
Full-Linear Bandwidth		SINAD > 49dB		2.5		MHz
Small-Signal Bandwidth				45		MHz
<b>CONVERSION RATE</b>						
Throughput		MAX11116	0.03		3	Msps
		MAX11115	0.02		2	
Conversion Time		MAX11116	260			ns
		MAX11115	391			
Acquisition Time	t <sub>ACQ</sub>		52			ns
Aperture Delay		From $\overline{CS}$ falling edge		4		ns
Aperture Jitter				15		ps
Serial-Clock Frequency	f <sub>CLK</sub>	MAX11116	0.48		48	MHz
		MAX11115	0.32		32	
<b>ANALOG INPUT (AIN)</b>						
Input Voltage Range	V <sub>AIN</sub>		0		V <sub>DD</sub>	V
Input Leakage Current	I <sub>ILA</sub>			0.002	±1	μA
Input Capacitance	C <sub>AIN</sub>	Track		20		pF
		Hold		4		
<b>DIGITAL INPUTS (SCLK, <math>\overline{CS}</math>)</b>						
Digital Input High Voltage	V <sub>IH</sub>		0.75 x		V <sub>DD</sub>	V



# MAX11102/03/05/06/10/11/15/16/17

## 2Msps/3Msps, Low-Power, Serial 12-/10-/8-Bit ADCs

### ELECTRICAL CHARACTERISTICS (MAX11115/MAX11116) (continued)

(V<sub>DD</sub> = 2.2V to 3.6V. MAX11115: f<sub>SCLK</sub> = 32MHz, 50% duty cycle, 2Msps. MAX11116: f<sub>SCLK</sub> = 48MHz, 50% duty cycle, 3Msps. C<sub>DOUT</sub> = 10pF, T<sub>A</sub> = -40°C to +125°C, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Digital Input Low Voltage	V <sub>IL</sub>				0.25 × V <sub>DD</sub>	V
Digital Input Hysteresis	V <sub>HYST</sub>			0.15 V <sub>DD</sub>		V
Digital Input Leakage Current	I <sub>IL</sub>	Inputs at GND or V <sub>DD</sub>		0.001	±1	μA
Digital Input Capacitance	C <sub>IN</sub>			2		pF
<b>DIGITAL OUTPUT (DOUT)</b>						
Output High Voltage	V <sub>OH</sub>	I <sub>SOURCE</sub> = 200μA	0.85 × V <sub>DD</sub>			V
Output Low Voltage	V <sub>OL</sub>	I <sub>SINK</sub> = 200μA			0.15 × V <sub>DD</sub>	V
High-Impedance Leakage Current	I <sub>OL</sub>				±1.0	μA
High-Impedance Output Capacitance	C <sub>OUT</sub>			4		pF
<b>POWER SUPPLY</b>						
Positive Supply Voltage	V <sub>DD</sub>		2.2		3.6	V
Positive Supply Current (Full-Power Mode)	I <sub>VDD</sub>	MAX11116, V <sub>AIN</sub> = V <sub>GND</sub>			3.55	mA
		MAX11115, V <sub>AIN</sub> = V <sub>GND</sub>			2.6	
Positive Supply Current (Full-Power Mode), No Clock	I <sub>VDD</sub>	MAX11116		1.98		mA
		MAX11115		1.48		
Power-Down Current	I <sub>PD</sub>	Leakage only		1.3	10	μA
Line Rejection		V <sub>DD</sub> = +2.2V to +3.6V		0.17		LSB/V
<b>TIMING CHARACTERISTICS (Note 1)</b>						
Quiet Time	t <sub>Q</sub>	(Note 2)	4			ns
CS Pulse Width	t <sub>1</sub>	(Note 2)	10			ns
CS Fall to SCLK Setup	t <sub>2</sub>	(Note 2)	5			ns
CS Falling Until DOUT High-Impedance Disabled	t <sub>3</sub>	(Note 2)	1			ns
Data Access Time After SCLK Falling Edge	t <sub>4</sub>	Figure 2, V <sub>DD</sub> = +2.2V to +3.6V			15	ns
SCLK Pulse Width Low	t <sub>5</sub>	Percentage of clock period (Note 2)	40		60	%
SCLK Pulse Width High	t <sub>6</sub>	Percentage of clock period (Note 2)	40		60	%
Data Hold Time From SCLK Falling Edge	t <sub>7</sub>	Figure 3	5			ns
SCLK Falling Until DOUT High-Impedance	t <sub>8</sub>	Figure 4 (Note 2)	2.5		14	ns
Power-Up Time		Conversion cycle (Note 2)			1	Cycle

**Note 1:** All timing specifications given are with a 10pF capacitor.

**Note 2:** Guaranteed by design in characterization; not production tested.

# MAX11102/03/05/06/10/11/15/16/17

## 2MSPS/3MSPS, Low-Power, Serial 12-/10-/8-Bit ADCs

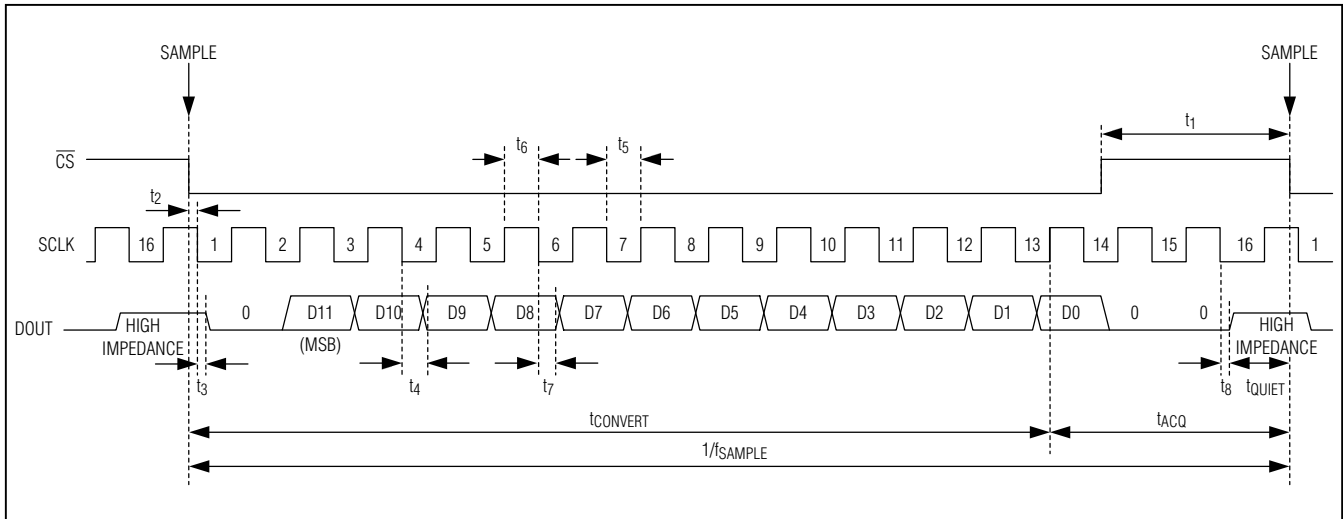


Figure 1. Interface Signals for Maximum Throughput, 12-Bit Devices

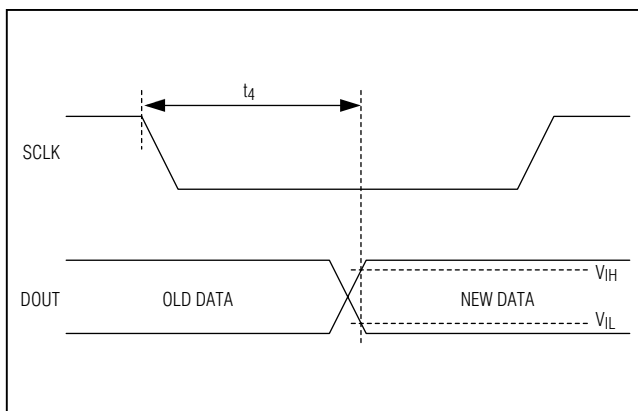


Figure 2. Setup Time After SCLK Falling Edge

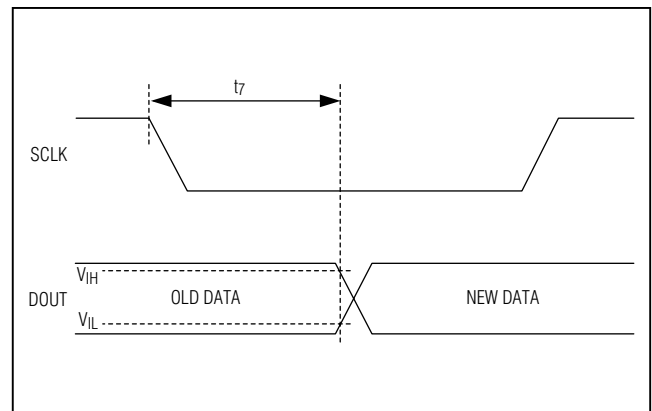


Figure 3. Hold Time After SCLK Falling Edge

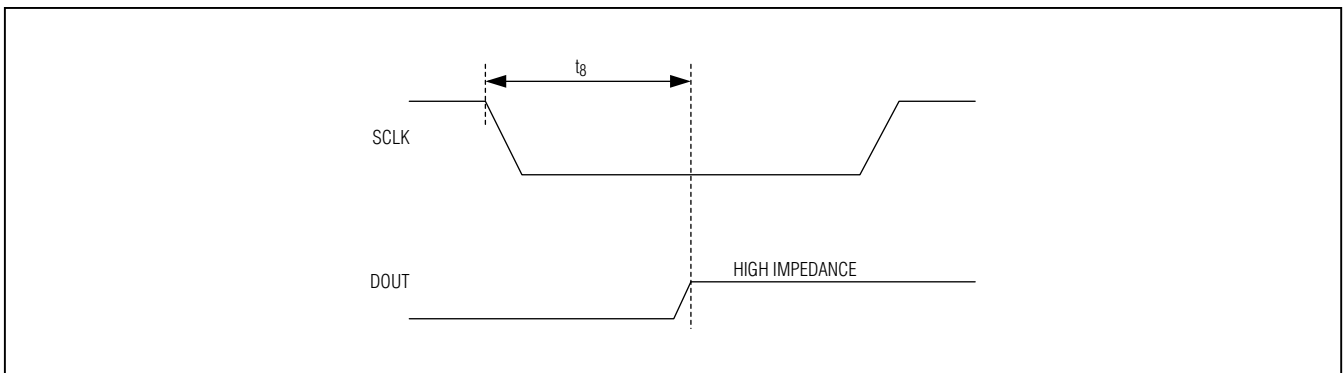


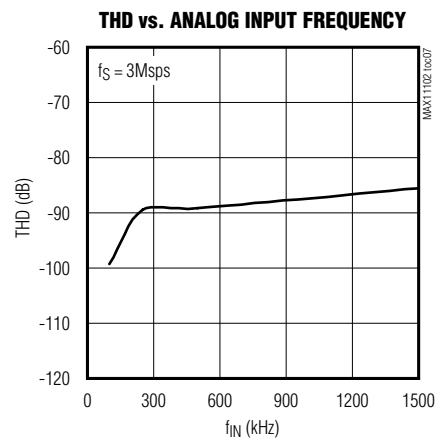
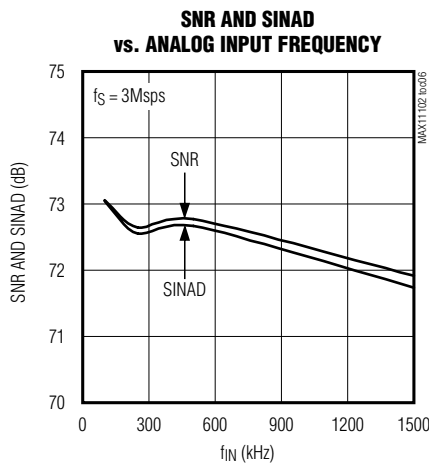
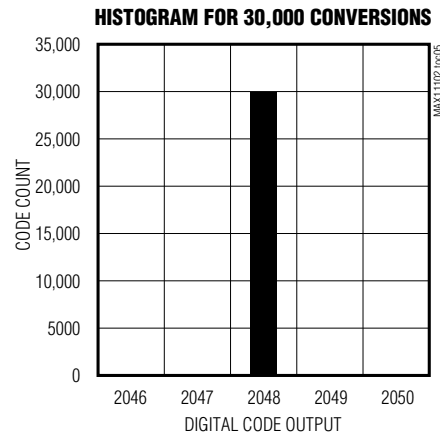
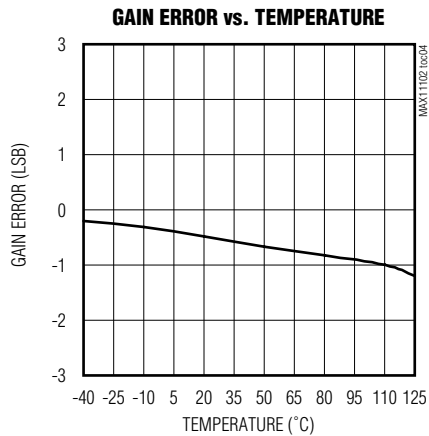
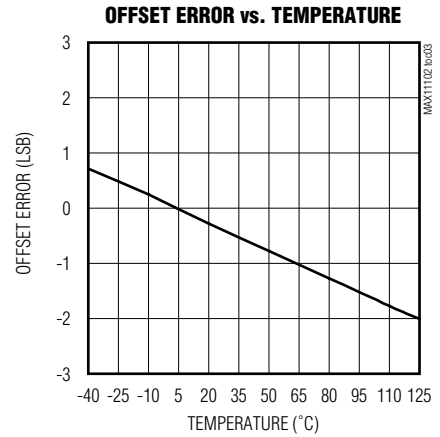
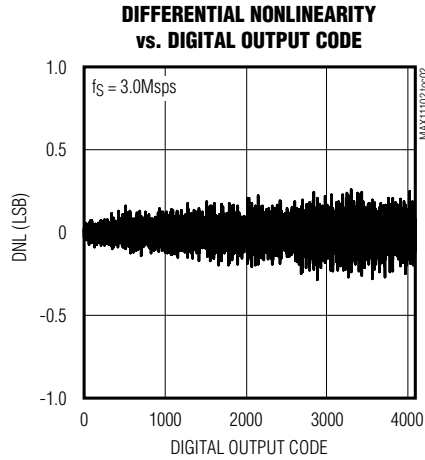
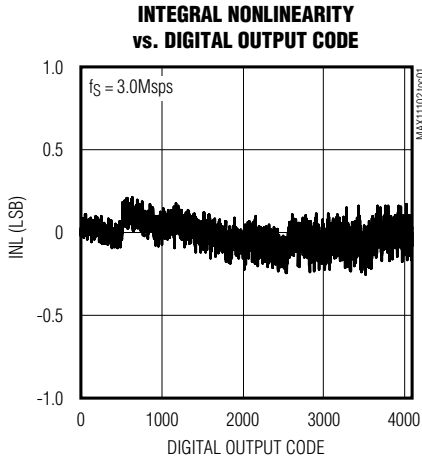
Figure 4. SCLK Falling Edge DOUT Three-State

# MAX1102/03/05/06/10/11/15/16/17

## 2MSPS/3MSPS, Low-Power, Serial 12-/10-/8-Bit ADCs

### $\mu$ MAX Typical Operating Characteristics

(MAX11103AUB+,  $T_A = +25^\circ\text{C}$ , unless otherwise noted.)

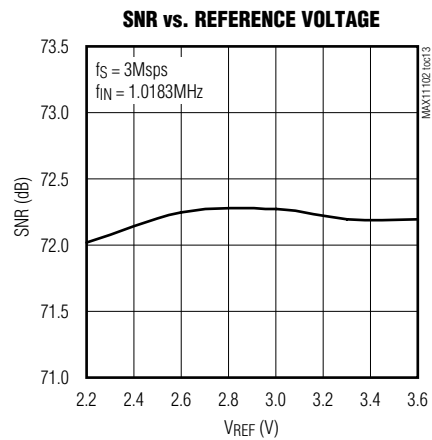
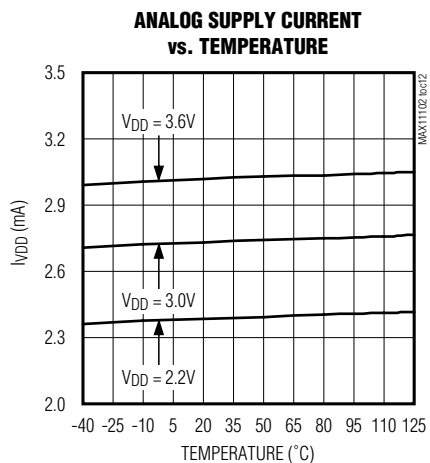
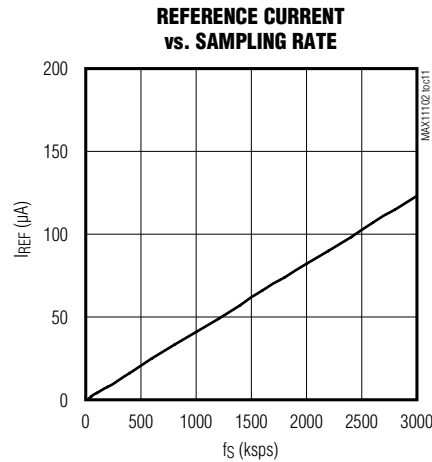
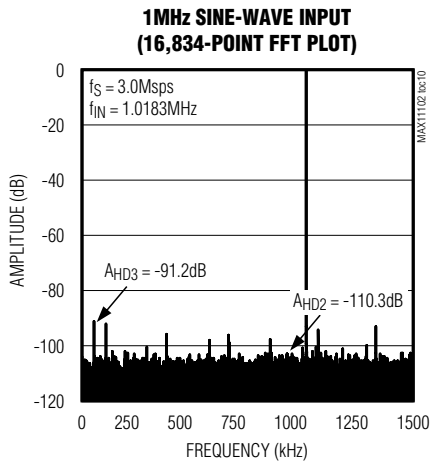
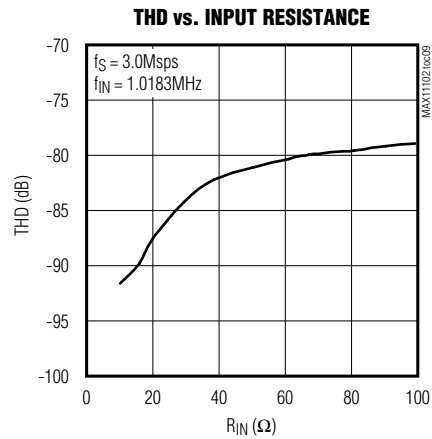
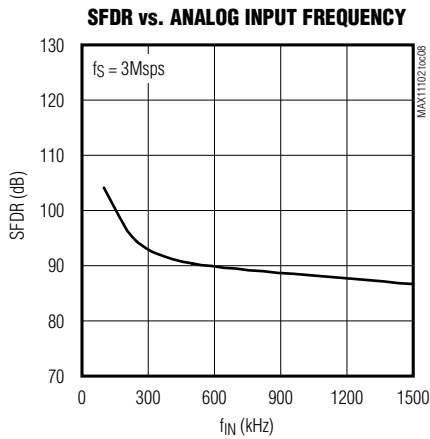


# MAX11102/03/05/06/10/11/15/16/17

## 2Msps/3Msps, Low-Power, Serial 12-/10-/8-Bit ADCs

### ***μMAX Typical Operating Characteristics (continued)***

(MAX11103AUB+,  $T_A = +25^\circ\text{C}$ , unless otherwise noted.)

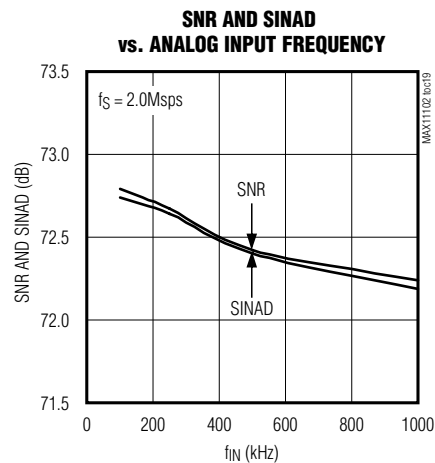
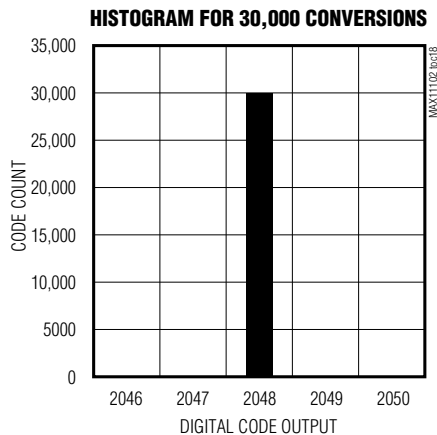
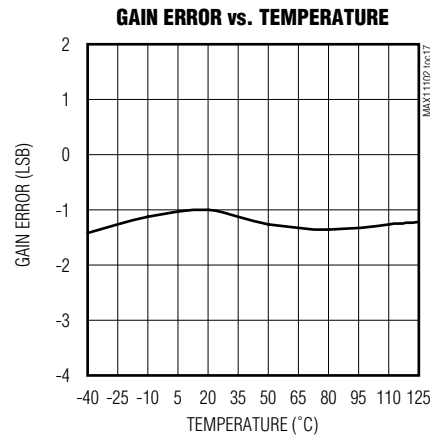
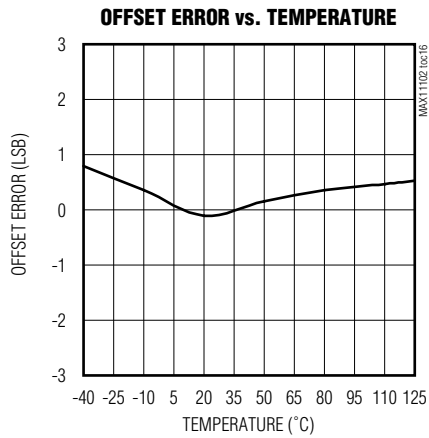
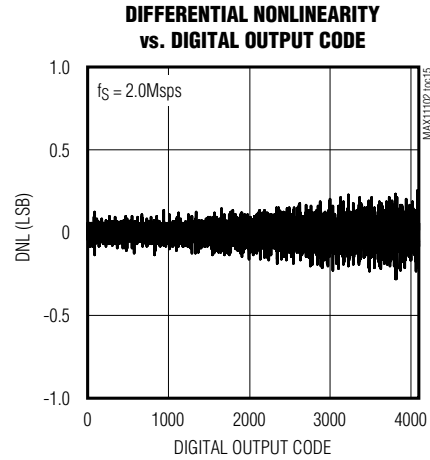
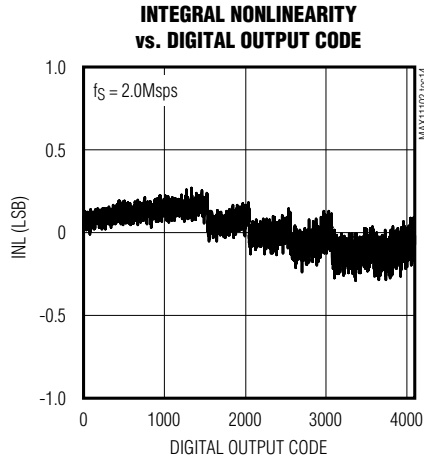


# MAX1102/03/05/06/10/11/15/16/17

## 2MSPS/3MSPS, Low-Power, Serial 12-/10-/8-Bit ADCs

### SOT Typical Operating Characteristics

(MAX1105AUB+,  $T_A = +25^\circ\text{C}$ , unless otherwise noted.)

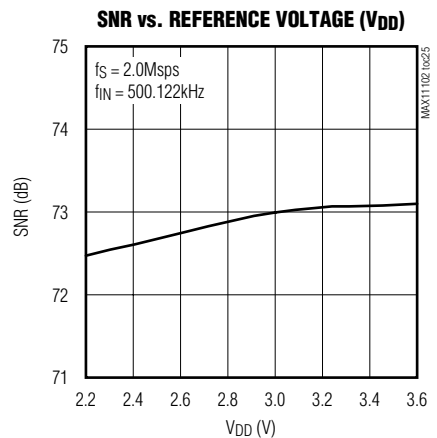
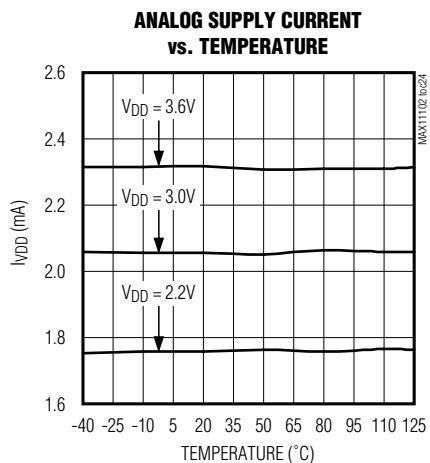
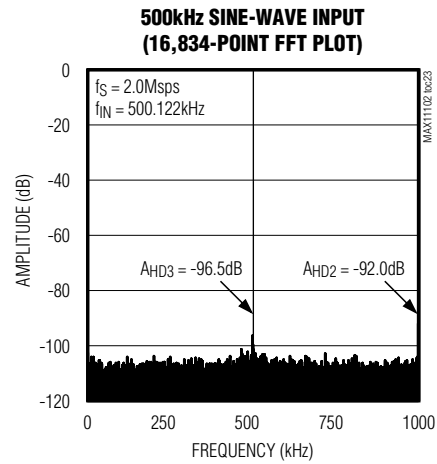
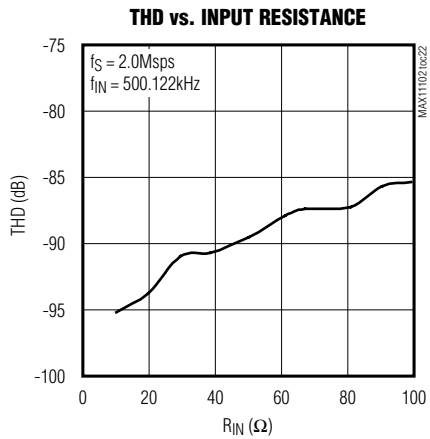
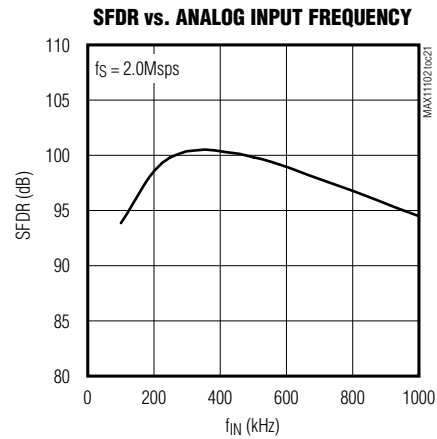
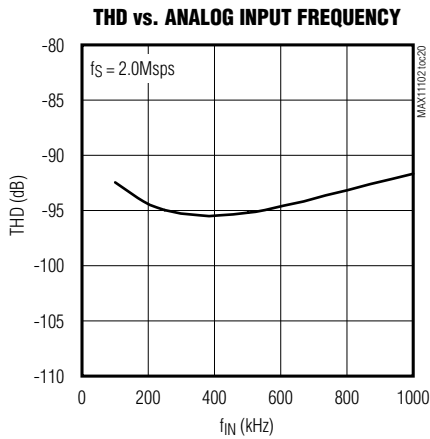


# MAX1102/03/05/06/10/11/15/16/17

## 2MSPS/3MSPS, Low-Power, Serial 12-/10-/8-Bit ADCs

### SOT Typical Operating Characteristics (continued)

(MAX1105AUB+,  $T_A = +25^\circ\text{C}$ , unless otherwise noted.)

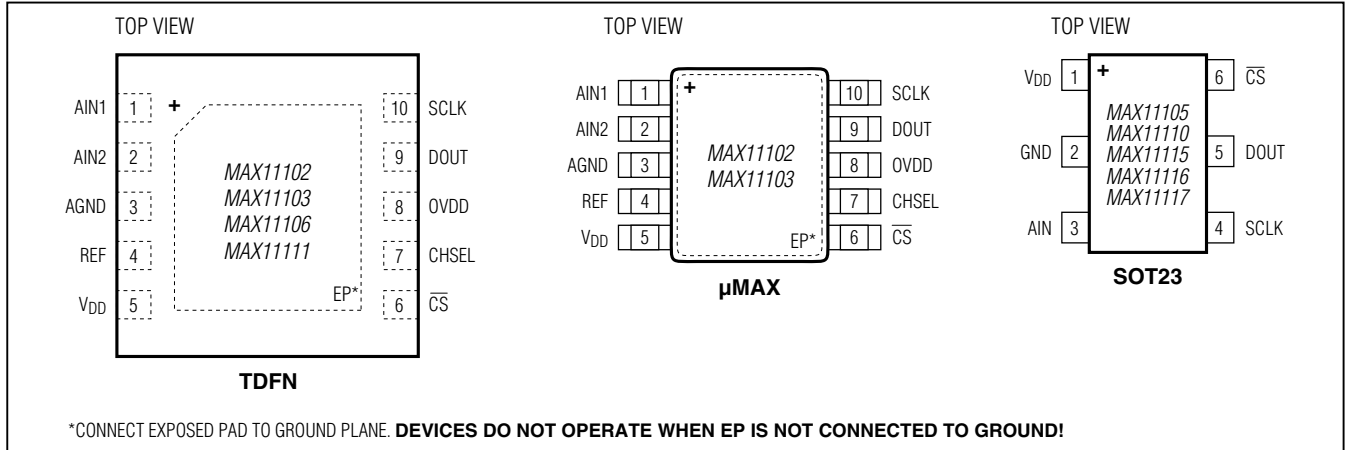




# MAX11102/03/05/06/10/11/15/16/17

## 2MSPS/3MSPS, Low-Power, Serial 12-/10-/8-Bit ADCs

### Pin Configurations



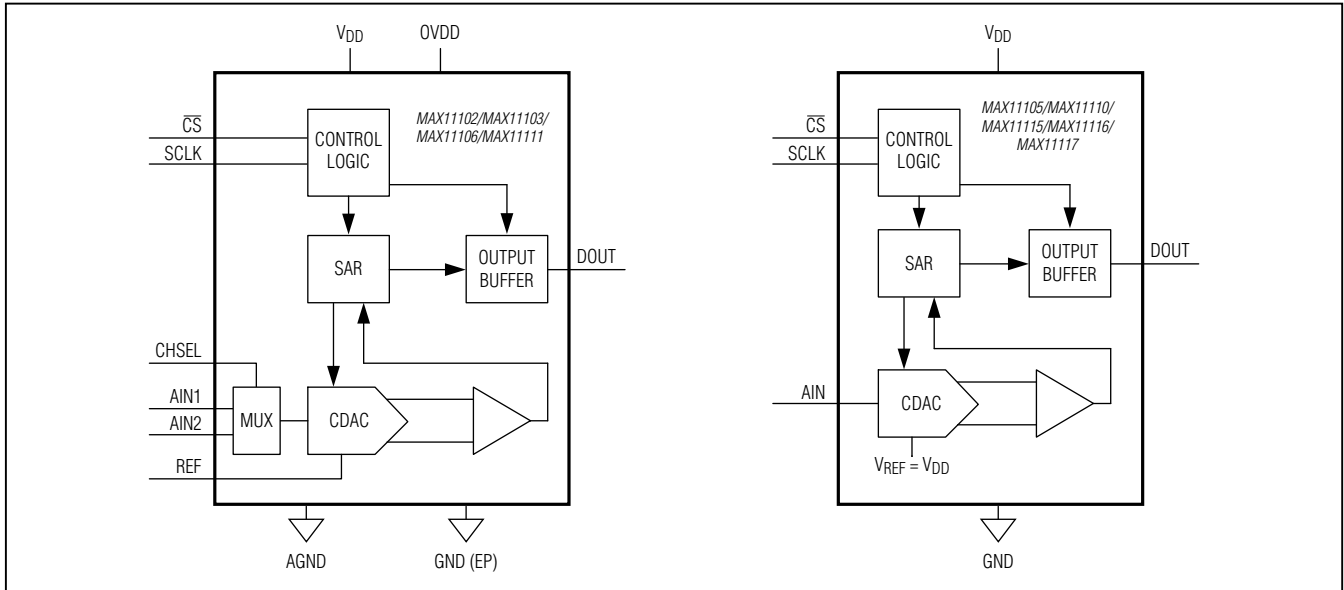
### Pin Description

PIN			NAME	FUNCTION
TDFN	μMAX	SOT23		
1	1	—	AIN1	Analog Input Channel 1. Single-ended analog input with respect to AGND with range of 0V to VREF.
2	2	—	AIN2	Analog Input Channel 2. Single-ended analog input with respect to AGND with range of 0V to VREF.
—	—	3	AIN	Analog Input Channel. Single-ended analog input with respect to GND with range of 0V to VDD.
—	—	2	GND	Ground. Connect GND to the GND ground plane.
3	3	—	AGND	Analog Ground. Connect AGND directly the GND ground plane.
4	4	—	REF	External Reference Input. REF defines the signal range of the input signal AIN1/AIN2: 0V to VREF. The range of VREF is 1V to VDD. Bypass REF to AGND with 10μF    0.1μF capacitor.
5	5	1	VDD	Positive Supply Voltage. Bypass VDD with a 10μF    0.1μF capacitor to GND. VDD range is 2.2V to 3.6V. For the SOT23 package, VDD also defines the signal range of the input signal AIN: 0V to VDD.
6	6	6	$\overline{CS}$	Active-Low Chip-Select Input. The falling edge of $\overline{CS}$ samples the analog input signal, starts a conversion, and frames the serial data transfer.
7	7	—	CHSEL	Channel Select. Set CHSEL high to select AIN2 for conversion. Set CHSEL low to select AIN1 for conversion.
8	8	—	OVDD	Digital Interface Supply for SCLK, $\overline{CS}$ , DOUT, and CHSEL. The OVDD range is 1.5V to VDD. Bypass OVDD with a 10μF    0.1μF capacitor to GND.
9	9	5	DOUT	Three-State Serial Data Output. ADC conversion results are clocked out on the falling edge of SCLK, MSB first. See Figure 1.
10	10	4	SCLK	Serial Clock Input. SCLK drives the conversion process. DOUT is updated on the falling edge of SCLK. See Figures 2 and 3.
—	—	EP	GND	Exposed Pad (TDFN and μMAX only). Connect EP directly to a solid ground plane. <b>Devices do not operate unless EP is connected to ground!</b>

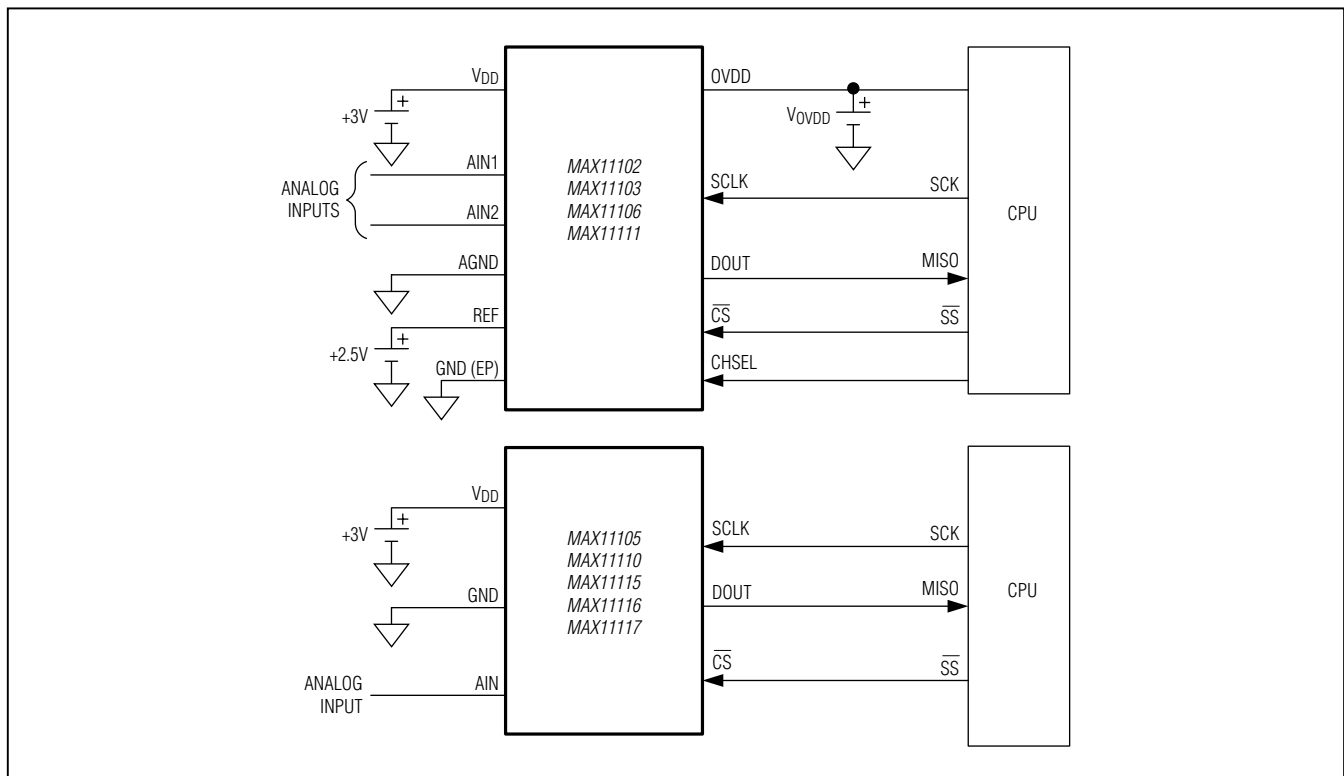
# MAX1102/03/05/06/10/11/15/16/17

## 2MSPS/3MSPS, Low-Power, Serial 12-/10-/8-Bit ADCs

### Functional Diagrams



### Typical Operating Circuit



# MAX11102/03/05/06/10/11/15/16/17

## 2MSPS/3MSPS, Low-Power, Serial 12-/10-/8-Bit ADCs

### Detailed Description

The MAX11102/MAX11103/MAX11105/MAX11106/MAX11110/MAX11111/MAX11115/MAX11116/MAX11117 are fast, 12-/10-/8-bit, low-power, single-supply ADCs. The devices operate from a 2.2V to 3.6V supply and consume only 8.3mW ( $V_{DD} = 3V$ )/5.2mW ( $V_{DD} = 2.2V$ ) at 3MSPS and 6.2mW ( $V_{DD} = 3V$ )/3.7mW ( $V_{DD} = 2.2V$ ) at 2MSPS. The 3MSPS devices are capable of sampling at full rate when driven by a 48MHz clock and the 2MSPS devices can sample at full rate when driven by a 32MHz clock. The dual-channel devices provide a separate digital supply input (OVDD) to power the digital interface enabling communication with 1.5V, 1.8V, 2.5V, or 3V digital systems.

The conversion result appears at DOUT, MSB first, with a leading zero followed by the 12-bit, 10-bit, or 8-bit result. A 12-bit result is followed by two trailing zeros, a 10-bit result is followed by four trailing zeros, and an 8-bit result is followed by six trailing zeros. See Figures 1 and 5.

The dual-channel devices feature a dedicated reference input (REF). The input signal range for AIN1/AIN2 is defined as 0V to  $V_{REF}$  with respect to AGND. The single-channel devices use  $V_{DD}$  as the reference. The input signal range of AIN is defined as 0V to  $V_{DD}$  with respect to GND.

These ADCs include a power-down feature allowing minimized power consumption at 2.5 $\mu$ A/kSPS for lower throughput rates. The wake-up and power-down feature is controlled by using the SPI interface as described in the *Operating Modes* section.

### Serial Interface

The devices feature a 3-wire serial interface that directly connects to SPI, QSPI, and MICROWIRE devices without external logic. Figures 1 and 5 show the interface signals for a single conversion frame to achieve maximum throughput.

The falling edge of  $\overline{CS}$  defines the sampling instant. Once  $\overline{CS}$  transitions low, the external clock signal (SCLK) controls the conversion.

The SAR core successively extracts binary-weighted bits in every clock cycle. The MSB appears on the data bus during the 2nd clock cycle with a delay outlined in the timing specifications. All extracted data bits appear successively on the data bus with the LSB appearing during the 13th/11th/9th clock cycle for 12-/10-/8-bit operation. The serial data stream of conversion bits is preceded by a leading "zero" and succeeded by trailing "zeros." The data output (DOUT) goes into high-impedance state during the 16th clock cycle.

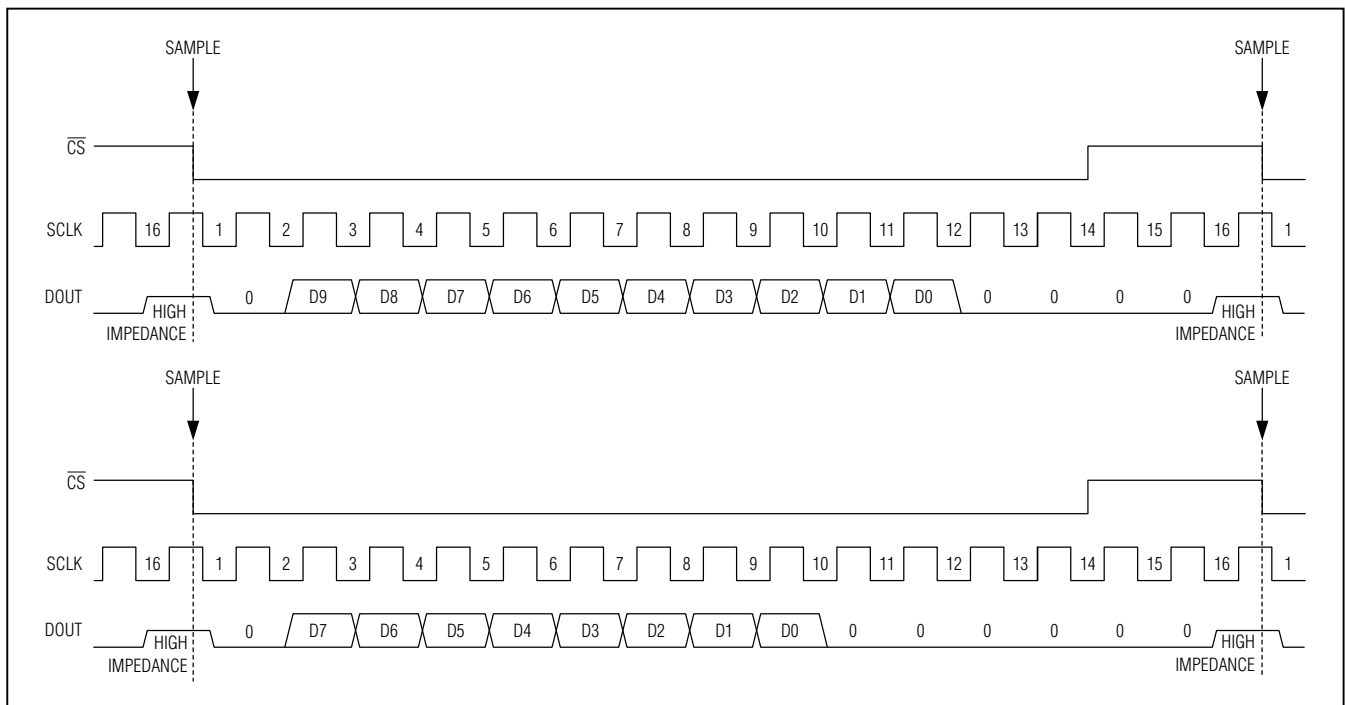


Figure 5. 10-/8-Bit Timing Diagrams

# MAX11102/03/05/06/10/11/15/16/17

## 2MSPS/3MSPS, Low-Power, Serial 12-/10-/8-Bit ADCs

To sustain the maximum sample rate, all devices have to be resampled immediately after the 16th clock cycle. For lower sample rates, the  $\overline{CS}$  falling edge can be delayed leaving DOUT in a high-impedance condition. Pull  $\overline{CS}$  high after the 10th SCLK falling edge (see the *Operating Modes* section).

### Analog Input

The devices produce a digital output that corresponds to the analog input voltage within the specified operating range of 0 to  $V_{REF}$  for the dual-channel devices and 0 to  $V_{DD}$  for the single-channel devices.

Figure 6 shows an equivalent circuit for the analog input AIN (for single-channel devices) and AIN1/AIN2 (for dual-channel devices). Internal protection diodes D1/D2 confine the analog input voltage within the power rails ( $V_{DD}$ , GND). The analog input voltage can swing from  $GND - 0.3V$  to  $V_{DD} + 0.3V$  without damaging the device.

The electric load presented to the external stage driving the analog input varies depending on which mode the ADC is in: track mode vs. conversion mode. In track mode, the internal sampling capacitor  $C_S$  (16pF) has to be charged through the resistor  $R$  ( $R = 50\Omega$ ) to the input voltage. For faithful sampling of the input, the capacitor voltage on  $C_S$  has to settle to the required accuracy during the track time.

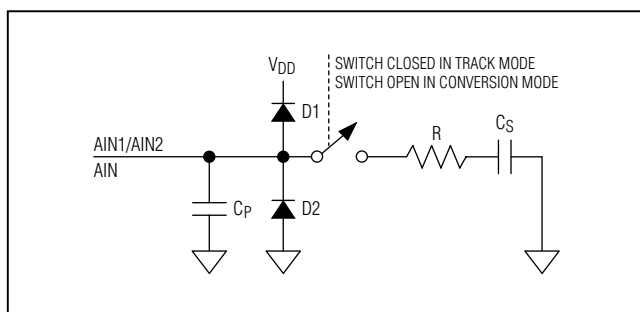


Figure 6. Analog Input Circuit

The source impedance of the external driving stage in conjunction with the sampling switch resistance affects the settling performance. The THD vs. Input Resistance graph in the *Typical Operating Characteristics* shows THD sensitivity as a function of the signal source impedance. Keep the source impedance at a minimum for high-dynamic performance applications. Use a high-performance op amp such as the MAX4430 to drive the analog input, thereby decoupling the signal source and the ADC.

While the ADC is in conversion mode, the sampling switch is open presenting a pin capacitance,  $C_P$  ( $C_P = 5pF$ ), to the driving stage. See the *Applications Information* section for information on choosing an appropriate buffer for the ADC.

### ADC Transfer Function

The output format is straight binary. The code transitions midway between successive integer LSB values such as 0.5 LSB, 1.5 LSB, etc. The LSB size for single-channel devices is  $V_{DD}/2^n$  and for dual-channel devices is  $V_{REF}/2^n$ , where  $n$  is the resolution. The ideal transfer characteristic is shown in Figure 10.

### Operating Modes

The ICs offer two modes of operation: normal mode and power-down mode. The logic state of the  $\overline{CS}$  signal during a conversion activates these modes. The power-down mode can be used to optimize power dissipation with respect to sample rate.

#### Normal Mode

In normal mode, the devices are powered up at all times, thereby achieving their maximum throughput rates. Figure 7 shows the timing diagram of these devices in normal mode. The falling edge of  $\overline{CS}$  samples the analog input signal, starts a conversion, and frames the serial data transfer.

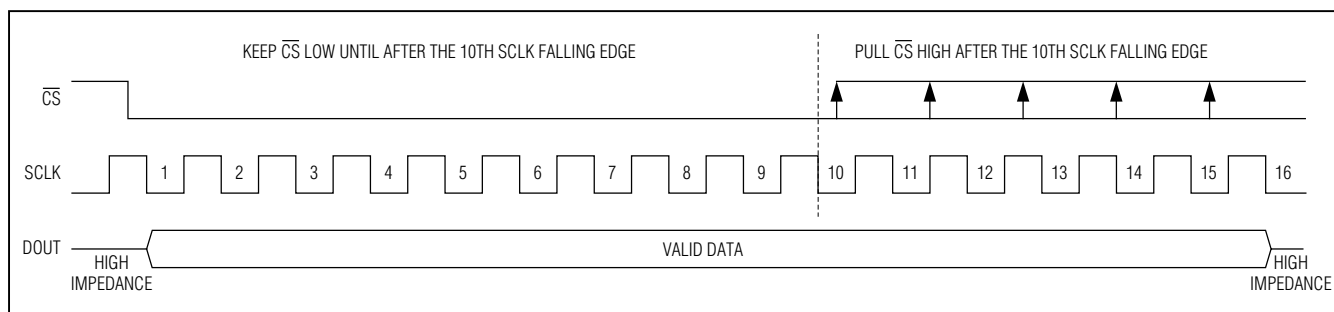


Figure 7. Normal Mode

# MAX11102/03/05/06/10/11/15/16/17

## 2MSPS/3MSPS, Low-Power, Serial 12-/10-/8-Bit ADCs

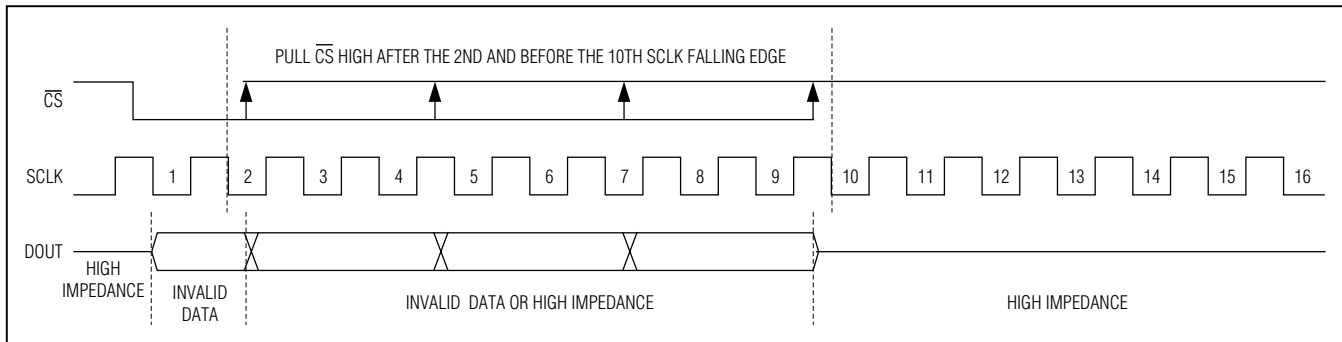


Figure 8. Entering Power-Down Mode

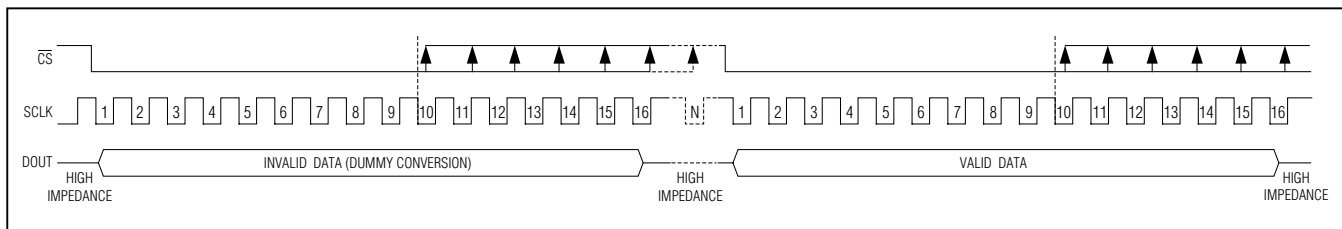


Figure 9. Exiting Power-Down Mode

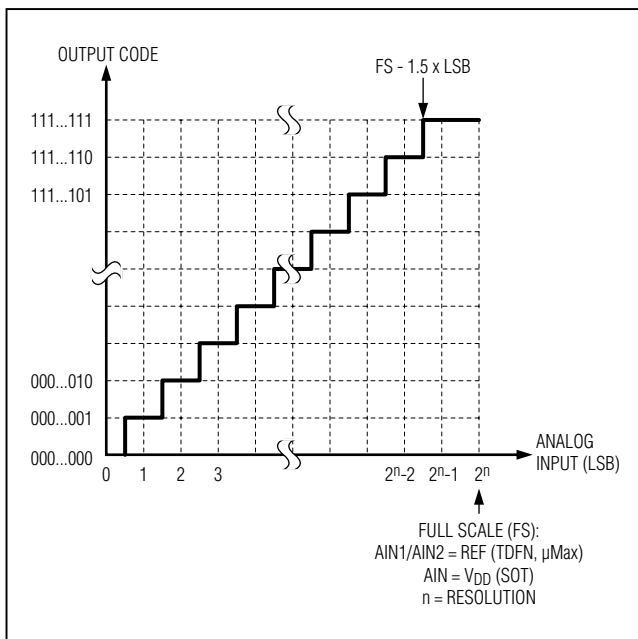


Figure 10. ADC Transfer Function

To remain in normal mode, keep  $\overline{CS}$  low until the falling edge of the 10th SCLK cycle. Pulling  $\overline{CS}$  high after the 10th SCLK falling edge keeps the part in normal mode. However, pulling  $\overline{CS}$  high before the 10th SCLK falling

edge terminates the conversion, DOUT goes into high-impedance mode, and the device enters power-down mode. See Figure 8.

### Power-Down Mode

In power-down mode, all bias circuitry is shut down drawing typically only 1.3 $\mu$ A of leakage current. To save power, put the device in power-down mode between conversions. Using the power-down mode between conversions is ideal for saving power when sampling the analog input infrequently.

### Entering Power-Down Mode

To enter power-down mode, drive  $\overline{CS}$  high between the 2nd and 10th falling edges of SCLK (see Figure 8). By pulling  $\overline{CS}$  high, the current conversion terminates and DOUT enters high impedance.

### Exiting Power-Down Mode

To exit power-down mode, implement one dummy conversion by driving  $\overline{CS}$  low for at least 10 clock cycles (see Figure 9). The data on DOUT is invalid during this dummy conversion. The first conversion following the dummy cycle contains a valid conversion result.

The power-up time equals the duration of the dummy cycle, and is dependent on the clock frequency. The power-up time for 3MSPS operation (48MHz SCLK) is 333ns. The power-up time for 2MSPS operation (32MHz SCLK) is 500ns.

# MAX11102/03/05/06/10/11/15/16/17

## 2Msps/3Msps, Low-Power, Serial 12-/10-/8-Bit ADCs

### Supply Current vs. Sampling Rate

For applications requiring lower throughput rates, the user can reduce the clock frequency ( $f_{SCLK}$ ) to lower the sample rate. Figure 11 shows the typical supply current ( $I_{VDD}$ ) as a function of sample rate ( $f_s$ ) for the 3Msps devices. The part operates in normal mode and is never powered down. Figure 13 pertains to the 2Msps devices.

The user can also power down the ADC between conversions by using the power-down mode. Figure 12 shows for the 3Msps device that as the sample rate is reduced, the device remains in the power-down state longer and the average supply current ( $I_{VDD}$ ) drops accordingly. Figure 14 pertains to the 2Msps devices.

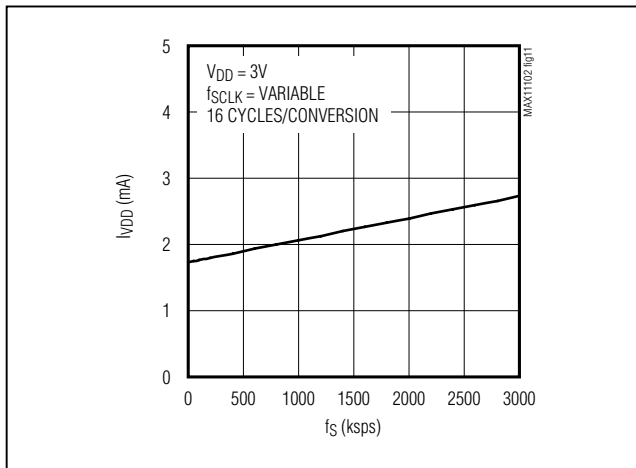


Figure 11. Supply Current vs. Sample Rate (Normal Operating Mode, 3Msps Devices)

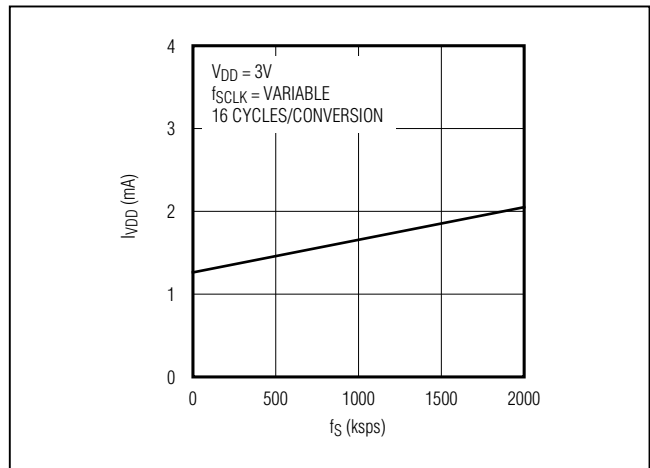


Figure 13. Supply Current vs. Sample Rate (Normal Operating Mode, 2Msps Devices)

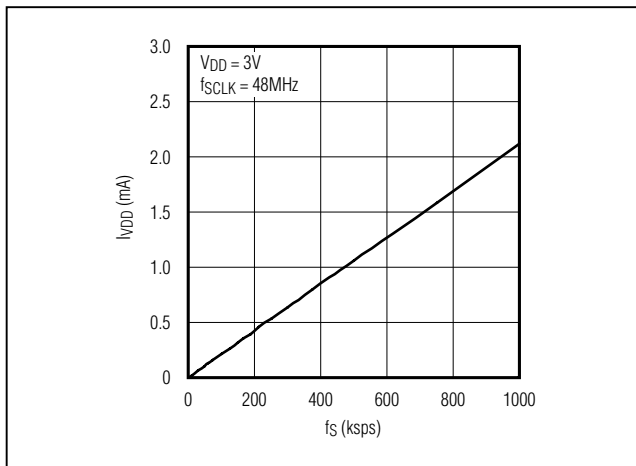


Figure 12. Supply Current vs. Sample Rate (Device Powered Down Between Conversions, 3Msps Devices)

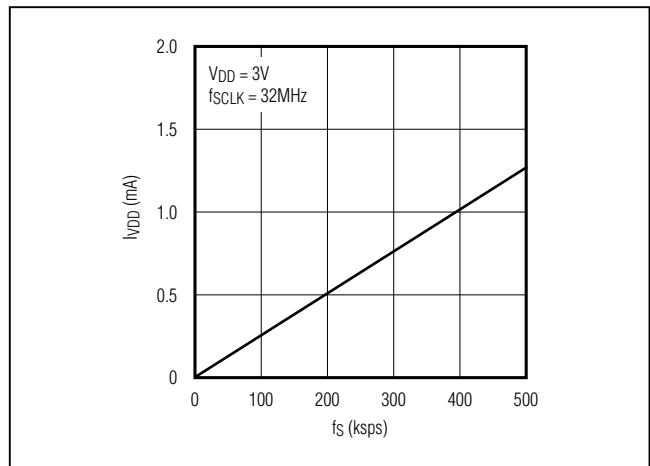


Figure 14. Supply Current vs. Sample Rate (Device Powered Down Between Conversions, 2Msps Devices)