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EVALUATION KIT AVAILABLE

MAX11129–MAX11132

3Msps, Low-Power, Serial 12-/10-Bit, 8-/16-Channel ADCs

General Description

The MAX11129–MAX11132 are 12-/10-bit with external reference and industry-leading 1.5MHz, full linear bandwidth, high speed, low-power, serial output successive approximation register (SAR) analog-to-digital converters (ADCs). The MAX11129–MAX11132 include both internal and external clock modes. These devices feature scan mode in both internal and external clock modes. The internal clock mode features internal averaging to increase SNR. The external clock mode features the SampleSet™ technology, a user-programmable analog input channel sequencer. The SampleSet approach provides greater sequencing flexibility for multichannel applications while alleviating significant microcontroller or DSP (controlling unit) communication overhead.

The internal clock mode features an integrated FIFO allowing data to be sampled at high speeds and then held for readout at any time or at a lower clock rate. Internal averaging is also supported in this mode improving SNR for noisy input signals. The devices feature analog input channels that can be configured to be single-ended inputs, fully differential pairs, or pseudo-differential inputs with respect to one common input. The MAX11129–MAX11132 operate from a 2.35V to 3.6V supply and consume only 15.2mW at 3Msps.

The MAX11129–MAX11132 include AutoShutdown™, fast wake-up, and a high-speed 3-wire serial interface. The devices feature full power-down mode for optimal power management.

The 48MHz, 3-wire serial interface directly connects to SPI, QSPI™, and MICROWIRE® devices without external logic.

Excellent dynamic performance, low voltage, low power, ease of use, and small package size make these converters ideal for portable battery-powered data-acquisition applications, and for other applications that demand low power consumption and small space.

The MAX11129–MAX11132 are available in 28-pin, 5mm x 5mm, TQFN packages and the MAX11131 is available in a 28-pin TSSOP package. All devices operate over the -40°C to +125°C temperature range.

SampleSet and AutoShutdown are trademarks of Maxim Integrated Products, Inc.
QSPI is a trademark of Motorola, Inc.
MICROWIRE is a registered trademark of National Semiconductor Corporation.

Benefits and Features

- **Scan Modes, Internal Averaging, and Internal Clock**
- **16-Entry First-In/First-Out (FIFO)**
- **SampleSet: User-Defined Channel Sequence with Maximum Length of 256**
- **Analog Multiplexer with True Differential Track/Hold**
  - ✧ **16-/8-Channel Single-Ended**
  - ✧ **8-/4-Channel Fully-Differential Pairs**
  - ✧ **15-/8-Channel Pseudo-Differential Relative to a Common Input**
- **Two Software-Selectable Bipolar Input Ranges**
  - ✧ **$\pm V_{REF+}/2$, $\pm V_{REF+}$**
- **Flexible Input Configuration Across All Channels**
- **High Accuracy**
  - ✧ **±1 LSB INL, ±1 LSB DNL, No Missing Codes Over Temperature Range**
- **70dB SINAD Guaranteed at 500kHz Input Frequency**
- **1.5V to 3.6V Wide Range I/O Supply**
  - ✧ **Allows the Serial Interface to Connect Directly to 1.8V, 2.5V, or 3.3V Digital Systems**
- **2.35V to 3.6V Supply Voltage**
- **Longer Battery Life for Portable Applications**
  - ✧ **Low Power**
  - ✧ **15.2mW at 3Msps with 3V Supplies**
  - ✧ **2µA Full-Shutdown Current**
- **External Differential Reference (1V to V_{DD})**
- **48MHz, 3-Wire SPI-/QSPI-/MICROWIRE-/DSP-Compatible Serial Interface**
- **Wide -40°C to +125°C Operation**
- **Space-Saving, 28-Pin, 5mm x 5mm TQFN Packages**
- **3Msps Conversion Rate, No Pipeline Delay**
- **12-/10-Bit Resolution**

Applications

High-Speed Data Acquisition Systems
High-Speed Closed-Loop Systems
Industrial Control Systems
Medical Instrumentation
Battery-Powered Instruments
Portable Systems

***Ordering Information* appears at end of data sheet.**

For related parts and recommended products to use with this part, refer to www.maximintegrated.com/MAX11129.related.

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maximintegrated.com.

19-6026; Rev 5; 9/12

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND.....-0.3V to +4V
OVDD, AIN0–AIN13, $\overline{CNVST}$/AIN14, REF+, REF-/AIN15 to GND.....-0.3V to the lower of (V_{DD} + 0.3V) and +4V
$\overline{CS}$, SCLK, DIN, DOUT, $\overline{EOC}$ TO GND ..... -0.3V to the Lower of (V_{OVDD} + 0.3V) and +4V
DGND to GND.....-0.3V to +0.3V
Input/Output Current (all pins) 50mA

Continuous Power Dissipation (T_A = +70°C)
TQFN (derate 34.4mW/°C above +70°C).....2758mW
TSSOP (derate 27mW/°C above +70°C).....2162mW
Operating Temperature Range ..... -40°C to +125°C
Junction Temperature .....+150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 1)

TQFN
Junction-to-Ambient Thermal Resistance (θ_{JA}).....29°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....2°C/W

TSSOP
Junction-to-Ambient Thermal Resistance (θ_{JA}).....37°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....2°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

ELECTRICAL CHARACTERISTICS (MAX11131/MAX11132)

(V_{DD} = 2.35V to 3.6V, V_{OVDD} = 1.5V to 3.6V, f_{SAMPLE} = 3Msps, f_{SCLK} = 48MHz, 50% duty cycle, V_{REF+} = V_{DD}, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY (Notes 3 and 4)						
Resolution	RES	12 bit	12			Bits
Integral Nonlinearity	INL				±1.0	LSB
Differential Nonlinearity	DNL	No missing codes			±1.0	LSB
Offset Error				-0.1	±4.0	LSB
Gain Error		(Note 5)		+0.3	±4.0	LSB
Offset Error Temperature Coefficient	OE_{TC}			±2		ppm/°C
Gain Temperature Coefficient	GE_{TC}			±0.8		ppm/°C
Channel-to-Channel Offset Matching				±0.5		LSB
Line Rejection	PSR	(Note 6)		±0.5	±2	LSB/V
DYNAMIC PERFORMANCE (500kHz, input sine wave) (Notes 3 and 7)						
Signal-to-Noise Plus Distortion	SINAD		70	72.2		dB
Signal-to-Noise Ratio	SNR		70	72.3		dB
Total Harmonic Distortion (Up to the 5th Harmonic)	THD			-88	-78	dB
Spurious-Free Dynamic Range	SFDR		79	90		dB
Intermodulation Distortion	IMD	f_1 = 398.4375kHz, f_2 = 275.8125kHz		-85		dB

ELECTRICAL CHARACTERISTICS (MAX11131/MAX11132) (continued)

(V_{DD} = 2.35V to 3.6V, V_{OVDD} = 1.5V to 3.6V, f_{SAMPLE} = 3Msps, f_{SCLK} = 48MHz, 50% duty cycle, V_{REF+} = V_{DD}, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Full-Power Bandwidth		-3dB			50		MHz
		-0.1dB			7.5		
Full-Linear Bandwidth		SINAD > 70dB			1.5		MHz
Crosstalk		-0.5dB below full scale of 492.1875kHz sine wave input to the channel being sampled, apply full-scale 398.4375kHz sine wave signal to all 15 nonselected input channels			-88		dB
CONVERSION RATE							
Power-Up Time	t_{PU}	Conversion cycle, external clock				2	Cycles
Acquisition Time	t_{ACQ}				52		ns
Conversion Time	t_{CONV}	Internally clocked (Note 8)			2.1		µs
		Externally clocked, f_{SCLK} = 48MHz, 16 cycles (Note 8)		333			ns
External Clock Frequency	f_{SCLK}			0.48		48	MHz
Aperture Delay					8		ns
Aperture Jitter		RMS			30		ps
ANALOG INPUT							
Input Voltage Range	V_{INA}	Unipolar (single-ended and pseudo differential)		0		V_{REF+}	V
		Bipolar (Note 9)	RANGE bit set to 0	$-V_{REF+}/2$		$V_{REF+}/2$	
			RANGE bit set to 1	$-V_{REF+}$		V_{REF+}	
Absolute Input Voltage Range		AIN+, AIN- relative to GND		-0.1		V_{REF+} + 0.1	V
Static Input Leakage Current	I_{ILA}	$V_{AIN\_}$ = V_{DD}, GND			-0.1	±1.5	µA
Input Capacitance	C_{AIN}	During acquisition time, RANGE bit = 0 (Note 10)			15		pF
		During acquisition time, RANGE bit = 1 (Note 10)			7.5		
EXTERNAL REFERENCE INPUT							
REF- Input Voltage Range	V_{REF-}			-0.3		+1	V
REF+ Input Voltage Range	V_{REF+}			1		V_{DD} + 50mV	V
REF+ Input Current	I_{REF+}	V_{REF+} = 2.5V, f_{SAMPLE} = 3Msps			110		µA
		V_{REF+} = 2.5V, f_{SAMPLE} = 0			0.1		

ELECTRICAL CHARACTERISTICS (MAX11131/MAX11132) (continued)

(V_{DD} = 2.35V to 3.6V, V_{OVDD} = 1.5V to 3.6V, f_{SAMPLE} = 3Msps, f_{SCLK} = 48MHz, 50% duty cycle, V_{REF+} = V_{DD}, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DIGITAL INPUTS (SCLK, DIN, $\overline{CS}$, $\overline{CNVST}$)							
Input Voltage Low	V_{IL}					V_{OVDD} x 0.25	V
Input Voltage High	V_{IH}			V_{OVDD} x 0.75			V
Input Hysteresis	V_{HYST}				V_{OVDD} x 0.15		mV
Input Leakage Current	I_{IN}	$V_{AIN\_}$ = 0V or V_{DD}			±0.09	±1.0	µA
Input Capacitance	C_{IN}				3		pF
DIGITAL OUTPUTS (DOUT, $\overline{EOC}$)							
Output Voltage Low	V_{OL}	I_{SINK} = 200µA				V_{OVDD} x 0.15	V
Output Voltage High	V_{OH}	I_{SOURCE} = 200µA		V_{OVDD} x 0.85			V
Three-State Leakage Current	I_L	$\overline{CS}$ = V_{DD}			–0.3	±1.5	µA
Three-State Output Capacitance	C_{OUT}	$\overline{CS}$ = V_{DD}			4		pF
POWER REQUIREMENTS							
Positive Supply Voltage	V_{DD}			2.35	3.0	3.6	V
Digital I/O Supply Voltage	V_{OVDD}			1.5	3.0	3.6	V
Positive Supply Current	I_{DD}	f_{SAMPLE} = 3Msps			5.1	6.5	mA
		f_{SAMPLE} = 0 (3Msps devices)			2.5		
		Full shutdown			0.0013	0.006	
Power Dissipation		Normal mode (external reference)	V_{DD} = 3V, f_{SAMPLE} = 3Msps		15.2		mW
			V_{DD} = 2.35V, f_{SAMPLE} = 3Msps		10.3		
		AutoStandby	V_{DD} = 3V, f_{SAMPLE} = 3Msps		7.3		
			V_{DD} = 2.35V, f_{SAMPLE} = 3Msps		4.35		
		Full/ AutoShutdown	V_{DD} = 3V		3.9		µW
			V_{DD} = 2.35V		1.7		

ELECTRICAL CHARACTERISTICS (MAX11131/MAX11132) (continued)

(V_{DD} = 2.35V to 3.6V, V_{OVDD} = 1.5V to 3.6V, f_{SAMPLE} = 3Msps, f_{SCLK} = 48MHz, 50% duty cycle, V_{REF+} = V_{DD}, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
TIMING CHARACTERISTICS (Figure 1) (Note 11)							
SCLK Clock Period	t_{CP}	Externally clocked conversion		20.8			ns
SCLK Duty Cycle	t_{CH}			40		60	%
SCLK Fall to DOUT Transition	t_{DOT}	C_{LOAD} = 10pF	V_{OVDD} = 1.5V to 2.35V	4		16.5	ns
			V_{OVDD} = 2.35V to 3.6V	4		15	
16th SCLK Fall to DOUT Disable	t_{DOD}	C_{LOAD} = 10pF, channel ID on				15	ns
14th SCLK Fall to DOUT Disable		C_{LOAD} = 10pF, channel ID off				16	ns
SCLK Fall to DOUT Enable	t_{DOE}	C_{LOAD} = 10pF				14	ns
DIN to SCLK Rise Setup	t_{DS}			4			ns
SCLK Rise to DIN Hold	t_{DH}			1			ns
$\overline{CS}$ Fall to SCLK Fall Setup	t_{CSS}			4			ns
SCLK Fall to $\overline{CS}$ Fall Hold	t_{CSH}			1			ns
$\overline{CNVST}$ Pulse Width	t_{CSW}	See Figure 6		5			ns
$\overline{CS}$ or $\overline{CNVST}$ Rise to $\overline{EOC}$ Low (Note 6)	t_{CNV_INT}	See Figure 7, f_{SAMPLE} = 3Msps			1.7	2.4	µs
$\overline{CS}$ Pulse Width	t_{CSBW}			5			ns

ELECTRICAL CHARACTERISTICS (MAX11129/MAX11130)

(V_{DD} = 2.35V to 3.6V, V_{OVDD} = 1.5V to 3.6V, f_{SAMPLE} = 3Msps, f_{SCLK} = 48MHz, 50% duty cycle, V_{REF+} = V_{DD}, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY (Notes 3 and 4)						
Resolution	RES	10 bit	10			Bits
Integral Nonlinearity	INL				±0.4	LSB
Differential Nonlinearity	DNL	No missing codes			±0.4	LSB
Offset Error				0.3	±1.0	LSB
Gain Error		(Note 5)		0.1	±1.2	LSB
Offset Error Temperature Coefficient	OE_{TC}			±2		ppm/°C
Gain Temperature Coefficient	GE_{TC}			±0.8		ppm/°C
Channel-to-Channel Offset Matching				±0.5		LSB
Line Rejection	PSR	(Note 6)		0.2	±1.0	LSB/V

ELECTRICAL CHARACTERISTICS (MAX11129/MAX11130) (continued)

(V_{DD} = 2.35V to 3.6V, V_{OVDD} = 1.5V to 3.6V, f_{SAMPLE} = 3Msps, f_{SCLK} = 48MHz, 50% duty cycle, V_{REF+} = V_{DD}, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DYNAMIC PERFORMANCE (500kHz, input sine wave) (Notes 3 and 7)						
Signal-to-Noise Plus Distortion	SINAD		61	61.5		dB
Signal-to-Noise Ratio	SNR		61	61.5		dB
Total Harmonic Distortion (Up to the 5th Harmonic)	THD			-86	-76	dB
Spurious-Free Dynamic Range	SFDR		77	86		dB
Intermodulation Distortion	IMD	f_1 = 398.4375kHz, f_2 = 275.8125kHz		-83		dB
Full-Power Bandwidth		-3dB		50		MHz
		-0.1dB		7.5		MHz
Full-Linear Bandwidth		SINAD > 59dB		1.5		MHz
Crosstalk		-0.5dB below full-scale of 492.1875kHz sine-wave input to the channel being sampled; apply full-scale 398.4375kHz sine wave signal to all 15 nonselected input channels		-88		dB
CONVERSION RATE						
Power-Up Time	t_{PU}	Conversion cycle, external clock			2	Cycles
Acquisition Time	t_{ACQ}			52		ns
Conversion Time	t_{CONV}	Internally clocked (Note 8)		2.1		µs
		Externally clocked, f_{SCLK} = 48MHz, 16 cycles (Note 8)	333			ns
External Clock Frequency	f_{SCLK}		0.48		48	MHz
Aperture Delay				8		ns
Aperture Jitter		RMS		30		ps
ANALOG INPUT						
Input Voltage Range	V_{INA}	Unipolar (single-ended and pseudo differential)	0		V_{REF+}	V
		Bipolar (Note 9), RANGE bit set to 0	$-V_{REF+}/2$		$+V_{REF+}/2$	
		Bipolar (Note 9), RANGE bit set to 1	$-V_{REF+}$		$+V_{REF+}$	
Absolute Input Voltage Range		AIN+, AIN- relative to GND	-0.1		V_{REF+} + 0.1	V
Static Input Leakage Current	I_{ILA}	$V_{AIN\_}$ = V_{DD}, GND		–0.1		µA
Input Capacitance	C_{AIN}	During acquisition time, RANGE bit = 0 (Note 10)		15		pF
		During acquisition time, RANGE bit = 1 (Note 10)		7.5		

ELECTRICAL CHARACTERISTICS (MAX11129/MAX11130) (continued)

(V_{DD} = 2.35V to 3.6V, V_{OVDD} = 1.5V to 3.6V, f_{SAMPLE} = 3Msps, f_{SCLK} = 48MHz, 50% duty cycle, V_{REF+} = V_{DD}, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
EXTERNAL REFERENCE INPUT							
REF- Input Voltage Range	V_{REF-}			-0.3		+1	V
REF+ Input Voltage Range	V_{REF+}			1		V_{DD} + 50mV	V
REF+ Input Current	I_{REF+}	V_{REF+} = 2.5V, f_{SAMPLE} = 3Msps			110		µA
		V_{REF+} = 2.5V, f_{SAMPLE} = 0			0.1		µA
DIGITAL INPUTS (SCLK, DIN, $\overline{CS}$, $\overline{CNVST}$)							
Input Voltage Low	V_{IL}					V_{OVDD} x 0.25	V
Input Voltage High	V_{IH}			V_{OVDD} x 0.75			V
Input Hysteresis	V_{HYST}				V_{OVDD} x 0.15		mV
Input Leakage Current	I_{IN}	$V_{AIN\_}$ = 0V or V_{DD}			±0.09		µA
Input Capacitance	C_{IN}				3		pF
DIGITAL OUTPUTS (DOUT, $\overline{EOC}$)							
Output Voltage Low	V_{OL}	I_{SINK} = 200µA				V_{OVDD} x 0.15	V
Output Voltage High	V_{OH}	I_{SOURCE} = 200µA		V_{OVDD} x 0.85			V
Three-State Leakage Current	I_L	$\overline{CS}$ = V_{DD}			-0.3		µA
Three-State Output Capacitance	C_{OUT}	$\overline{CS}$ = V_{DD}			4		pF
POWER REQUIREMENTS							
Positive Supply Voltage	V_{DD}			2.35	3.0	3.6	V
Digital I/O Supply Voltage	V_{OVDD}			1.5	3.0	3.6	V
Positive Supply Current	I_{DD}	f_{SAMPLE} = 3Msps			5.1		mA
		f_{SAMPLE} = 0 (3Msps devices)			2.5		
		Full shutdown			0.0013	0.006	
Power Dissipation		Normal mode (external reference)	V_{DD} = 3V, f_{SAMPLE} = 3Msps		15.2		mW
			V_{DD} = 2.35V, f_{SAMPLE} = 3Msps		10.3		
		AutoStandby	V_{DD} = 3V, f_{SAMPLE} = 3Msps		7.3		
			V_{DD} = 2.35V, f_{SAMPLE} = 3Msps		4.35		
		Full/ AutoShutdown	V_{DD} = 3V		3.9		µW
			V_{DD} = 2.35V		1.7		

ELECTRICAL CHARACTERISTICS (MAX11129/MAX11130) (continued)

(V_{DD} = 2.35V to 3.6V, V_{OVDD} = 1.5V to 3.6V, f_{SAMPLE} = 3Msps, f_{SCLK} = 48MHz, 50% duty cycle, V_{REF+} = V_{DD}, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
TIMING CHARACTERISTICS (Figure 1) (Note 11)							
SCLK Clock Period	t_{CP}	Externally clocked conversion		20.8			ns
SCLK Duty Cycle	t_{CH}			40		60	%
SCLK Fall to DOUT Transition	t_{DOT}	C_{LOAD} = 10pF	V_{OVDD} = 1.5V to 2.35V	4		16.5	ns
			V_{OVDD} = 2.35V to 3.6V	4		15	
16th SCLK Fall to DOUT Disable	t_{DOD}	C_{LOAD} = 10pF, channel ID on				15	ns
14th SCLK Fall to DOUT Disable		C_{LOAD} = 10pF, channel ID off				16	ns
SCLK Fall to DOUT Enable	t_{DOE}	C_{LOAD} = 10pF				14	ns
DIN to SCLK Rise Setup	t_{DS}			4			ns
SCLK Rise to DIN Hold	t_{DH}			1			ns
$\overline{CS}$ Fall to SCLK Fall Setup	t_{CSS}			4			ns
SCLK Fall to $\overline{CS}$ Fall Hold	t_{CSH}			1			ns
$\overline{CNVST}$ Pulse Width	t_{CSW}	See Figure 6		5			ns
$\overline{CS}$ or $\overline{CNVST}$ Rise to $\overline{EOC}$ Low (Note 7)	t_{CNV_INT}	See Figure 7, f_{SAMPLE} = 3Msps			2.1	2.4	µs
$\overline{CS}$ Pulse Width	t_{CSBW}			5			ns

Note 2: Limits are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design.
Note 3: Channel ID disabled.
Note 4: Tested in single-ended mode.
Note 5: Offset nulled.
Note 6: Line rejection $\Delta(D_{OUT})$ with V_{DD} = 2.35V to 3.6V and V_{REF+} = 2.35V.
Note 7: Tested and guaranteed with fully differential input.
Note 8: Conversion time is defined as the number of clock cycles multiplied by the clock period with a 50% duty cycle.
Maximum conversion time: 1.91µs + N x 16 x T_{OSC_MAX}
T_{OSC_MAX} = 29.4ns, T_{OSC_TYP} = 25ns.
Note 9: The operational input voltage range for each individual input of a differentially configured pair is from V_{DD} to GND. The operational input voltage difference is from -V_{REF+}/2 to +V_{REF+}/2 or -V_{REF+} to +V_{REF+}.
Note 10: See Figure 3 (Equivalent Input Circuit).
Note 11: Guaranteed by characterization.

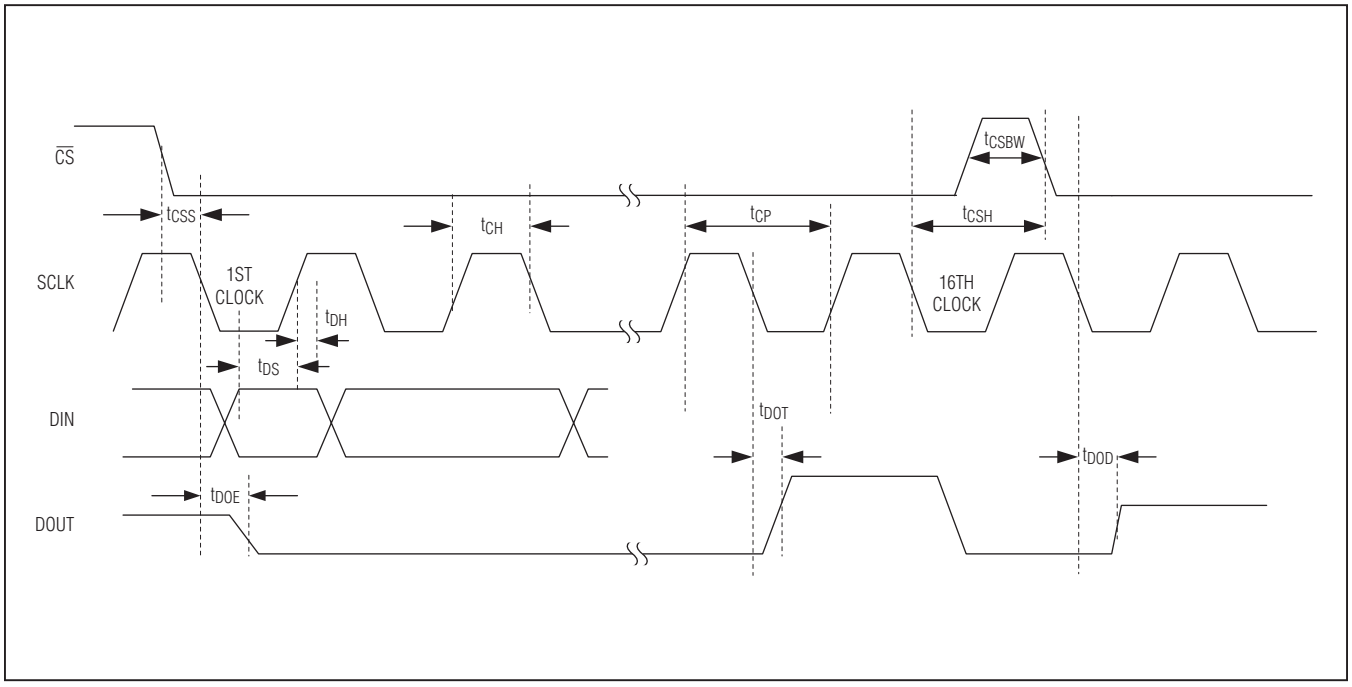
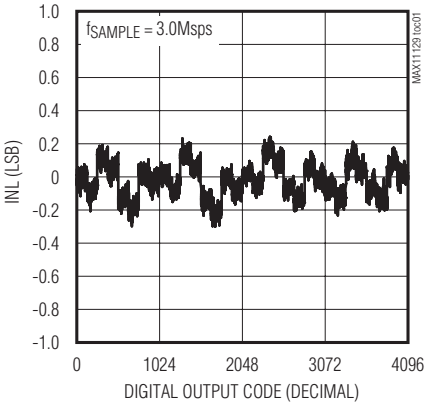


Figure 1. Detailed Serial-Interface Timing Diagram

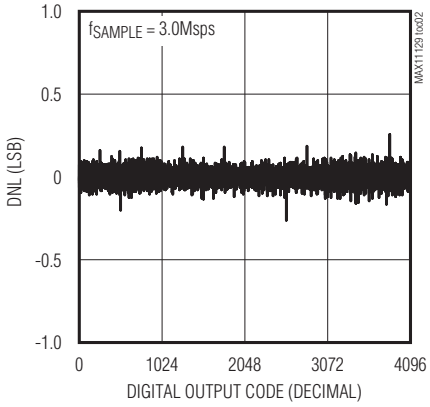
Typical Operating Characteristics

(MAX11131ATI+/MAX11132ATI+, T_A = +25°C, unless otherwise noted.)

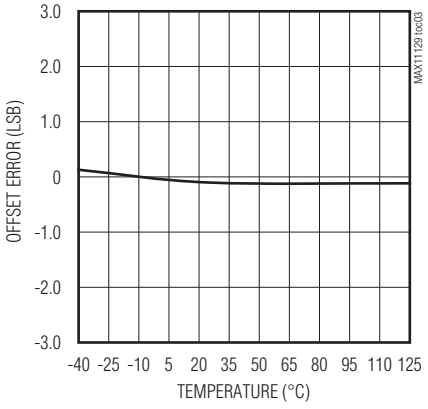
INTEGRAL NONLINEARITY vs. DIGITAL OUTPUT CODE



DIFFERENTIAL NONLINEARITY vs. OUTPUT CODE



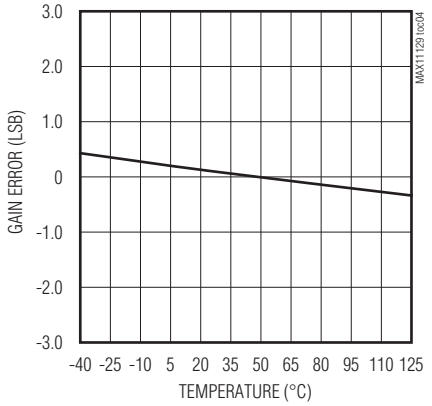
OFFSET ERROR vs. TEMPERATURE



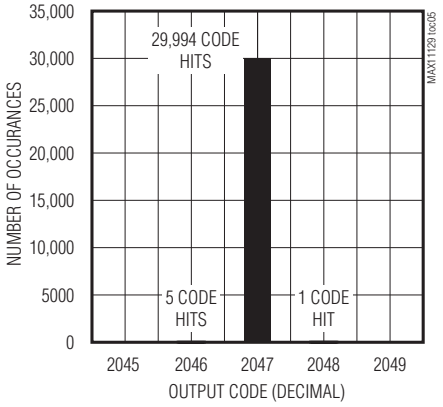
Typical Operating Characteristics (continued)

(MAX11131ATI+/MAX11132ATI+, T_A = +25°C, unless otherwise noted.)

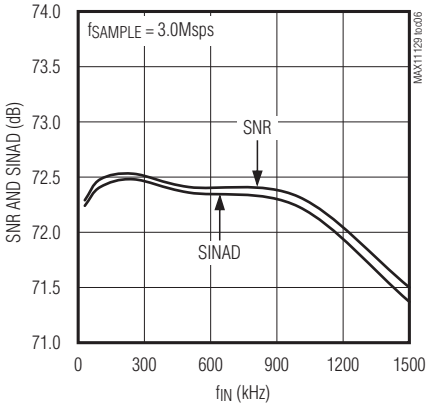
GAIN ERROR vs. TEMPERATURE



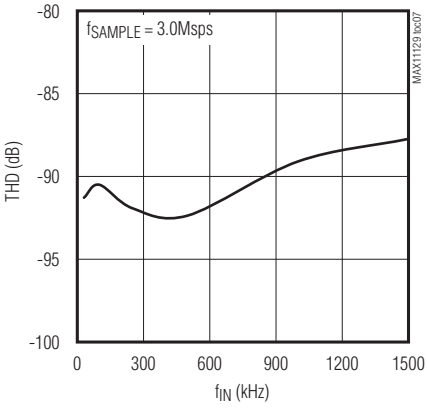
HISTOGRAM FOR 30,000 CONVERSIONS (f_{SAMPLE} = 3.0Msps)



SNR AND SINAD vs. ANALOG INPUT FREQUENCY



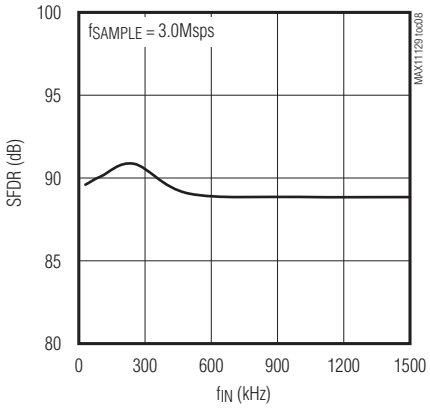
THD vs. ANALOG INPUT FREQUENCY



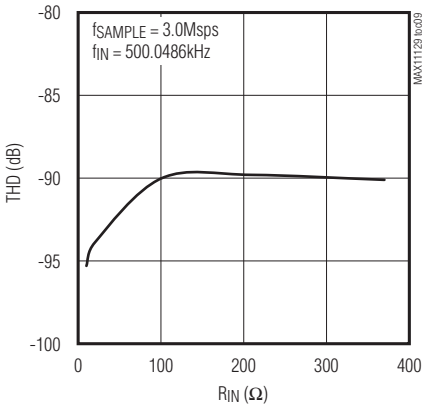
Typical Operating Characteristics (continued)

(MAX11131ATI+/MAX11132ATI+, T_A = +25°C, unless otherwise noted.)

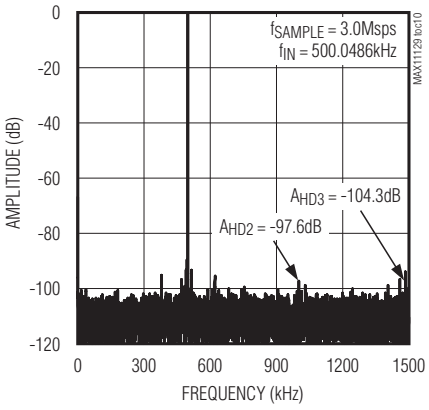
SFDR vs. ANALOG INPUT FREQUENCY



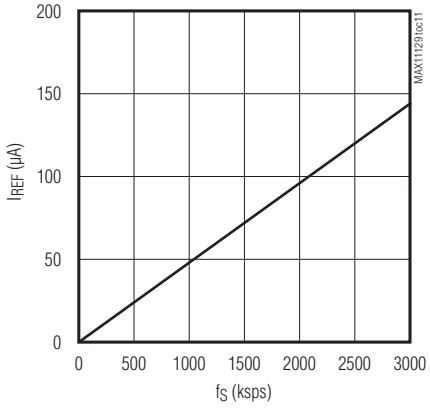
THD vs. INPUT RESISTANCE



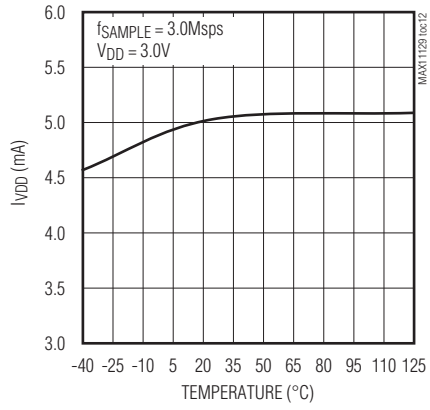
500kHz SINE-WAVE INPUT (8192-POINT FFT PLOT)



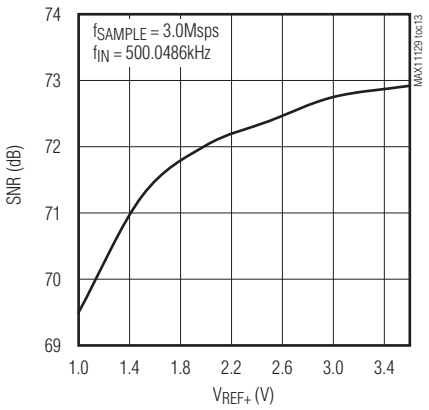
REFERENCE CURRENT vs. SAMPLING RATE



ANALOG SUPPLY CURRENT vs. TEMPERATURE

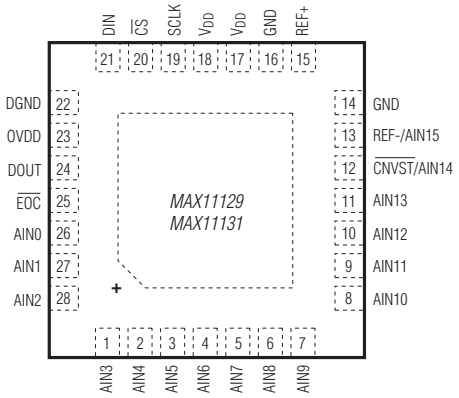


SNR vs. REFERENCE VOLTAGE

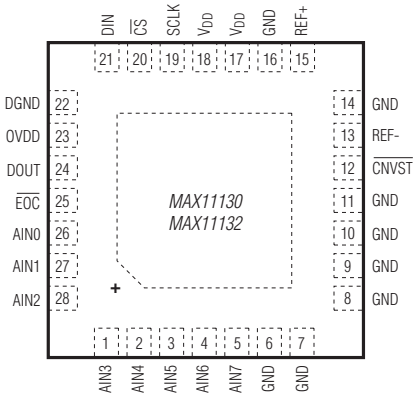


Pin Configurations

TOP VIEW

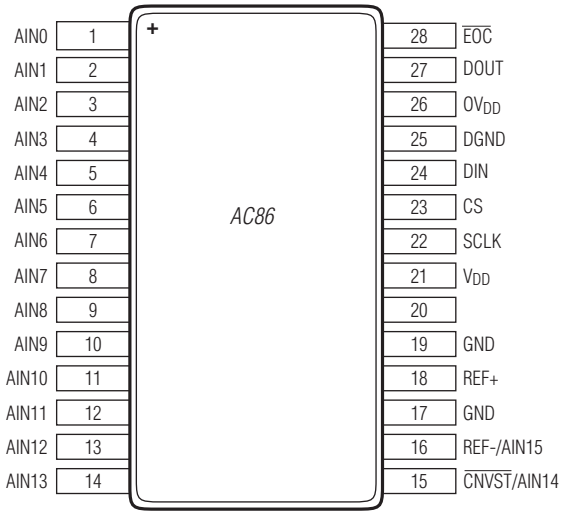


TQFN
16 CHANNEL



TQFN
8 CHANNEL

TOP VIEW

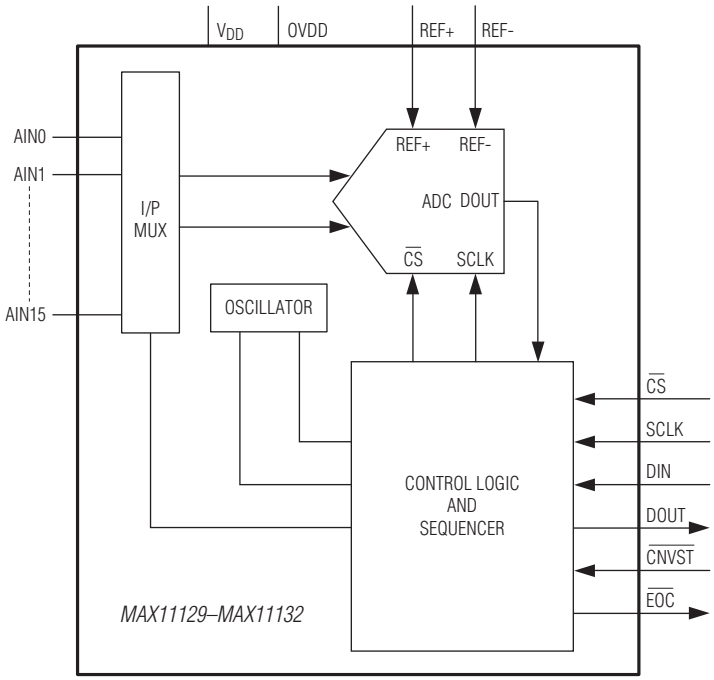


TSSOP-28
16 CHANNEL

Pin Description

MAX11129 MAX11131 (16 CHANNEL) TQFN	MAX11131 (16 CHANNEL) TSSOP	MAX11130 MAX11132 (8 CHANNEL) TQFN	NAME	FUNCTION
26, 27, 28, 1–11	1–14	—	AIN0–AIN13	Analog Inputs
—	—	26, 27, 28, 1–5	AIN0–AIN7	Analog Inputs
12	15	—	$\overline{CNVST}$/ AIN14	Active-Low Conversion Start Input/Analog Input 14
—	—	12	$\overline{CNVST}$	Active-Low Conversion Start Input
13	16	—	REF-/AIN15	External Differential Reference Negative Input /Analog Input 15
—	—	13	REF-	External Differential Reference Negative Input
14, 16	17, 19	6–11, 14, 16	GND	Ground
15	18	15	REF+	External Positive Reference Input. Apply a reference voltage at REF+. Bypass to GND with a 0.47µF capacitor.
17, 18	20, 21	17, 18	V_{DD}	Power-Supply Input. Bypass to GND with a 10µF in parallel with a 0.1µF capacitors.
19	22	19	SCLK	Serial Clock Input. Clocks data in and out of the serial interface
20	23	20	$\overline{CS}$	Active-Low Chip Select Input. When $\overline{CS}$ is low, the serial interface is enabled. When $\overline{CS}$ is high, DOUT is high impedance or three-state.
21	24	21	DIN	Serial Data Input. DIN data is latched into the serial interface on the rising edge of SCLK.
22	25	22	DGND	Digital I/O Ground
23	26	23	OVDD	Interface Digital Power-Supply Input. Bypass to GND with a 10µF in parallel with a 0.1µF capacitors.
24	27	24	DOUT	Serial Data Output. Data is clocked out on the falling edge of SCLK. When $\overline{CS}$ is high, DOUT is high impedance or three-state.
25	28	25	$\overline{EOC}$	End of Conversion Output. Data is valid after $\overline{EOC}$ pulls low (internal clock mode only).
—	—	—	EP	Exposed Pad. Connect EP directly to GND plane for guaranteed performance.

Functional Diagram



Detailed Description

The MAX11129–MAX11132 are 12-/10-bit with external reference and industry-leading 1.5MHz, full linear bandwidth, high-speed, low-power, serial output successive approximation register (SAR) analog-to-digital converters (ADC). These devices feature scan mode, internal averaging to increase SNR, and AutoShutdown.

The external clock mode features the SampleSet technology, a user-programmable analog input channel sequencer. The user may define and load a unique sequencing pattern into the ADC allowing both high- and low-frequency inputs to be converted without interface activity. This feature frees the controlling unit for other tasks while lowering overall system noise and power consumption.

The MAX11129–MAX11132 includes internal clock. The internal clock mode features an integrated FIFO, allowing data to be sampled at high speed and then held for readout at any time or at a lower clock rate. Internal averaging is also supported in this mode improving SNR for noisy input signals. All input channels are configurable for single-ended, fully differential or pseudo-differential inputs in unipolar or bipolar mode. The MAX11129–MAX11132 operate from a 2.35V to 3.6V supply and consume only 15mW at 3Msps.

The MAX11129–MAX11132 include AutoShutdown, fast wake-up, and a high-speed 3-wire serial interface. The devices feature full power-down mode for optimal power management.

Data is converted from analog voltage sources in a variety of channel and data-acquisition configurations. Microprocessor (µP) control is made easy through a 3-wire SPI-/QSPI-/MICROWIRE-compatible serial interface.

Input Bandwidth

The ADC's input-tracking circuitry features a 1.5MHz small-signal full-linear bandwidth to digitize high-speed transient events and measure periodic signals with bandwidths exceeding the ADC's sampling rate by using undersampling techniques. Anti-alias filtering of the input signals is necessary to avoid high-frequency signals aliasing into the frequency band of interest.

3-Wire Serial Interface

The MAX11129–MAX11132 feature a serial interface compatible with SPI/QSPI and MICROWIRE devices. For SPI/QSPI, ensure the CPU serial interface runs in master mode to generate the serial clock signal. Select the SCLK frequency of 48MHz or less, and set clock polarity (CPOL) and phase (CPHA) in the µP control registers to the same value. The MAX11129–MAX11132 operate with SCLK idling high, and thus operate with CPOL = CPHA = 1.

Set $\overline{CS}$ low to latch input data at DIN on the rising edge of SCLK. Output data at DOUT is updated on the falling edge of SCLK. A high-to-low transition on $\overline{CS}$ samples the analog inputs and initiates a new frame. A frame is defined as the time between two falling edges of $\overline{CS}$. There is a minimum of 16 bits per frame. The serial data input, DIN, carries data into the control registers clocked in by the rising edge of SCLK. The serial data output, DOUT, delivers the conversion results and is clocked out by the falling edge of SCLK. DOUT is a 16-bit data word containing a 4-bit channel address, followed by a 12-bit conversion result led by the MSB when CHAN_ID is set to 1 in the ADC Mode Control register (Figure 2a). In this mode, keep the clock high for at least one full SCLK period before the $\overline{CS}$ falling edge to ensure best performance (Figure 2b). When CHAN_ID is set to 0 (external clock mode only), the 16-bit data word includes a leading zero and the 12-bit conversion result is followed by 3 trailing zeros (Figure 2c). In the 10-bit ADC, the last 2 LSBs are set to 0.

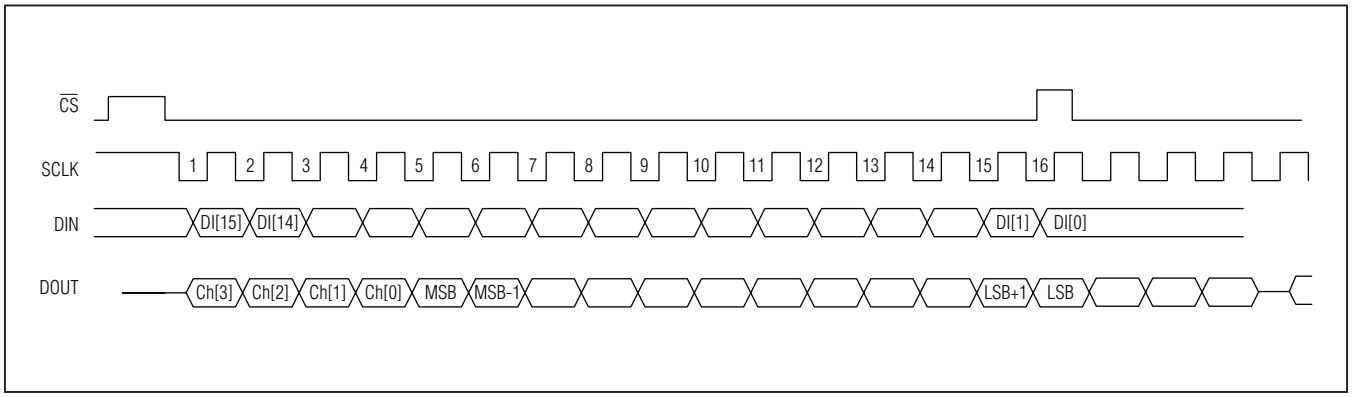


Figure 2a. External Clock Mode Timing Diagram with CHAN_ID=1

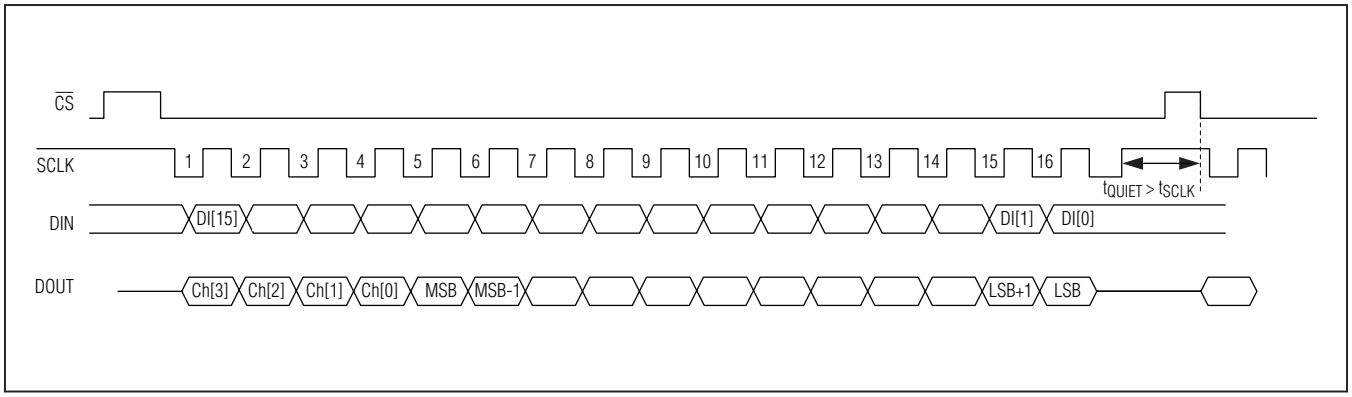


Figure 2b. External Clock Mode Timing Diagram with CHAN_ID=1 for Best Performance

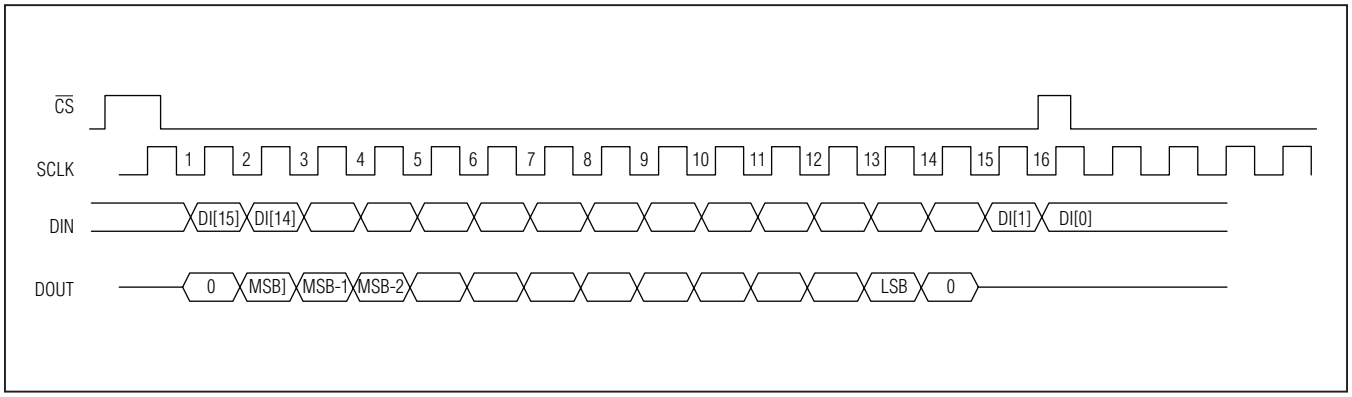


Figure 2c. External Clock Mode Timing Diagram with CHAN_ID=0

Single-Ended, Differential, and Pseudo-Differential Input

The MAX11129–MAX11132 include up to 16 analog input channels that can be configured to 16 single-ended inputs, 8 fully differential pairs, or 15 pseudo-differential inputs with respect to one common input (REF-/AIN15 is the common input).

The analog input range is 0V to V_{REF+} in single-ended and pseudo-differential mode (unipolar) and $\pm V_{REF+}/2$ or $\pm V_{REF+}$ in fully differential mode (bipolar) depending on the RANGE register settings. See Table 7 for the RANGE register setting.

Unipolar mode sets the differential input range from 0 to V_{REF+}. If the positive analog input swings below the negative analog input in unipolar mode, the digital output code is zero. Selecting bipolar mode sets the differential input range to $\pm V_{REF+}/2$ or $\pm V_{REF+}$ depending on the RANGE register settings (Table 7).

In single-ended mode, the ADC always operates in unipolar mode. The analog inputs are internally referenced to GND with a full-scale input range from 0 to V_{REF+}. Single-ended conversions are internally referenced to GND (Figure 3).

The MAX11129–MAX11132 feature 15 pseudo differential inputs by setting the PDIFF_COM bits in the Unipolar register to 1 (Table 10). The 15 analog input signals inputs are referenced to a DC signal applied to the REF-/AIN15.

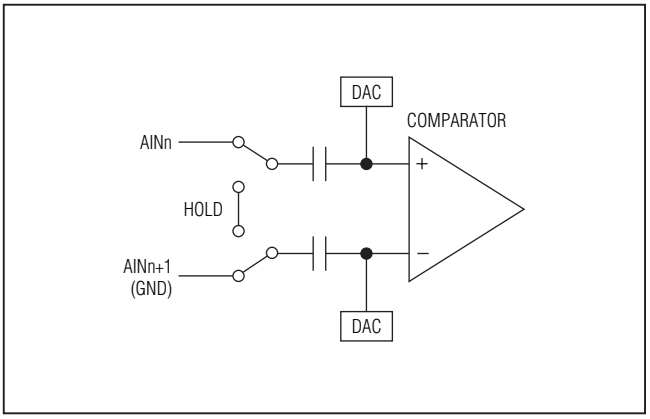


Figure 3. Equivalent Input Circuit

Fully Differential Reference (REF+, REF-)

When the reference is used in fully differential mode (REFSEL = 1), the full-scale range is set by the difference between REF+ and REF-. The output clips if the input signal surpasses this reference range.

ADC Transfer Function

The output format of the MAX11129–MAX11132 is straight binary in unipolar mode and two's complement in bipolar mode. The code transitions midway between successive integer LSB values, such as 0.5 LSB, 1.5 LSB. Figure 4 and Figure 5 show the unipolar and bipolar transfer function, respectively. Output coding is binary, with 1 LSB = $V_{REF+}/4096$.

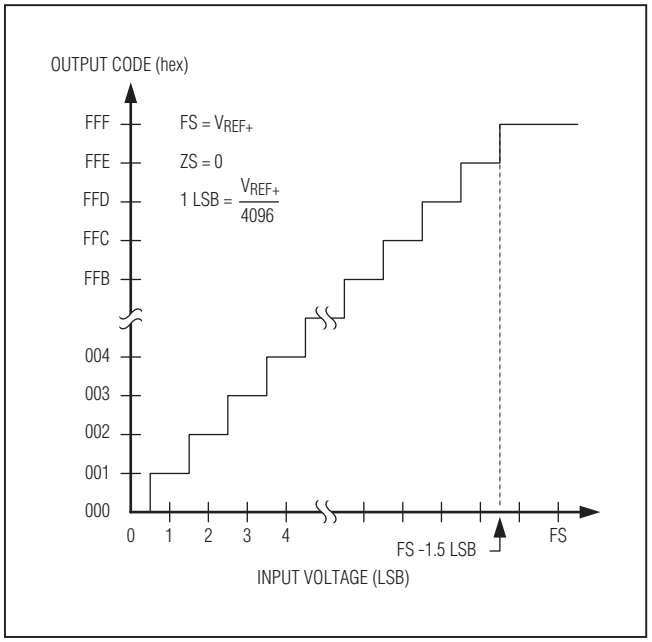


Figure 4. Unipolar Transfer Function for 12-Bit Resolution

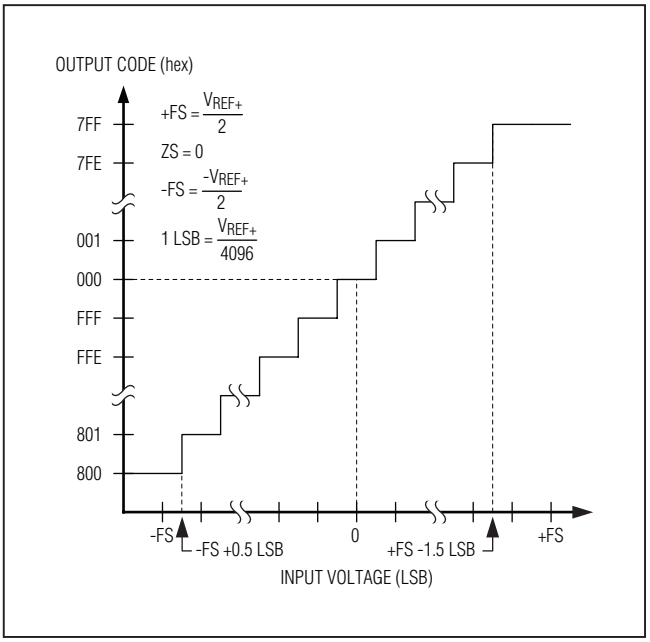


Figure 5. Bipolar Transfer Function for 12-Bit Resolution

Internal FIFO

The MAX11129–MAX11132 contain a FIFO buffer that can hold up to 16 ADC results. This allows the ADC to handle multiple internally clocked conversions without tying up the serial bus. If the FIFO is filled and further conversions are requested without reading from the FIFO, the oldest ADC results are overwritten by the new ADC results. Each result contains 2 bytes, with the MSB preceded by four leading channel address bits. After each falling edge of $\overline{CS}$, the oldest available byte of data is available at DOUT. When the FIFO is empty, DOUT is zero.

External Clock

In external clock mode, the analog inputs are sampled at the falling edge of $\overline{CS}$. Serial clock (SCLK) is used to perform the conversion. The sequencer reads in the channel to be converted from the serial data input (DIN) at each frame. The conversion results are sent to the serial output (DOUT) at the next frame.

Internal Clock

The MAX11129–MAX11132 operate from an internal oscillator, which is accurate within ±15% of the 40MHz nominal clock rate. Request internally timed conversions by writing the appropriate sequence to the ADC Mode Control register (Table 2). The wake-up, acquisition, conversion, and shutdown sequences are initiated through $\overline{CNVST}$ and are performed automatically using the internal oscillator. Results are added to the internal FIFO.

With $\overline{CS}$ high, initiate a scan by setting $\overline{CNVST}$ low for at least 5ns before pulling it high (Figure 6). Then, the MAX11129–MAX11132 wake up, scan all requested channels, store the results in the FIFO, and shut down. After the scan is complete, $\overline{EOC}$ is pulled low and the results are available in the FIFO. Wait until $\overline{EOC}$ goes low before pulling $\overline{CS}$ low to communicate with the serial interface. $\overline{EOC}$ stays low until $\overline{CS}$ or $\overline{CNVST}$ is pulled low again. Do not initiate a second $\overline{CNVST}$ before $\overline{EOC}$ goes low; otherwise, the FIFO may become corrupted.

Alternatively, set SWCNV to 1 in the ADC Mode Control register to initiate conversions with $\overline{CS}$ rising edge instead of cycling $\overline{CNVST}$ (Table 2). For proper operation, $\overline{CS}$ must be held low for 17 clock cycles to guarantee that the device interprets the SWCNV setting. A delay is initiated at the rising edge of $\overline{CS}$ and the conversion is started when the delay times out. Upon completing the conversion, this bit is reset to 0 (Figure 7). Apply a soft reset when changing from internal to external clock mode: RESET[1:0] = 10.

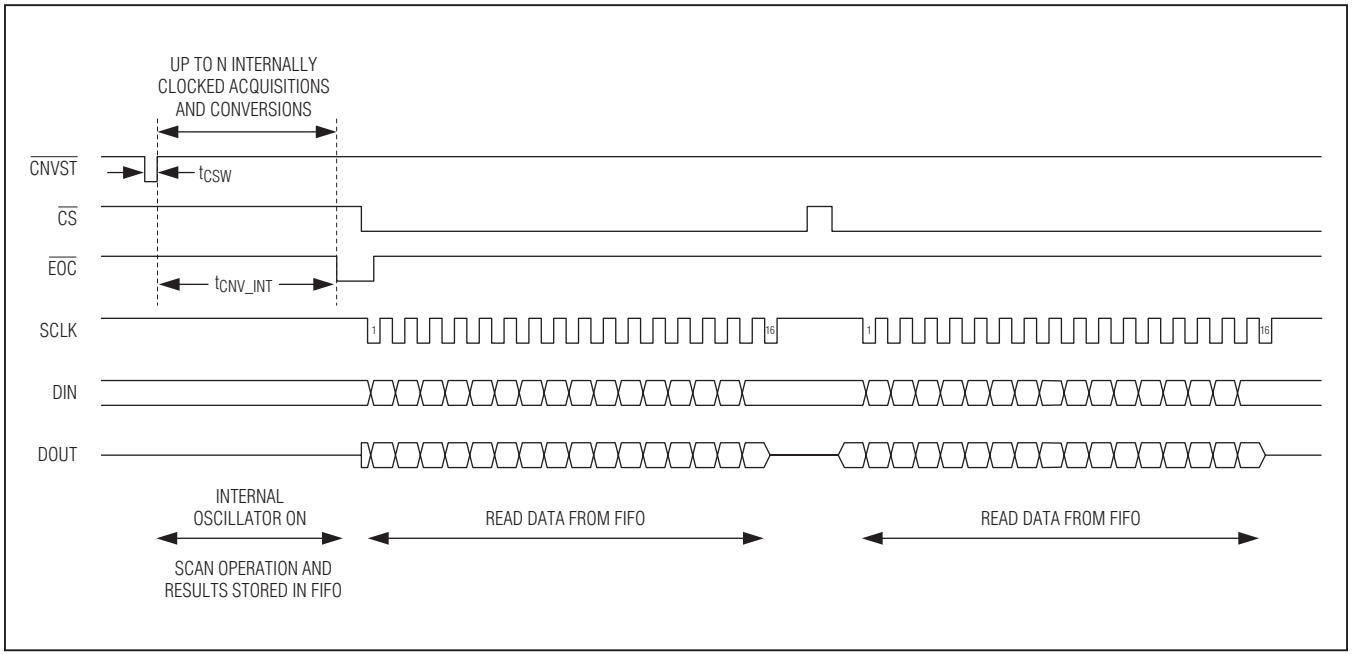


Figure 6. Internal Conversions with $\overline{CNVST}$

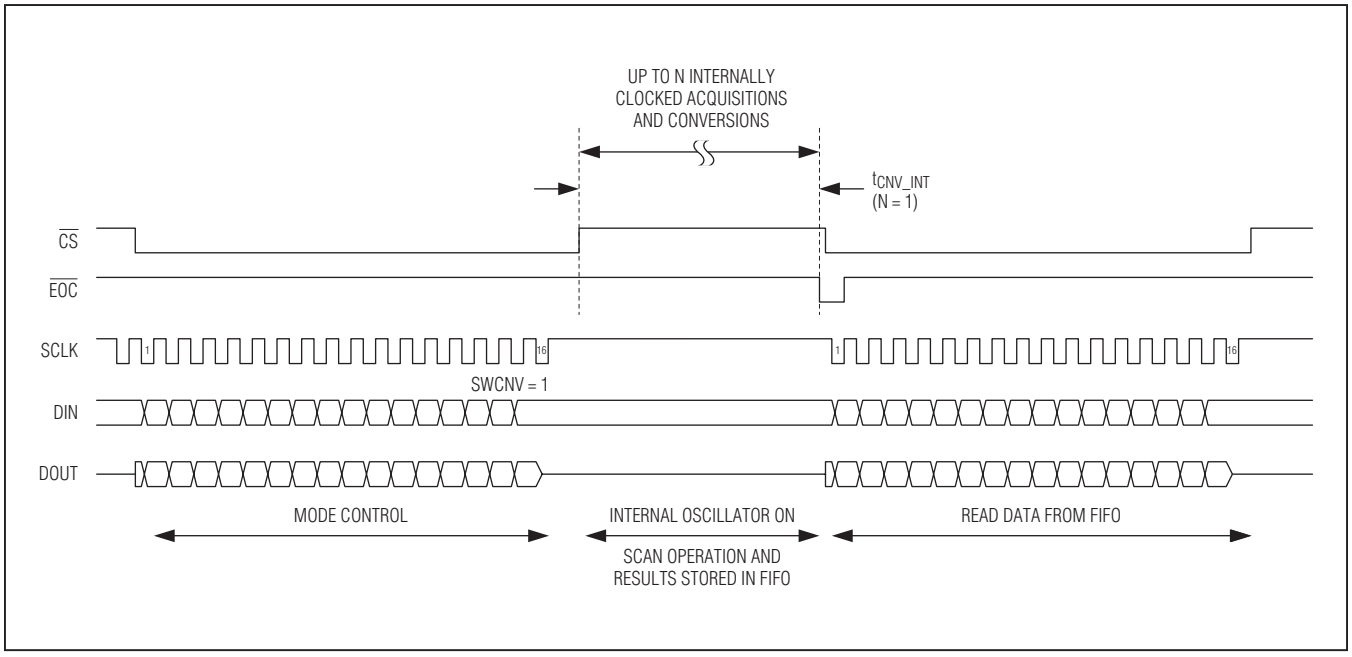


Figure 7. Internal Conversions with SWCNV

Analog Input

The MAX11129–MAX11132 produce a digital output that corresponds to the analog input voltage as long as the analog inputs are within the specified operating range. Internal protection diodes confine the analog input voltage within the region of the analog power input rails (V_{DD}, GND) and allow the analog input voltage to swing from GND - 0.3V to V_{DD} + 0.3V without damaging the device. Input voltages beyond GND - 0.3V and V_{DD} + 0.3V forward bias the internal protection diodes. Limit the forward diode current to less than 50mA to avoid damage to the MAX11129–MAX11132.

ECHO

When writing to the ADC Configuration register, set ECHO to 1 in ADC Configuration register to echo back the configuration data onto DOUT at time n+1 (Figure 8, Table 6).

Scan Modes

The MAX11129–MAX11132 feature nine scan modes (Table 3).

Manual Mode

The next channel to be selected is identified in each SPI frame. The conversion results are sent out in the next frame. The manual mode works with the external clock only. The FIFO is unused.

Repeat Mode

Repeat scanning channel N for number of times and store all the conversion results in the FIFO. The number of scans is programmed in the ADC Configuration register. The repeat mode works with the internal clock only.

Custom_Int and Custom_Ext

In Custom_Int and Custom_Ext modes, the device scans preprogrammed channels in ascending order. The channels to be scanned in sequence are programmed in the Custom Scan0 or Custom Scan1 registers. A new I/P MUX is selected every frame on the thirteenth falling edge of SCLK. Custom_Int works with the internal clock. Custom_Ext works with the external clock.

Standard_Int and Standard_Ext

In Standard_Int and Standard_Ext modes, the device scans channels 0 through N in ascending order where N is the last channel specified in the ADC Mode Control register. A new I/P MUX is selected every frame on the thirteenth falling edge of SCLK. Standard_Int works with the internal clock. Standard_Ext works with the external clock.

Upper_Int and Upper_Ext

In Upper_Int and Upper_Ext modes, the device scans channels N through 15/11/7/3 in ascending order where N is the first channel specified in the ADC Mode Control register. A new I/P MUX is selected every frame on the thirteenth falling edge of SCLK. Upper_Int works with the internal clock. Upper_Ext works with the external clock.

SampleSet

The SampleSet mode of operation allows the definition of a unique channel sequence combination with maximum length of 256. SampleSet is supported only in the external clock mode. SampleSet is ideally suited for multichannel measurement applications where some analog inputs must be converted more often than others.

The SampleSet approach provides greater sequencing flexibility for multichannel applications while alleviating significant microcontroller or DSP (controlling unit) communication overhead. SampleSet technology allows the user to exploit available ADC input bandwidth without need for constant communication between the ADC and controlling unit. The user may define and load a unique sequencing pattern into the ADC allowing both high- and low-frequency inputs to be converted appropriately without interface activity. With the unique sequence loaded

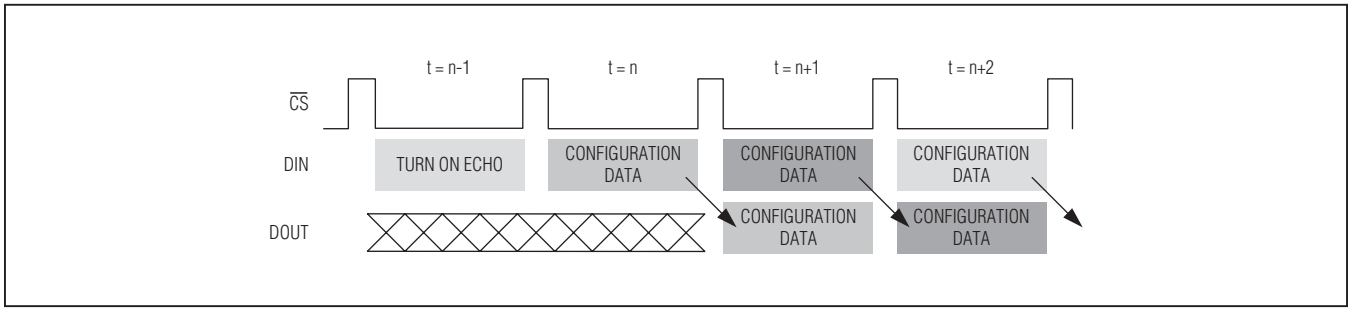


Figure 8. Echo Back the Configuration Data

into ADC memory, the pattern may be repeated indefinitely or changed at any time.

For example, the maximum throughput of MAX11129–MAX11132 is 3Msps. Traditional ADC scan modes allow up to 16-channel conversions in ascending order. In this case, the effective throughput per channel is 3Msps/16 channel or 187.5ksps. The maximum input frequency that the ADC can resolve (Nyquist Theorem) is 93.75kHz. If all 16 channels must be measured, with some channels having greater than 93.75kHz input frequency, the user must revert back to manual mode requiring constant communication on the serial interface. SampleSet technology solves this problem. Figure 9 provides a SampleSet use-model example.

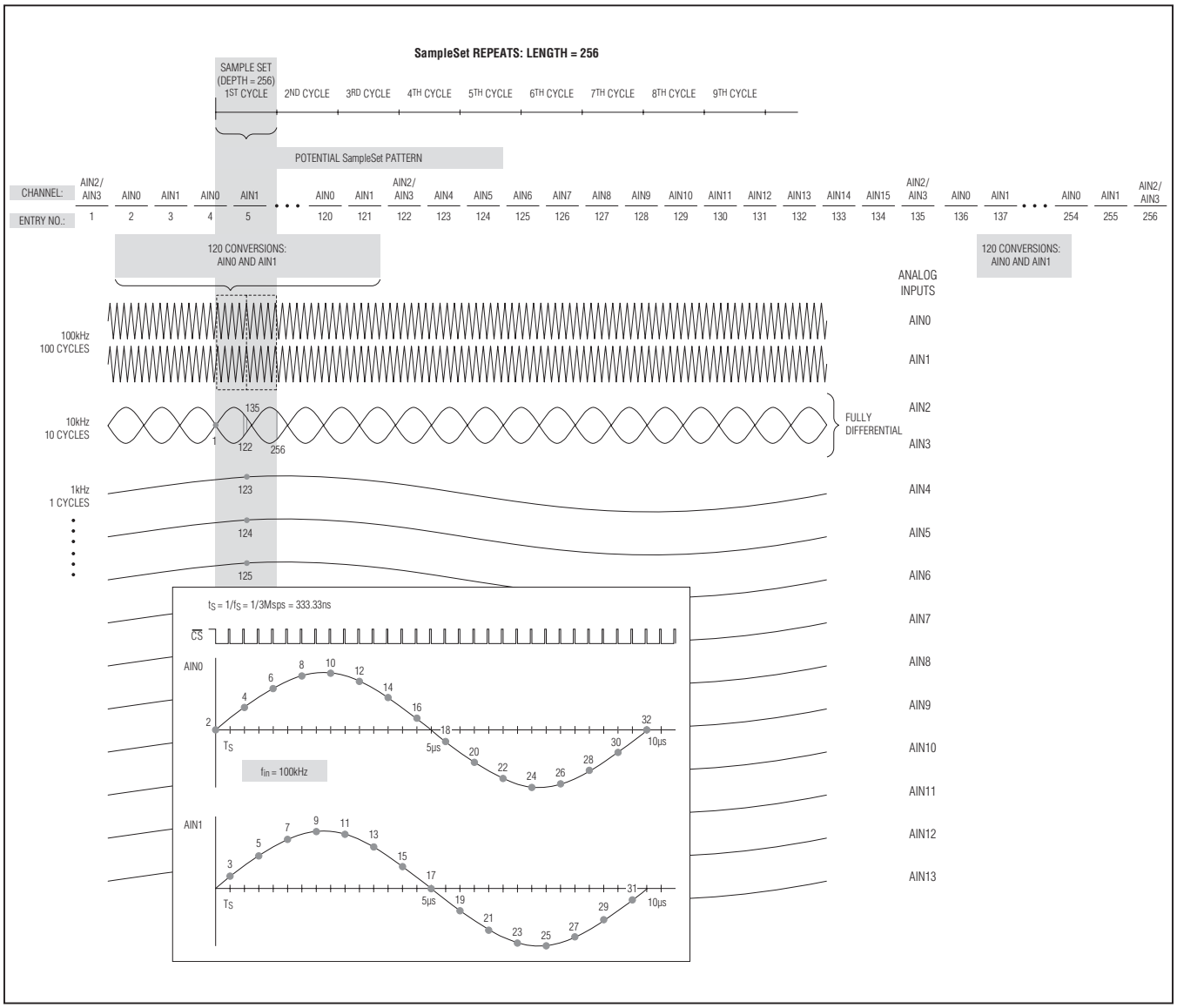


Figure 9. SampleSet Use-Model Example

Averaging Mode

In averaging mode, the device performs the specified number of conversions and returns the average for each requested result in the FIFO. The averaging mode works with internal clock only.

Scan Modes and Unipolar/Bipolar Setting

When the Unipolar or Bipolar registers are configured as pseudo-differential or fully differential, the analog input pairs are repeated in this automated mode. For example, if N is set to 15 to scan all 16 channels and all analog input pairs are configured for fully-differential conversion, the ADC converts the channels twice. In this case, the user may avoid dual conversions on input pairs by implementing Manual mode or using Custom_Int or Custom_Ext scan modes.

Register Descriptions

The MAX11129–MAX11132 communicate between the internal registers and the external circuitry through the SPI-/QSPI-compatible serial interface. Table 1 details the register access and control. Table 2 through Table 14 detail the various functions and configurations.

For ADC mode control, set bit 15 of the register code identification to zero. The ADC Mode Control register determines when and under what scan condition the ADC operates.

To set the ADC data configuration, set the bit 15 of the register code identification to one.

Table 1. Register Access and Control

REGISTER NAME	REGISTER IDENTIFICATION CODE					DIN ≡ DATA INPUTS
	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT [10:0]
ADC Mode Control	0	DIN	DIN	DIN	DIN	DIN
ADC Configuration	1	0	0	0	0	DIN
Unipolar	1	0	0	0	1	DIN
Bipolar	1	0	0	1	0	DIN
RANGE	1	0	0	1	1	DIN
Custom Scan0	1	0	1	0	0	DIN
Custom Scan1	1	0	1	0	1	DIN
SampleSet	1	0	1	1	0	DIN
Reserved. Do not use.	1	1	1	1	1	DIN

Table 2. ADC Mode Control Register

BIT NAME	BIT	DEFAULT STATE	FUNCTION		
REG_CNTL	15	0	Set to 0 to select the ADC Mode Control register		
SCAN[3:0]	14:11	0001	ADC Scan Control register (Table 3)		
CHSEL[3:0]	10:7	0000	Analog Input Channel Select register (Table 4). See Table 3 to determine which modes use CHSEL[3:0] for the channel scan instruction.		
RESET[1:0]	6:5	00	RESET1	RESET0	FUNCTION
			0	0	No reset
			0	1	Reset the FIFO only (resets to zero)
			1	0	Reset all registers to default settings (includes FIFO)
			1	1	Unused

Table 2. ADC Mode Control Register (continued)

BIT NAME	BIT	DEFAULT STATE	FUNCTION
PM[1:0]	4:3	00	Power Management Modes (Table 5). In external clock mode, PM[1:0] selects between normal mode and various power-down modes of operation.
CHAN_ID	2	0	External Clock Mode. Channel address is always present in internal clock mode. Set to 1, DOUT is a 16-bit data word containing a 4-bit channel address, followed by a 12-bit conversion result led by the MSB.
SWCNV	1	0	Set to 1 to initiate conversions with the rising edge of $\overline{CS}$ instead of cycling $\overline{CNVST}$ (internal clock mode only). This bit is used for the internal clock mode only and must be reasserted in the ADC mode control, if another conversion is desired.
—	0	0	Unused

Table 3. ADC Scan Control

SCAN3	SCAN2	SCAN1	SCAN0	MODE NAME	FUNCTION
0	0	0	0	N/A	Continue to operate in the previously selected mode. Ignore data on bits [10:0]. This feature is provided so that DIN can be held low when no changes are required in the ADC Mode Control register. Bits [6:3, 1] can be still written without changing the scan mode properties.
0	0	0	1	Manual	The next channel to be selected is identified in each SPI frame. The conversion results are sent out in the next frame.
					Clock mode: External clock only
					Channel scan/sequence: Single channel per frame
					Channel selection: See Table 4, CHSEL[3:0]
					Averaging: No
0	0	1	0	Repeat	Scans channel N repeatedly. The FIFO stores 4, 8, 12, or 16 conversion results for channel N.
					Clock mode: Internal clock only
					Channel scan/sequence: Single channel per frame
					Channel selection: See Table 4, CHSEL[3:0]
					Averaging: Yes
0	0	1	1	Standard_Int	Scans channels 0 through N. The FIFO stores N conversion results.
					Clock mode: Internal clock
					Channel scan/sequence: N channels in ascending order
					Channel selection: See Table 4, CHSEL[3:0] determines channel N
					Averaging: Yes

Table 3. ADC Scan Control (continued)

SCAN3	SCAN2	SCAN1	SCAN0	MODE NAME	FUNCTION
0	1	0	0	Standard_Ext	Scans channels 0 through N
					Clock mode: External clock
					Channel scan/sequence: N channels in ascending order
					Channel selection: See Table 4, CHSEL[3:0] determines channel N
					Averaging: No
0	1	0	1	Upper_Int	Scans channel N through the highest numbered channel. The FIFO stores X conversion results where:
					X = Channel 16–N; 16-channel devices
					X = Channel 8–N; 8-channel devices
					Clock mode: Internal clock
					Channel scan/sequence: Channel N through the highest numbered channel in ascending order
					Channel selection: See Table 4, CHSEL[3:0] determines channel N
					Averaging: Yes
0	1	1	0	Upper_Ext	Scans channel N through the highest numbered channel
					Clock mode: External clock
					Channel scan/sequence: Channel N through the highest numbered channel in ascending order
					Channel selection: See Table 4, CHSEL[3:0] determines channel N
					Averaging: No
0	1	1	1	Custom_Int	Scans preprogrammed channels in ascending order. The FIFO stores conversion results for this unique channel sequence.
					Clock mode: Internal clock
					Channel scan/sequence: Unique ascending channel sequence
					Maximum depth: 16 conversions
					Channel selection: See Table 12, Custom Scan0 register and Table 13, Custom Scan1 register
					Averaging: Yes
1	0	0	0	Custom_Ext	Scans preprogrammed channels in ascending order
					Clock mode: External clock
					Channel scan/sequence: Unique ascending channel sequence
					Maximum depth: 16 conversions
					Channel selection: See Table 12, Custom Scan0 register and Table 13, Custom Scan1 register
					Averaging: No

Table 3. ADC Scan Control (continued)

SCAN3	SCAN2	SCAN1	SCAN0	MODE NAME	FUNCTION
1	0	0	1	SampleSet	Scans preprogrammed channel sequence with maximum length of 256. There is no restriction on the channel pattern.
					Clock mode: External clock only
					Channel scan/sequence: Unique channel sequence
					Maximum depth: 256 conversions
					Channel Selection: See Table 4
					Averaging: No
1	0	1	0	—	Continue to operate in the previously selected mode. Ignore data on bits [10:0].
1	0	1	1	—	Continue to operate in the previously selected mode. Ignore data on bits [10:0].
1	1	0	0	—	Continue to operate in the previously selected mode. Ignore data on bits [10:0].
1	1	0	1	—	Continue to operate in the previously selected mode. Ignore data on bits [10:0].
1	1	1	0	—	Continue to operate in the previously selected mode. Ignore data on bits [10:0].
1	1	1	1	—	Continue to operate in the previously selected mode. Ignore data on bits [10:0].

Table 4. Analog Input Channel Select

CHSEL3	CHSEL2	CHSEL1	CHSEL0	SELECTED CHANNEL (N)
0	0	0	0	AIN0
0	0	0	1	AIN1
0	0	1	0	AIN2
0	0	1	1	AIN3
0	1	0	0	AIN4
0	1	0	1	AIN5
0	1	1	0	AIN6
0	1	1	1	AIN7
1	0	0	0	AIN8
1	0	0	1	AIN9
1	0	1	0	AIN10
1	0	1	1	AIN11
1	1	0	0	AIN12
1	1	0	1	AIN13
1	1	1	0	AIN14
1	1	1	1	AIN15

Power-Down Mode

The MAX11129–MAX11132 feature three power-down modes.

Static Shutdown

The devices shut down when the SPM bits in the ADC Configuration register are asserted (Table 6). There are two shutdown options:

- Full shutdown where all circuitry is shutdown.
- Partial shutdown where all circuitry is powered down except for the internal bias generator.

AutoShutdown with External Clock Mode

When the PM_ bits in the ADC Mode Control register are asserted (Table 5), the device shuts down at the rising edge of $\overline{CS}$ in the next frame. The device powers up again at the following falling edge of $\overline{CS}$. There are two available options:

- AutoShutdown where all circuitry is shutdown.
- AutoStandby where all circuitry are powered down except for the internal bias generator.

AutoShutdown with Internal Clock Mode

The device shuts down after all conversions are completed. The device powers up again at the next falling edge of $\overline{CNVST}$ or at the rising edge of $\overline{CS}$ after the SWCNV bit is asserted.

Table 5. Power Management Modes

PM1	PM0	MODE	FUNCTION
0	0	Normal	All circuitry is fully powered up at all times.
0	1	AutoShutdown	The device enters full shutdown mode at the end of each conversion. All circuitry is powered down. The device powers up following the falling edge of $\overline{CS}$. It takes 2 cycles before valid conversions take place. The information in the registers is retained.
1	0	AutoStandby	The device powers down all circuitry except for the internal bias generator. The part powers up following the falling edge of $\overline{CS}$. It takes 2 cycles before valid conversions take place. The information in the registers is retained.
1	1	—	Unused.

Table 6. ADC Configuration Register

BIT NAME	BIT	DEFAULT STATE	FUNCTION		
CONFIG_SETUP	15:11	N/A	Set to 10000 to select the ADC Configuration register.		
REFSEL	10	0	**REFSEL**	**VOLTAGE REFERENCE**	**REF- CONFIGURATION**
			0	External single-ended	AIN15 (for the 16-channel devices)
			1	External differential	REF-
AVGON	9	0	Set to 1 to turn averaging on. Valid for internal clock mode only. Set to 0 to turn averaging off.		