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MAX11152

18-Bit, 500ksps, +5V Unipolar Input, SAR ADC, in Tiny 10-Pin µMAX

General Description

The MAX11152 is an 18-bit, 500ksps, +5V unipolar pseudo-differential input SAR ADC that offers excellent AC and DC performance in a small standard package.

This ADC typically achieves 95dB SNR, -106dB THD, and ±2 LSB INL, ±0.5 LSB DNL. The MAX11152 guarantees 18-bit no-missing codes.

The MAX11152 communicates using a SPI-compatible serial interface at 2.5V, 3V, 3.3V, or 5V logic.

The serial interface can be used to daisy-chain multiple ADCs for multichannel applications and provides a busy indicator option for simplified system synchronization and timing.

The MAX11152 is offered in a 10-pin, 3mm x 5mm, µMAX® package and is specified over the -40°C to +85°C temperature range.

Applications

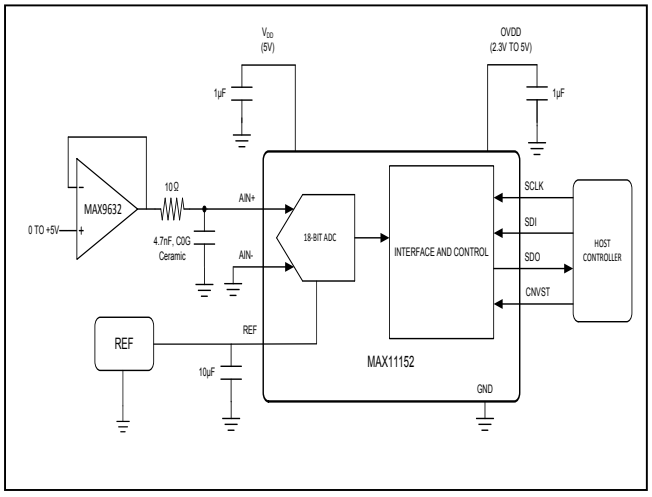
- Process Control and Industrial Automation
- Medical Instrumentation
- Test and Measurement
- Automatic Test Equipment
- Narrowband Receivers

***Selector Guide* and *Ordering Information* appear at end of data sheet.**

Benefits and Features

- High DC/AC Accuracy Improves Measurement Quality
  - 18-Bit Resolution with No Missing Codes
  - 500ksps Throughput Rates Without Pipeline Delay/Latency
  - 95dB SNR and -106dB THD at 10kHz
  - 1.65 LSB_{RMS} Transition Noise
  - ±0.5 LSB DNL (typ) and ±2 LSB INL (typ)
- Wide Supply Range Simplifies Power-Supply Design
  - 5V Analog Supply
  - 2.3V to 5V Digital Supply
  - 23mW Power Consumption at 500ksps
  - 10µA in Shutdown Mode
- Multi-Industry Standard Serial Interface and Small Package Reduce Size
  - SPI/QSPI™/MICROWIRE®/DSP-Compatible Serial Interface
  - 3mm x 5mm, Tiny 10-Pin µMAX Package

Typical Operating Circuit



16-Bit to 18-Bit SAR ADC Family

	16 BIT/ 250ksps	16 BIT/ 500ksps	18 BIT/ 500ksps
±5V Input Internal REF	MAX11167 MAX11169	MAX11166 MAX11168	MAX11156 MAX11158
+5V Input Internal REF	MAX11165 MAX11161	MAX11164 MAX11160	MAX11154 MAX11150
+5V Input External REF	MAX11163	MAX11162	MAX11152

maxim integrated™

Absolute Maximum Ratings

V_{DD} to GND .....-0.3V to +6V
OVDD to GND..... -0.3V to the lower of (V_{DD} + 0.3V) and +6V
AIN+ to GND .....-0.3V to +6V
AIN-, REF to GND. -0.3V to the lower of (V_{DD} + 0.3V) and +6V
SCLK, DIN, DOUT, CNVST
to GND..... -0.3V to the lower of (V_{DD} + 0.3V) and +6V
Maximum Current into Any Pin.....50mA

Continuous Power Dissipation (T_A = +70°C)
µMAX (derate 8.8mW/°C above +70°C) 707mW
Operating Temperature Range..... -40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

µMAX
Junction-to-Ambient Thermal Resistance (θ_{JA})..... 113°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) .....36°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{DD} = 4.75V to 5.25V, V_{OVDD} = 2.3V to 5.25V, f_{SAMPLE} = 500kHz, V_{REF} = 5V; T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG INPUT (Note 3)						
Input Voltage Range		AIN+ to AIN-	0		V_{REF}	V
Absolute Input Voltage Range		AIN+ to GND	-0.1		V_{REF} + 0.1	V
		AIN- to GND	-0.1		+0.1	
Input Leakage Current		Acquisition phase	-10	+0.001	+10	µA
Input Capacitance				40		pF
Input-Clamp Protection Current		Both inputs	-20		+20	mA
STATIC PERFOMANCE (Note 4)						
Resolution	N		18			Bits
No Missing Codes			18			Bits
Offset Error			-0.5	±0.1	+0.5	mV
			-25	±5	+25	LSB
Offset Temperature Coefficient				±1		µV/°C
Gain Error			-57	±8	+57	LSB
Gain Error Temperature Coefficient				±0.25		ppm/°C
Integral Nonlinearity	INL		-5.5	±2	+5.5	LSB
Differential Nonlinearity	DNL		-0.9	±0.5	+0.9	LSB
Positive Full-Scale Error			-65		+65	LSB

Electrical Characteristics (continued)

(V_{DD} = 4.75V to 5.25V, V_{OVDD} = 2.3V to 5.25V, f_{SAMPLE} = 500kHz, V_{REF} = 5V; T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Analog Input CMR	CMR			12.5		LSB/V
Power-Supply Rejection (Note 5)	PSR	PSR vs. V_{DD}		14.5		LSB/V
Transition Noise				1.65		LSB_{RMS}
REFERENCE (Note 7)						
REF Voltage Input Range	V_{REF}		2.5		V_{DD}	V
REF Input Capacitance				20		pF
REF Load Current				140		µA
DYNAMIC PERFOMANCE (Note 6)						
Signal-to-Noise Ratio (Note 7)	SNR	f_{IN} = 10kHz, V_{REF} = 5V		95		dB
		f_{IN} = 10kHz, V_{REF} = 2.5V		89		dB
Signal-to-Noise Plus Distortion (Note 7)	SINAD	f_{IN} = 10kHz, V_{REF} = 5V		94.7		dB
Spurious-Free Dynamic Range	SFDR		96	106		dB
Total Harmonic Distortion	THD			-106	-96	dB
Intermodulation Distortion (Note 8)	IMD			-115		dBFS
SAMPLING DYNAMICS						
Throughput Sample Rate			0		500	ksps
Transient Response		Full-scale step			400	ns
Full-Power Bandwidth		-3dB point		6		MHz
		-0.1dB point		> 0.2		
Aperture Delay				2.5		ns
Aperture Jitter				10		ps_{RMS}
POWER SUPPLIES						
Analog Supply Voltage	V_{DD}		4.75		5.25	V
Interface Supply Voltage	V_{OVDD}		2.3		5.25	V
Analog Supply Current	I_{VDD}		2.8		3.8	mA
V_{DD} Shutdown Current				0.01	10	µA
Interface Supply Current (Note 9)		V_{OVDD} = 2.3V		1.5	2.0	mA
		V_{OVDD} = 5.25V		4.1	5.0	
OVDD Shutdown Current				0.01	10	µA
Power Dissipation		V_{DD} = 5V, V_{OVDD} = 3.3V		23		mW

Electrical Characteristics (continued)

(V_{DD} = 4.75V to 5.25V, V_{OVDD} = 2.3V to 5.25V, f_{SAMPLE} = 500kHz, V_{REF} = 5V; T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL INPUTS (SDI, SCLK, CNVST)						
Input Voltage High	V_{IH}		0.7 x V_{OVDD}			V
Input Voltage Low	V_{IL}				0.3 x V_{OVDD}	V
Input Hysteresis	V_{HYS}			±0.05 x V_{OVDD}		V
Input Capacitance	C_{IN}			10		pF
Input Current	I_{IN}	V_{IN} = 0V or V_{OVDD}	-10		+10	µA
DIGITAL OUTPUT (SDO)						
Output Voltage High	V_{OH}	I_{SOURCE} = 2mA	V_{OVDD} - 0.4			V
Output Voltage Low	V_{OL}	I_{SINK} = 2mA			0.4	V
Three-State Leakage Current			-10		+10	µA
Three-State Output Capacitance				15		pF
TIMING (Note 9)						
Time Between Conversions	t_{CYC}		2			µs
Conversion Time	t_{CONV}	CNVST rising to data available	1.3		1.5	µs
Acquisition Time	t_{ACQ}	t_{ACQ} = t_{CYC} - t_{CONV}	0.5			µs
CNVST Pulse Width	t_{CNVPW}	$\overline{CS}$ mode	5			ns
SCLK Period ($\overline{CS}$ Mode)	t_{SCLK}	V_{OVDD} > 4.5V	14			ns
		V_{OVDD} > 2.7V	20			
		V_{OVDD} > 2.3V	25			
SCLK Period (Daisy-Chain Mode)	t_{SCLK}	V_{OVDD} > 4.5V	16			ns
		V_{OVDD} > 2.7V	24			
		V_{OVDD} > 2.3V	30			
SCLK Low Time	t_{SCLKL}		6			ns
SCLK High Time	t_{SCLKH}		6			ns
SCLK Falling Edge to Data Valid Delay	t_{DSDO}	V_{OVDD} > 4.5V			12	ns
		V_{OVDD} > 2.7V			18	
		V_{OVDD} > 2.3V			23	
CNVST Low to SDO D15 MSB Valid ($\overline{CS}$ Mode)	t_{EN}	V_{OVDD} > 2.7V			14	ns
		V_{OVDD} < 2.7V			18	
CNVST High or SDI High or Last SCLK Falling Edge to SDO High Impedance	t_{DIS}	$\overline{CS}$ mode			20	ns

Electrical Characteristics (continued)

(V_{DD} = 4.75V to 5.25V, V_{OVDD} = 2.3V to 5.25V, f_{SAMPLE} = 500kHz, V_{REF} = 5V; T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

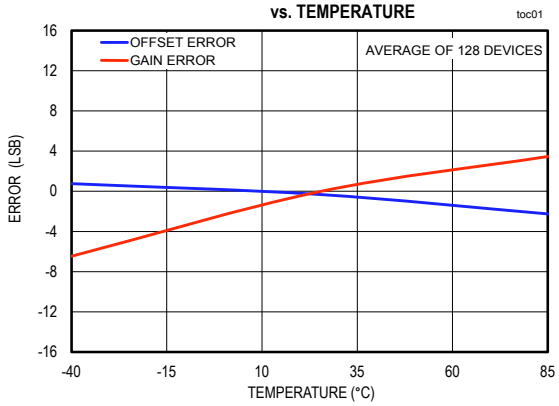
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SDI Valid Setup Time from CNVST Rising Edge	$t_{SSDISCK}$	4-wire $\overline{CS}$ mode	5			ns
SDI Valid Hold Time from SCLK Rising Edge	$t_{HSDISCK}$	4-wire $\overline{CS}$ mode	0			ns
SCLK Valid Setup Time from CNVST Rising Edge	$t_{SSCKCNV}$	Daisy-chain mode	5			ns
SCLK Valid Hold Time from CNVST Rising Edge	$t_{HSCKCNV}$	Daisy-chain mode	5			ns
SDI Valid Setup Time from SCLK Falling Edge	$t_{SSDISCK}$	Daisy-chain mode	6			ns
SDI Valid Hold Time from SCLK Falling Edge	$t_{HSDISCK}$	Daisy-chain mode	0			ns
SDI High to SDO High	$t_{DSDOSDI}$	Daisy-chain mode with busy indicator, V_{OVDD} > 4.5V		15		ns
		V_{OVDD} > 2.3V			20	

Note 2: Maximum and minimum limits are fully production tested over the specified supply voltage range and at a temperature of +25°C and +85°C. Limits below +25°C are guaranteed by design and device characterization.
Note 3: See the *Analog Inputs* and *Overvoltage Input Clamps* sections.
Note 4: See the *Definitions* section.
Note 5: Defined as the change in positive full-scale code transition caused by a ±5% variation in the V_{DD} supply voltage.
Note 6: 10kHz sine wave input, -0.1dB below full scale.
Note 7: See Table 4 for definition of the reference modes.
Note 8: f_{IN1} ~ 9.4kHz, f_{IN2} ~ 10.7kHz, Each tone at -6.1dB below full scale.
Note 9: C_{LOAD} = 65pF on SDO.

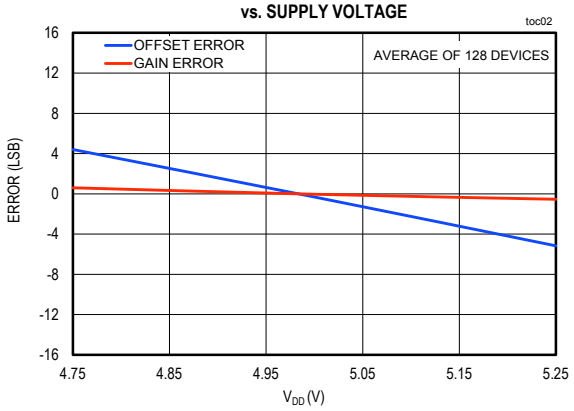
Typical Operating Characteristics

(V_{DD} = 5.0V, V_{OVDD} = 3.3V, f_{SAMPLE} = 500kHz, V_{REF} = 5V; T_A = +25°C, unless otherwise noted.)

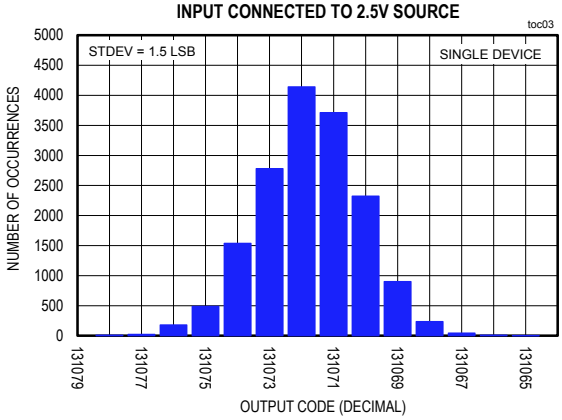
OFFSET AND GAIN ERROR vs. TEMPERATURE



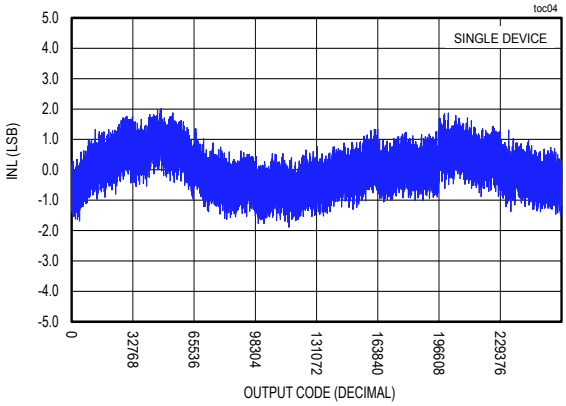
OFFSET AND GAIN ERROR vs. SUPPLY VOLTAGE



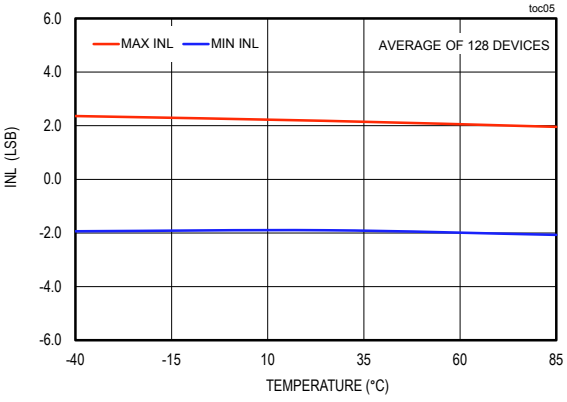
OUTPUT NOISE HISTOGRAM WITH INPUT CONNECTED TO 2.5V SOURCE



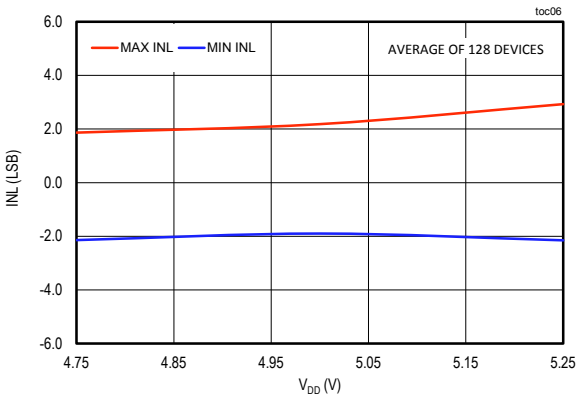
INTEGRAL NONLINEARITY vs. CODE



INL vs. TEMPERATURE



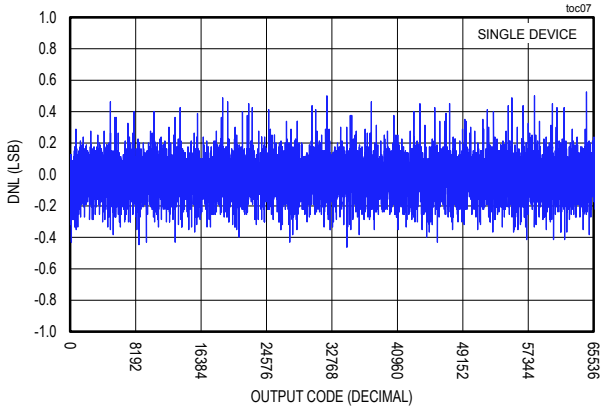
INL vs. V_{DD} SUPPLY VOLTAGE



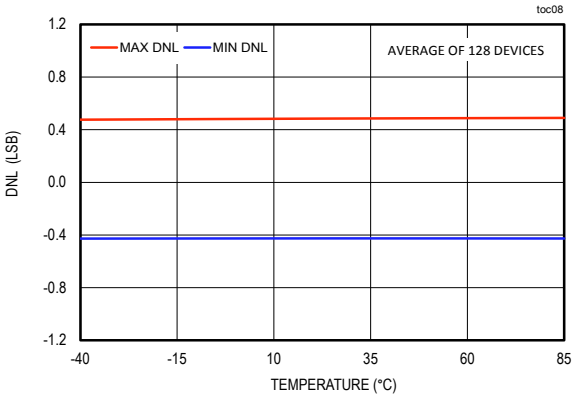
Typical Operating Characteristics (continued)

(V_{DD} = 5.0V, V_{OVDD} = 3.3V, f_{SAMPLE} = 500kHz, V_{REF} = 5V; T_A = +25°C, unless otherwise noted.)

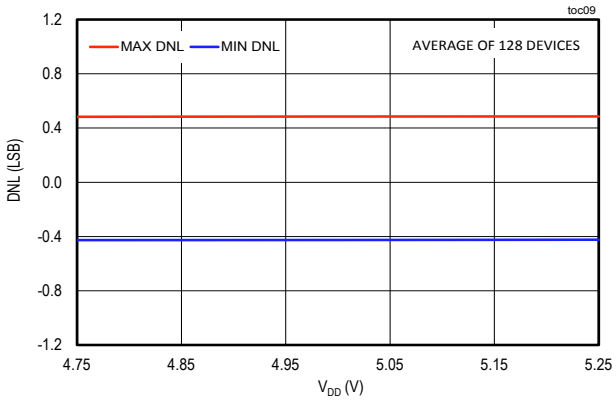
DIFFERENTIAL NONLINEARITY vs. CODE



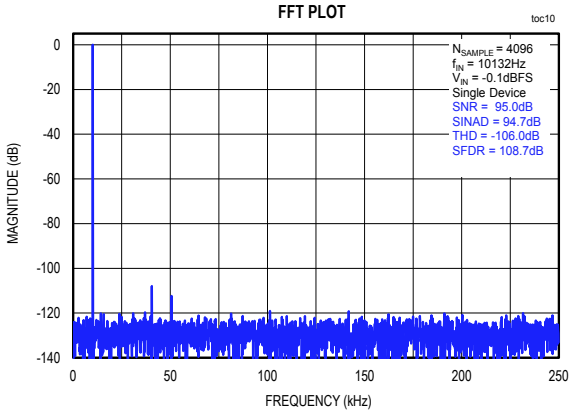
DNL vs. TEMPERATURE



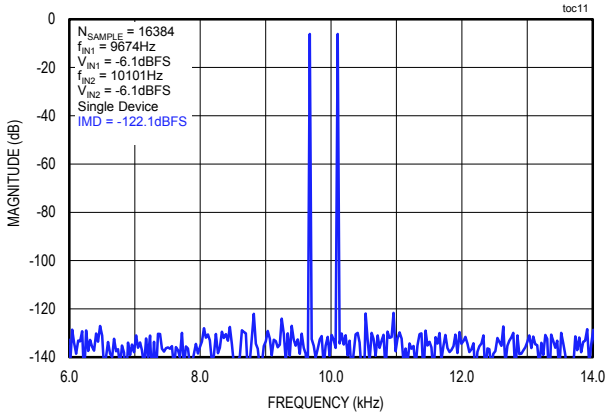
DNL vs. V_{DD} SUPPLY VOLTAGE



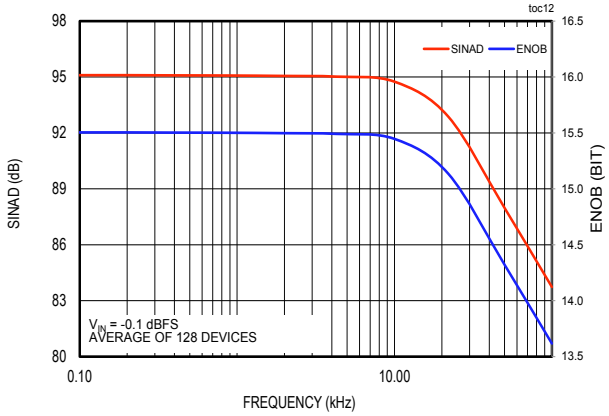
FFT PLOT



TWO TONES IMD



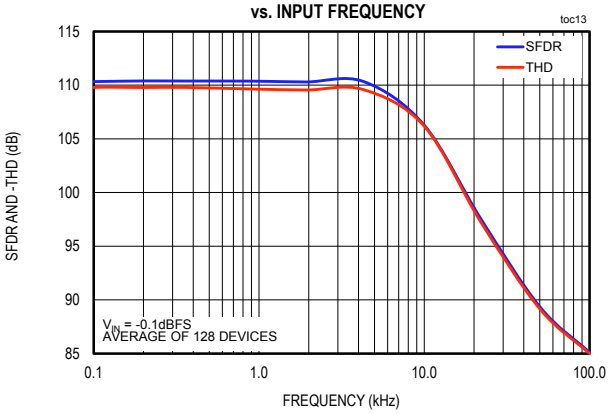
SINAD and ENOB vs. FREQUENCY



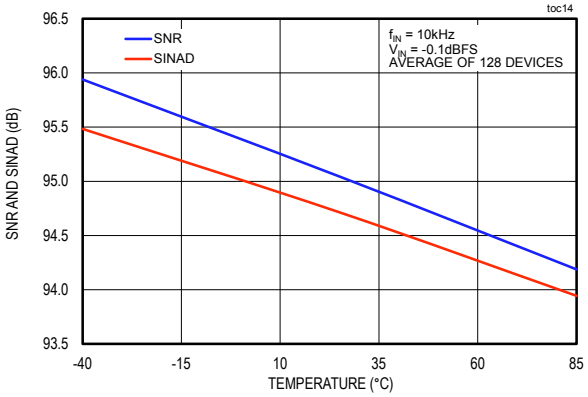
Typical Operating Characteristics (continued)

(V_{DD} = 5.0V, V_{OVDD} = 3.3V, f_{SAMPLE} = 500kHz, V_{REF} = 5V; T_A = +25°C, unless otherwise noted.)

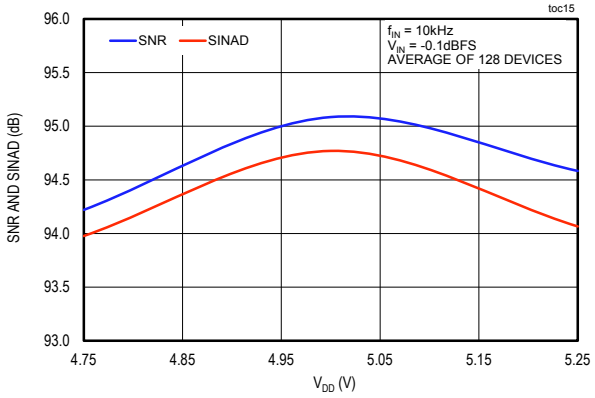
SFDR and -THD vs. INPUT FREQUENCY



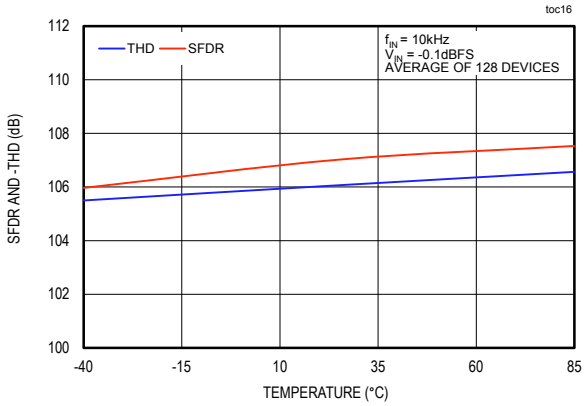
SNR AND SINAD vs. TEMPERATURE



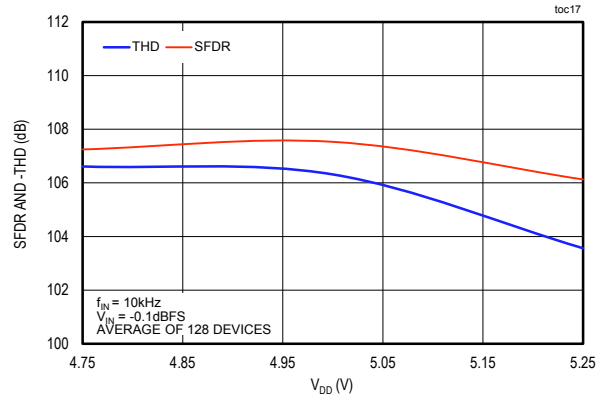
SNR AND SINAD vs. V_{DD} SUPPLY VOLTAGE



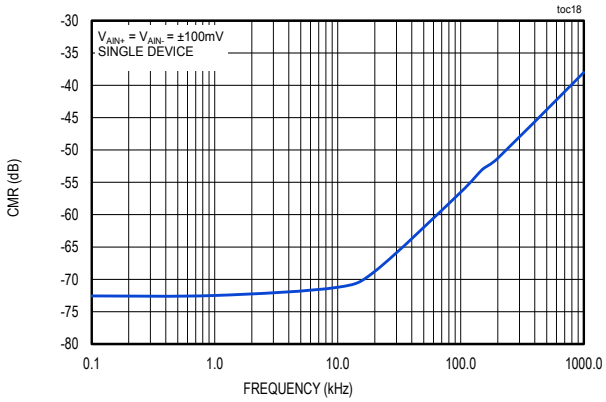
SFDR AND THD vs. TEMPERATURE



THD AND SFDR vs. V_{DD} SUPPLY VOLTAGE



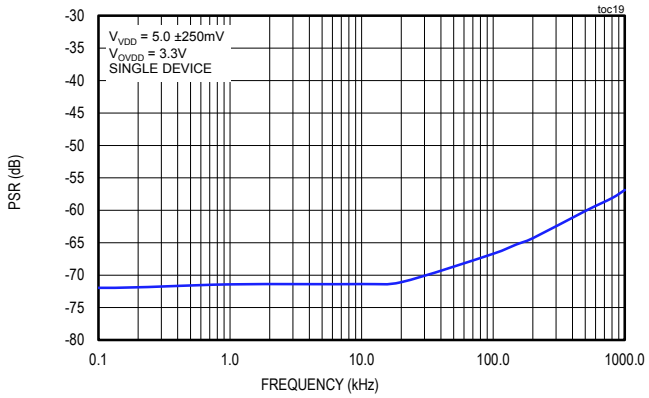
CMR vs. INPUT FREQUENCY



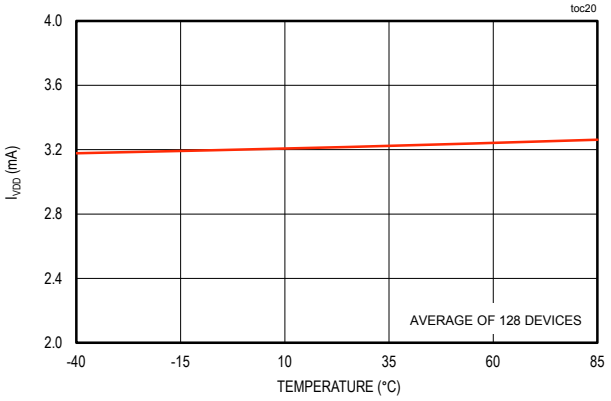
Typical Operating Characteristics (continued)

(V_{DD} = 5.0V, V_{OVDD} = 3.3V, f_{SAMPLE} = 500kHz, V_{REF} = 5V; T_A = +25°C, unless otherwise noted.)

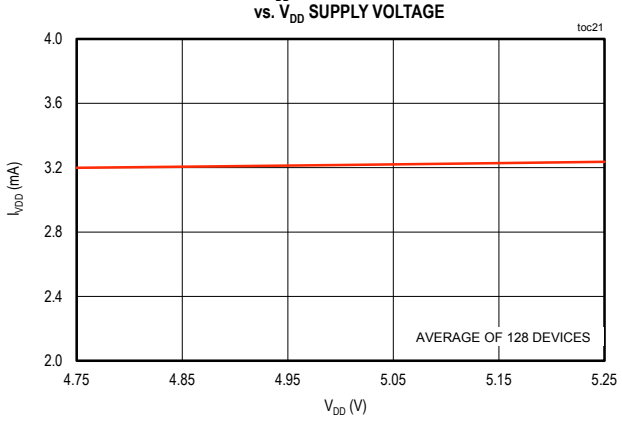
PSR vs. INPUT FREQUENCY



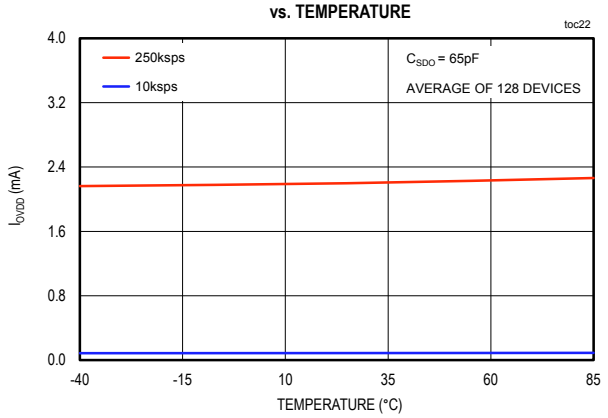
V_{DD} SUPPLY CURRENT vs. TEMPERATURE



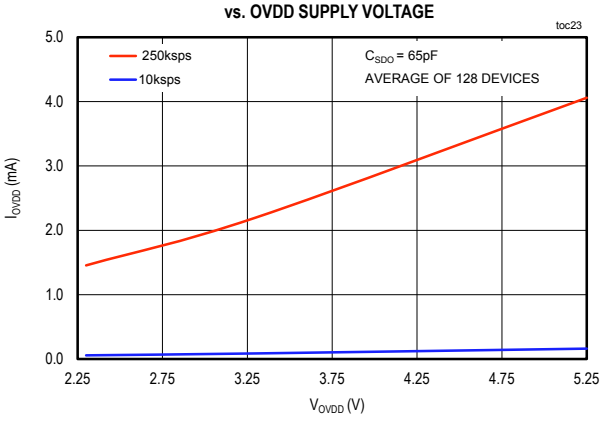
V_{DD} SUPPLY CURRENT vs. V_{DD} SUPPLY VOLTAGE



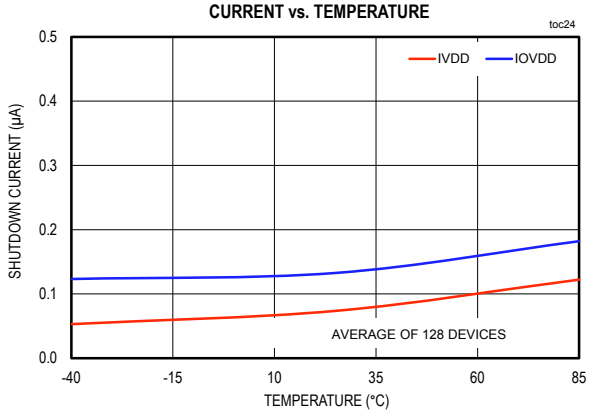
OVDD SUPPLY CURRENT vs. TEMPERATURE



OVDD SUPPLY CURRENT vs. OVDD SUPPLY VOLTAGE

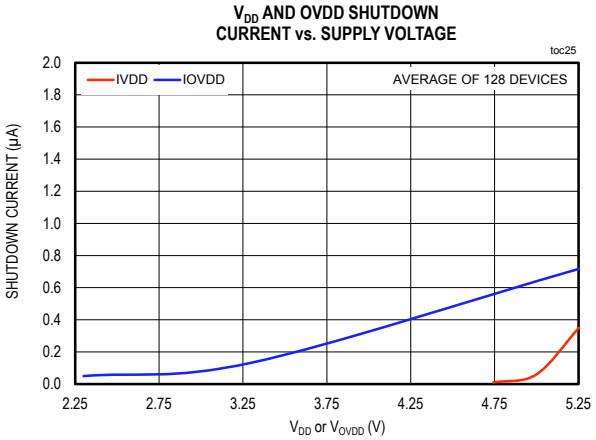


ANALOG AND DIGITAL SHUTDOWN CURRENT vs. TEMPERATURE

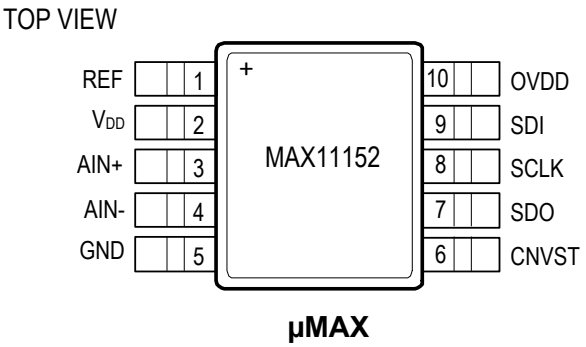


Typical Operating Characteristics (continued)

(V_{DD} = 5.0V, V_{OVDD} = 3.3V, f_{SAMPLE} = 500kHz, V_{REF} = 5V; T_A = +25°C, unless otherwise noted.)



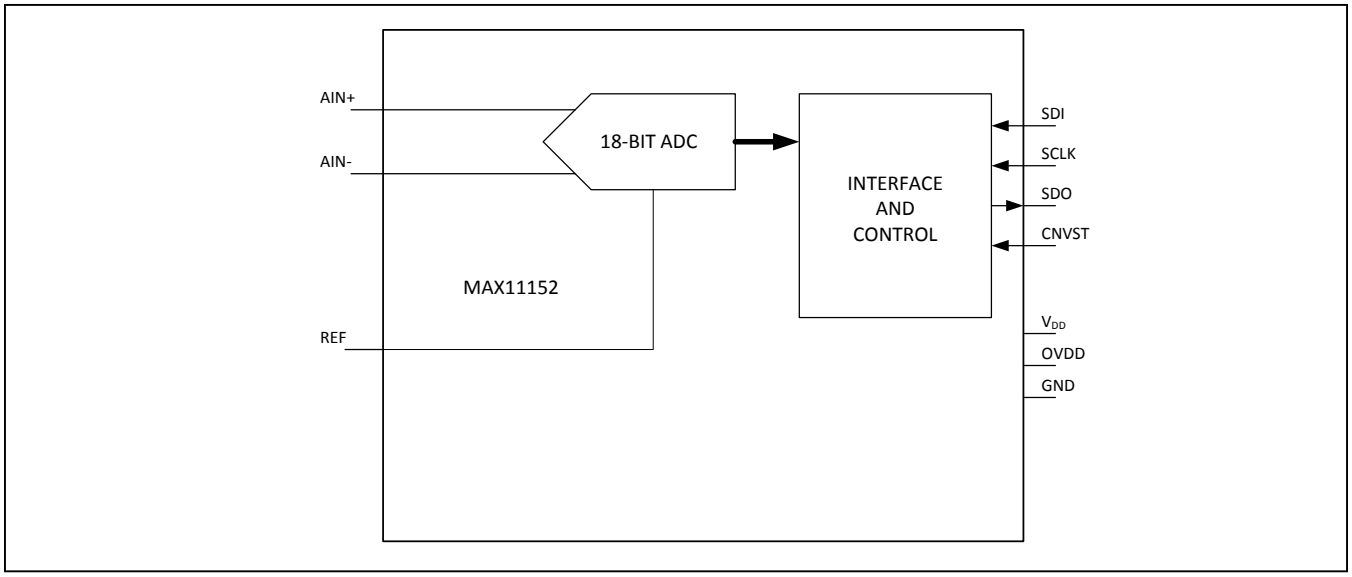
Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1	REF	External Reference Input. Bypass to GND in close proximity with a X5R or X7R 10µF 16V chip. See the *Layout, Grounding, and Bypassing* section..
2	V_{DD}	Analog Power Supply. Bypass V_{DD} to GND with a 0.1µF capacitor as close as possible to each device and one 10µF capacitor per board.
3	AIN+	Positive Analog Input
4	AIN-	Negative Analog Input. Connect AIN- to the analog ground plane or to a remote sense ground.
5	GND	Power-Supply Ground
6	CNVST	Conversion Start Input. The rising edge of CNVST initiates the conversions and selects the interface mode: daisy-chain or $\overline{CS}$. In $\overline{CS}$ mode, set CNVST low to enable the SDO output. In daisy-chain mode, read the data when CNVST is high.
7	SDO	Serial Data Output. SDO transitions on the falling edge of SCLK.
8	SCLK	Serial Clock Input. Clocks data out of the serial interface when the device is selected.
9	SDI	Serial Data Input and Mode Select Input. Daisy-chain mode is selected if SDI is low during the CNVST rising edge. In this mode, SDI is used as a data input to daisy-chain the conversion results of two or more ADCs onto a single SDO line. $\overline{CS}$ mode is selected if SDI is high during the CNVST rising edge. In this mode, either SDI or CNVST can enable the serial output signals when low. If SDI or CNVST is low when the conversion is completed, the busy indicator feature is enabled.
10	OVDD	Digital Power Supply. OVDD can range from 2.3V to V_{DD}. Bypass OVDD to GND with a 0.1µF capacitor for each device and one 10µF per board.

Functional Diagram



Detailed Description

The MAX11152 is an 18-bit single-channel, pseudo-differential ADC with maximum throughput rates of 500ksps. This ADC measures an unipolar input voltage interval from 0V to V_{REF}. The external reference interval ranges from +2.5V to V_{DD}. Both inputs (AIN+ and AIN-) are sampled with a integrated pseudo-differential track-and-hold (T/H) exhibiting no pipeline delay or latency, making this ADC ideal for multiplexed channel applications.

The MAX11152 inputs are protected for up to ±20mA of overrange current. This ADC is powered from a 4.75V to 5.25V analog supply (V_{DD}) and a separate 2.3V to 5.25V digital supply (OVDD). The MAX11152 requires 500ns to acquire the input sample on an internal track-and-hold and then convert the sampled signal to 18 bits of resolution using an internally clocked converter.

Analog Inputs

The MAX11152 ADC consists of a true sampling pseudo-differential input stage with high-impedance, capacitive inputs. The internal T/H circuitry features a small-signal bandwidth of about 6MHz to provide 18-bit accurate sampling in 500ns. This allows for accurate sampling of a number of scanned channels through an external multiplexer.

The MAX11152 on the AIN+ input accurately converts input signals in the interval from AIN- to (V_{REF} + AIN-).

AIN+ has a maximum input interval from -0.1V to (V_{DD} + 0.1V).AIN- has a maximum input interval from -0.1V to +0.1V.

The MAX11152 performs a true differential sampling on inputs between AIN+ and AIN- with good common-mode rejection (see the *Typical Operating Circuit*). Connecting AIN- to the ground reference of the input signal source improves the rejection of common-mode noise of remote transducer inputs.

Overvoltage Input Clamps

The MAX11152 includes an input clamping circuit that activates when the input voltage at AIN+ is above (V_{DD} + 300mV) or below -300mV. The clamp circuit remains high impedance while the input signal is within the range of -100mV to (V_{DD} + 100mV) and draws little to no current. However, when the input signal exceeds this range the clamps begin to turn on. Consequently, to obtain the highest accuracy, ensure that the input voltage does not exceed the range of -100mV to (V_{DD} + 100mV).

To make use of the input clamps, connect a resistor (R_S) between the AIN+ input and the voltage source to limit the voltage at the analog input and to ensure the fault current into the devices does not exceed ±20mA. Note that the voltage at the AIN+ input pin limits to approximately 7V during a fault condition so the following equation can be used to calculate the value of R_S:

$$\frac{V_{FAULT\,MAX} \quad 7V}{20mA}$$

where $V_{FAULTMAX}$ is the maximum voltage that the source produces during a fault condition.

Figure 1 and Figure 2 illustrate the clamp circuit voltage current characteristics for a source impedance R_S = 1170Ω. While the input voltage is within the -300mV to (V_{DD} + 300mV) range, no current flows in the input clamps. Once the input voltage goes beyond this voltage range, the clamps turn on and limit the voltage at the input pin.

Reference

The MAX11152 requires a low-impedance reference source on the REF pin to support 18-bit accuracy.

Maxim offers a wide range of precision references ideal for 18-bit accuracy. Table 1 lists some of the options recommended.

It is recommended that a reference buffer or the output of one of these recommended reference sources be used to drive this pin. In addition, an external bypass capacitor of at least 10µF with low inductance and ESR should be placed as close as possible to the REF pin, thus minimizing the PCB inductance. X7R or X5R ceramic capacitors in a 1210 case size or smaller have been found to provide adequate bypass performance. Y5U or Z5U ceramic capacitors are not recommended due to their high voltage and temperature coefficients.

Table 1. MAX11152 External Reference Recommendations

PART	V_{OUT} (V)	TEMPERATURE COEFFICIENT (MAX)	INITIAL ACCURACY (%)	NOISE (0.1Hz TO 10Hz) (μV_{P-P})	PACKAGE
MAX6126	2.5, 3, 4.096, 5.0	3 (A), 5 (B)	0.06	1.35	µMAX-8 SO-8
MAX6325	2.5	1	0.04	1.5	SO-8
MAX6341	4.096	1	0.02	2.4	SO-8

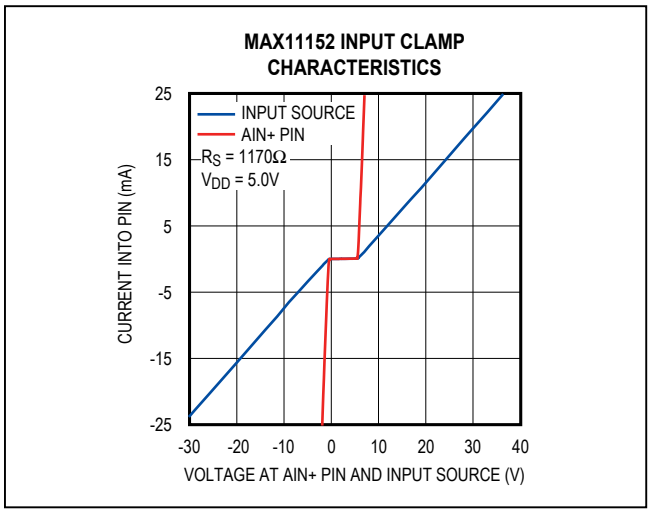


Figure 1. Input Clamp Characteristics

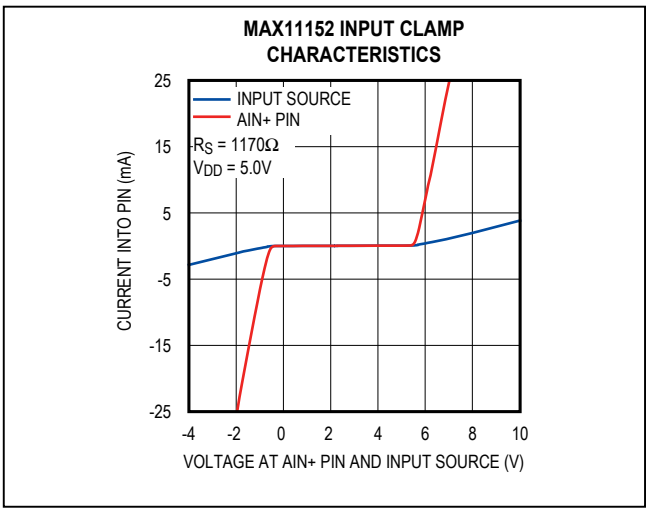


Figure 2. Input Clamp Characteristics (Zoom In)

Input Amplifier

The conversion results are accurate when the ADC acquires the input signal for an interval longer than the input signal's worst-case settling time. The ADC input sampling capacitor charges during the acquisition period. During this acquisition period, the settling of the sampled voltage is affected by the source resistance and the input sampling capacitance. Sampling error can be estimated by modeling the time constant of the total input capacitance and the driving source impedance.

Although the MAX11152 is easy to drive, an amplifier buffer is recommended if the source impedance is such that when driving a switch capacitor of ~40pF a significant settling error in the desired sampling period will occur. If this is the case, it is recommended that a configuration shown in the *Typical Operating Circuit* is used where at least a 4.7nF capacitor is attached to the AIN+ pin. This capacitance reduces the size of the transient at the start of the acquisition period, which in some buffers will cause an input signal dependent offset.

Regardless of whether an external buffer amp is used or not, the time constant, $R_{SOURCE} \times C_{LOAD}$, of the input should not exceed $t_{ACQ}/13$, where R_{SOURCE} is the total signal source impedance, C_{LOAD} is the total capacitance at the ADC input (external and internal) and t_{ACQ} is the acquisition period. Thus to obtain accurate sampling in a 500ns acquisition time a source impedance of less than 950Ω should be used if driving the ADC directly. When driving the ADC from a buffer, series resistance (5Ω to 15Ω typical) is recommended between the amplifier and the external input capacitance as shown in the *Typical Operating Circuit*.

These amplifier features help to select the ADC driver.

1) Fast settling time: For multichannel multiplexed applications the driving operational amplifier must be able to settle to 18-bit resolution when a full-scale step is applied during the minimum acquisition time.
2) Low noise: It is important to ensure that the driver amplifier has a low average noise density appropriate for the desired bandwidth of the application. In the case of the MAX11152, settling in a 0.5µs duration requires an RC filter bandwidth of approximatly 4.2MHz. With this bandwidth, it is preferable to use an amplifier that will produce an output noise-spectral density of less than 3.5nV/√Hz to ensure that the overall SNR is not degraded significantly. It is recommended to insert an external RC filter at the MAX11152 AIN+ input to attenuate out-of-band input noise and preserve the ADC's SNR. The effective RMS noise at the MAX11152 AIN+ input is 27µV, thus additional noise from a buffer circuit should be significantly lower to achieve the maximum SNR performance.
3) THD performance: The input buffer amplifier used should have a better THD performance than the MAX11152 to ensure the THD of the digitized signal is not degraded.

Table 2 summarizes the operational amplifiers that are compatible with the MAX11152. The MAX9632 has sufficient bandwidth, low enough noise and distortion to support the full performance of the MAX11152. The MAX9633 is a dual amplifier and supports buffering for true pseudo-differential sampling.

Transfer Function

The ideal transfer characteristic for the MAX11152 is shown in Figure 3. The precise location of various points on the transfer function are given in Table 3.

Table 2. List of Recommended ADC Driver Op Amps for MAX11152

AMPLIFIER	INPUT-NOISE DENSITY (nV/√Hz)	SMALL-SIGNAL BANDWIDTH (MHz)	SLEW RATE (V/µs)	THD (dB)	I_{CC} (mA)	COMMENTS
MAX9632	1	55	30	-128	3.9	Low noise, THD at 10kHz
MAX9633	3	27	18	-128	3.5	Low noise, dual amp, THD at 10kHz

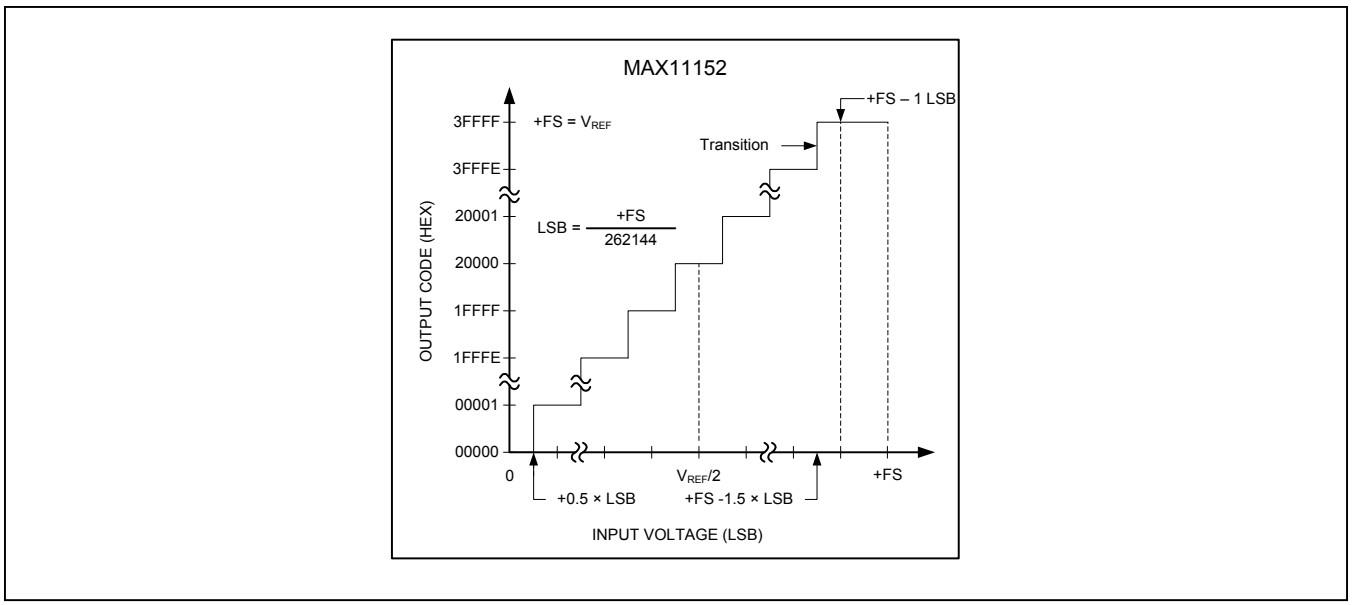


Figure 3. Unipolar Transfer Function

Table 3. Transfer Function Example

CODE TRANSITION	BIPOLAR INPUT (V)	DIGITAL OUTPUT CODE (HEX)
+FS - 1.5 LSB	4.9999714	3FFFE - 3FFFF
Midscale + 0.5 LSB	2.5000095	20000 - 20001
Midscale	2.500000	20000
Midscale - 0.5 LSB	2.4999905	1FFFF - 20000
0.5 LSB	0.0000095	00000 - 00001

Digital Interface

The MAX11152 includes three digital inputs (CNVST, SCLK, and SDI) and a single digital output (SDO). The ADC can be configured for one of six interface modes, allowing the device to support a wide variety of application needs.

The 3-wire and 4-wire $\overline{CS}$ interface modes are compatible with SPI, QSPI, digital hosts, and DSPs. The 3-wire interface uses CNVST, SCLK, and SDO for minimal wiring complexity and is ideally suited for isolated applications. The 4-wire interface allows CNVST to be independent of output data readback (SDI) affording the highest level of individual device control. This configuration is useful for low jitter or multichannel, simultaneously sampled applications.

The 3-wire daisy-chain mode is the easiest way to configure a multichannel, simultaneous-sampling system. This system is built by cascading multiple ADCs into a shift register structure. The CNVST and SCLK inputs are common to all ADCs, while the SDO output of one device feeds the SDI input of the next device in the chain. The 3-wire interface is simply the CNVST, SCLK, and SDO of the last ADC in the chain.

The selection of $\overline{CS}$ or daisy-chain modes are controlled by the SDI logic level during the rising edge of CNVST. The $\overline{CS}$ mode is selected if SDI is high and the daisy-chain mode is selected if SDI is low. If SDI and CNVST are connected together, the daisy-chain mode is selected.

In each of the three modes described above (3-wire and 4-wire $\overline{CS}$ mode and daisy-chain mode), the user must externally timeout the maximum ADC conversion time before commencing readback. Alternatively, the MAX11152 offers a busy indicator feature on SDO in each mode to eliminate external timer circuits.

When busy indication is enabled, SDO provides a busy indicator bit to signal the end of conversion. One additional SCLK is required to flush the SDO busy indication bit prior to reading back the data. Busy indicator is enabled in $\overline{CS}$ mode if CNVST or SDI is low when the ADC conversion completes. In daisy-chain mode, the busy indicator is selected based on the state of SCLK at the rising edge of CNVST. If SCLK is high, the busy indicator is enabled; otherwise, the busy indicator is not enabled.

The following sections provide specifics for each of the six serial interface modes. Due to the possibility of performance degradation, digital activity should only occur after conversion is completed or limited to the first half of the conversion phase. Having SCLK or SDI transitions near the sampling instant can also corrupt the input sample accuracy. Therefore, keep the digital inputs quiet for approximately 25ns before and 10ns after the rising edge of CNVST. These times are denoted as $t_{SSCSKCNV}$ and $t_{HSCKCNV}$ in all subsequent timing diagrams.

In all interface modes, the data on SDO is valid on both SCLK edges. However, input setup time into the receiving host will be maximized when data is clocked into that host on the falling SCLK edge. Doing so will allow for higher data transfer rates between the MAX11152 and the receiving host and consequently higher converter throughput.

In all interface modes all data bits from a previous conversion must be read before reading bits from a new conversion. If in a given conversion, too few SCLK falling edges are provided and all data bits are not read out in one conversion/acquisitions cycle, the remaining unread data bits will be output on the next conversion/acquisitions cycle. Thus, if insufficient SCLK falling edges are provided in a single conversion/acquisition cycle, the output data will appear to have been truncated in every other conversion. This is the user's indication that there are insufficient SCLK falling edges in a given conversion/acquisition cycle in their stimulus pattern.

Shutdown

In all interface modes, the MAX11152 can be placed into a shutdown state by holding SCLK high while pulling CNVST from high to low. Supply current is reduced to less than 10µA on both V_{DD} and OVDD supplies (see Figure 4). To wake up from shutdown mode, hold SCLK low and pull CNVST from high to low.

ADC Modes of Operation

The MAX11152's six modes of operation are summarized in Table 4. For each of the six modes of operation a typical application model and list of benefits are described.

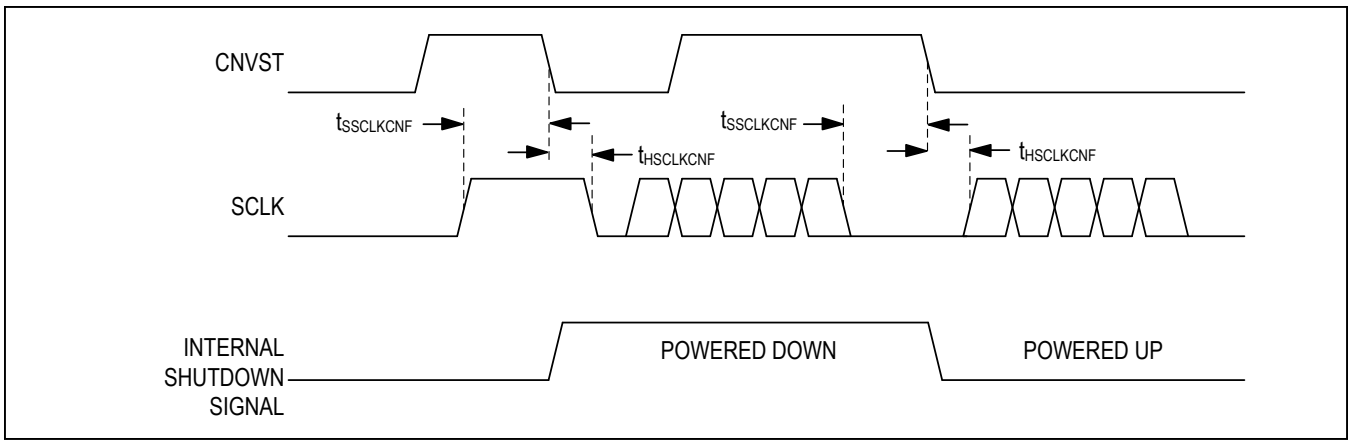


Figure 4. Entering and Exiting Shutdown Mode

Table 4. ADC Modes of Operation

MODE	TYPICAL APPLICATION AND BENEFITS
$\overline{CS}$ Mode 3-Wire, No-Busy Indicator	Single ADC connected to a SPI-compatible digital host. Minimal wiring complexity; ideally suited for isolated applications.
$\overline{CS}$ Mode 3-Wire, with Busy Indicator	Single ADC connected to a SPI-compatible digital host with interrupt input. Minimal wiring complexity; ideally suited for isolated applications.
$\overline{CS}$ Mode 4-Wire, No-Busy Indicator	Multiple ADCs connected to a SPI-compatible digital host. CNVST used for acquisition and conversion; ideally suited for low jitter applications and simultaneous sampling. SDI used to control data readback.
$\overline{CS}$ Mode 4-Wire, with Busy Indicator	Single ADC connected to aSPI-compatible digital host with interrupt input. CNVST used for acquisition and conversion; ideally suited for low jitter applications.
Daisy-Chain Mode, No-Busy Indicator	Multiple ADCs connected to a 3-wire serial interface. Minimal wiring complexity; ideally suited for multichannel, simultaneous sampled, isolated applications.
Daisy-Chain Mode, with Busy Indicator	Multiple ADCs connected to 3-wire serial interface with busy indicator. Minimal wiring complexity; ideally suited for multichannel simultaneous-sampled, isolated applications.

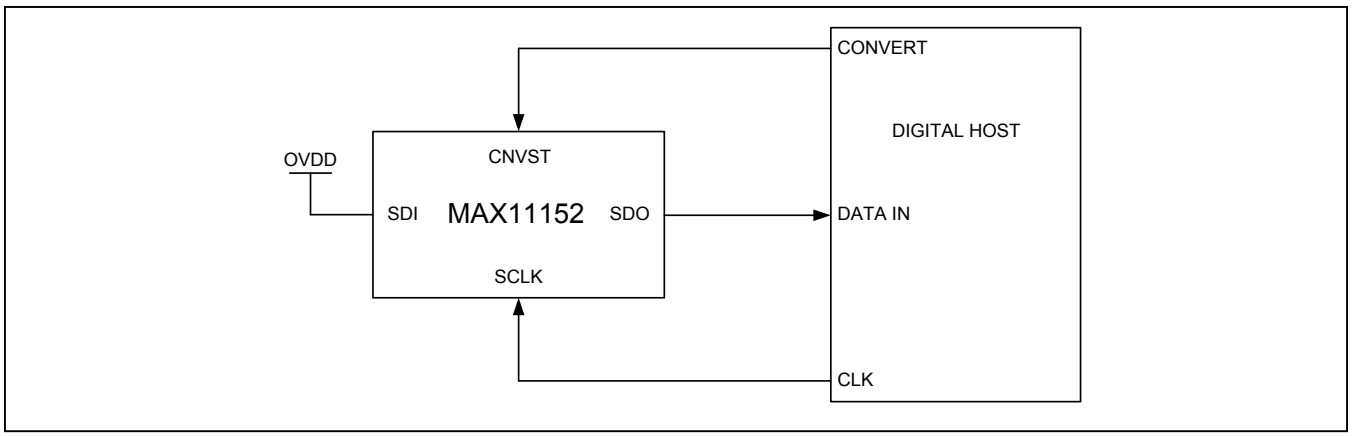


Figure 5. $\overline{CS}$ Mode, 3-Wire No-Busy Indicator Connection Diagram (SDI High)

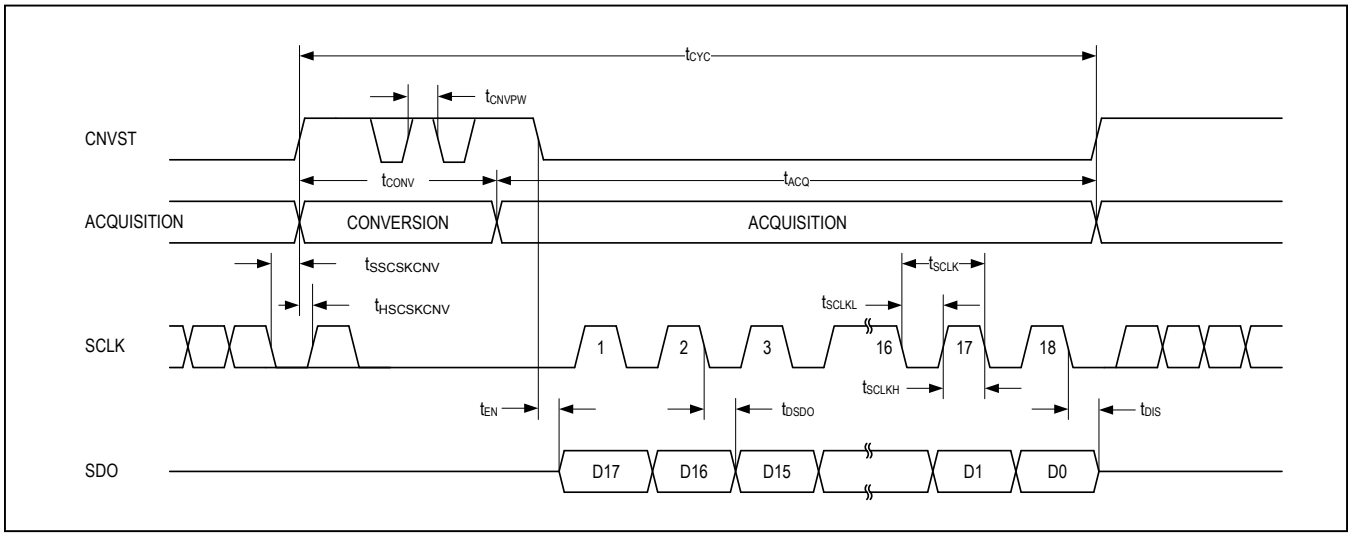


Figure 6. $\overline{CS}$ Mode 3-Wire, No-Busy Indicator Serial Interface Timing (SDI High)

$\overline{CS}$ Mode 3-Wire, No Busy Indicator

The 3-wire $\overline{CS}$ mode with no busy indicator is ideally suited for isolated applications that require minimal wiring complexity. In Figure 5, a single ADC is connected to an SPI-compatible digital host with corresponding timing given in Figure 6.

With SDI connected to OVDD, a rising edge on CNVST completes the acquisition, initiates the conversion and forces SDO to high impedance. The conversion continues to completion irrespective of the state of CNVST, allowing CNVST to be used as a select line for other devices on the board. CNVST must be returned high before the minimum conversion time and held high until the maximum conversion time to avoid generating the busy signal indicator.

When the conversion is complete, the MAX11152 enters the acquisition phase. Drive CNVST low to output the MSB onto SDO. The remaining data bits are then clocked by subsequent SCLK falling edges. SDO returns to high impedance after the 18th SCLK falling edge or when CNVST goes high.

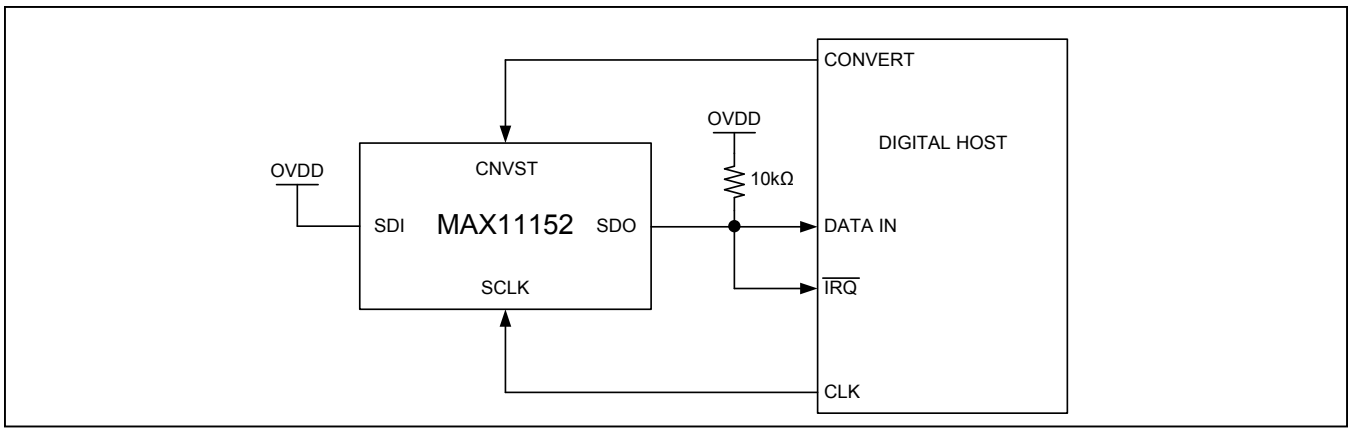


Figure 7. $\overline{CS}$ Mode 3-Wire With Busy Indicator Connection Diagram (SDI HIgh)

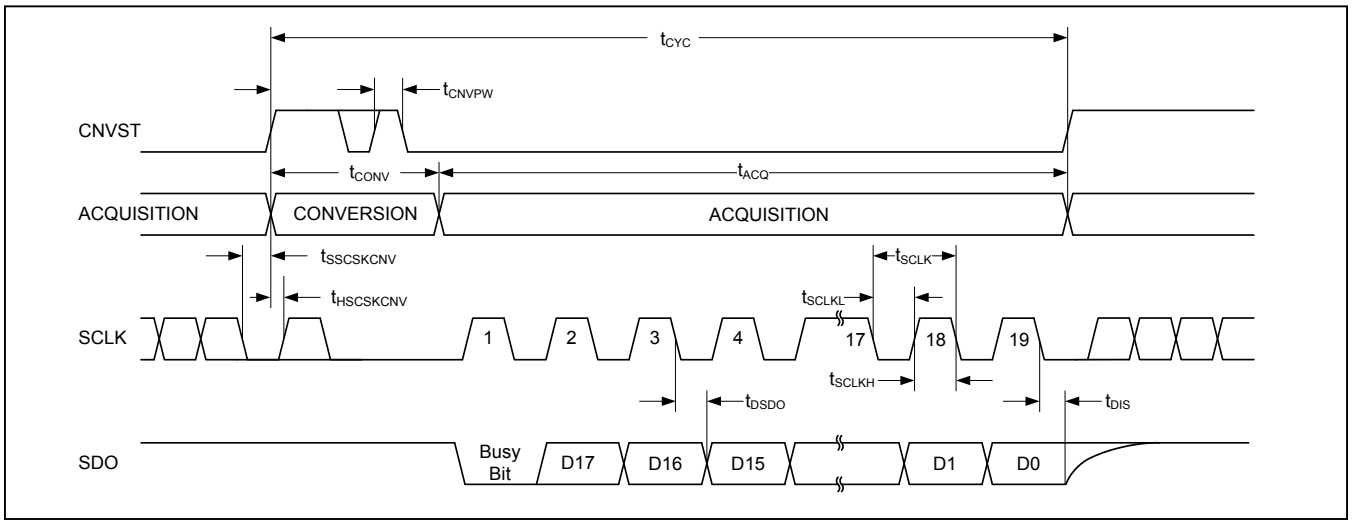


Figure 8. $\overline{CS}$ Mode 3-Wire With Busy Indicator Serial Interface Timing (SDI High)

$\overline{CS}$ Mode 3-Wire, With Busy Indicator

The 3-wire $\overline{CS}$ mode with busy indicator is shown in Figure 7 where a single ADC is connected to an SPI-compatible digital host with interrupt input. The corresponding timing is given in Figure 8.

With SDI connected to OVDD, a rising edge on CNVST completes the acquisition, initiates the conversion and forces SDO to high impedance. The conversion continues to completion irrespective of the state of CNVST allowing CNVST to be used as a select line for other devices on the board. CNVST must be returned low before the minimum conversion time and held low until the busy signal is generated. When the conversion is complete, SDO transitions from high impedance to a low logic level signaling to the digital host through the interrupt input that data readback can commence. The MAX11152 then enters the acquisition phase. The data bits are clocked out, MSB first, by subsequent SCLK falling edges. SDO returns to high impedance after the 19th SCLK falling edge or when CNVST goes high and is then pulled to OVDD through the external pullup resistor.

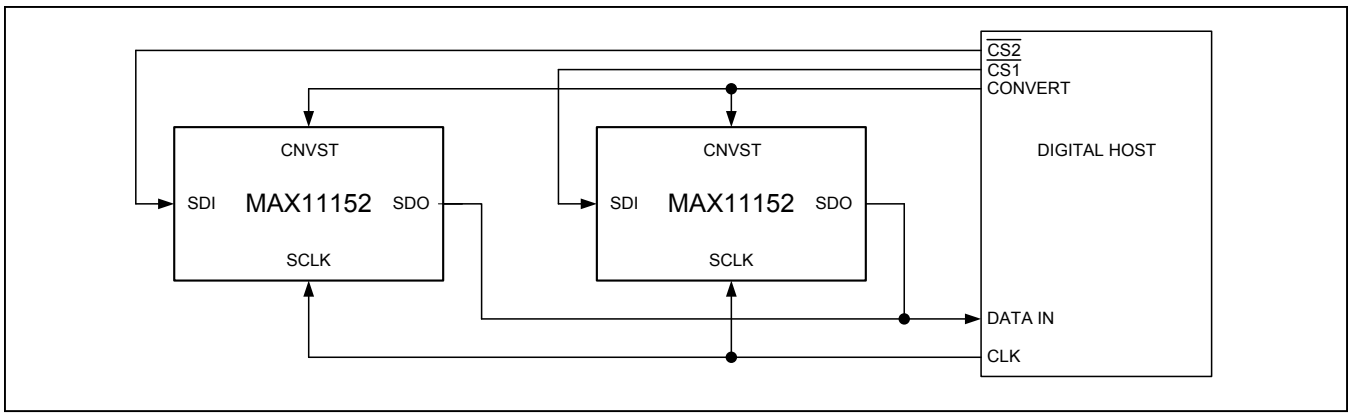


Figure 9. $\overline{CS}$ Mode 4-Wire, No-Busy Indicator Connection Diagram

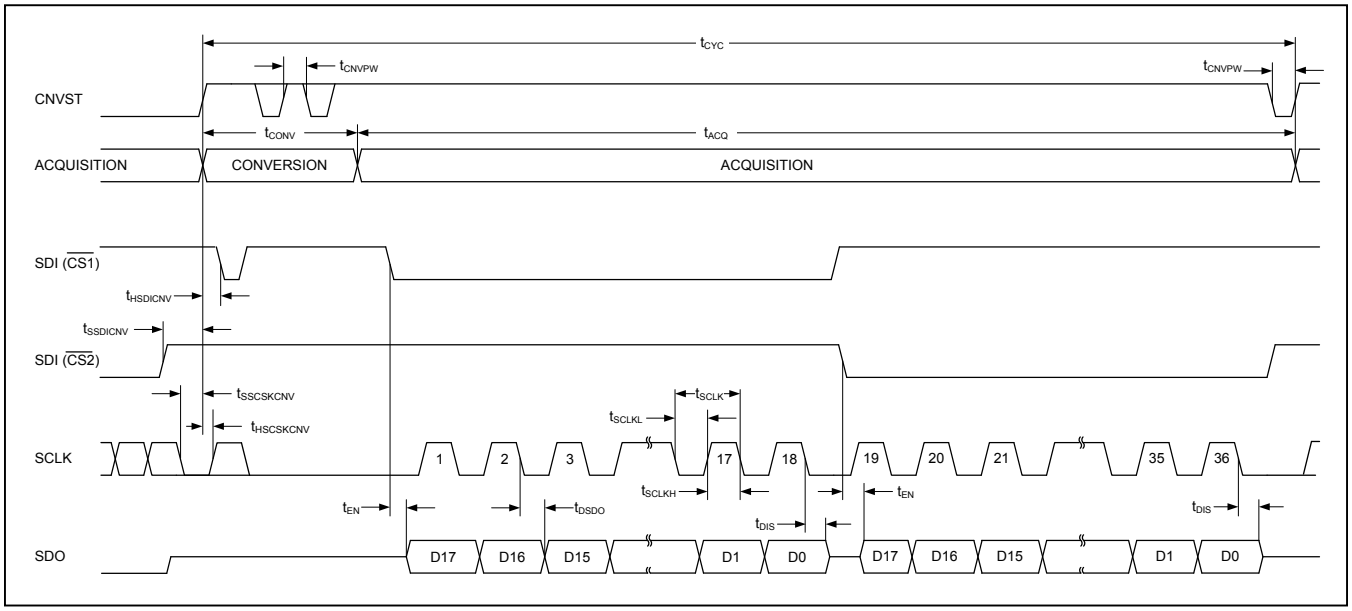


Figure 10. $\overline{CS}$ Mode 4-Wire, No-Busy Indicator Serial Interface Timing

$\overline{CS}$ Mode 4-Wire, No Busy Indicator

The 4-wire $\overline{CS}$ mode with no busy indicator is ideally suited for multichannel applications. In this case, the CNVST pin may be used for low-jitter simultaneous sampling while the SDI pin(s) are used to control data readback. In Figure 9, two ADCs are connected to an SPI-compatible digital host with corresponding timing given in Figure 10.

With SDI high, a rising edge on CNVST completes the acquisition, initiates the conversion, and forces SDO to high impedance. This mode requires CNVST to be held high during the conversion and data readback phases. Note that if CNVST and SDI are low, SDO is driven low. During the conversion, the SDI pin(s) can be used as a select line for other devices on the board, but must be returned high before the minimum conversion time and held high until the maximum conversion time to avoid generating the busy signal indicator.

When the conversion is complete, the MAX11152 enters the acquisition phase. ADC data is read by driving its respective SDI line low, outputting the MSB onto SDO. The remaining data bits are then clocked by subsequent SCLK falling edges. SDO returns to high impedance after the 18th SCLK falling edge or when CNVST goes high.

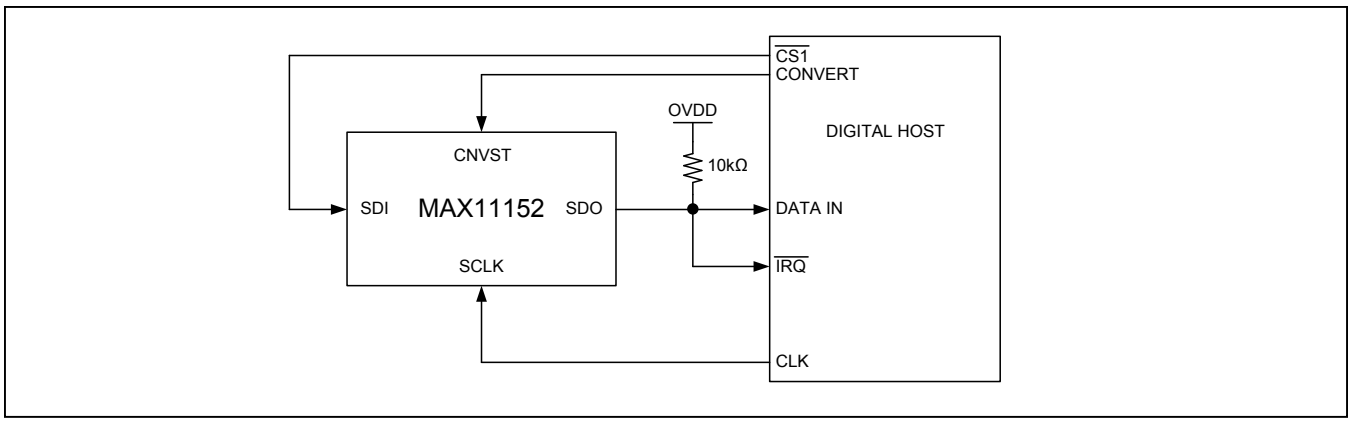


Figure 11. $\overline{CS}$ Mode 4-Wire with Busy Indicator Connection Diagram

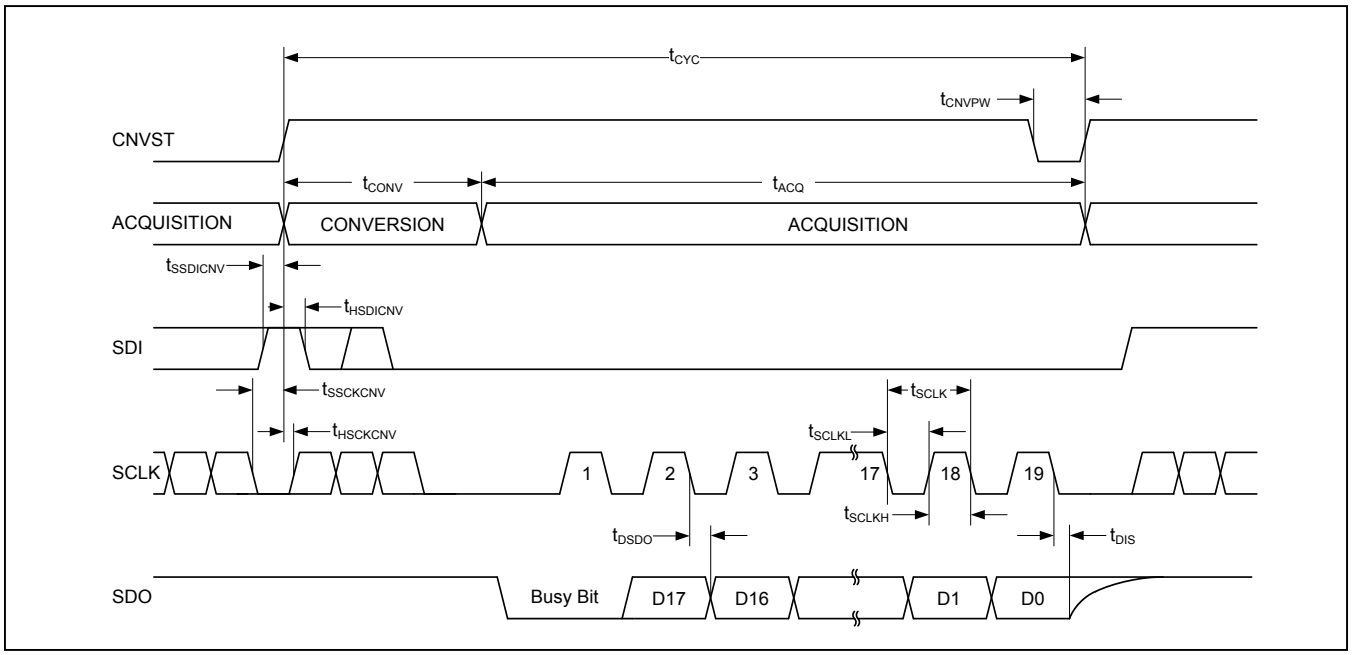


Figure 12. $\overline{CS}$ Mode 4-Wire with Busy Indicator Serial Interface Timing

$\overline{CS}$ Mode 4-Wire, With Busy Indicator

The 4-wire $\overline{CS}$ mode with busy indicator is shown in Figure 11 where a single ADC is connected to an SPI-compatible digital host with interrupt input. The corresponding timing is given in Figure 12. This mode is ideally suited for single ADC applications where the CNVST pin may be used for low-jitter sampling while the SDI pin is used for data readback.

With SDI high, a rising edge on CNVST completes the acquisition, initiates the conversion and forces SDO to high impedance. This mode requires CNVST to be held high during the conversion and data readback phases. Note that if CNVST and SDI are low, SDO is driven low. During the conversion, the SDI pin can be used as a select line for other devices on the board, but must be returned low before the minimum conversion time and held low until the busy signal is generated.

When the conversion is complete, SDO transitions from high impedance to a low logic level signaling to the digital host through the interrupt input that data readback can commence. The MAX11152 then enters the acquisition phase. The data bits are clocked out, MSB first, by sub-

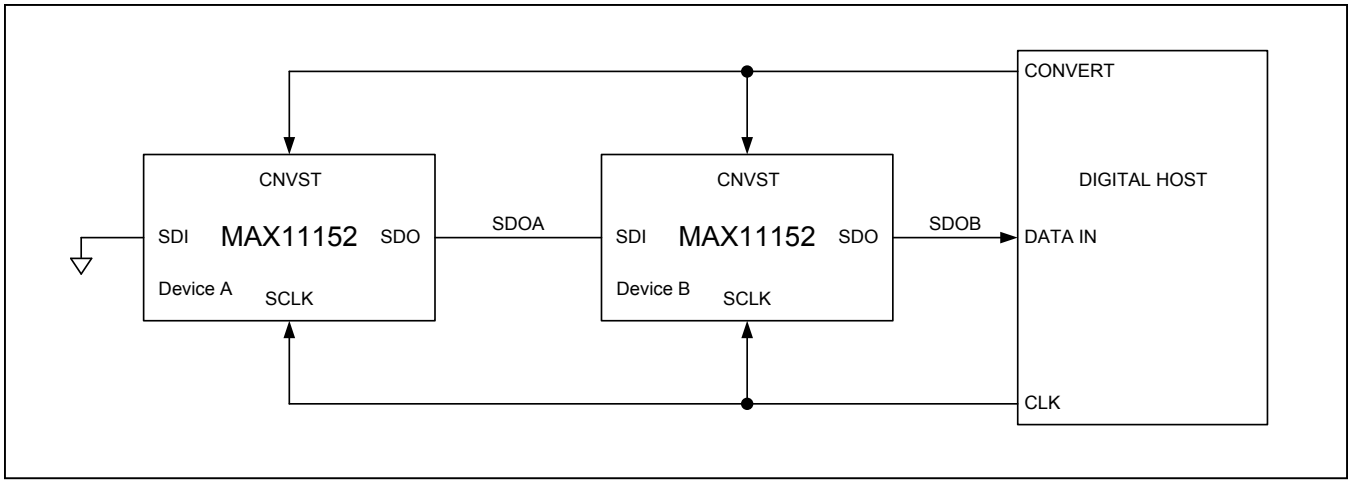


Figure 13. Daisy-Chain , No-Busy Indicator Mode Connection Diagram

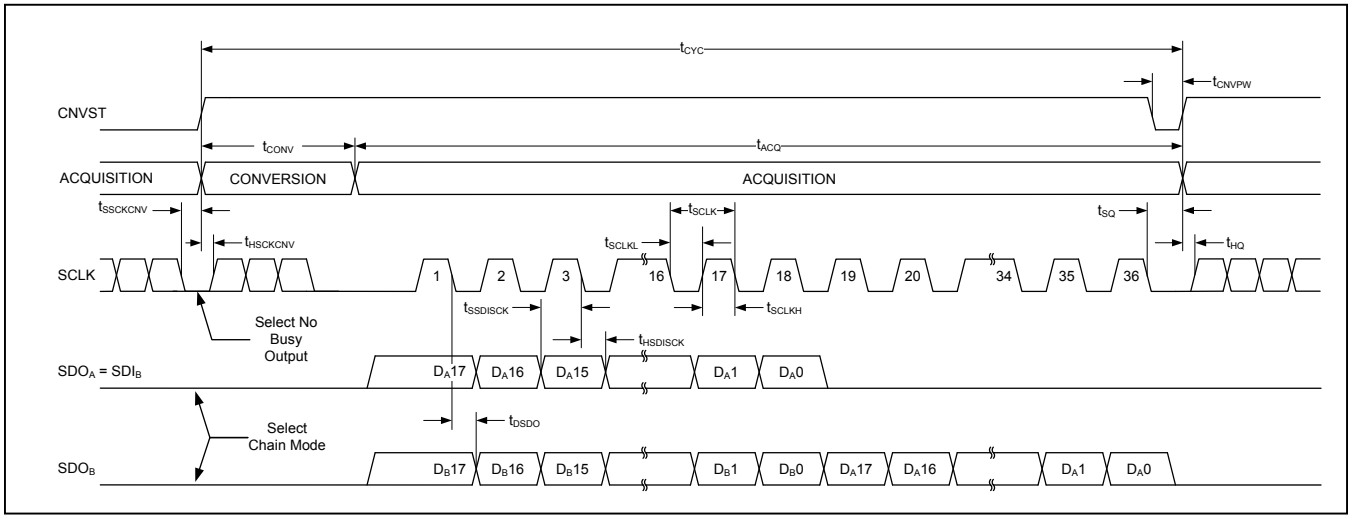


Figure 14. Daisy-Chain, No-Busy Indicator Mode Timing

sequent SCLK falling edges. SDO returns to high impedance after the 19th SCLK falling edge or when CNVST goes high and is then pulled to OVDD through the external pullup resistor.

Daisy-Chain, No-Busy Indicator Mode

The daisy-chain mode with no busy indicator is ideally suited for multichannel isolated applications that require minimal wiring complexity. Simultaneous sampling of multiple ADC channels is realized on a 3-wire serial interface where data readback is analogous to clocking a shift register. In Figure 13, two ADCs are connected to an SPI-compatible digital host with corresponding timing given in Figure 14.

The daisy-chain mode is engaged when the MAX11152 detects the low state on SDI at the rising edge of CNVST. In this mode, CNVST is brought low and then high to trigger the completion of the acquisition phase and the start of a conversion. A low SCLK state on the rising edge of CNVST signals to the internal controller that the no-busy indicator will be output. When in chain mode, the SDO output is driven active at all times.

When SDI and CNVST are both low, SDO is driven low, thus engaging the daisy-chain mode of operations on the downstream MAX11152 parts. For example, in Figure 10, part A has its SDI tied low so the chain mode of operation will be selected on every conversion. When CNVST goes low to trigger another conversion, part A's SDO and con-

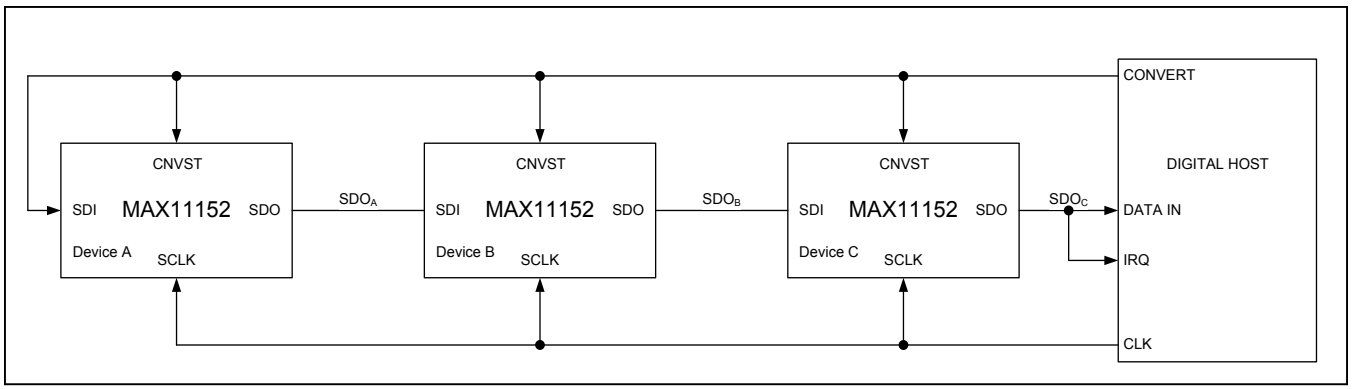


Figure 15. Daisy-Chain Mode with Busy Indicator Connection Diagram

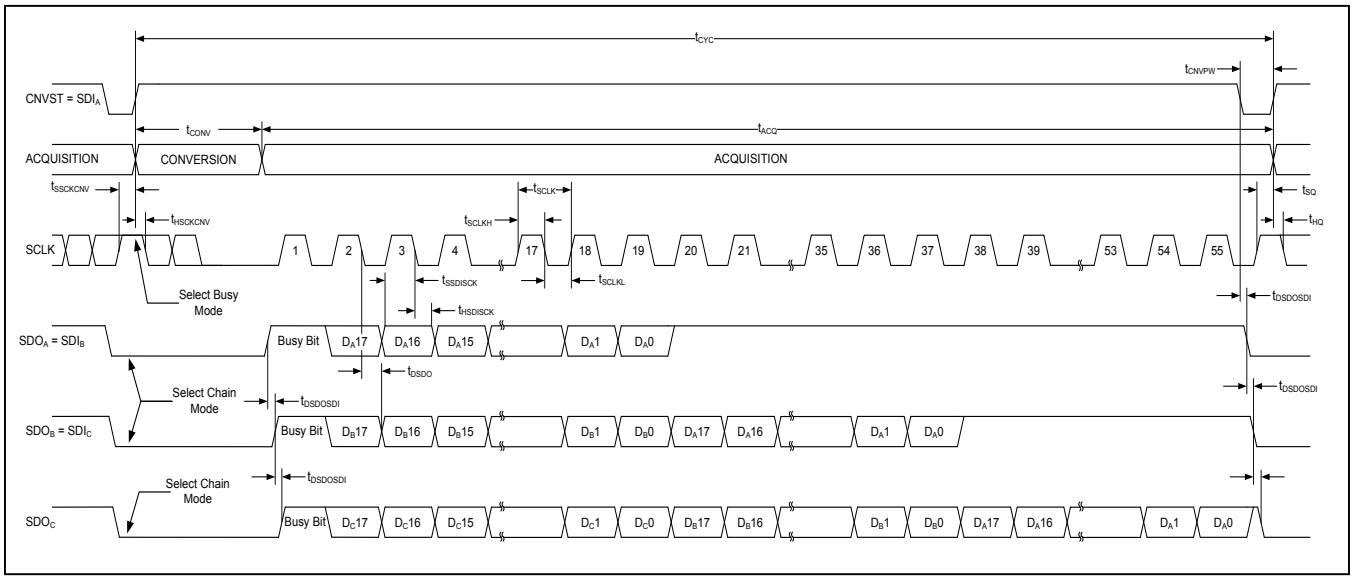


Figure 16. Daisy-Chain Mode with Busy Indicator Timing

sequently part B's SDI go low as well. On the next CNVST rising edge both parts A and B will select the daisy-chain mode interface.

When a conversion is complete, the MSB is presented onto SDO, and the MAX11152 returns to the acquisition phase. The remaining data bits, stored within the internal shift register, are clocked out on each subsequent SCLK falling edge. The SDI input of each ADC in the chain is used to transfer conversion data from the previous ADC into the internal shift register of the next ADC, thus allowing for data to be clocked through the multichip chain on each SCLK falling edge. Each ADC in the chain outputs its MSB data first requiring 18 × N clocks to read back N ADCs.

In daisy-chain mode, the maximum conversion rate is reduced due to the increased readback time. For instance, with a 6ns digital host setup time and 3V interface, up to four MAX11152 devices running at a conversion rate of 310ksps can be daisy-chained on a 3-wire port.

Daisy-Chain with Busy Indicator Mode

The daisy-chain mode with busy indicator is shown in Figure 15 where three ADCs are connected to an SPI-compatible digital host with corresponding timing given in Figure 16.

The daisy-chain mode is engaged when the MAX11152 detects a low state on SDI at the rising edge of CNVST. Additionally, SDI can be tied directly to CNVST to trigger

the chain interface mode. In this mode, CNVST is brought low and then high to trigger the completion of the acquisition phase and the start of a conversion. A high SCLK state on the rising edge of CNVST signals to the internal controller that the busy indicator will be outputted. When in daisy-chain mode the SDO output is driven active at all times.

When SDI and CNVST are both low, SDO is driven low, thus engaging the daisy-chain mode of operations on the downstream MAX11152 parts. For example, in Figure 12, part A has its SDI tied low so the daisy-chain mode of operation will be selected on every conversion. When CNVST goes low to trigger another conversion, part A's SDO and consequently part B's SDI go low as well. The same is true on part C's SDI input. Consequently, on the next CNVST rising edge all parts in the chain will select the daisy-chain mode interface.

When a conversion is complete, the busy indicator is presented onto each SDO, and the MAX11152 returns to the acquisition phase. Since the busy indicator is not propagated from one ADC to the next, it is necessary to wait 50ns from the receipt of the host interrupt before reading out data from all ADCs. This time ensures that all parts in the chain will have completed conversion before readout is attempted.

The conversion data bits are stored within the internal shift register and clocked out on each subsequent SCLK falling edge. The SDI input of each ADC in the chain is used to transfer conversion data from the previous ADC into the internal shift register of the next ADC, thus allowing for data to be clocked through the multichip chain on each SCLK falling edge. With busy indicator mode selected, the busy bit from each part is not chained on the first falling SCLK edge in the readout pattern. Consequently, the number of falling SCLKs needed to read back all data from N ADCs is 18 × N + 1 falling edges.

In daisy-chain mode, the maximum conversion rate is reduced due to the increased read back time. For instance, with a 6ns digital host setup time and 3V interface, up to four MAX11152 devices running at a conversion rate of 308ksps can be daisy-chained on a 3-wire port.

Layout, Grounding, and Bypassing

For best performance, use PCBs with ground planes. Ensure that digital and analog signal lines are separated from each other. Do not run analog and digital lines parallel to one another (especially clock lines), and avoid running digital lines underneath the ADC package. A single solid GND plane configuration with digital signals routed from one direction and analog signals from the other provides the best performance. Connect the GND pin on the MAX11152 to this ground plane. Keep the ground return to the power supply low impedance and as short as possible for noise-free operation.

A 4.7nF C0G (or NPO) ceramic chip capacitor should be placed between AIN+ and the ground plane as close as possible to the MAX11152. This capacitor reduces the inductance seen by the sampling circuitry and reduces the voltage transient seen by the input source circuit.

For best performance, connect the REF output to the ground plane with a 16V, 10µF ceramic chip capacitor with a X5R or X7R dielectric in a 1210 or smaller case size. Ensure that all bypass capacitors are connected directly into the ground plane with an independent via.

Bypass V_{DD} and OVDD to the ground plane with 0.1µF ceramic chip capacitors on each pin as close as possible to the device to minimize parasitic inductance. Add at least one bulk 10µF decoupling capacitor to V_{DD} and OVDD per PCB. For best performance, bring a V_{DD} power plane in on the analog interface side of the MAX11152 and a OVDD power plane from the digital interface side of the device.

Definitions

Integral Nonlinearity

Integral nonlinearity (INL) is the deviation of the values on an actual transfer function from a straight line. For these devices, this straight line is a line drawn between the end points of the transfer function, once offset and gain errors have been nullified.

Differential Nonlinearity

Differential nonlinearity (DNL) is the difference between an actual step width and the ideal value of 1 LSB. For these devices, the DNL of each digital output code is measured and the worst-case value is reported in the *Electrical Characteristics* table. A DNL error specification of less than ±1 LSB guarantees no missing codes and a monotonic transfer function.

Offset Error

For the MAX11152, the offset error is defined at the code transition of 0x00000 to 0x00001. The code transition of 0x00000 to 0x00001 should occur with an analog input voltage 0.5 LSB above GND or +9.5µV. The offset error is defined as the deviation between the actual analog input voltage required to produce the code transition of 0x00000 to 0x00001 and the ideal analog input of +9.5µV, expressed in LSBs.

Gain Error

Gain error is defined as the difference between the change in analog input voltage required to produce a top code transition minus a bottom code transition, subtracted from the ideal change in analog input voltage on V_{REF} x (262142/262144). For the MAX11152, top code transition is 0x3FFFE to 0X3FFFF. The bottom code transition is 0x00000 to 0x00001. For the MAX11152, the analog input voltage to produce these code transitions is measured and then the gain error is computed by subtracting V_{REF} x (262142/262144) from this measurement.

Signal-to-Noise Ratio

For a waveform perfectly reconstructed from digital samples, signal-to-noise ratio (SNR) is the ratio of the full-scale analog input power to the RMS quantization error (residual error). The ideal, theoretical minimum analog-to-digital noise is caused by quantization noise error only and results directly from the ADC's resolution (N bits):

$$SNR = (6.02 \times N + 1.76)dB$$

In reality, there are other noise sources besides quantization noise: thermal noise, reference noise, clock jitter, etc. SNR is computed by taking the ratio of the power signal to the power noise, which includes all spectral components not including the fundamental, the first five harmonics, and the DC offset.

Signal-to-Noise Plus Distortion

Signal-to-noise plus distortion (SINAD) is the ratio of the fundamental input frequency's power to the power of all the other ADC output signals:

$$SINAD(dB) = 10 \times \log\left[\frac{Signal}{(Noise + Distortion)}\right]$$

Effective Number of Bits

The effective number of bits (ENOB) indicates the global accuracy of an ADC at a specific input frequency and sampling rate. An ideal ADC's error consists of quantization noise only. With an input range equal to the full-scale range of the ADC, calculate the ENOB as follows:

$$ENOB = \frac{SINAD - 1.76}{6.02}$$

Total Harmonic Distortion

Total harmonic distortion (THD) is the ratio of the power contained in the first five harmonics of the converted data to the power of the fundamental. This is expressed as:

$$THD = 10 \times \log\left[\frac{P_2^2 + P_3^2 + P_4^2 + P_5^2}{P_1^2}\right]$$

where P_1 is the fundamental power and P_2 through P_5 is the power of the 2nd- through 5th-order harmonics.

Spurious-Free Dynamic Range

Spurious-free dynamic range (SFDR) is the ratio of the power of the fundamental (maximum signal component) to the power of the next-largest frequency component.

Aperture Delay

Aperture delay (t_{AD}) is the time delay from the sampling clock edge to the instant when an actual sample is taken.

Aperture Jitter

Aperture jitter (t_{AJ}) is the sample-to-sample variation in aperture delay.

Small-Signal Bandwidth

A small -20dBFS analog input signal is applied to an ADC in a manner that ensures that the signal's slew rate does not limit the ADC's performance. The input frequency is then swept up to the point where the amplitude of the digitized conversion result has decreased 3dB.

Full-Power Bandwidth

A large -0.5dBFS analog input signal is applied to an ADC, and the input frequency is swept up to the point where the amplitude of the digitized conversion result has decreased by 3dB. This point is defined as full-power input bandwidth frequency.