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MAX11166/MAX11167

16-Bit, 500ksps/250ksps, ±5V SAR ADCs with Internal Reference in TDFN

General Description

The MAX11166/MAX11167 16-bit, 500ksps/250ksps, SAR ADCs offer excellent AC and DC performance with true bipolar input range, small size, and internal reference. The MAX11166/MAX11167 measure a ±5V ($10V_{P-P}$) input range while operating from a single 5V supply. A patented charge-pump architecture allows direct sampling of high-impedance sources. The MAX11166/MAX11167 integrate an optional 6ppm/°C reference with internal buffer, saving the cost and space of an external reference.

These ADCs achieve 92.6dB SNR and -105dB THD. The MAX11166/MAX11167 guarantee 16-bit no-missing codes and ±0.5 LSB INL (typ).

The MAX11166/MAX11167 communicate using an SPI-compatible serial interface at 2.5V, 3V, 3.3V, or 5V logic. The serial interface can be used to daisy-chain multiple ADCs in parallel for multichannel applications and provides a busy indicator option for simplified system synchronization and timing.

The MAX11166/MAX11167 are offered in 12-pin, 3mm x 3mm, TDFN packages and are specified over the -40°C to +85°C temperature range.

Applications

- Data Acquisition Systems
- Industrial Control Systems/Process Control
- Medical Instrumentation
- Automatic Test Equipment

***Selector Guide* and *Ordering Information* appear at end of data sheet.**

Features

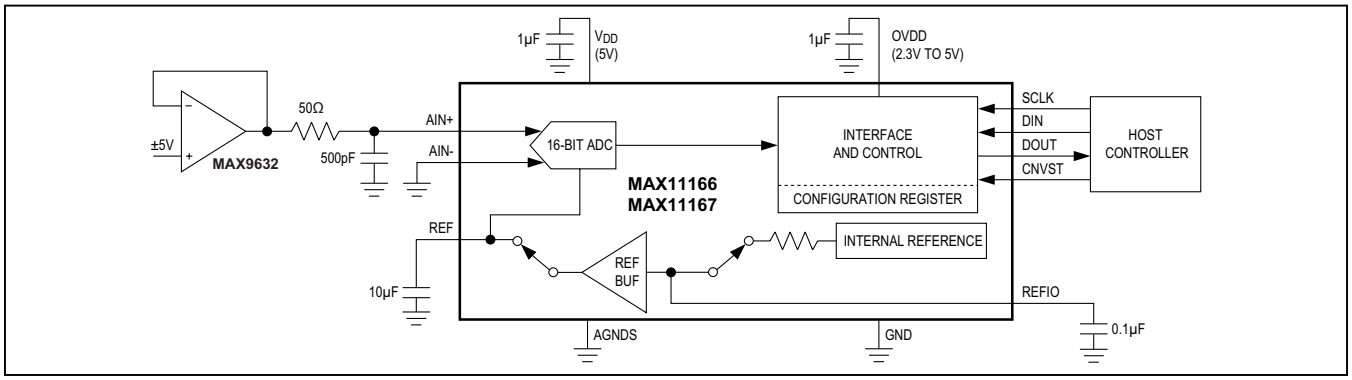
- High DC and AC Accuracy
- 16-Bit Resolution with No Missing Codes
- SNR: 92.6dB
- THD: -105dB at 10kHz
- ±0.5 LSB INL (typ)
- ±0.2 LSB DNL (typ)
- Internal Reference and Reference Buffer Saves Cost and Board Space
- 6ppm/°C typ
- Tiny 12-Pin 3mm x 3mm TDFN Package
- Bipolar ±5V Analog Input Range Saves External Signal Conditioning
- Single-Supply ADC with Low Power
- 5V Analog Supply
- 2.3V to 5V Digital Supply
- 26.4mW at 500ksps
- 1µA Shutdown Mode
- 500ksps Throughput Rate (MAX11166)
- 250ksps Throughput Rate (MAX11167)
- No Pipeline Delay/Latency
- Flexible Industry-Standard Serial Interface Saves I/O Pins
- SPI/QSPI™/MICROWIRE®/DSP-Compatible

QSPI is a trademark of Motorola, Inc.

MICROWIRE is a registered trademark of National Semiconductor Corporation.

*For related parts and recommended products to use with this part, refer to **www.maximintegrated.com/MAX11166.related**.*

Typical Operating Circuit



maxim integrated™

Absolute Maximum Ratings

V_{DD} to GND .....-0.3V to +6V
OVDD to GND..... -0.3V to the lower of (V_{DD} + 0.3V) and +6V
AIN+ to GND ..... ±7V
AIN-, REF, REFIO, AGNDS
to GND..... -0.3V to the lower of (V_{DD} + 0.3V) and +6V
SCLK, DIN, DOUT, CNVST
to GND..... -0.3V to the lower of (V_{DD} + 0.3V) and +6V
Maximum Current into Any Pin.....50mA

Continuous Power Dissipation (T_A = +70°C)
TDFN (derate 18.2mW/°C above +70°C).....1349mW
Operating Temperature Range..... -40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

TDFN
Junction-to-Ambient Thermal Resistance (θ_{JA}).....59.3°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) .....22.5°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{DD} = 4.75V to 5.25V, V_{OVDD} = 2.3V to 5.25V, f_{SAMPLE} = 500kHz or 250kHz, V_{REF} = 4.096V; T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG INPUT (Note 3)						
Input Voltage Range		AIN+ to AIN-, K = $\frac{5.000}{4.096}$	-K x V_{REF}		+K x V_{REF}	V
Absolute Input Voltage Range		AIN+ to GND	-(V_{DD} + 0.1)		+(V_{DD} + 0.1)	V
		AIN- to GND	-0.1		+0.1	
Input Leakage Current		Acquisition phase	-10	+0.001	+10	µA
Input Capacitance				15		pF
Input-Clamp Protection Current		Both inputs	-20		+20	mA
DC ACCURACY (Note 4)						
Resolution	N		16			Bits
No Missing Codes			16			Bits
Offset Error			-1.5	±0.1	+1.5	mV
Offset Temperature Coefficient				±2.4		µV/°C
Gain Error				±2	±10	LSB
Gain Error Temperature Coefficient				±1		ppm/°C
Integral Nonlinearity	INL	MAX11167, T_A = T_{MIN} to T_{MAX}	-2.0	±0.5	+2.0	LSB
		MAX11167, T_A = +25°C to +85°C	-1.0	±0.5	+1.0	
		MAX11166, T_A = T_{MIN} to T_{MAX}	-2.4	±0.5	+2.4	
		MAX11166, T_A = +25°C to +85°C	-1.5	±0.5	+1.5	
Differential Nonlinearity	DNL		-0.5	±0.2	+0.5	LSB
Positive Full-Scale Error					±14	LSB

Electrical Characteristics (continued)

(V_{DD} = 4.75V to 5.25V, V_{OVDD} = 2.3V to 5.25V, f_{SAMPLE} = 500kHz or 250kHz, V_{REF} = 4.096V; T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Negative Full-Scale Error						±13	LSB
Analog Input CMRR	CMRR				-77		dB
Power-Supply Rejection (Note 5)	PSR				±3.0		LSB
Transition Noise					0.5		LSB_{RMS}
REFERENCE (Note 7)							
REF Output Initial Accuracy	V_{REF}	Reference mode 0		4.092	4.096	4.100	V
REF Output Temperature Coefficient	TC_{REF}	Reference mode 0			±9	±17	ppm/°C
REFIO Output Initial Accuracy	V_{REFIO}	Reference modes 0 and 2		4.092	4.096	4.100	V
REFIO Output Temperature Coefficient	TC_{REFIO}	Reference modes 0 and 2			±6	±15	ppm/°C
REFIO Output Impedance		Reference modes 0 and 2			10		kΩ
REFIO Input Voltage Range		Reference mode 1		3	4.096	4.25	V
Reference Buffer Initial Offset		Reference mode 1		-500		+500	µV
Reference Buffer Temperature Coefficient		Reference mode 1			±6	±10	µV/°C
External Compensation Capacitor	C_{EXT}	Required for reference modes 0 and 1, recommended for reference modes 2 and 3		10			µF
REF Voltage Input Range	V_{REF}	Reference modes 2 and 3		2.5		4.25	V
REF Input Capacitance		Reference modes 2 and 3			20		pF
REF Load Current	I_{REF}	V_{REF} = 4.096V, reference modes 2 and 3	MAX11167, 250ksps		65		µA
			MAX11166, 500ksps		130		
AC ACCURACY (Note 6)							
Signal-to-Noise Ratio (Note 7)	SNR	f_{IN} = 10kHz	V_{REF} = 4.096V, reference mode 3	91.5	92.6		dB
			V_{REF} = 4.096V, reference mode 1		92.4		
			V_{REF} = 2.5V, reference mode 3		89.8		
			Internal reference, reference mode 0		92.4		
Signal-to-Noise Plus Distortion (Note 7)	SINAD	f_{IN} = 10kHz	V_{REF} = 4.096V, reference mode 3	90	92.3		dB
			V_{REF} = 4.096V, reference mode 1		92.3		
			V_{REF} = 2.5V, reference mode 3		89.5		
			Internal reference, reference mode 0		91.8		
Spurious-Free Dynamic Range	SFDR			96	105		dB
Total Harmonic Distortion	THD				-105	-96	dB
Intermodulation Distortion (Note 8)	IMD				-115		dB

Electrical Characteristics (continued)

(V_{DD} = 4.75V to 5.25V, V_{OVDD} = 2.3V to 5.25V, f_{SAMPLE} = 500kHz or 250kHz, V_{REF} = 4.096V; T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SAMPLING DYNAMICS						
Throughput Sample Rate		MAX11166	0.01		500	ksps
		MAX11167	0.01		250	
Transient Response		Full-scale step			400	ns
Full-Power Bandwidth		-3dB point		6		MHz
		-0.1dB point		> 0.2		
Aperture Delay				2.5		ns
Aperture Jitter				< 50		ps_{RMS}
POWER SUPPLIES						
Analog Supply Voltage	V_{DD}		4.75		5.25	V
Interface Supply Voltage	V_{OVDD}		2.3		5.25	V
Analog Supply Current	I_{VDD}	Internal reference mode	5.0	5.8	6.5	mA
		External reference mode	3.0	3.5	4.0	
V_{DD} Shutdown Current				6.3	10	µA
Interface Supply Current (Note 9)	I_{OVDD}	V_{OVDD} = 2.3V, MAX11167		0.75	0.85	mA
		V_{OVDD} = 5.25V, MAX11167		2.0	2.4	
		V_{OVDD} = 2.3V, MAX11166		1.5	2.0	
		V_{OVDD} = 5.25V, MAX11166		4.3	5.0	
OVDD Shutdown Current				0.9	10	µA
Power Dissipation		V_{DD} = 5V, V_{OVDD} = 3.3V, MAX11167 reference mode = 2, 3		21.2		mW
		V_{DD} = 5V, V_{OVDD} = 3.3V, MAX11167 reference mode = 0, 1		33.3		
		V_{DD} = 5V, V_{OVDD} = 3.3V, MAX11166 reference mode = 2, 3		26.4		
		V_{DD} = 5V, V_{OVDD} = 3.3V, MAX11166 reference mode = 0, 1		40.5		
DIGITAL INPUTS (DIN, SCLK, CNVST)						
Input Voltage High	V_{IH}		0.7 x V_{OVDD}			V
Input Voltage Low	V_{IL}			0.3 x V_{OVDD}		V
Input Hysteresis	V_{HYS}			±0.05 x V_{OVDD}		V
Input Capacitance	C_{IN}			10		pF
Input Current	I_{IN}	V_{IN} = 0V or V_{OVDD}	-10		+10	µA
DIGITAL OUTPUT (DOUT)						
Output Voltage High	V_{OH}	I_{SOURCE} = 2mA	V_{OVDD} - 0.4			V
Output Voltage Low	V_{OL}	I_{SINK} = 2mA			0.4	V
Three-State Leakage Current			-10		+10	µA
Three-State Output Capacitance				15		pF

Electrical Characteristics (continued)

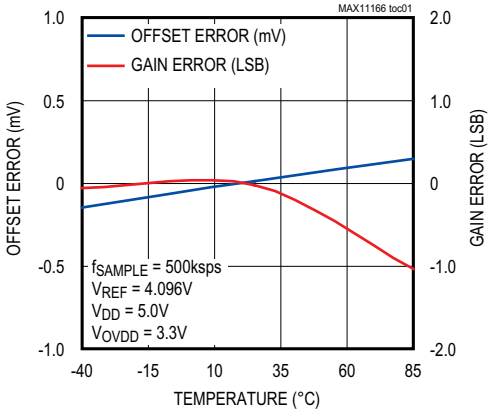
(V_{DD} = 4.75V to 5.25V, V_{OVDD} = 2.3V to 5.25V, f_{SAMPLE} = 500kHz or 250kHz, V_{REF} = 4.096V; T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
TIMING (Note 9)							
Time Between Conversions	t_{CYC}	MAX11166		2		100000	µs
		MAX11167		4		100000	µs
Conversion Time	t_{CONV}	CNVST rising to data available	MAX11166	1.35		1.5	µs
			MAX11167	2.7		3.0	
Acquisition Time	t_{ACQ}	t_{ACQ} = t_{CYC} - t_{CONV}	MAX11166	0.5			µs
			MAX11167	1			
CNVST Pulse Width	t_{CNVPW}	$\overline{CS}$ mode		5			ns
SCLK Period ($\overline{CS}$ Mode)	t_{SCLK}	V_{OVDD} > 4.5V		14			ns
		V_{OVDD} > 2.7V		20			
		V_{OVDD} > 2.3V		26			
SCLK Period (Daisy-Chain Mode)	t_{SCLK}	V_{OVDD} > 4.5V		16			ns
		V_{OVDD} > 2.7V		24			
		V_{OVDD} > 2.3V		30			
SCLK Low Time	t_{SCLKL}			5			ns
SCLK High Time	t_{SCLKH}			5			ns
SCLK Falling Edge to Data Valid Delay	t_{DDO}	V_{OVDD} > 4.5V				12	ns
		V_{OVDD} > 2.7V				18	
		V_{OVDD} > 2.3V				23	
CNVST Low to DOUT D15 MSB Valid ($\overline{CS}$ Mode)	t_{EN}	V_{OVDD} > 2.7V				14	ns
		V_{OVDD} < 2.7V				17	
CNVST High or Last SCLK Falling Edge to DOUT High Impedance	t_{DIS}	$\overline{CS}$ Mode				20	ns
DIN Valid Setup Time from SCLK Falling Edge	$t_{SDINSCK}$	V_{OVDD} > 4.5V		3			ns
		V_{OVDD} > 2.7V		5			
		V_{OVDD} > 2.3V		6			
DIN Valid Hold Time from SCLK Falling Edge	$t_{HDINSCK}$			0			ns
SCLK Valid Setup Time to CNVST Falling Edge	$t_{SSCKCNF}$			3			ns
SCLK Valid Hold Time to CNVST Falling Edge	$t_{HSCKCNF}$			6			ns

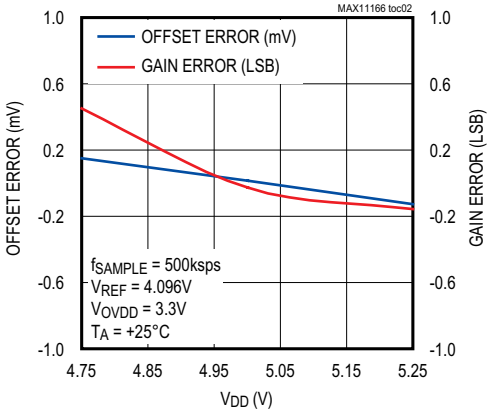
Note 2: Maximum and minimum limits are fully production tested over specified supply voltage range and at a temperature of +25°C and +85°C. Limits below +25°C are guaranteed by design and device characterization. Typical values are not guaranteed.
Note 3: See the *Analog Inputs* and *Overvoltage Input Clamps* sections.
Note 4: See the *Definitions* section.
Note 5: Defined as the change in positive full-scale code transition caused by a ±5% variation in the V_{DD} supply voltage.
Note 6: 10kHz sine wave input, -0.1dB below full scale.
Note 7: See Table 4 for definition of the reference modes.
Note 8: f_{IN1} ~ 9.4kHz, f_{IN2} ~ 10.7kHz, Each tone at -6.1dB below full scale.
Note 9: C_{LOAD} = 65pF on DOUT.

Typical Operating Characteristics—MAX11166

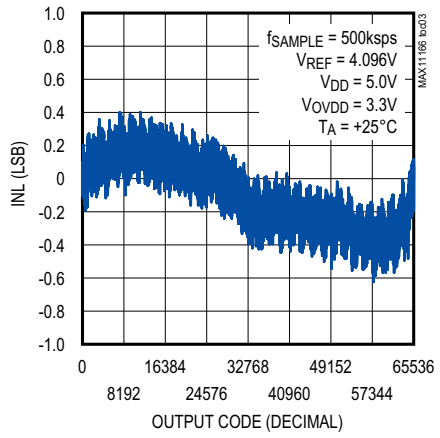
OFFSET AND GAIN ERROR vs. TEMPERATURE



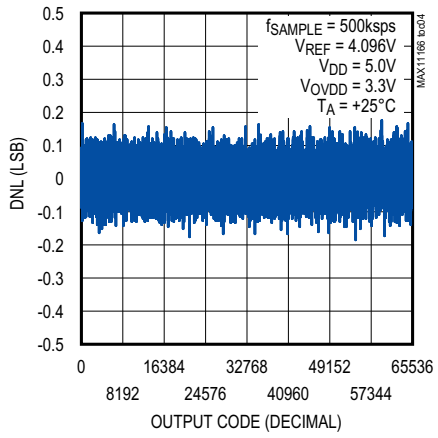
OFFSET AND GAIN ERROR vs. SUPPLY VOLTAGE



INTEGRAL NONLINEARITY vs. CODE

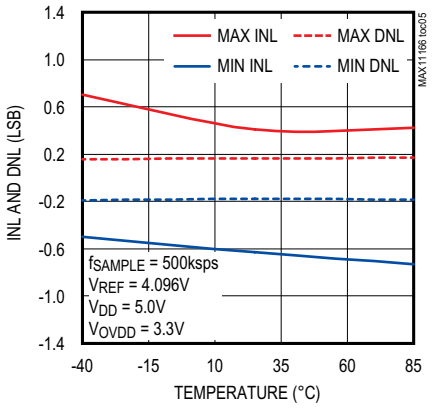


DIFFERENTIAL NONLINEARITY vs. CODE

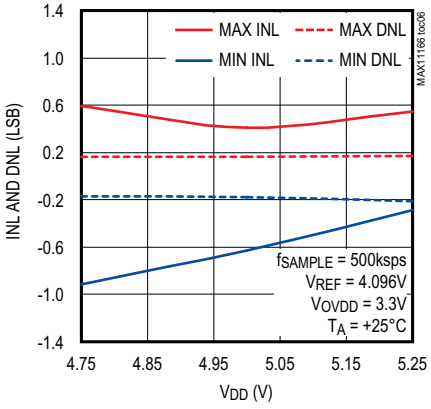


Typical Operating Characteristics—MAX11166 (continued)

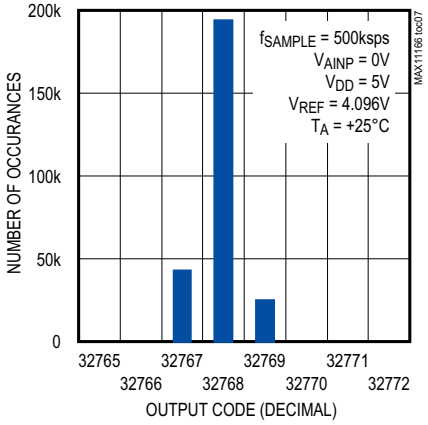
INL AND DNL vs. TEMPERATURE



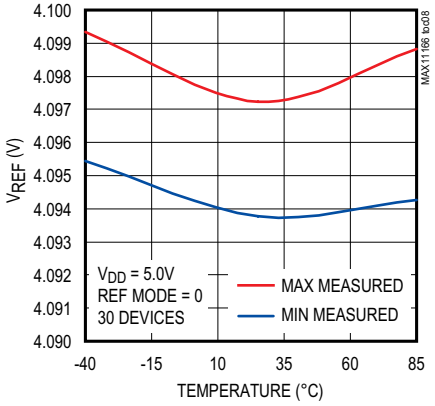
INL AND DNL vs. V_{DD} SUPPLY VOLTAGE



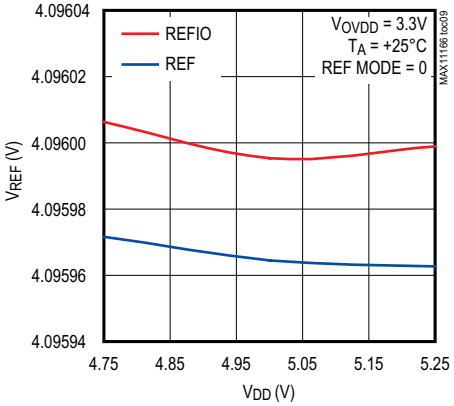
OUTPUT NOISE HISTOGRAM WITH INPUT CONNECTED TO GND



INTERNAL REFERENCE VOLTAGE vs. TEMPERATURE (REF PIN)

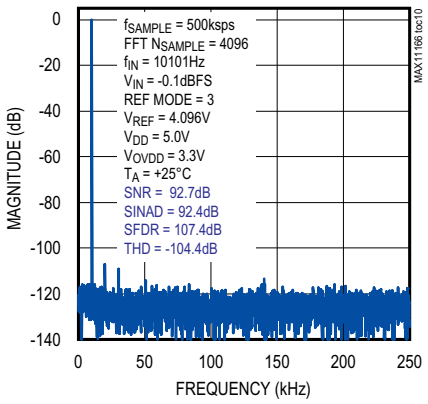


INTERNAL REFERENCE VOLTAGES vs. V_{DD} VOLTAGE

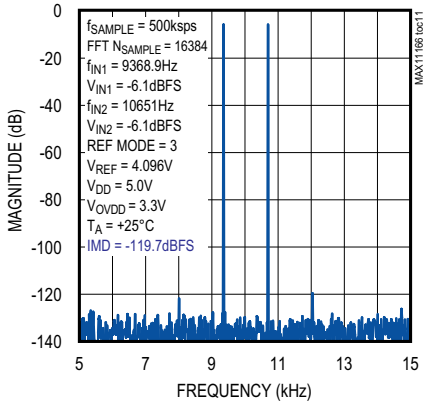


Typical Operating Characteristics—MAX11166 (continued)

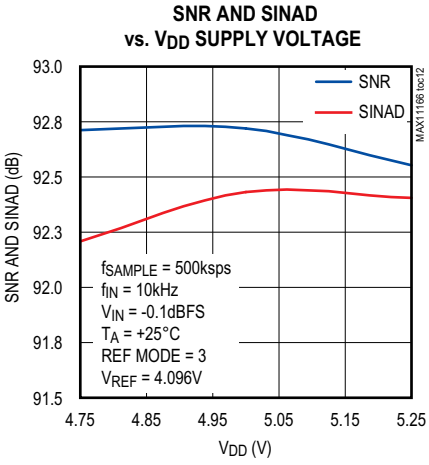
FFT PLOT



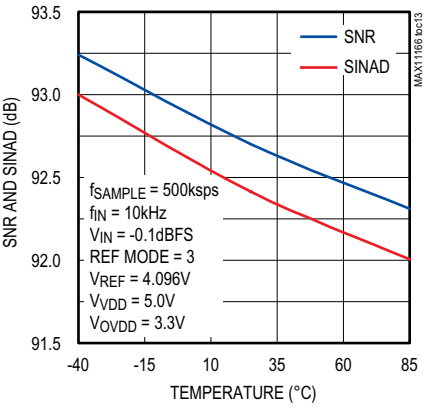
TWO TONES IMD



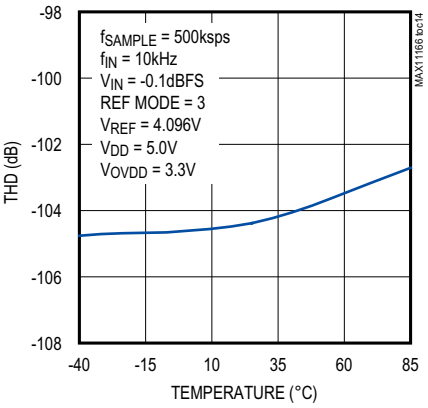
SNR AND SINAD vs. V_{DD} SUPPLY VOLTAGE



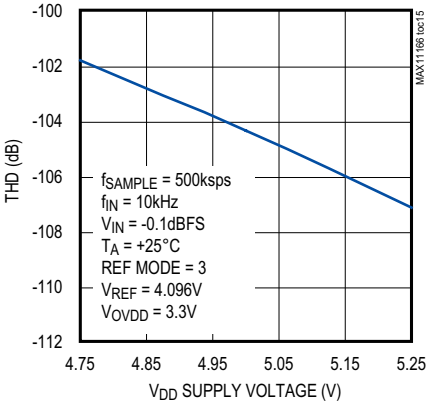
SIGNAL-TO-NOISE RATIO AND SIGNAL-TO-NOISE AND DISTORTION RATIO vs. TEMPERATURE



THD vs. TEMPERATURE

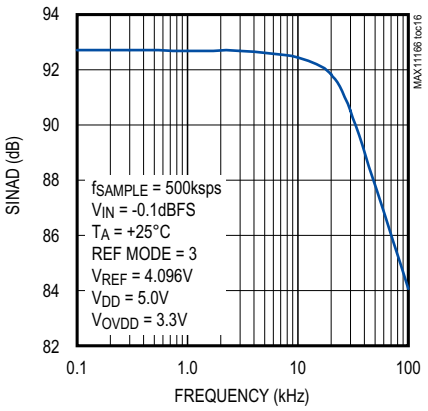


THD vs. V_{DD} SUPPLY VOLTAGE

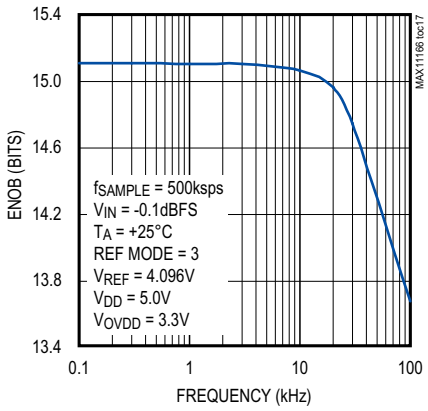


Typical Operating Characteristics—MAX11166 (continued)

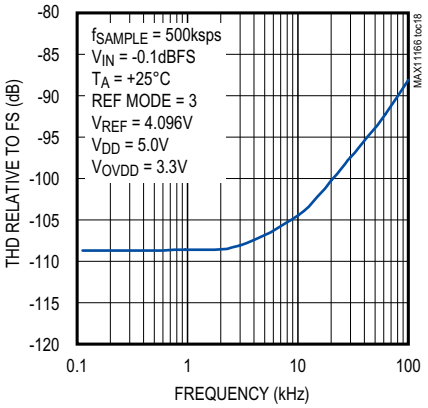
SINAD vs. FREQUENCY



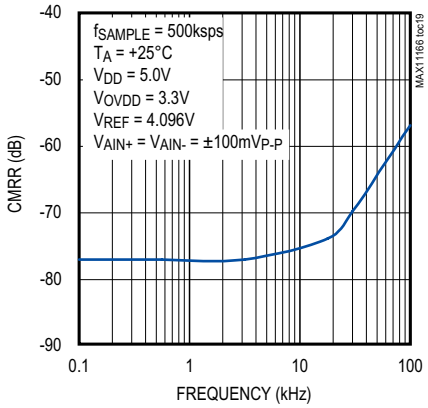
ENOB vs. INPUT SIGNAL FREQUENCY



THD vs. INPUT FREQUENCY

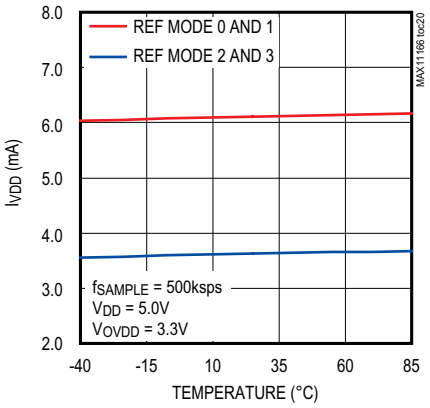


CMRR vs. INPUT FREQUENCY

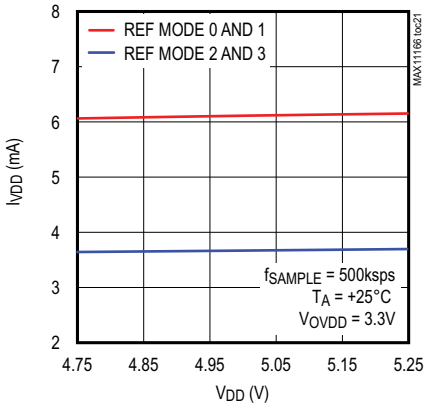


Typical Operating Characteristics—MAX11166 (continued)

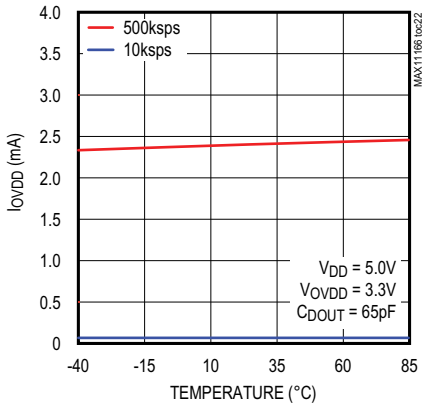
V_{DD} SUPPLY CURRENT vs. TEMPERATURE



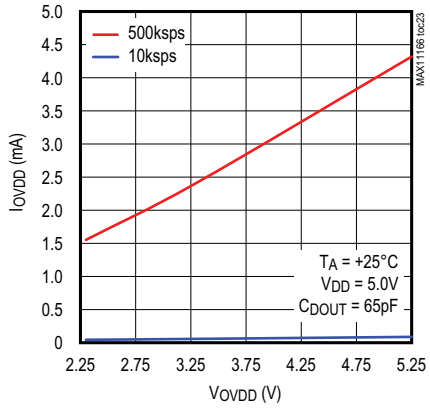
V_{DD} SUPPLY CURRENT vs. V_{DD} SUPPLY VOLTAGE



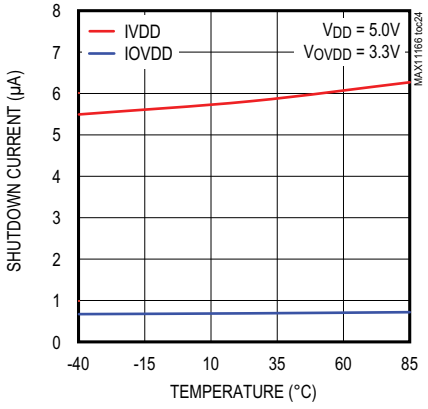
OVDD SUPPLY CURRENT vs. TEMPERATURE



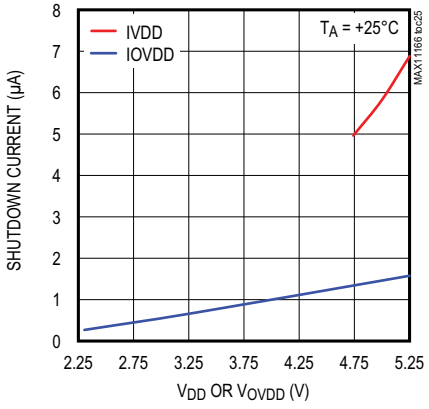
OVDD SUPPLY CURRENT vs. OVDD SUPPLY VOLTAGE



ANALOG AND DIGITAL SHUTDOWN CURRENT vs. TEMPERATURE

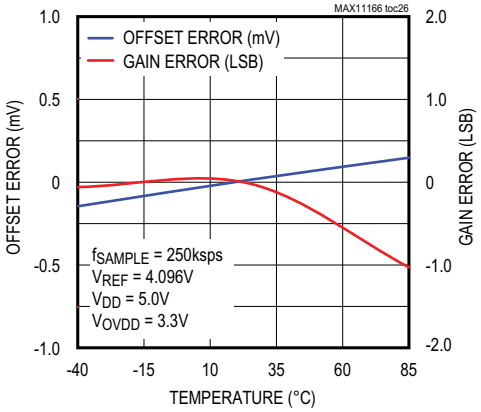


V_{DD} AND OVDD SHUTDOWN CURRENT vs. SUPPY VOLTAGE

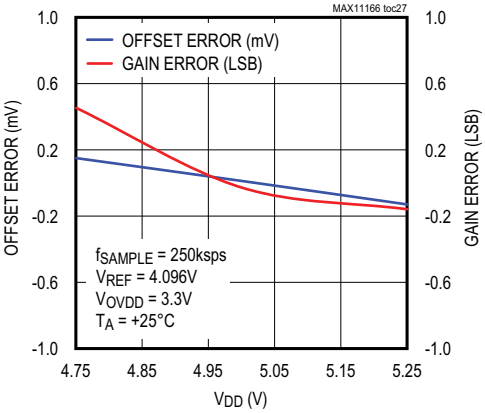


Typical Operating Characteristics—MAX11166 (continued)

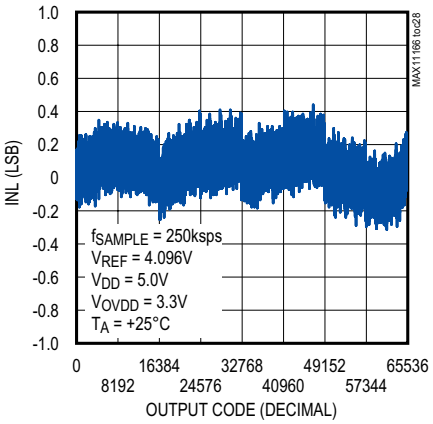
OFFSET AND GAIN ERROR vs. TEMPERATURE



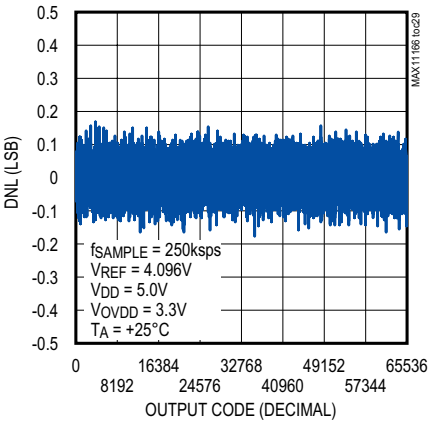
OFFSET AND GAIN ERROR vs. SUPPLY VOLTAGE



INTEGRAL NONLINEARITY vs. CODE

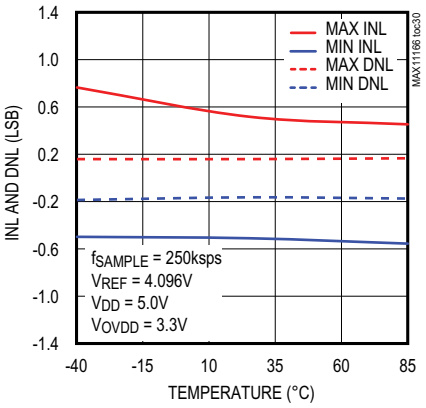


DIFFERENTIAL NONLINEARITY vs. CODE

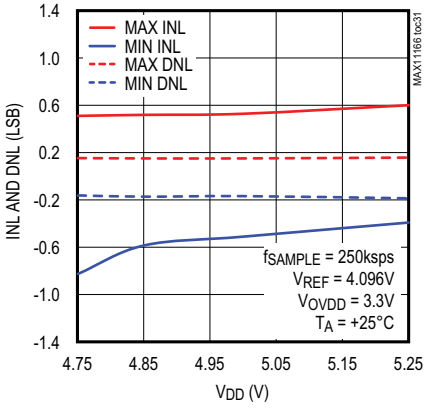


Typical Operating Characteristics—MAX11167 (continued)

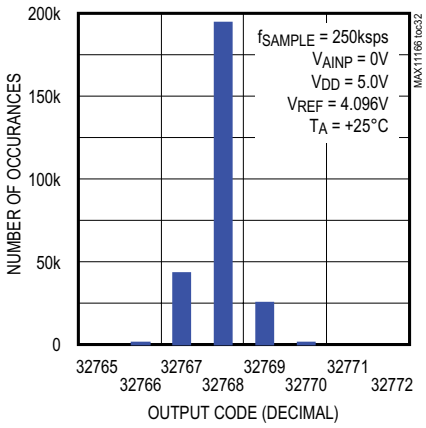
INL AND DNL vs. TEMPERATURE



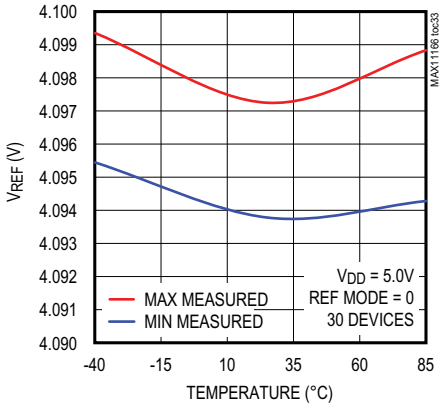
INL AND DNL vs. VDD SUPPLY VOLTAGE



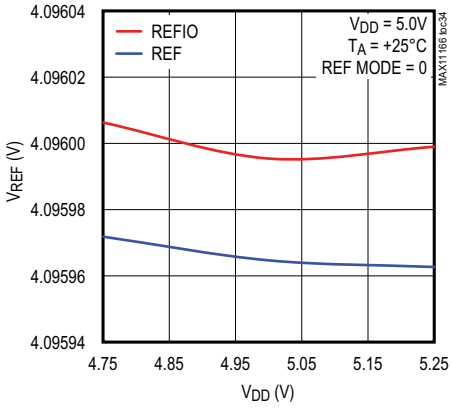
OUTPUT NOISE HISTOGRAM WITH INPUT CONNECTED TO GND



INTERNAL REFERENCE VOLTAGE vs. TEMPERATURE (REF PIN)

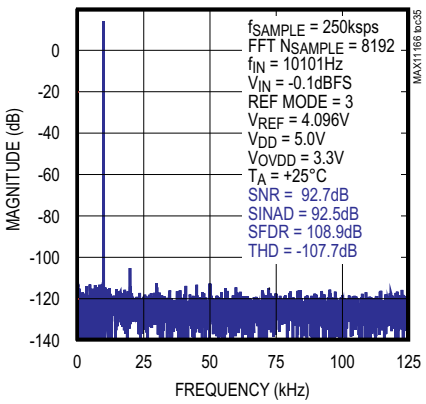


INTERNAL REFERENCE VOLTAGES vs. VDD VOLTAGE

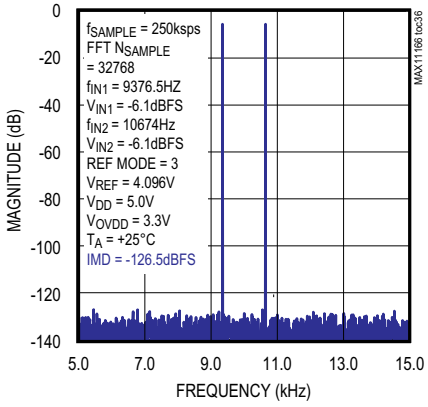


Typical Operating Characteristics—MAX11167 (continued)

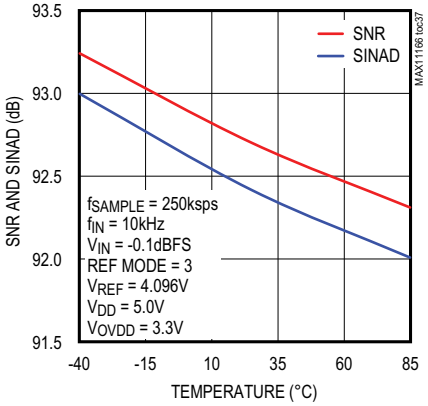
FFT PLOT



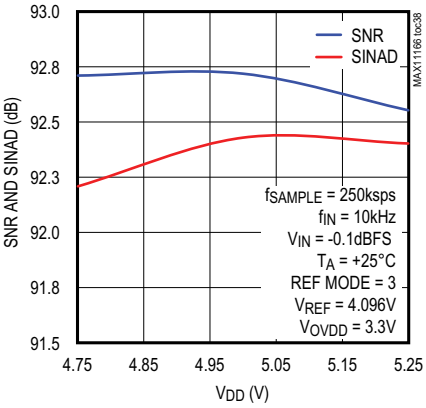
TWO TONES IMD



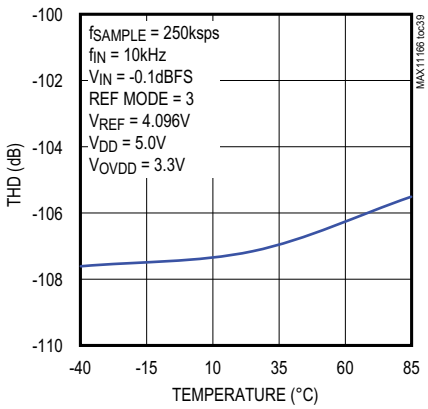
SNR AND SINAD vs. TEMPERATURE



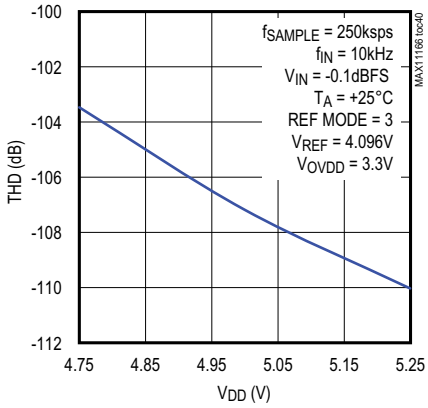
SNR AND SINAD vs. V_{DD} SUPPLY VOLTAGE



THD vs. TEMPERATURE

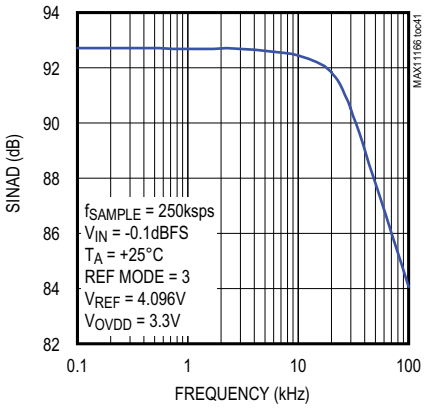


THD vs. V_{DD} SUPPLY VOLTAGE

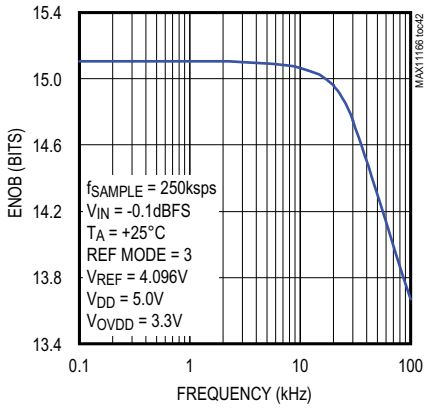


Typical Operating Characteristics—MAX11167 (continued)

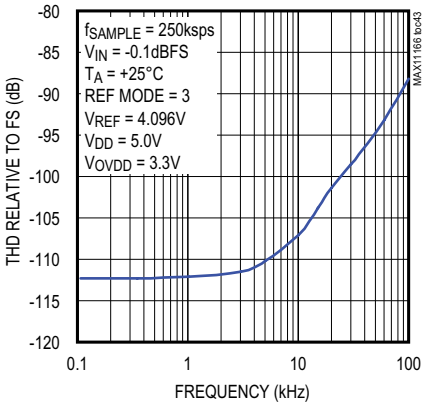
SINAD vs. FREQUENCY



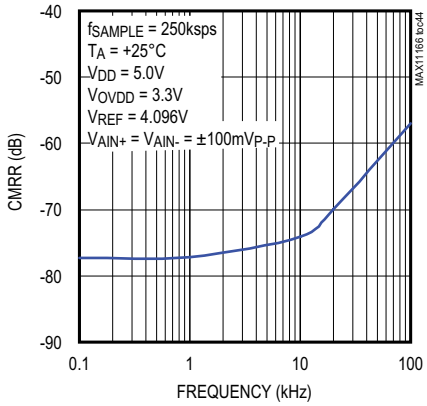
ENOB vs. INPUT SIGNAL FREQUENCY



THD vs. INPUT FREQUENCY

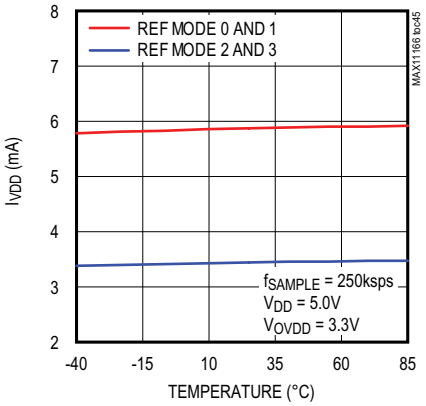


CMRR vs. INPUT FREQUENCY

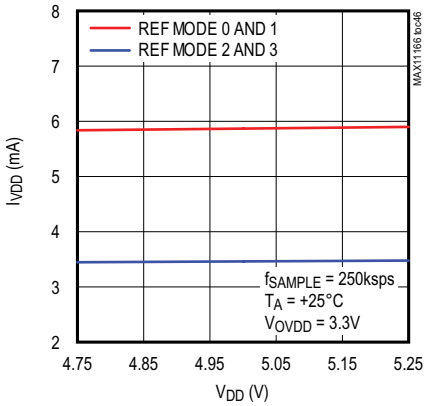


Typical Operating Characteristics—MAX11167 (continued)

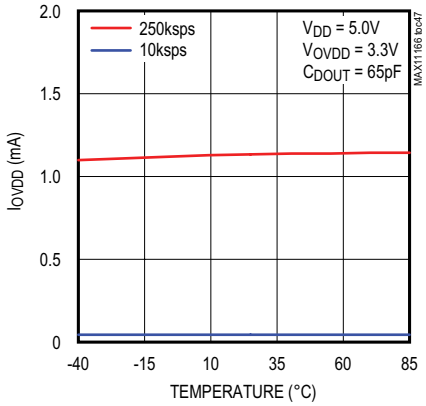
V_{DD} SUPPLY CURRENT vs. TEMPERATURE



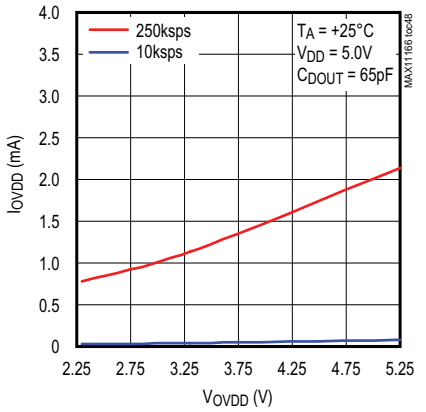
V_{DD} SUPPLY CURRENT vs. V_{DD} SUPPLY VOLTAGE



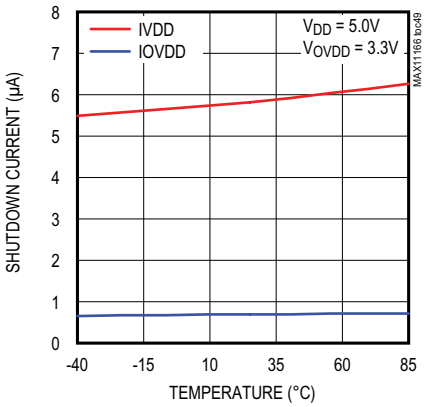
OVDD SUPPLY CURRENT vs. TEMPERATURE



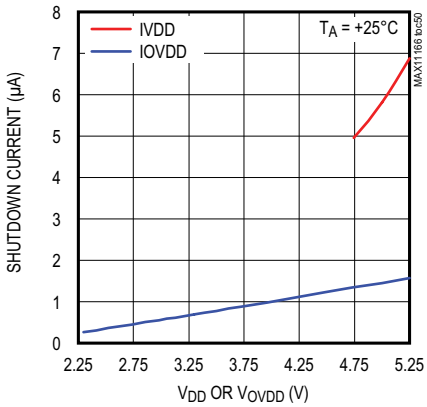
OVDD SUPPLY CURRENT vs. OVDD SUPPLY VOLTAGE



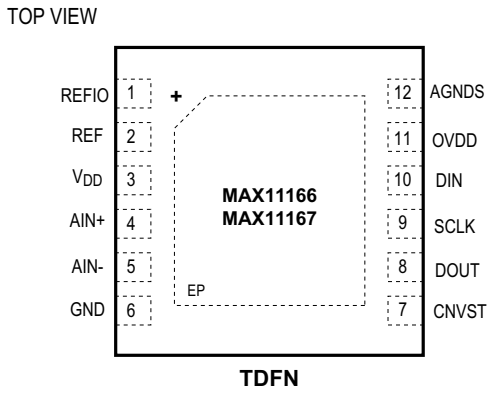
ANALOG AND DIGITAL SHUTDOWN CURRENT vs. TEMPERATURE



V_{DD} AND OVDD SHUTDOWN CURRENT vs. SUPPY VOLTAGE



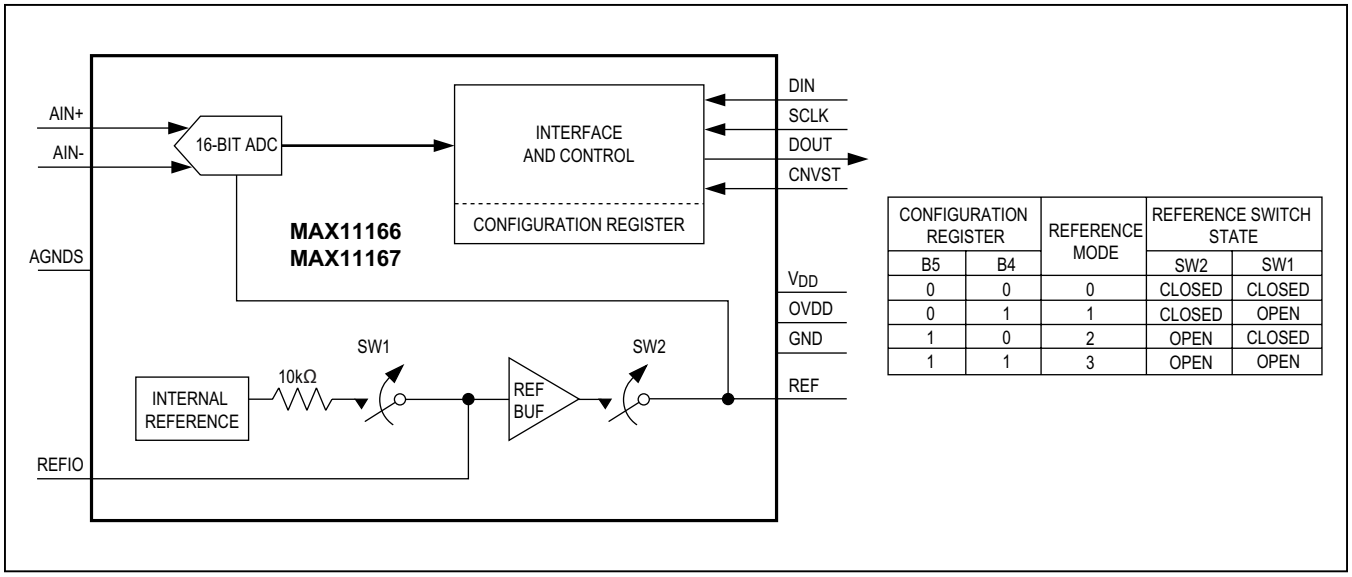
Pin Configuration



Pin Description

PIN	NAME	I/O	FUNCTION
1	REFIO	I/O	External Reference Input/Internal Reference Output. Place a 0.1µF capacitor from REFIO to AGNDS.
2	REF	I/O	External Reference Input/Reference Buffer Decoupling. Bypass to AGNDS in close proximity with a X5R or X7R 10µF 16V chip. See the *Layout*, *Grounding*, and *Bypassing* section.
3	V_{DD}	I	Analog Power Supply. Bypass to GND with a 0.1µF capacitor for each device and one 10µF per PCB.
4	AIN+	I	Positive Analog Input
5	AIN-	I	Negative Analog Input. Connect AIN- to the analog ground plane or to a remote-sense ground.
6	GND	I	Power-Supply Ground
7	CNVST	I	Convert Start Input. The rising edge of CNVST initiates conversions. The falling edge of CNVST with SCLK high enables the serial interface.
8	DOUT	O	Serial Data Output. DOUT will change stated on the falling edge of SCLK.
9	SCLK	I	Serial Clock Input. Clocks data out of the serial interface when the device is selected.
10	DIN	I	Serial Data Input. DIN data is latched into the serial interface on the rising edge of SCLK.
11	OVDD	I	Digital Power Supply. Bypass to GND with a 0.1µF capacitor for each device and one 10µF per PCB.
12	AGNDS	I	Analog Ground Sense. Zero current reference for the on-board DAC and reference source. Reference for REFIO and REF.
—	EP	—	Exposed Pad. EP is connected internally to GND. Connect to PCB GND.

Functional Diagram



CONFIGURATION REGISTER		REFERENCE MODE	REFERENCE SWITCH STATE	
B5	B4		SW2	SW1
0	0	0	CLOSED	CLOSED
0	1	1	CLOSED	OPEN
1	0	2	OPEN	CLOSED
1	1	3	OPEN	OPEN

Detailed Description

The MAX11166/MAX11167 are 16-bit single-channel, pseudo-differential ADCs with maximum throughput rates of 500ksps/250ksps. These ADCs include a precision internal reference that allows for measuring a bipolar input voltage range of ±5V. An external reference can also be applied for input ranges between ±3.05V and ±5.19V. Both inputs (AIN+ and AIN-) are sampled with a pseudo-differential on-chip track-and-hold.

The MAX11166/MAX11167 measure a true bipolar voltage of ±5V ($10V_{P-P}$) and the inputs are protected for up to ±20mA of overrange current. These ADCs are powered from a 4.75 to 5.25V analog supply (V_{DD}) and a separate 2.3V to 5.25V digital supply (OVDD). The MAX11166/MAX11167 require 500ns/1µs to acquire the input sample on an internal track-and-hold and then convert the sampled signal to 16 bits of accuracy using an internally clocked converter.

Analog Inputs

The MAX11166/MAX11167 ADCs consist of a true sampling pseudo-differential input stage with high-impedance, capacitive inputs. The internal T/H circuitry feature a small-signal bandwidth of about 6MHz to provide 16-bit accurate sampling in 500ns (MAX11166)/1µs (MAX11167). This allows for accurate sampling of a number of scanned channels through an external multiplexer.

The MAX11166/MAX11167 can thus convert input signals on AIN+ in the range of $-(K \times V_{REF} + AIN-)$ to $+(K \times V_{REF} + AIN-)$ where K = 5.000/4.096. AIN+ should also be limited to $\pm(V_{DD} + 0.1V)$ for accurate conversions. AIN- has an input range of -0.1V to +0.1V and should be connected to the ground reference of the input signal source. The MAX11166/MAX11167 performs a true differential sampling on inputs between AIN+ and AIN- with good common-mode rejection (see the *Typical Operating Circuit*). This allows for improved sampling of remote transducer inputs.

Many traditional ADCs with single supplies that measure bipolar input signals use resistive divider networks directly on the analog inputs. These networks increase the complexity of the input signal conditioning. However, the MAX11166/MAX11167 include a patented input switch architecture that allows direct sampling of high-impedance sources. This architecture requires a minimum sample rate of 10Hz to maintain accurate conversions over the designed temperature and supply ranges.

Overvoltage Input Clamps

The MAX11166/MAX11167 include an input clamping circuit that activates when the input voltage at AIN+ is above (V_{DD} + 300mV) or below -(V_{DD} + 300mV). The clamp circuit remains high impedance while the input signal is within the range of ±(V_{DD} + 100mV) and draws little to no current. However, when the input signal exceeds this range the clamps begin to turn on. Consequently, to obtain the highest accuracy, ensure that the input voltage does not exceed the range of ±(V_{DD} + 100mV).

To make use of the input clamps, connect a resistor (R_S) between the AIN+ input and the voltage source to limit the voltage at the analog input and to ensure the fault current into the devices does not exceed ±20mA. Note that the voltage at the AIN+ input pin limits to approximately 7V during a fault condition so the following equation can be used to calculate the value of R_S:

$$R_S = \frac{V_{FAULT\,MAX} - 7V}{20mA}$$

where $V_{FAULTMAX}$ is the maximum voltage that the source produces during a fault condition.

Figure 1 and Figure 2 illustrate the clamp circuit voltage current characteristics for a source impedance R_S = 1280Ω. While the input voltage is within the ±(V_{DD} + 300mV) range, no current flows in the input clamps. Once the input voltage goes beyond this voltage range, the clamps turn on and limit the voltage at the input pin.

Internal/External Reference (REFIO) Configuration

The MAX11166/MAX11167 include a standard SPI interface that selects internal or external reference modes of operation through an input configuration register (see the *Input Configuration Interface* section). The MAX11166/MAX11167 feature an internal bandgap reference circuit (V_{REFIO} = 4.096V) that is buffered with an internal reference buffer that drives the REF pin. The MAX11166/MAX11167 configure register allows four combinations of reference configuration. These reference mode are:

Reference Mode 00: ADC reference is provided by the internal bandgap feed out the REFIO pin, noise filtered with an external capacitor on the REFIO pin, then buffered by the internal reference buffer and decoupled with an external capacitor on the REF pin. In this mode the ADC requires no external reference source.

Reference Mode 01: ADC reference is provided externally and feeds into the REFIO pin, buffered with the internal reference buffer and decoupled with an external capacitor on the REF pin. This mode is typically used when a common reference source is needed for more than one MAX11166/MAX11167.

Reference Mode 10: The internal bandgap is used as a reference source output and feed out the REFIO pin. However, the internal reference buffer is in a shutdown state and the REF pin is high impedance. This state would typically be used to provide a common reference source to a set of external reference buffers for several MAX11166/MAX11167.

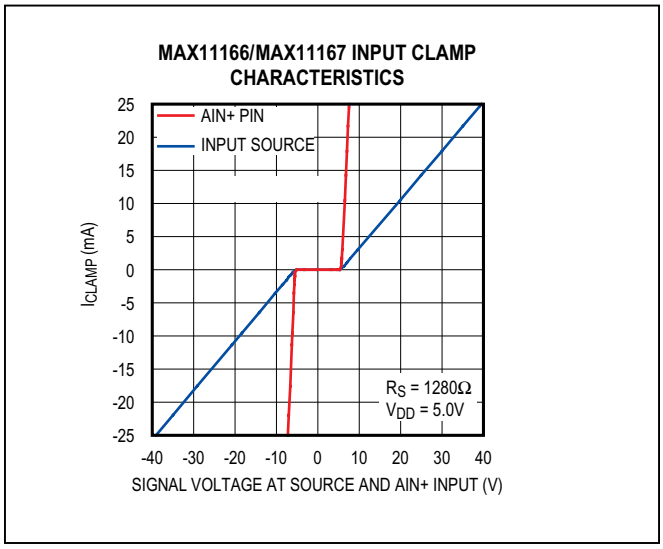


Figure 1. Input Clamp Characteristics

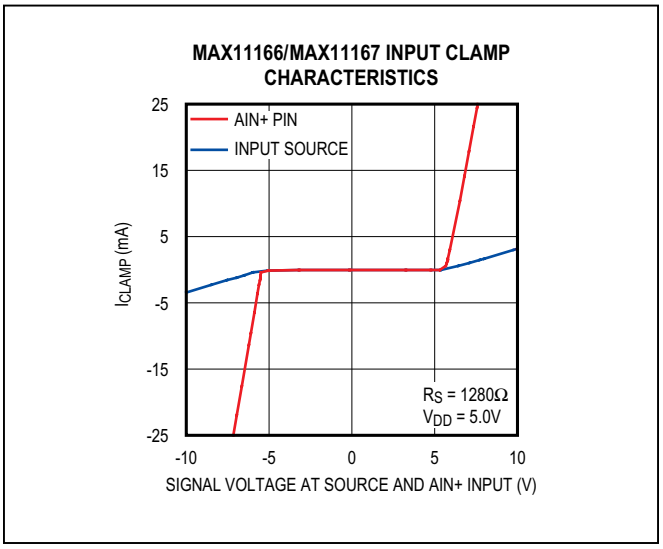


Figure 2. Input Clamp Characteristics (Zoom In)

Reference Mode 11: The internal bandgap reference source as well as the internal reference buffer are both in a shutdown state. The REF pin is in a high-impedance state. This mode would typically be used when an external reference source and external reference buffer is used to drive all MAX11166/MAX11167 parts in a system.

Regardless of the reference mode used, the MAX11166/MAX11167 require a low-impedance reference source on the REF pin to support 16-bit accuracy. When using the internal reference buffer, externally bypass the reference buffer output using at least a 10µF, low-inductance, low-ESR capacitor placed as close as possible to the REF pin, thus minimizing additional PCB inductance. When using the internal bandgap reference source, bypass the REFIO pin with a 0.1µF capacitor to ground. If providing an external reference and using the internal reference buffer, drive the REFIO pin directly with an external reference source in the range of 3.0V to 4.25V. Finally, if disabling the MAX11166/MAX11167 internal bandgap reference source and internal reference buffer, drive the REF pin with a reference voltage in the range of 2.5V to 4.25V and place at least a 10µF, low-inductance, low-ESR capacitor placed as close as possible to the REF pin .

When using the MAX11166/MAX11167 in external reference mode, it is recommended that an external reference buffer be used. For bypass capacitors on the REF pin, X7R or X5R ceramic capacitors in a 1210 case size or smaller have been found to provide adequate bypass performance. Y5U or Z5U ceramics capacitors are not recommended due to their high voltage and temperature coefficients.

Maxim offers a wide range of precision references ideal for 16-bit accuracy. Table 1 lists some of the options recommended.

Input Amplifier

The conversion results are accurate when the ADC acquires the input signal for an interval longer than the input signal's worst-case settling time. The ADC input sampling capacitor charges during the acquisition period. During this acquisition period, the settling of the sampled voltage is affected by the source resistance and the input sampling capacitance. Sampling error can be estimated by modeling the time constant of the total input capacitance and the driving source impedance.

Although the MAX11166/MAX11167 are easy to drive, an amplifier buffer is recommended if the source impedance is such that when driving a switch capacitor of ~20pF a significant settling error in the desired sampling period will occur. If this is the case, it is recommended that a configuration shown in the *Typical Operating Circuit* is used where at least a 500pF capacitor is attached to the AIN+ pin. This capacitance reduces the size of the transient at the start of the acquisition period, which in some buffers will cause an input signal dependent offsets.

Regardless of whether an external buffer amp is used or not, the time constant, $R_{SOURCE} \times C_{LOAD}$, of the input should not exceed $t_{ACQ}/12$, where R_{SOURCE} is the total signal source impedance, C_{LOAD} is the total capacitance at the ADC input (external and internal) and t_{ACQ} is the acquisition period. Thus to obtain accurate sampling in a 500ns acquisition time a source impedance of less than 1042Ω should be used if driving the ADC directly. When driving the ADC from a buffer, it is recommended a series resistance (5Ω to 50Ω typical) between the amplifier and the external input capacitance as shown in the *Typical Operating Circuit*.

1) Fast settling time: For multichannel multiplexed applications the driving operational amplifier must be able to settle to 16-bit resolution when a full-scale step is applied during the minimum acquisition time.
2) Low noise: It is important to ensure that the driver amplifier has a low average noise density appropriate for the desired bandwidth of the application. When the MAX11166/MAX11167 are used with its full bandwidth of 6MHz, it is preferable to use an amplifier that will produce an output noise spectral density of less than 6nV/√Hz, to ensure that the overall SNR is not

Table 1. MAX11166/MAX11167 External Reference Recommendations

PART	V_{OUT} (V)	TEMPERATURE COEFFICIENT (MAX)	INITIAL ACCURACY (%)	NOISE (0.1Hz TO 10Hz) (μV_{P-P})	PACKAGE
MAX6126	2.5, 3, 4.096, 5.0	3 (A), 5 (B)	0.06	1.35	µMAX-8 SO-8
MAX6325 MAX6341 MAX6350	2.5, 4.096, 5.0	1	0.04, 0.02	1.5, 2.4, 3.0	SO-8

degraded significantly. It is recommended to insert an external RC filter at the MAX11166/MAX11167 AIN+ input to attenuate out-of-band input noise and preserve the ADCs SNR. The effective RMS noise at the MAX11166/MAX11167 AIN+ input is 64µV, thus additional noise from a buffer circuit should be significantly lower in order to achieve the maximum SNR performance.

3) THD performance: The input buffer amplifier used should have a comparable THD performance with that of the MAX11166/MAX11167 to ensure the THD of the digitized signal is not degraded.

Table 2 summarizes the operational amplifiers that are compatible with the MAX11166/MAX11167. The MAX9632 has sufficient bandwidth, low enough noise and distortion to support the full performance of the MAX11166/MAX11167. The MAX9633 is a dual amp and can support buffering for true pseudo-differential sampling.

Transfer Function

The ideal transfer characteristic for the MAX11166/MAX11167 is shown in Figure 3. The precise location of various points on the transfer function are given in Table 3.

1) This is also the code for an overranged analog input (V_{AIN+} - V_{AIN-} greater than +K x V_{REF}, K = 5.000/4.096).

2) This is also the code for an underranged analog input (V_{AIN+} - V_{AIN-} less than -K x V_{REF}, K = 5.000/4.096)

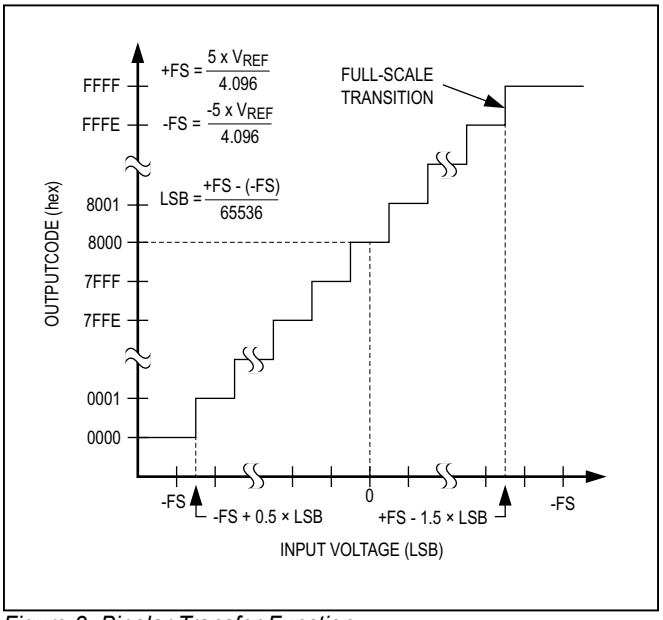


Figure 3. Bipolar Transfer Function

Table 2. List of Recommended ADC Driver Op Amps for MAX11166/MAX11167

AMPLIFIER	INPUT-NOISE DENSITY (nV/√Hz)	SMALL-SIGNAL BANDWIDTH (MHz)	SLEW RATE (V/µs)	THD (dB)	I_{CC} (mA)	COMMENTS
MAX9632	1	55	30	-128	3.9	Low noise, THD at 10kHz
MAX9633	3	27	18	-128	3.5	Low noise, dual amp, THD at 10kHz

Table 3. Transfer Function Example

CODE TRANSITION	BIPOLAR INPUT (V)	DIGITAL OUTPUT CODE (HEX)
+FS - 1.5 LSB	+4.999771	FFFE - FFFF
Midscale + 0.5 LSB	+0.000076	8000 - 8001
Midscale	0	8000
Midscale - 0.5 LSB	-0.000076	7FFF - 8000
-FS + 0.5 LSB	-4.999924	0000 - 0001[2]

Input Configuration Interface

An SPI interface clocked at up to 50MHz controls the MAX11166/MAX11167. Input configuration data is clocked into the configuration register on the falling edge of SCLK through the DIN pin. The data on DIN is used to program the ADC configuration register. The construct of this register is illustrated in Table 4. The configuration register defines the output interface mode, the reference mode, and the power-down state of the MAX11166/MAX11167.

Configuring in $\overline{CS}$ Mode

Figure 4 details the timing for loading the input configuration register when the MAX11166/MAX11167 are connected in $\overline{CS}$ mode (see Figure 6 and Figure 8 for hardware connections). The load process is enabled on the falling edge of CNVST when SCLK is held high. The configuration data is clocked into the configuration register through DIN on the next 8 SCLK falling edges. Pull CNVST high to complete the input configuration register load process. DIN should idle high outside an input configuration register read.

Table 4. ADC Configuration Register

BIT NAME	BIT	DEFAULT STATE	LOGIC STATE	FUNCTION
MODE	7:6	00	00	$\overline{CS}$ Mode, No-Busy Indicator
			01	$\overline{CS}$ Mode, with Busy Indicator
			10	Daisy-Chain Mode, No-Busy Indicator
			11	Daisy-Chain Mode, with Busy Indicator
REF	5:4	00	00	Reference Mode 0. Internal reference and reference buffer are both powered on.
			01	Reference Mode 1. Internal reference is turned off, but internal reference buffer powered on. Apply the external reference voltage at REFIO.
			10	Reference Mode 2. Internal reference is powered on, but the internal reference buffer is powered off. This mode allows for internal reference to be used with an external reference buffer.
			11	Reference Mode 3. Internal reference and reference buffer are both powered off. Apply an external reference voltage at REF.
SHDN	3	0	0	Normal Mode. All circuitry is fully powered up at all times.
			1	Static Shutdown. All circuitry is powered down.
Reserved	2:0	0	0	Reserved, Set to 0

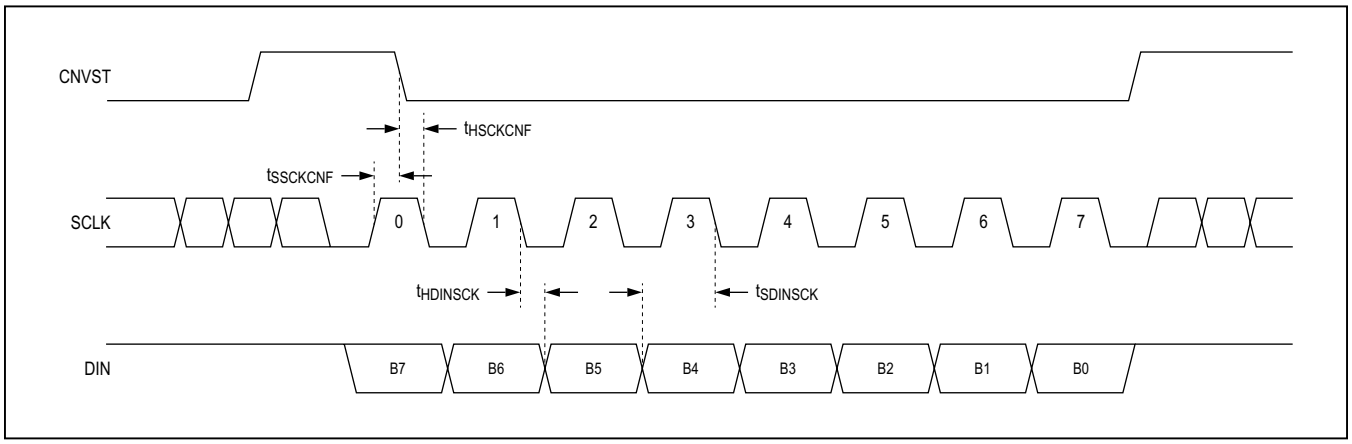


Figure 4. Input Configuration Timing in $\overline{CS}$ Mode

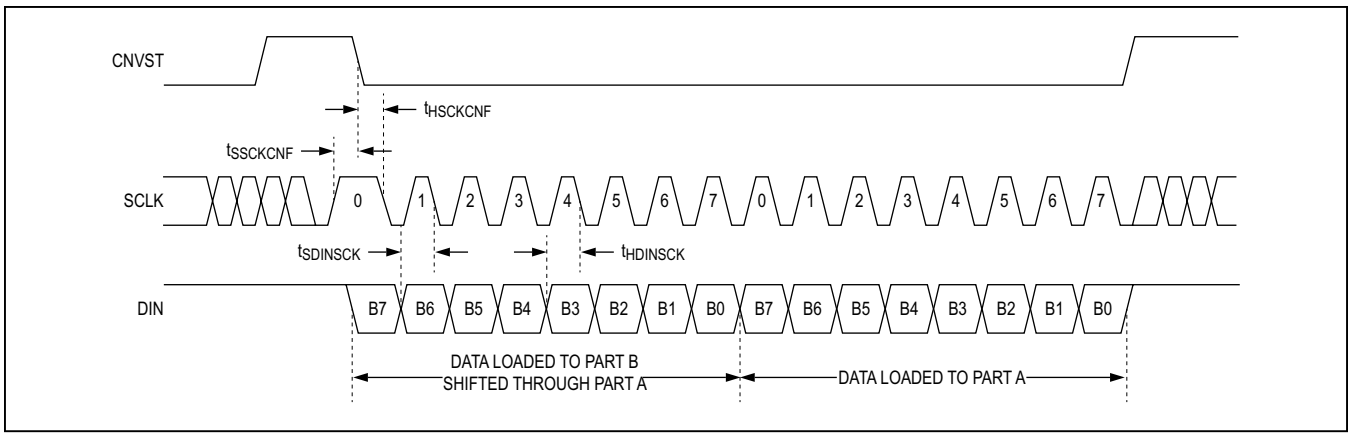


Figure 5. Input Configuration Timing in Daisy-Chain Mode

Configuring in Daisy-Chain Mode

Figure 5 details the configuration register load process when the MAX11166/MAX11167 are connected in a daisy-chain configuration (see Figure 12 and Figure 14 for hardware connections). The load process is enabled on the falling edge of CNVST when SCLK is held high. In daisy-chain mode, the input configuration registers are chained together through DOUT to DIN. Device A's DOUT will drive device B's DIN. The input configuration register is an 8-bit, first-in first-out shift register. The configuration data is clocked in N times through 8 x N falling SCLK edges. After the MAX11166/MAX11167 ADCs in the chain are loaded with the configuration byte, pull CNVST high to complete the configuration register loading process. Figure 5 illustrates a configuration sequence for loading two devices in a chain.

Data loaded into the configuration register alters the state of the MAX11166/MAX11167 on the next conversion cycle after the register is loaded. However, powering up the internal reference buffer or stabilizing the REFIO pin voltage will take several milliseconds to settle to 16-bit accuracy.

Shutdown Mode

The SHDN bit in the configuration register forces the MAX11166/MAX11167 into and out of shutdown. Set SHDN to 0 for normal operation. Set SHDN to 1 to shut down all internal circuitry and reset all registers to their default state.

Output Interface

The MAX11166/MAX11167 can be programmed into one of four output modes; $\overline{CS}$ modes with and without busy indicator and daisy-chain modes with and without busy indicator. When operating without busy indication, the user must externally timeout the maximum ADC conversion time before commencing readback. When operating in one of the two busy indication modes, the user can connect the DOUT output of the MAX11166/MAX11167 to an interrupt input on the digital host and use this interrupt to trigger the output data read.

Regardless of the output interface mode used, digital activity should be limited to the first half of the conversion phase. Having SCLK or DIN transitions near the sampling instance can also corrupt the input sample accuracy. Therefore, keep the digital inputs quiet for approximately 25ns before and 10ns after the rising edge of CNVST. These times are denoted as t_{SQ} and t_{HQ} in all subsequent timing diagrams.

In all interface modes, the data on DOUT is valid on both SCLK edges. However, the input setup time into the receiving digital host will be maximized when data is clocked into that digital host on the falling SCLK edge. Doing so will allow for higher data transfer rates between the MAX11166/MAX11167 and the digital host and consequently higher converter throughput.

In all interface modes, it is recommended that the SCLK be idled low to avoid triggering an input configuration write on the falling edge of CNVST. If at anytime the device detects a high SCLK state on a falling edge of CNVST, it will enter the input configuration write mode and will write the state of DIN on the next 8 falling SCLK edges to the input configuration register.

In all interface modes, all data bits from a previous conversion must be read before reading bits from a new conversion. When reading out conversion data, if too few SCLK falling edges are provided and all data bits are not read out, only the remaining unread data bits will be outputted during the next readout cycle. In such an event, the output data in every other readout cycle will appear to have been truncated as only the leftover bits from the previous readout cycle are outputted. This is an indication to the user that there are insufficient SCLK falling edges in a given readout cycle. Table 5 provides a guide to aid in the selection of the appropriate output interface mode for a given application.

$\overline{CS}$ No-Busy Indicator Mode

The $\overline{CS}$ no-busy indicator mode is ideally suited for maximum throughput when a single MAX11166/MAX11167 is connected to a SPI-compatible digital host. The connection diagram is shown in Figure 6, and the corresponding timing is provided in Figure 7.

A rising edge on CNVST completes the acquisition, initiates the conversion, and forces DOUT to high impedance. The conversion continues to completion irrespective of the state of CNVST allowing CNVST to be used as a select line for other devices on the board. If CNVST is brought low during a conversion and held low throughout the maximum conversion time, the MSB will be output at the end of the conversion.

When the conversion is complete, the MAX11166/MAX11167 enter the acquisition phase. Drive CNVST low to output the MSB onto DOUT. The remaining data bits are then clocked by subsequent SCLK falling edges. DOUT returns to high impedance after the 16th SCLK falling edge, or when CNVST goes high.

Table 5. ADC Output Interface Mode Selector Guide

MODE	TYPICAL APPLICATION AND BENEFITS
$\overline{CS}$ Mode, No-Busy Indicator	Single or multiple ADCs connected to SPI-compatible digital host. Ideally suited for maximum throughput.
$\overline{CS}$ Mode, With Busy Indicator	Single ADC connected to SPI-compatible digital host with interrupt input. Ideally suited for maximum throughput.
Daisy-Chain Mode, No-Busy Indicator	Multiple ADCs connected to a SPI-compatible digital host. Ideally suited for multichannel simultaneous sampled isolated applications.
Daisy-Chain Mode, With Busy Indicator	Multiple ADCs connected to a SPI-compatible digital host with interrupt input. Ideally suited for multichannel simultaneous sampled isolated applications.

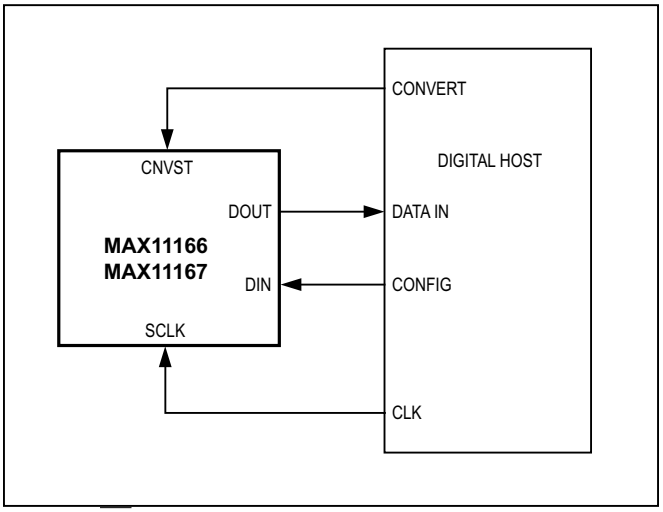


Figure 6. $\overline{CS}$ No-Busy Indicator Mode Connection Diagram

$\overline{CS}$ with Busy Indicator Mode

The $\overline{CS}$ with busy indicator mode is shown in Figure 8 where a single ADC is connected to a SPI-compatible digital host with interrupt input. The corresponding timing is given in Figure 9.

A rising edge on CNVST completes the acquisition, initiates the conversion and forces DOUT to high impedance. The conversion continues to completion irrespective of the state of CNVST allowing CNVST to be used as a select line for other devices on the board.

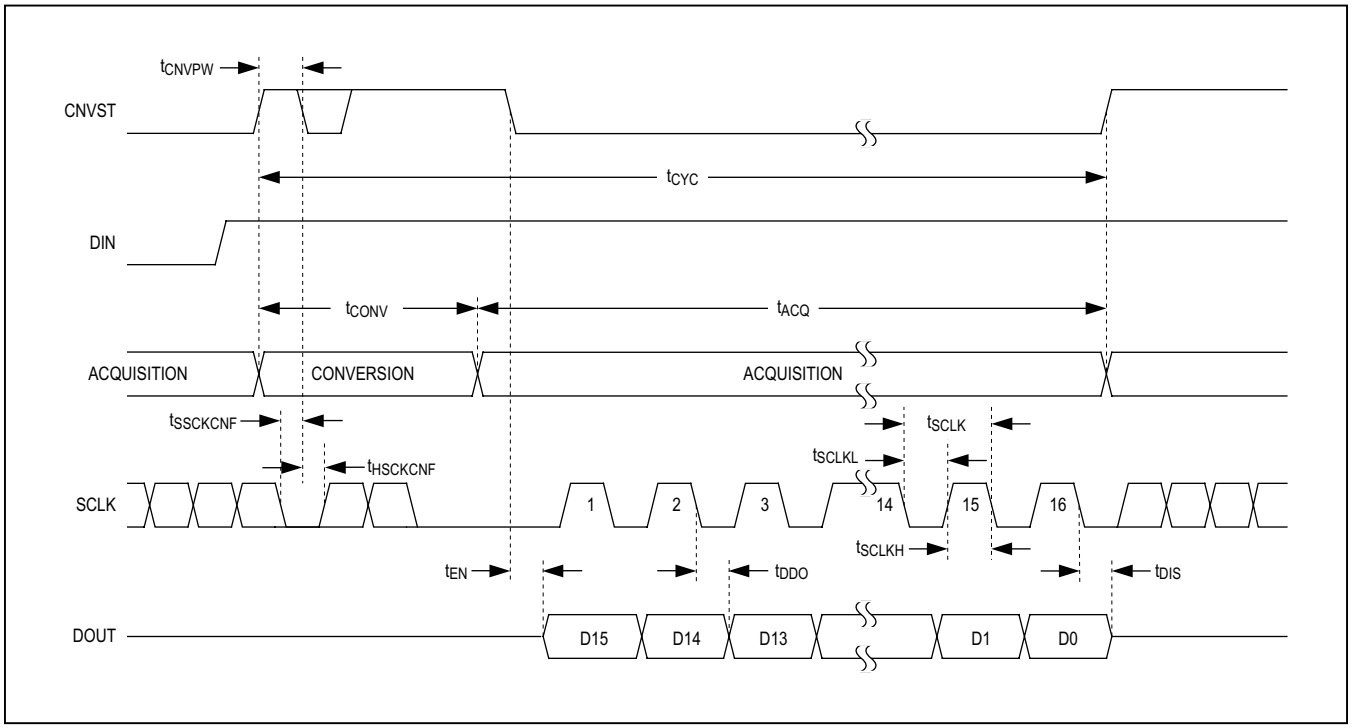


Figure 7. $\overline{CS}$ No Busy Indicator Mode Timing

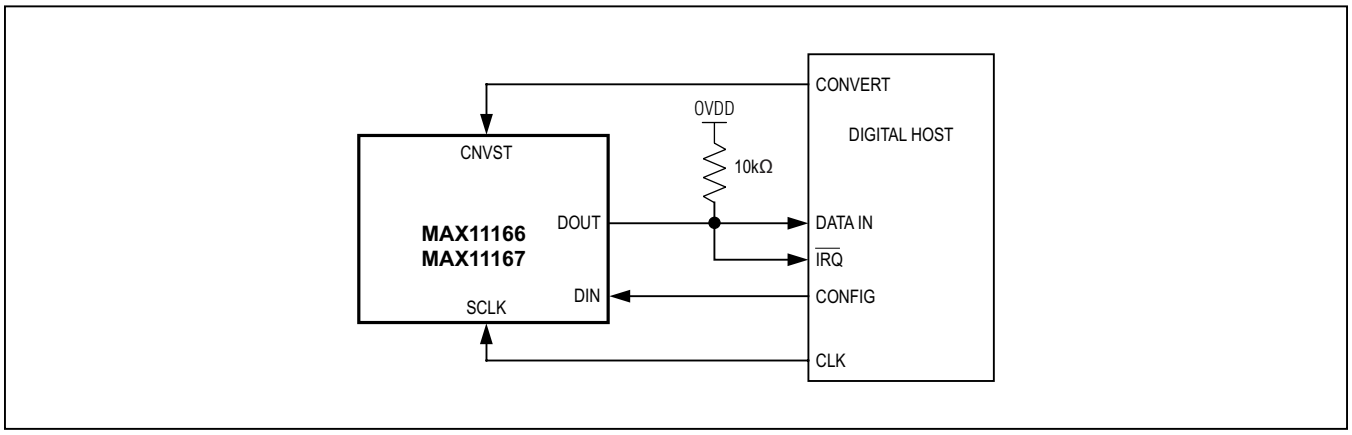


Figure 8. $\overline{CS}$ With Busy Indicator Mode Connection Diagram

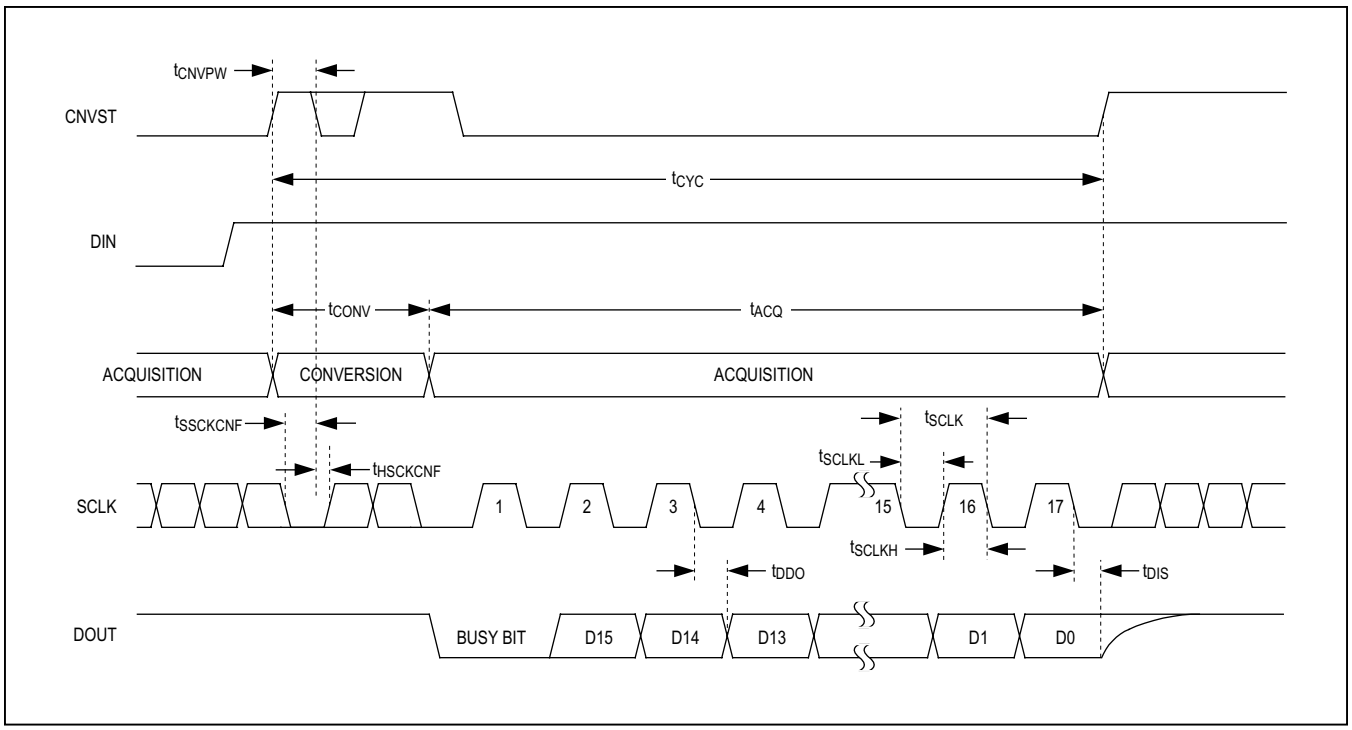


Figure 9. $\overline{CS}$ With Busy Indicator Mode Timing

When the conversion is complete, DOUT transitions from high impedance to a low logic level, signaling to the digital host through the interrupt input that data readback can commence. The MAX11166/MAX11167 then enter the acquisition phase. The data bits are then clocked out, MSB first, by subsequent SCLK falling edges. DOUT returns to high impedance after the 17th SCLK falling edge or when CNVST goes high, and is then pulled to OVDD through the external pullup resistor.