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MAX11192/MAX11195/ MAX11198

12-/14-/16-Bit, 2Msps, Dual Simultaneous Sampling SAR ADCs with Internal Reference

General Description

The MAX11192/MAX11195/MAX11198 is a dual-channel SAR ADCs with simultaneous sampling at 2Msps, 12-/14-/16-bit resolution, and differential inputs. Available in a tiny 16-pin, 3mm x 2mm ultra TDFN package, this ADC delivers excellent static and dynamic performance while operating from a supply voltage over the range of 3.0V to 5.25V. An integrated reference further reduces board area and component count.

The MAX11192/MAX11195/MAX11198 output conversion data using an SPI-compatible serial interface with a dual DOUT bus. Specifications apply over the extended industrial temperature range of -40°C to +125°C.

Applications

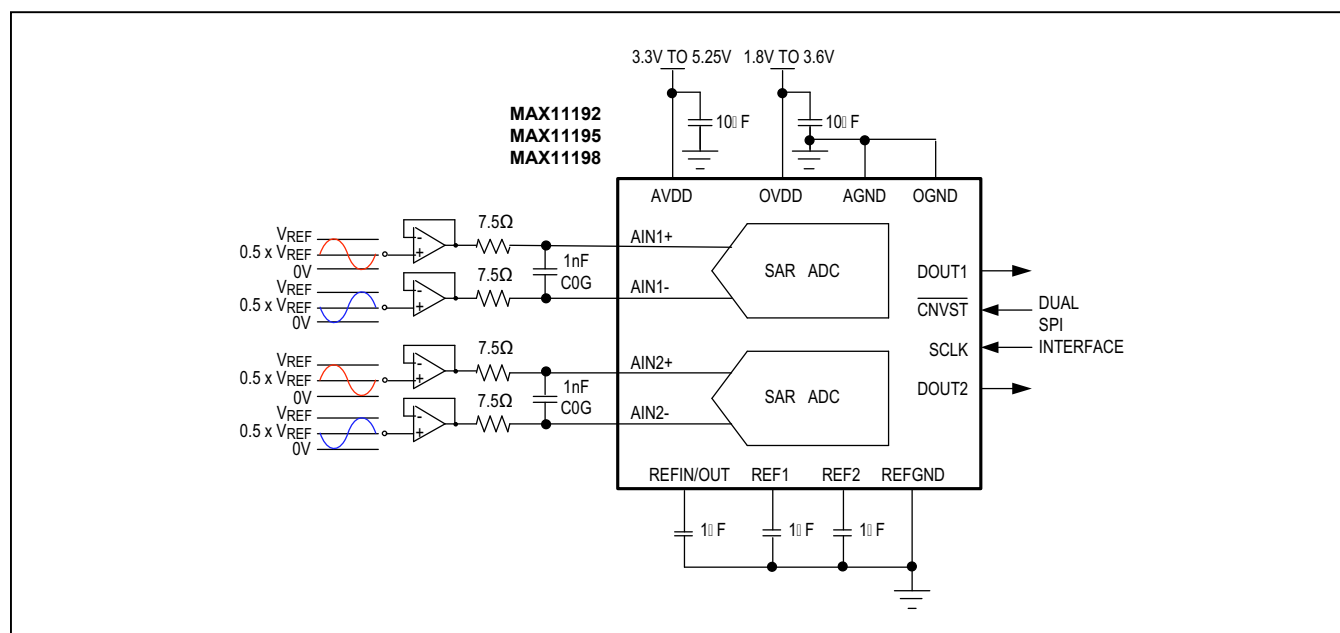
- Encoders
- Resolvers
- LVDT
- Current Sensing in Motors
- PLC

Benefits and Features

- Tiny 16-Pin, 3mm x 2mm, TDFN Package
- Up to 2Msps Throughput Rate
- Two Simultaneous-Sampling ADC Cores
- 2.5V Integrated Reference and Reference Buffers
- Two Data Outputs for the Two Simultaneous-Sampling ADCs
- No Overhead Clock Cycles; 12/14/16 Clock Cycles for 12-/14-/16-Bit Result
- Balanced, Differential Input Range of $\pm V_{REF}$

Ordering Information appears at end of data sheet.

Application Diagram



Absolute Maximum Ratings

AVDD to GND, REFGND, OGND-0.3V to +5.5V
 OVDD to GND, REFGND, OGND.....-0.3V to +5.5V
 AINn+, AINn- to GND, REFGND, OGND.. -0.3V to The lower of
 (V_{AVDD} + 0.3V) and +5.5V
 REF1N, REF1P, REF2N, REF2P to GND, REFGND, OGND.....-0.3V to
 The lower of (V_{AVDD} + 0.3V) and +5.5V
 CNVST, SCLK, DOUT1, DOUT2 to OGND.....-0.3V to
 The lower of (V_{OVDD} + 0.3V) and +5.5V
 GND to REFGND to OGND-0.3V to +0.3V

Maximum Current Into Any Pin-50mA to +50mA
 Continuous Power Dissipation (16 TDFN; T_A = +70°C;
 derate 16.7mW/°C above +70°C) ().....1333mW
 Operating Temperature Range.....-40°C to 125°C
 Junction Temperature.....+150°C
 Storage Temperature Range.....-65°C to +150°C
 Lead Temperature (soldering, 10s)+300°C
 Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

16 TDFN

PACKAGE CODE	T1623CN+1
Outline Number	21-100030
Land Pattern Number	—
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ _{JA})	60
Junction to Case (θ _{JC})	11

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Electrical Characteristics—MAX11192

(f_{Sample} = 2MSPS; V_{AVDD} = 5.0V, V_{OVDD} = 1.8V; V_{REFIN/OUT} = 2.5V (Internal Reference); T_A = T_{MIN} to T_{MAX} (Note 1). Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG INPUTS						
Input Voltage Range	V _{IN(DIFF)}	AINn+ – AINn-		±V _{REF}		V
Absolute Input Voltage Range	V _{IN(RNG)}	AINn+/AINn- relative to GND	-0.1		V _{AVDD} + 0.1	V
Common-Mode Input Voltage Range	CM _{IRNG}	(AINn+ + AINn-)/2	V _{REF/2} - 0.1		V _{REF/2} + 0.1	V
Input Leakage Current	I _{IN_LEAK}	Acquisition phase		1		µA
Input Capacitance	C _{IN}			10		pF

Electrical Characteristics—MAX11192 (continued)

($f_{\text{Sample}} = 2\text{MSPS}$; $V_{\text{AVDD}} = 5.0\text{V}$, $V_{\text{OVDD}} = 1.8\text{V}$; $V_{\text{REFIN/OUT}} = 2.5\text{V}$ (Internal Reference); $T_A = T_{\text{MIN}}$ to T_{MAX} (Note 1). Typical values are at $T_A = +25^\circ\text{C}$, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC PERFORMANCE (VREFIN/OUT = 2.5V, INTERNAL REFERENCE)						
Resolution	N		12			Bits
No Missing Codes			12			Bits
Offset Error	OE		-1		+1	LSB
Offset Error TC				1.2		mLSB/°C
Gain Error	GE	(Note 2)	-1		+1	LSB
Gain Error TC		(Note 2)		1.2		mLSB/°C
Integral Nonlinearity	INL		-0.5		+0.5	LSB
Differential Nonlinearity	DNL		-0.25		+0.25	LSB
Analog Input CMR	CMRR	Common Mode Range; $V_{\text{REF}/2} - 100\text{mV}$ to $V_{\text{REF}/2} + 100\text{mV}$		75		dB
Power-Supply Rejection	PSRR	AVDD		85		dB
Power Supply Rejection	PSRR	OVDD		90		dB
INTERNAL REFERENCE						
Initial Accuracy		$T_A = +25^\circ\text{C}$	2.498	2.500	2.502	V
Temperature Drift				5		ppm
EXTERNAL REFERENCE						
Input Voltage Range		External reference applied to REFIN	2.5		$V_{\text{AVDD}} - 0.25$	V
		External reference applied to REF1 or REF2	2.5		$V_{\text{AVDD}} + 0.1$	
REFERENCE BUFFERS						
Bypass Capacitor			1.0			μF
DYNAMIC PERFORMANCE (VREFIN/OUT = 2.5V, INTERNAL REFERENCE)						
Signal-to-Noise Ratio	SNR	10kHz input	73	73.5		dB
Signal-to-Noise And Distortion Ratio	SINAD	10kHz input		73.5		dB
Spurious-Free Dynamic Range	SFDR	10kHz input		102		dB
Total Harmonic Distortion	THD	10kHz input		-108		dB
Crossalk		10kHz input		-100		dB
DYNAMIC PERFORMANCE (VREFIN/OUT = 4.096V, EXTERNAL REFERENCE)						
Signal-to-Noise Ratio	SNR	10kHz input	73	73.5		dB
Signal-to-Noise And Distortion Ratio	SINAD	10kHz input		73.5		dB
Spurious-Free Dynamic Range	SFDR	10kHz input		102		dB
Total Harmonic Distortion	THD	10kHz input		-108		dB
Crossalk		10kHz input		-100		dB
SAMPLING DYNAMICS						
Throughput					2	Msps
Aperture Delay Match				150		ps
Input -3db Bandwidth	$f_{-3\text{dB}}$			50		MHz

Electrical Characteristics—MAX11192 (continued)

($f_{\text{Sample}} = 2\text{MSPS}$; $V_{\text{AVDD}} = 5.0\text{V}$, $V_{\text{OVDD}} = 1.8\text{V}$; $V_{\text{REFIN/OUT}} = 2.5\text{V}$ (Internal Reference); $T_A = T_{\text{MIN}}$ to T_{MAX} (Note 1). Typical values are at $T_A = +25^\circ\text{C}$, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLIES						
Analog Supply Voltage	AVDD		3.0	5.0	5.25	V
Interface Supply Voltage	OVDD		1.7		3.6	V
Analog Supply Current	I(AVDD)			5.5	6.2	mA
Interface Supply Current	I(OVDD)	DOUT load: $C_{\text{LOAD}} = 10\text{pF}$		0.75	1	mA
Analog Standby Current	$I_S(\text{AVDD})$	(Note 3)		1		mA
Interface Standby Current	$I_S(\text{OVDD})$	(Note 3)		1		μA
DIGITAL INPUTS						
Input Voltage High	V_{IH}		0.8 x V_{OVDD}			V
Input Voltage Low	V_{IL}				0.2 x V_{OVDD}	V
Input Capacitance			2			pF
Input Leakage			1			μA
DIGITAL OUTPUTS						
Output Voltage High	V_{OH}	$I_{\text{SOURCE}} = 2\text{mA}$	$V_{\text{OVDD}} - 0.4$			V
Output Voltage Low	V_{OL}	$I_{\text{SINK}} = 2\text{mA}$			$V_{\text{OGND}} + 0.4$	V
TIMING						
Conversion Period	t_1		500			ns
SCLK to DOUT Hold	t_2		1			ns
SCLK to DOUT Valid	t_3		14			ns
SCLK High	t_4		8			ns
SCLK Period	t_5		20			ns
SCLK low	t_6		8			ns
$\overline{\text{CNVST}}$ Rising Edge to SCLK Rising Edge	t_7		5			ns
SCLK Rising Edge to $\overline{\text{CNVST}}$ Rising Edge	t_8		5			ns
$\overline{\text{CNVST}}$ High	t_9		60			ns
$\overline{\text{CNVST}}$ Falling Edge to SCLK Rising Edge	t_{10}		10			ns
SCLK Falling Edge to $\overline{\text{CNVST}}$ Falling Edge	t_{11}		0			ns
$\overline{\text{CNVST}}$ Low Time for Valid Sample	t_{12}		400			ns

MAX11192/MAX11195/
MAX11198

12-/14-/16-Bit, 2MSPs, Dual Simultaneous
Sampling SAR ADCs with Internal Reference

Electrical Characteristics—MAX11195

($f_{\text{Sample}} = 2\text{MSPS}$; $V_{\text{AVDD}} = 5.0\text{V}$, $V_{\text{OVDD}} = 1.8\text{V}$; $V_{\text{REFIN/OUT}} = 2.5\text{V}$ (Internal Reference); $T_{\text{A}} = T_{\text{MIN}}$ to T_{MAX} (Note 1). Typical values are at $T_{\text{A}} = +25^{\circ}\text{C}$, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG INPUTS						
Input Voltage Range	$V_{\text{IN(DIFF)}}$	$\text{AINn+} - \text{AINn-}$		$\pm V_{\text{REF}}$		V
Absolute Input Voltage Range	$V_{\text{IN(RNG)}}$	$\text{AINn+}/\text{AINn-}$ relative to GND	-0.1		$V_{\text{AVDD}} + 0.1$	V
Common-Mode Input Voltage Range	CMI_{RNG}	$(\text{AINn+} + \text{AINn-})/2$	$V_{\text{REF}}/2 - 0.1$		$V_{\text{REF}}/2 + 0.1$	V
Input Leakage Current	$I_{\text{IN_LEAK}}$	Acquisition phase		1		μA
Input Capacitance	C_{IN}			10		pF
STATIC PERFORMANCE ($V_{\text{REFIN/OUT}} = 2.5\text{V}$, INTERNAL REFERENCE)						
Resolution	N		14			Bits
No Missing Codes			14			Bits
Offset Error	OE		-1.5		+1.5	LSB
Offset Error TC				4		mLSB/ $^{\circ}\text{C}$
Gain Error	GE	(Note 2)	-3.5		+3.5	LSB
Gain Error TC		(Note 2)		2		mLSB/ $^{\circ}\text{C}$
Integral Nonlinearity	INL		-1.0		+1.0	LSB
Differential Nonlinearity	DNL		-0.5		+0.5	LSB
Analog Input CMR	CMRR	Common Mode Range; $V_{\text{REF}}/2 - 100\text{mV}$ to $V_{\text{REF}}/2 + 100\text{mV}$		80		dB
Power-Supply Rejection	PSRR	AVDD		85		dB
Power Supply Rejection	PSRR	OVDD		90		dB
INTERNAL REFERENCE						
Initial Accuracy		$T_{\text{A}} = +25^{\circ}\text{C}$	2.498	2.500	2.502	V
Temperature Drift				5		ppm
EXTERNAL REFERENCE						
Input Voltage Range		External reference applied to REF _{IN}	2.5		$V_{\text{AVDD}} - 0.25$	V
		External reference applied to REF ₁ or REF ₂	2.5		$V_{\text{AVDD}} + 0.1$	
REFERENCE BUFFERS						
Bypass Capacitor			1.0			μF
DYNAMIC PERFORMANCE ($V_{\text{REFIN/OUT}} = 2.5\text{V}$, INTERNAL REFERENCE)						
Signal-to-Noise Ratio	SNR	10kHz input	82	83.7		dB
Signal-to-Noise And Distortion Ratio	SINAD	10kHz input		83.7		dB
Spurious-Free Dynamic Range	SFDR	10kHz input		115		dB
Total Harmonic Distortion	THD	10kHz input		-117		dB
Crossalk		10kHz input		-100		dB

Electrical Characteristics—MAX11195 (continued)

($f_{\text{Sample}} = 2\text{MSPS}$; $V_{\text{AVDD}} = 5.0\text{V}$, $V_{\text{OVDD}} = 1.8\text{V}$; $V_{\text{REFIN/OUT}} = 2.5\text{V}$ (Internal Reference); $T_A = T_{\text{MIN}}$ to T_{MAX} (Note 1). Typical values are at $T_A = +25^\circ\text{C}$, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DYNAMIC PERFORMANCE (VREFIN/OUT = 4.096V, EXTERNAL REFERENCE)						
Signal-to-Noise Ratio	SNR	10kHz input	84	84.6		dB
Signal-to-Noise And Distortion Ratio	SINAD	10kHz input		84.7		dB
Spurious-Free Dynamic Range	SFDR	10kHz input		112		dB
Total Harmonic Distortion	THD	10kHz input		-110		dB
Crossalk		10kHz input		-100		dB
SAMPLING DYNAMICS						
Throughput					2	MSPs
Aperture Delay Match				150		ps
Input -3db Bandwidth	$f_{-3\text{dB}}$			50		MHz
POWER SUPPLIES						
Analog Supply Voltage	AVDD		3.0	5.0	5.25	V
Interface Supply Voltage	OVDD		1.7		3.6	V
Analog Supply Current	$I(\text{AVDD})$			5.9	6.5	mA
Interface Supply Current	$I(\text{OVDD})$	DOUT load: $C_{\text{LOAD}} = 10\text{pF}$		0.75	1.1	mA
Analog Standby Current	$I_S(\text{AVDD})$	(Note 3)		1		mA
Interface Standby Current	$I_S(\text{OVDD})$	(Note 3)		1		μA
DIGITAL INPUTS						
Input Voltage High	V_{IH}		0.8 x V_{OVDD}			V
Input Voltage Low	V_{IL}			0.2 x V_{OVDD}		V
Input Capacitance				2		pF
Input Leakage				1		μA
DIGITAL OUTPUTS						
Output Voltage High	V_{OH}	$I_{\text{SOURCE}} = 2\text{mA}$	$V_{\text{OVDD}} - 0.4$			V
Output Voltage Low	V_{OL}	$I_{\text{SINK}} = 2\text{mA}$		$V_{\text{OGND}} + 0.4$		V
TIMING						
Conversion Period	t_1		500			ns
SCLK to DOUT Hold	t_2		1			ns
SCLK to DOUT Valid	t_3		14			ns
SCLK High	t_4		8			ns
SCLK Period	t_5		20			ns
SCLK low	t_6		8			ns
CNVST Rising Edge to SCLK Rising Edge	t_7		5			ns

Electrical Characteristics—MAX11195 (continued)

($f_{\text{Sample}} = 2\text{MSPS}$; $V_{\text{AVDD}} = 5.0\text{V}$, $V_{\text{OVDD}} = 1.8\text{V}$; $V_{\text{REFIN/OUT}} = 2.5\text{V}$ (Internal Reference); $T_A = T_{\text{MIN}}$ to T_{MAX} (Note 1). Typical values are at $T_A = +25^\circ\text{C}$, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLK Rising Edge to $\overline{\text{CNVST}}$ Rising Edge	t_8		5			ns
$\overline{\text{CNVST}}$ High	t_9		60			ns
$\overline{\text{CNVST}}$ Falling Edge to SCLK Rising Edge	t_{10}		10			ns
SCLK Falling Edge to $\overline{\text{CNVST}}$ Falling Edge	t_{11}		0			ns
$\overline{\text{CNVST}}$ Low Time for Valid Sample	t_{12}		400			ns

Electrical Characteristics—MAX11198

($f_{\text{Sample}} = 2\text{MSPS}$; $V_{\text{AVDD}} = 5.0\text{V}$, $V_{\text{OVDD}} = 1.8\text{V}$; $V_{\text{REFIN/OUT}} = 2.5\text{V}$ (Internal Reference); $T_A = T_{\text{MIN}}$ to T_{MAX} (Note 1). Typical values are at $T_A = +25^\circ\text{C}$, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG INPUTS						
Input Voltage Range	$V_{\text{IN(DIFF)}}$	$\text{AINn+} - \text{AINn-}$		$\pm V_{\text{REF}}$		V
Absolute Input Voltage Range	$V_{\text{IN(RNG)}}$	$\text{AINn+}/\text{AINn-}$ relative to GND	-0.1		$V_{\text{AVDD}} + 0.1$	V
Common-Mode Input Voltage Range	CMIRNG	$(\text{AINn+} + \text{AINn-})/2$	$V_{\text{REF}}/2 - 0.1$		$V_{\text{REF}}/2 + 0.1$	V
Input Leakage Current	$I_{\text{IN_LEAK}}$	Acquisition phase		1		μA
Input Capacitance	C_{IN}			10		pF
STATIC PERFORMANCE ($V_{\text{REFIN/OUT}} = 2.5\text{V}$, INTERNAL REFERENCE)						
Resolution	N		16			Bits
No Missing Codes			16			Bits
Offset Error	OE		-4		+4	LSB
Offset Error TC				10		mLSB/ $^\circ\text{C}$
Gain Error	GE	(Note 2)	-4		+4	LSB
Gain Error TC		(Note 2)		5		mLSB/ $^\circ\text{C}$
Integral Nonlinearity	INL		-1.5		+1.5	LSB
Differential Nonlinearity	DNL		-0.5		+0.5	LSB
Analog Input CMR	CMRR	Common Mode Range; $V_{\text{REF}}/2 - 100\text{mV}$ to $V_{\text{REF}}/2 + 100\text{mV}$		80.5		dB
Power-Supply Rejection	PSRR	AVDD		85		dB
Power Supply Rejection	PSRR	OVDD		90		dB
INTERNAL REFERENCE						
Initial Accuracy		$T_A = +25^\circ\text{C}$	2.498	2.500	2.502	V
Temperature Drift				5		ppm

Electrical Characteristics—MAX11198 (continued)

($f_{\text{Sample}} = 2\text{MSPS}$; $V_{\text{AVDD}} = 5.0\text{V}$, $V_{\text{OVDD}} = 1.8\text{V}$; $V_{\text{REFIN/OUT}} = 2.5\text{V}$ (Internal Reference); $T_A = T_{\text{MIN}}$ to T_{MAX} (Note 1). Typical values are at $T_A = +25^\circ\text{C}$, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
EXTERNAL REFERENCE						
Input Voltage Range		External reference applied to REFIN	2.5		$V_{\text{AVDD}} - 0.25$	V
		External reference applied to REF1 or REF2	2.5		$V_{\text{AVDD}} + 0.1$	
REFERENCE BUFFERS						
Bypass Capacitor			1.0			μF
DYNAMIC PERFORMANCE (VREFIN/OUT = 2.5V, INTERNAL REFERENCE)						
Signal-to-Noise Ratio	SNR	10kHz input	86	89		dB
Signal-to-Noise And Distortion Ratio	SINAD	10kHz input		88.8		dB
Spurious-Free Dynamic Range	SFDR	10kHz input		115		dB
Total Harmonic Distortion	THD	10kHz input		-117		dB
Crossalk		10kHz input		-100		dB
DYNAMIC PERFORMANCE (VREFIN/OUT = 4.096V, EXTERNAL REFERENCE)						
Signal-to-Noise Ratio	SNR	10kHz input	90	91.7		dB
Signal-to-Noise And Distortion Ratio	SINAD	10kHz input		91.6		dB
Spurious-Free Dynamic Range	SFDR	10kHz input		114		dB
Total Harmonic Distortion	THD	10kHz input		-111		dB
Crossalk		10kHz input		-100		dB
SAMPLING DYNAMICS						
Throughput					2	Msps
Aperture Delay Match				150		ps
Input -3db Bandwidth	$f_{-3\text{dB}}$			50		MHz
POWER SUPPLIES						
Analog Supply Voltage	AVDD		3.0	5.0	5.25	V
Interface Supply Voltage	OVDD		1.7		3.6	V
Analog Supply Current	$I(\text{AVDD})$			6.3	7	mA
Interface Supply Current	$I(\text{OVDD})$	DOUT load: $C_{\text{LOAD}} = 10\text{pF}$		0.75	1.2	mA
Analog Standby Current	$I_{\text{S}}(\text{AVDD})$	(Note 3)		1		mA
Interface Standby Current	$I_{\text{S}}(\text{OVDD})$	(Note 3)		1		μA
DIGITAL INPUTS						
Input Voltage High	V_{IH}		0.8 x V_{OVDD}			V
Input Voltage Low	V_{IL}		0.2 x V_{OVDD}			V
Input Capacitance				2		pF
Input Leakage				1		μA

Electrical Characteristics—MAX11198 (continued)

($f_{\text{Sample}} = 2\text{MSPS}$; $V_{\text{AVDD}} = 5.0\text{V}$, $V_{\text{OVDD}} = 1.8\text{V}$; $V_{\text{REFIN/OUT}} = 2.5\text{V}$ (Internal Reference); $T_A = T_{\text{MIN}}$ to T_{MAX} (Note 1). Typical values are at $T_A = +25^\circ\text{C}$, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL OUTPUTS						
Output Voltage High	V_{OH}	$I_{\text{SOURCE}} = 2\text{mA}$	$V_{\text{OVDD}} - 0.4$			V
Output Voltage Low	V_{OL}	$I_{\text{SINK}} = 2\text{mA}$			$V_{\text{OGND}} + 0.4$	V
TIMING						
Conversion Period	t_1		500			ns
SCLK to DOUT Hold	t_2		1			ns
SCLK to DOUT Valid	t_3		14			ns
SCLK High	t_4		8			ns
SCLK Period	t_5		20			ns
SCLK low	t_6		8			ns
$\overline{\text{CNVST}}$ Rising Edge to SCLK Rising Edge	t_7		5			ns
SCLK Rising Edge to $\overline{\text{CNVST}}$ Rising Edge	t_8		5			ns
$\overline{\text{CNVST}}$ High	t_9		60			ns
$\overline{\text{CNVST}}$ Falling Edge to SCLK Rising Edge	t_{10}		10			ns
SCLK Falling Edge to $\overline{\text{CNVST}}$ Falling Edge	t_{11}		0			ns
$\overline{\text{CNVST}}$ Low Time for Valid Sample	t_{12}		400			ns

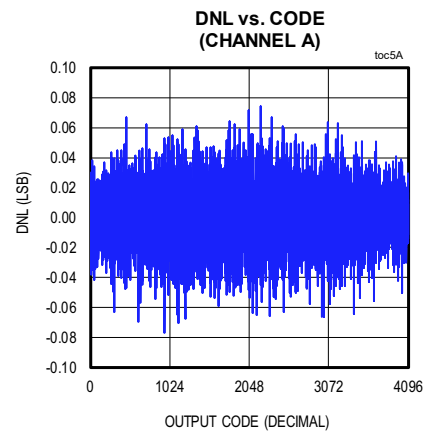
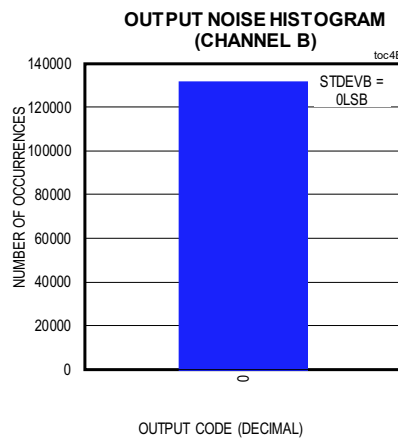
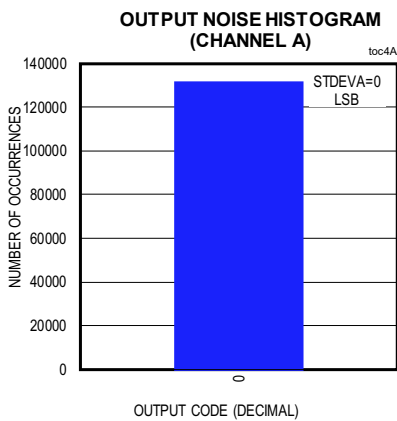
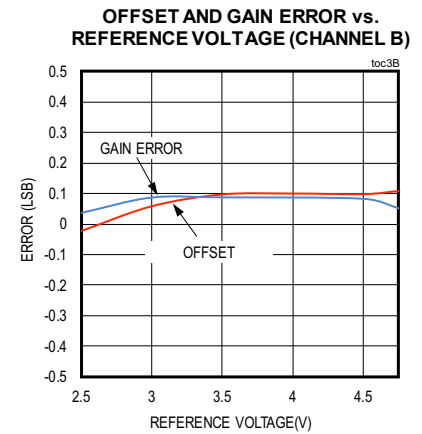
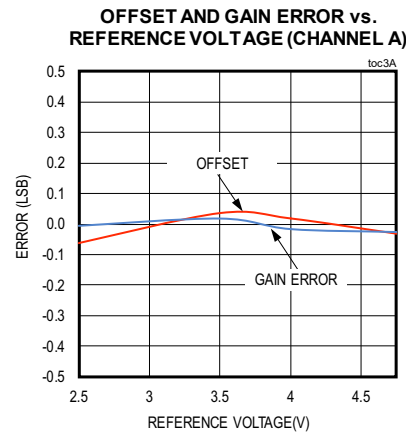
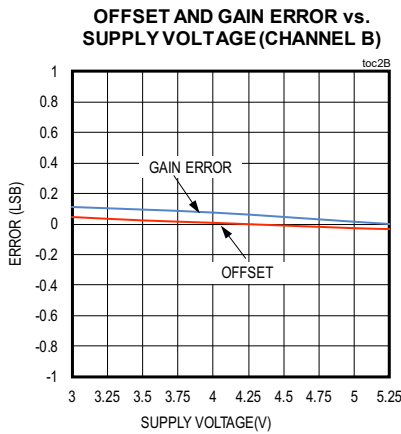
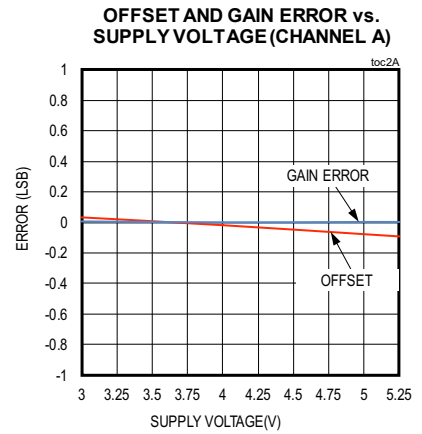
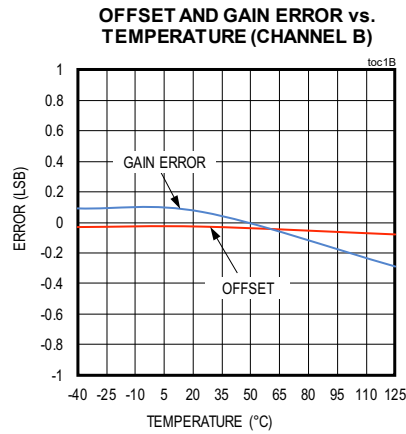
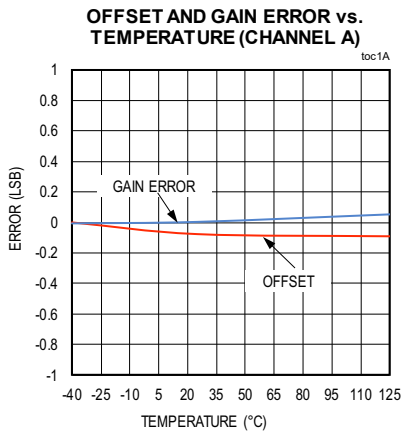
Note 1: Units are 100% production tested at $T_A = +25^\circ\text{C}$ and are guaranteed by design and characterization from $T_A = T_{\text{MIN}}$ to T_{MAX} .

Note 2: Exclude the reference drift and offset error.

Note 3: This current is drawn when the device has completed conversion and SCLK is idle.

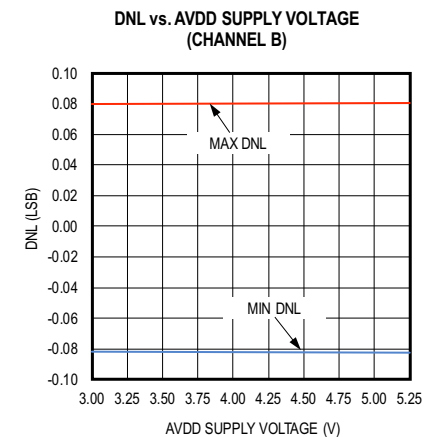
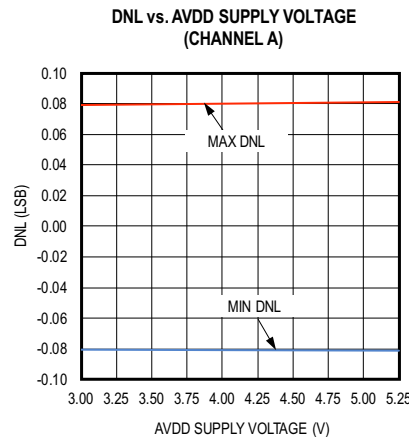
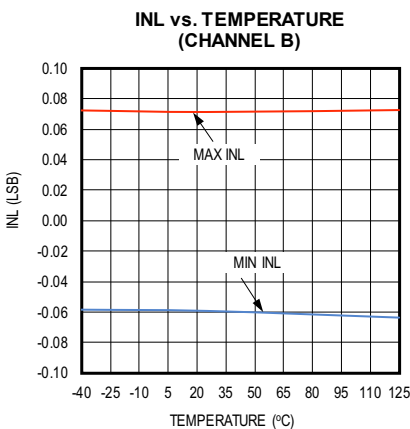
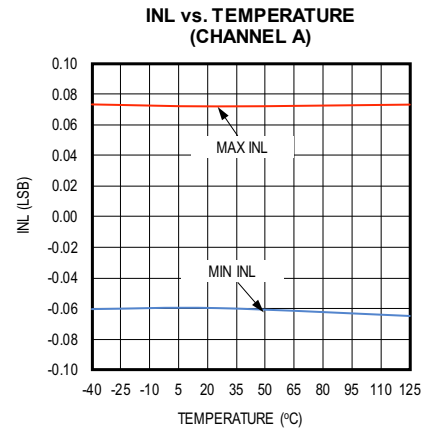
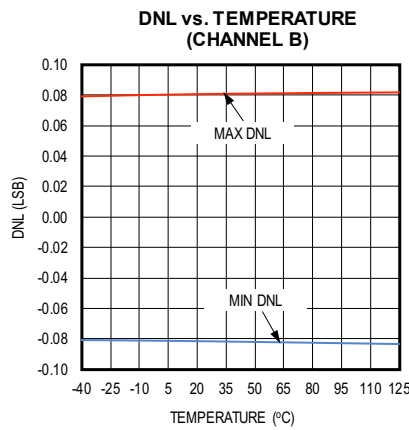
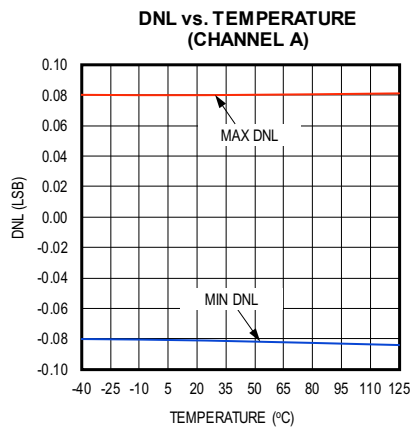
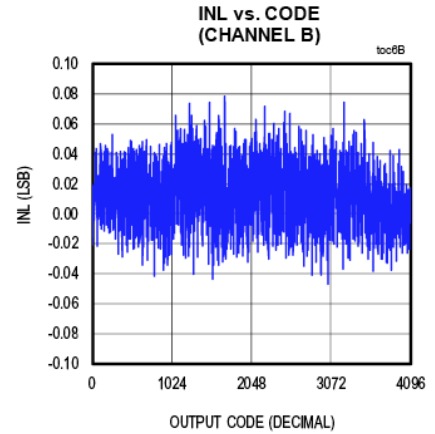
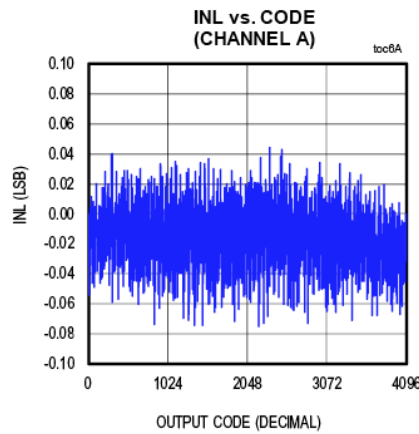
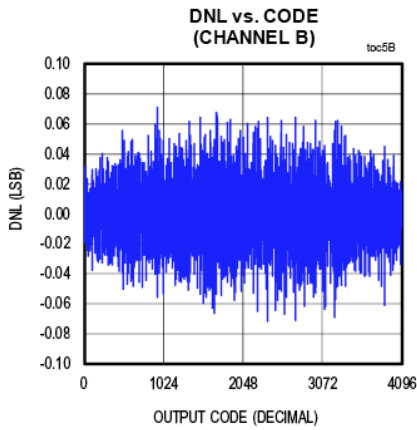
Typical Operating Characteristics—MAX11192

($f_{SAMPLE} = 2\text{MSPS}$; $V_{AVDD} = 5.0\text{V}$, $V_{OVDD} = 1.8\text{V}$; $V_{REFIN/OUT} = 2.5\text{V}$ (Internal Reference); $T_A = T_{MIN}$ to T_{MAX} . Typical values are at $T_A = +25^\circ\text{C}$, unless otherwise noted.)



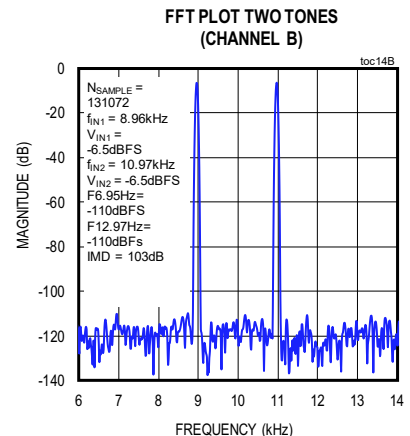
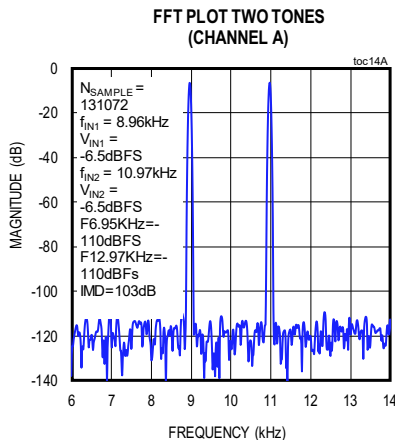
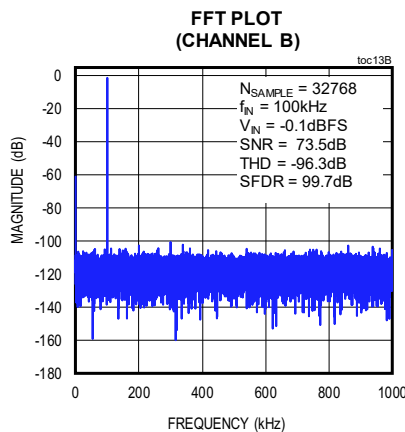
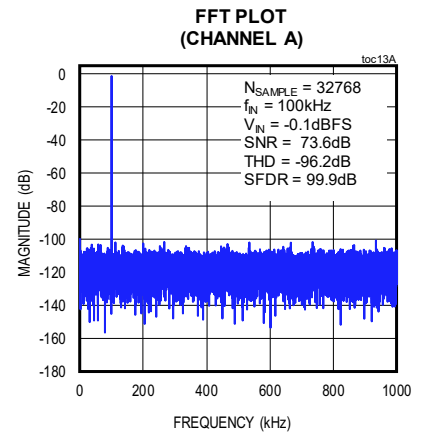
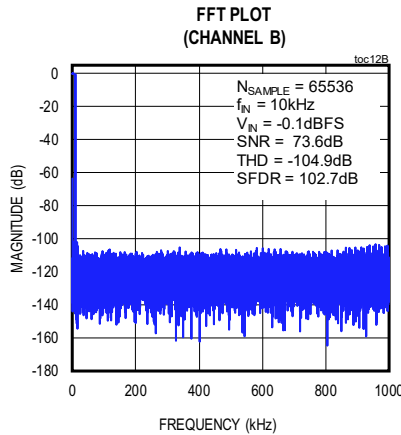
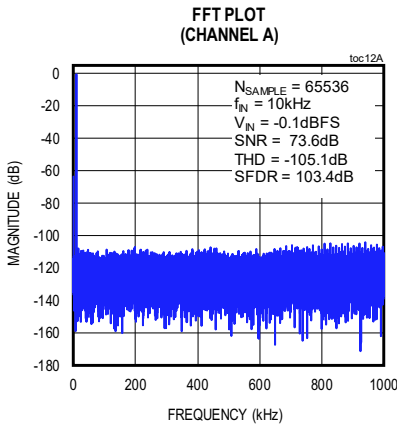
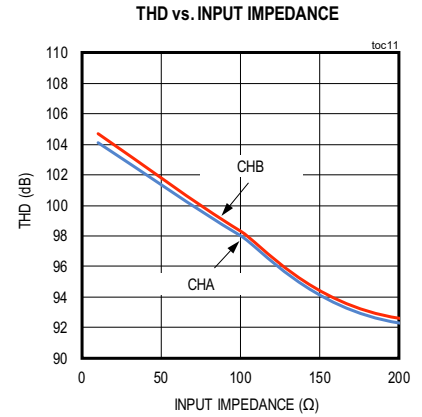
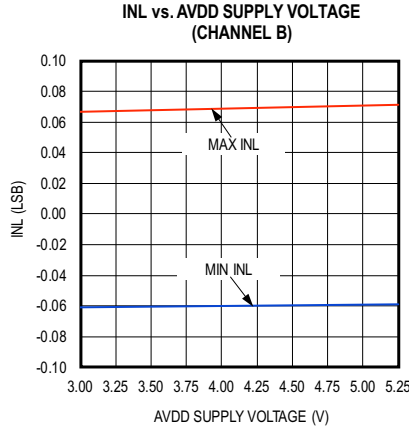
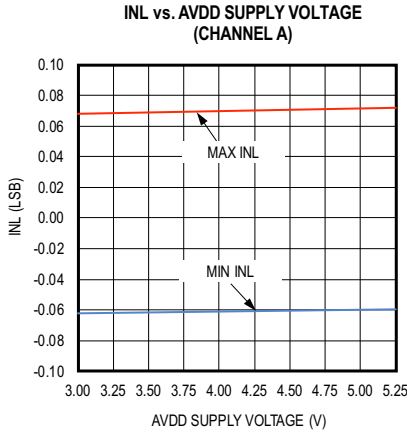
Typical Operating Characteristics—MAX11192 (continued)

($f_{SAMPLE} = 2\text{MSPS}$; $V_{AVDD} = 5.0\text{V}$, $V_{OVDD} = 1.8\text{V}$; $V_{REFIN/OUT} = 2.5\text{V}$ (Internal Reference); $T_A = T_{MIN}$ to T_{MAX} . Typical values are at $T_A = +25^\circ\text{C}$, unless otherwise noted.)



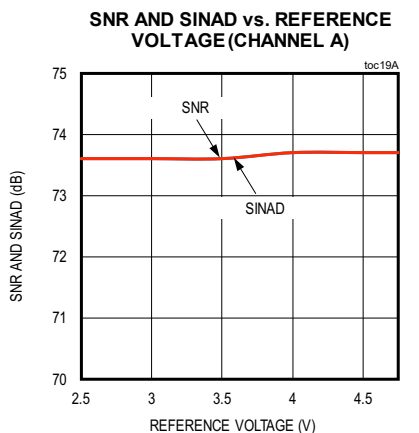
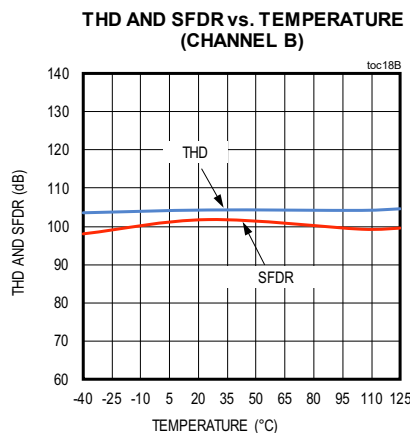
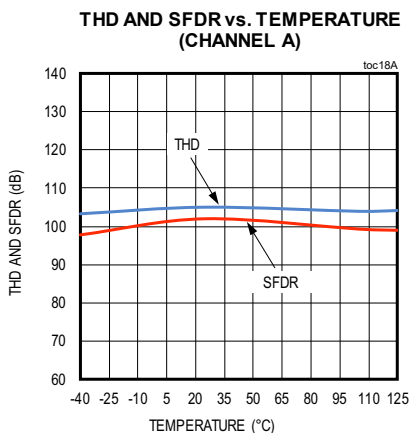
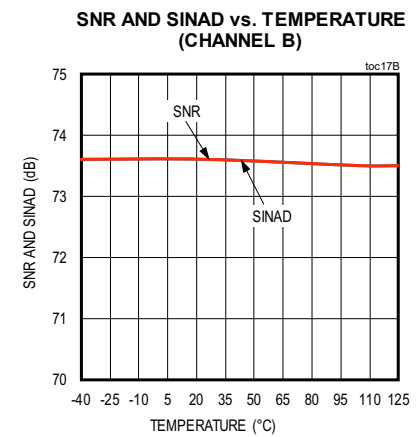
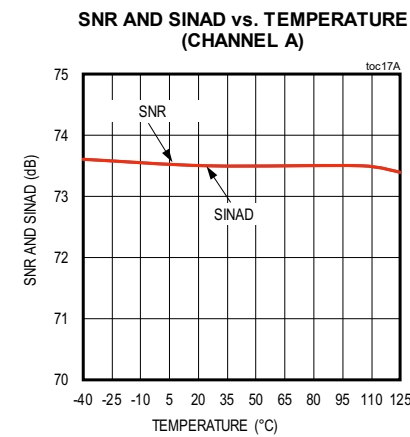
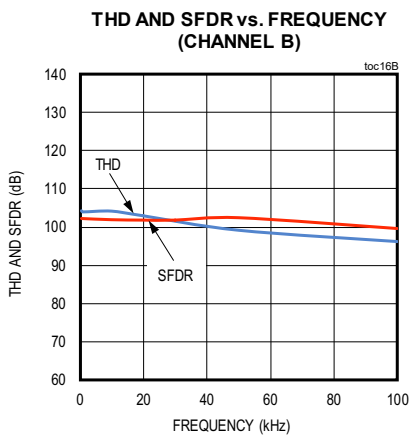
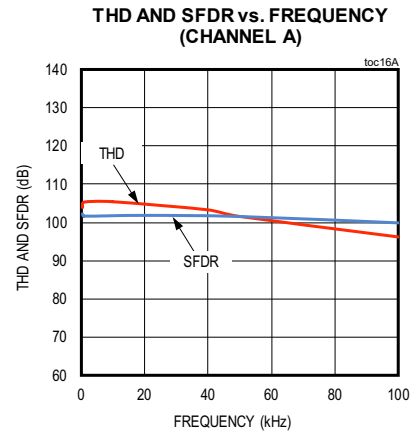
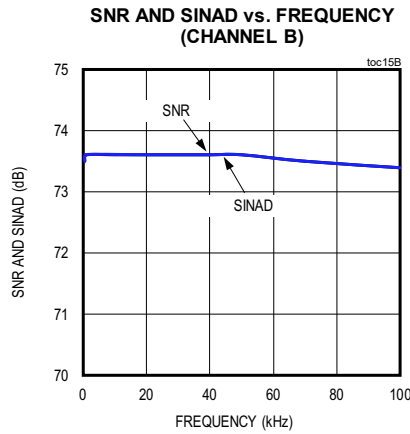
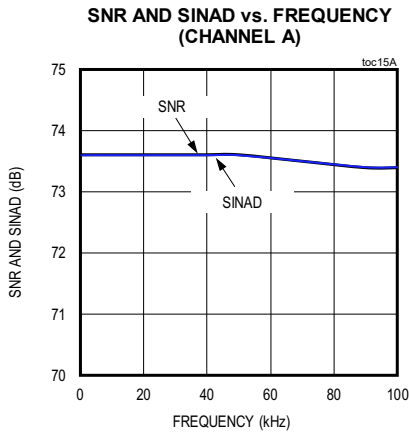
Typical Operating Characteristics—MAX11192 (continued)

($f_{SAMPLE} = 2\text{MSPS}$; $V_{AVDD} = 5.0\text{V}$, $V_{OVDD} = 1.8\text{V}$; $V_{REFIN/OUT} = 2.5\text{V}$ (Internal Reference); $T_A = T_{MIN}$ to T_{MAX} . Typical values are at $T_A = +25^\circ\text{C}$, unless otherwise noted.)



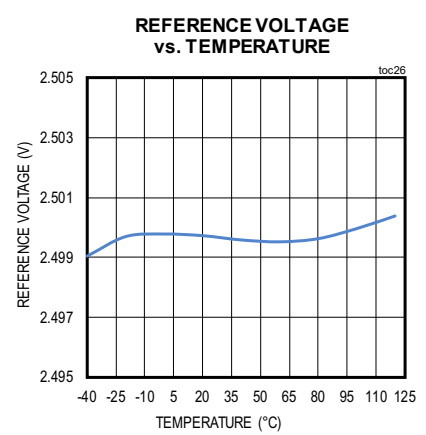
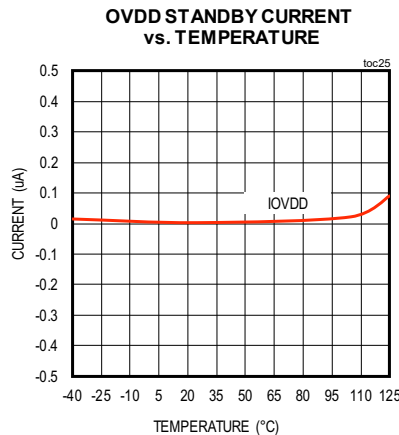
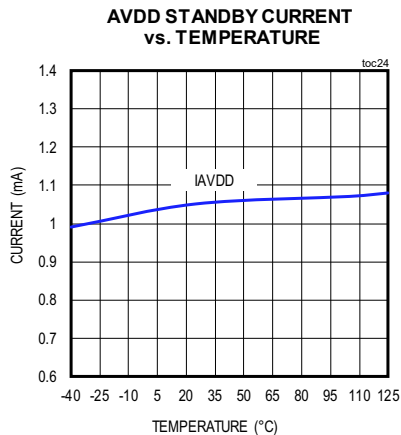
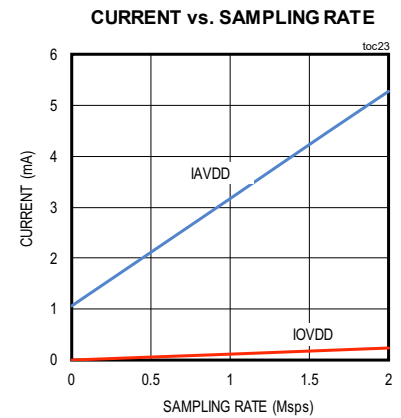
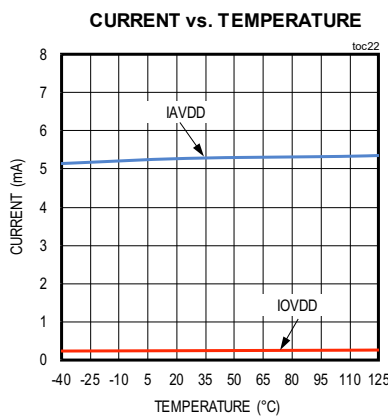
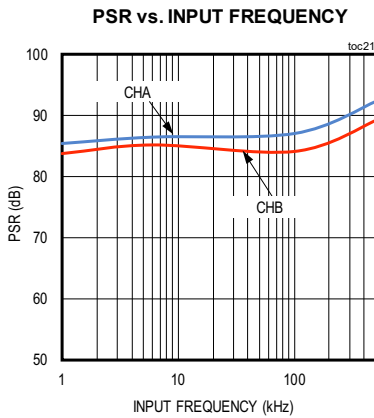
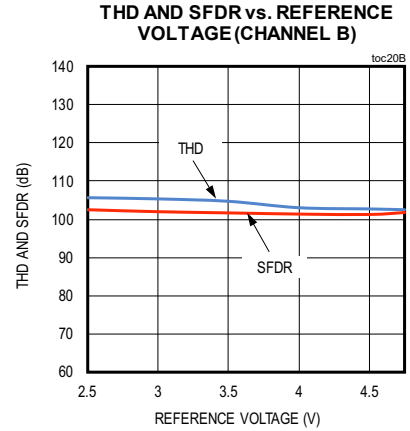
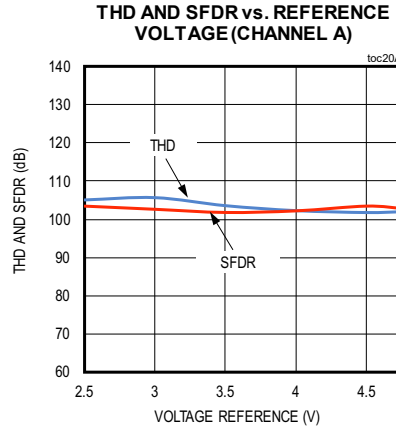
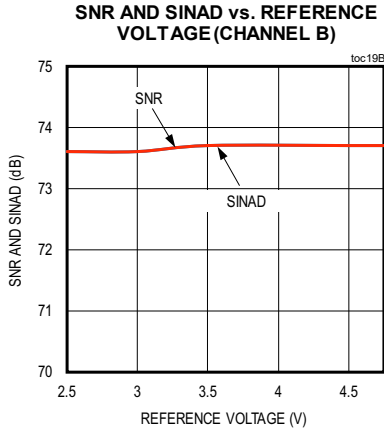
Typical Operating Characteristics—MAX11192 (continued)

($f_{SAMPLE} = 2\text{MSPS}$; $V_{AVDD} = 5.0\text{V}$, $V_{OVDD} = 1.8\text{V}$; $V_{REFIN/OUT} = 2.5\text{V}$ (Internal Reference); $T_A = T_{MIN}$ to T_{MAX} . Typical values are at $T_A = +25^\circ\text{C}$, unless otherwise noted.)



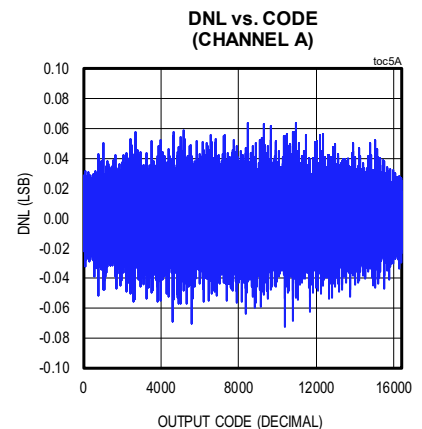
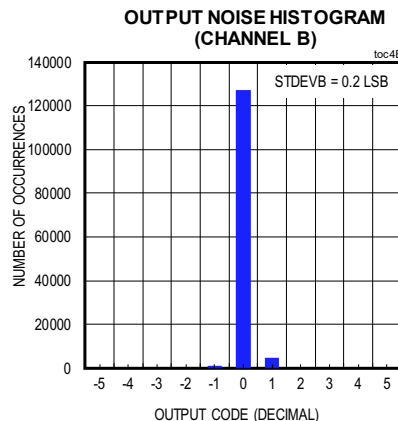
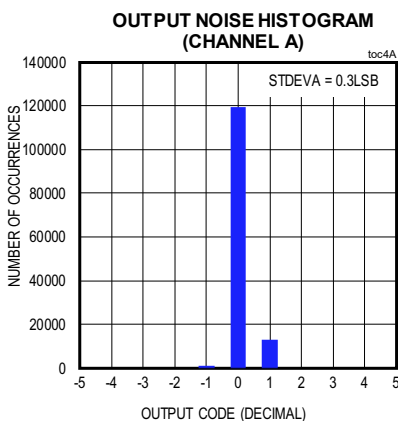
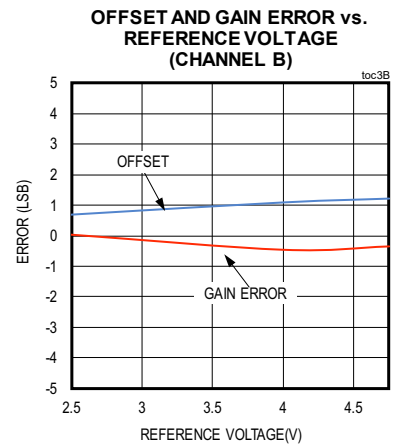
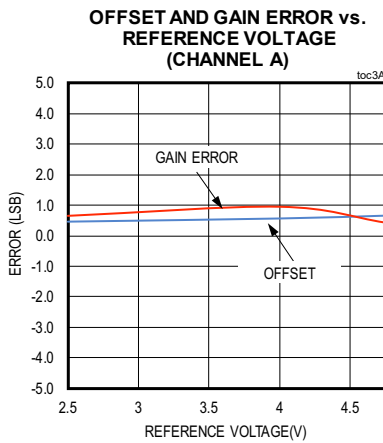
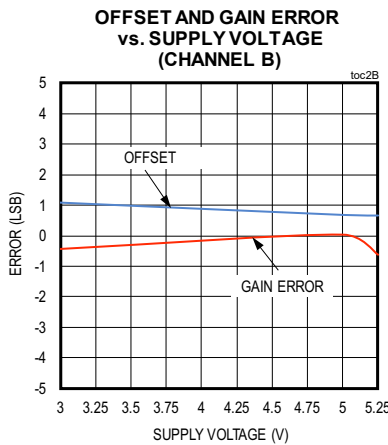
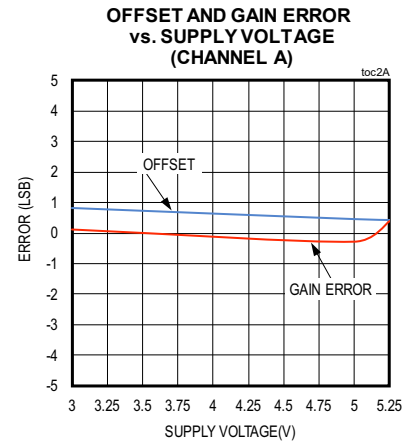
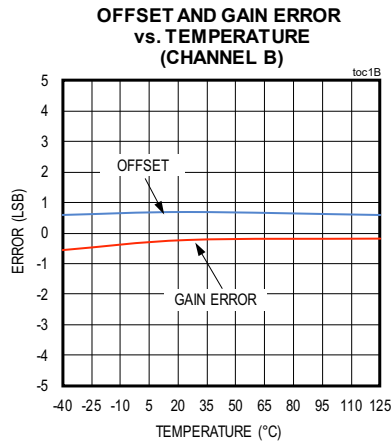
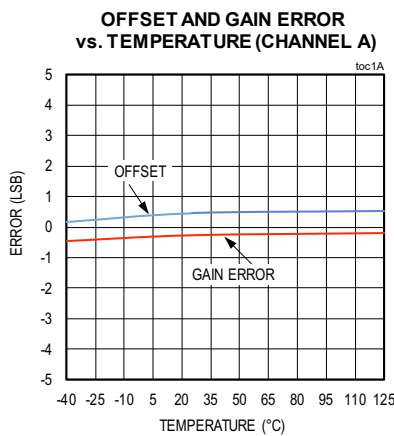
Typical Operating Characteristics—MAX11192 (continued)

($f_{SAMPLE} = 2\text{MSPS}$; $V_{AVDD} = 5.0\text{V}$, $V_{OVDD} = 1.8\text{V}$; $V_{REFIN/OUT} = 2.5\text{V}$ (Internal Reference); $T_A = T_{MIN}$ to T_{MAX} . Typical values are at $T_A = +25^\circ\text{C}$, unless otherwise noted.)



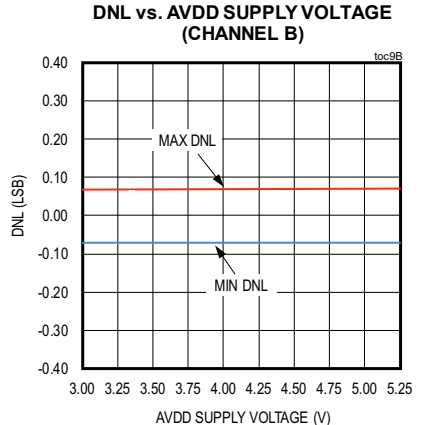
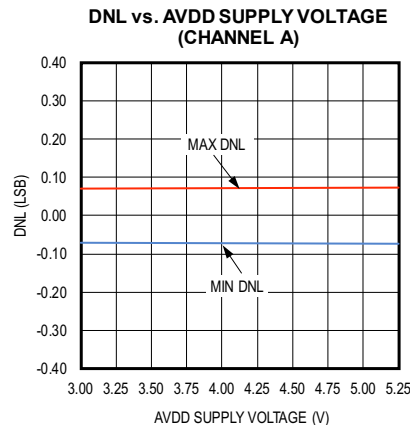
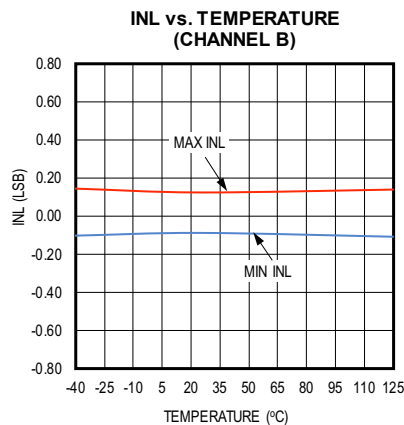
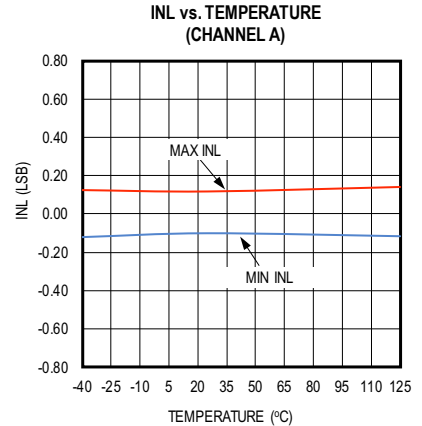
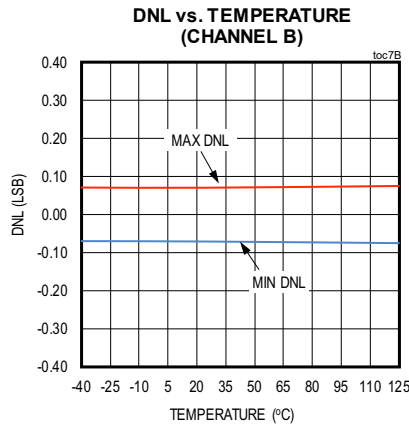
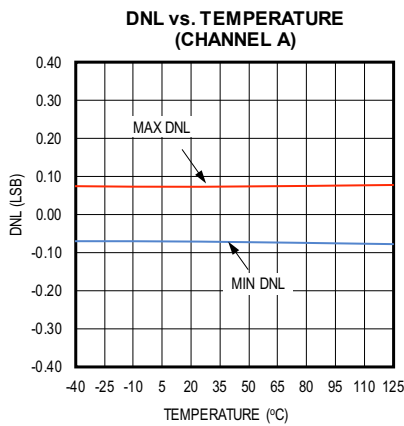
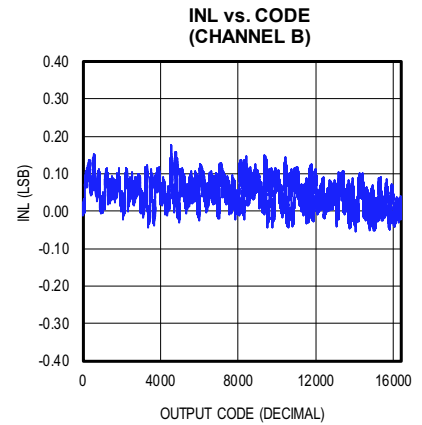
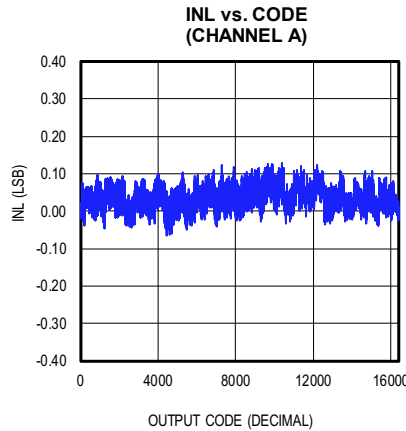
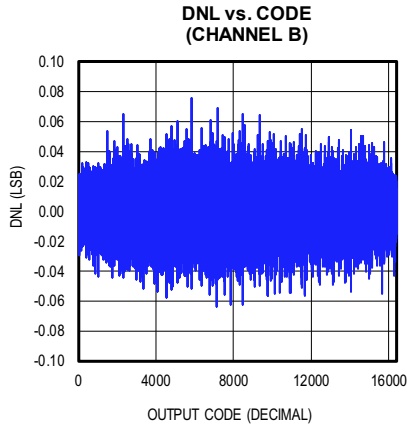
Typical Operating Characteristics—MAX11195

($f_{SAMPLE} = 2\text{MSPs}$; $V_{AVDD} = 5.0\text{V}$, $V_{OVDD} = 1.8\text{V}$; $V_{REFIN/OUT} = 2.5\text{V}$ (Internal Reference); $T_A = T_{MIN}$ to T_{MAX} . Typical values are at $T_A = +25^\circ\text{C}$, unless otherwise noted.)



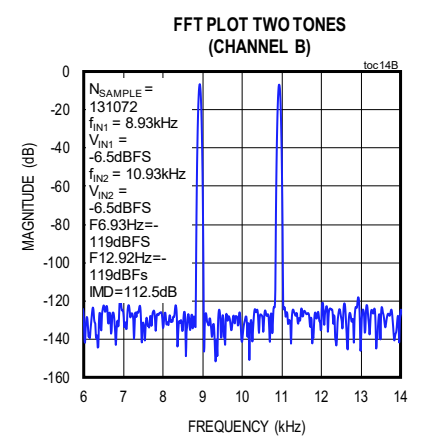
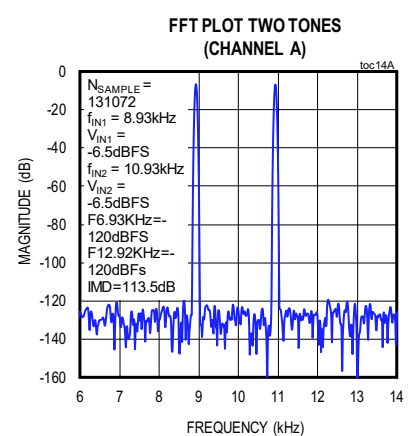
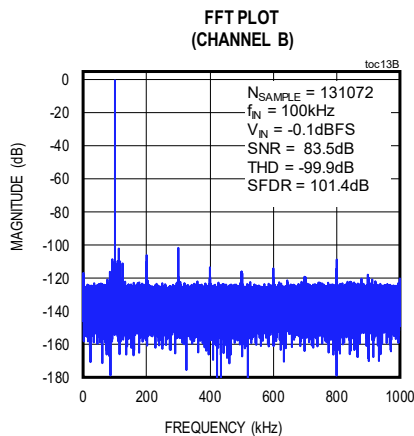
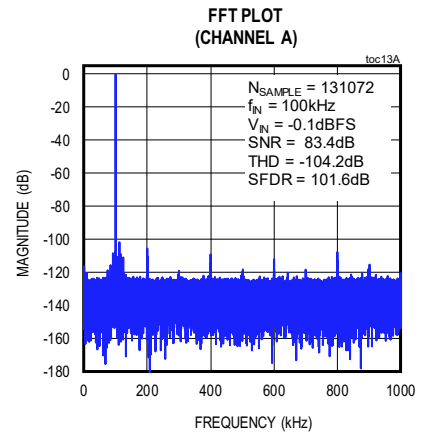
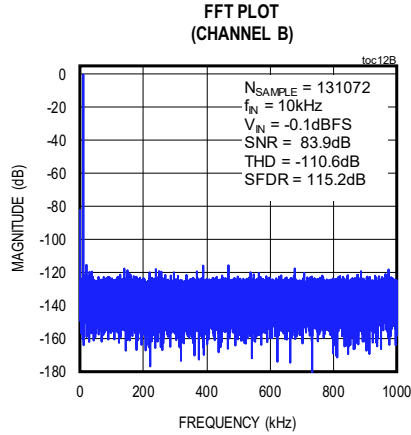
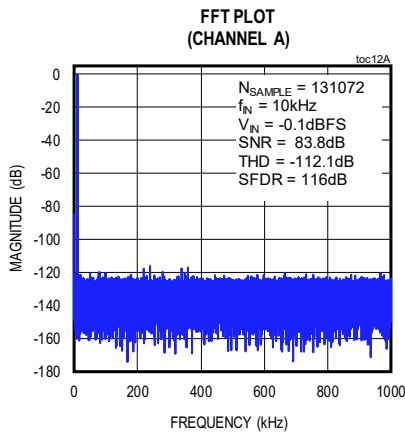
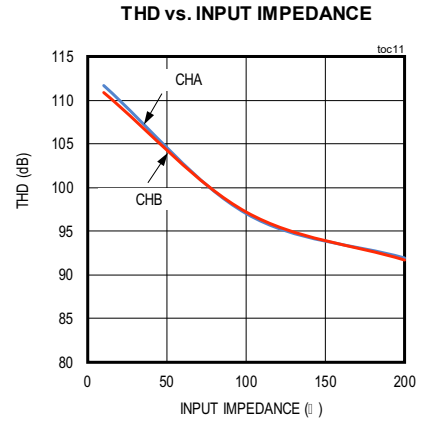
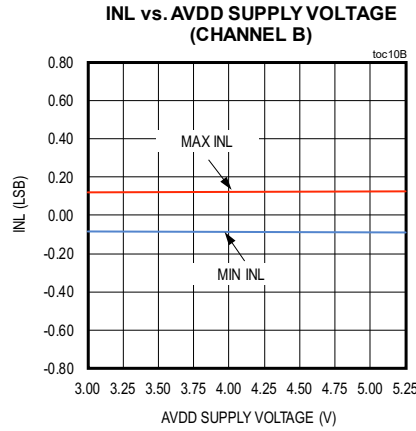
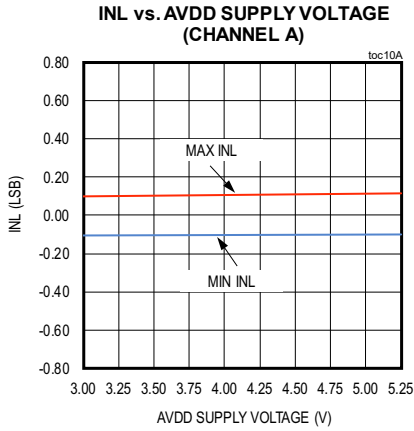
Typical Operating Characteristics—MAX11195 (continued)

($f_{SAMPLE} = 2\text{MSPS}$; $V_{AVDD} = 5.0\text{V}$, $V_{OVDD} = 1.8\text{V}$; $V_{REFIN/OUT} = 2.5\text{V}$ (Internal Reference); $T_A = T_{MIN}$ to T_{MAX} . Typical values are at $T_A = +25^\circ\text{C}$, unless otherwise noted.)



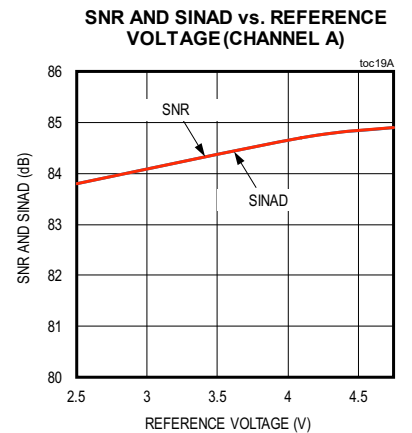
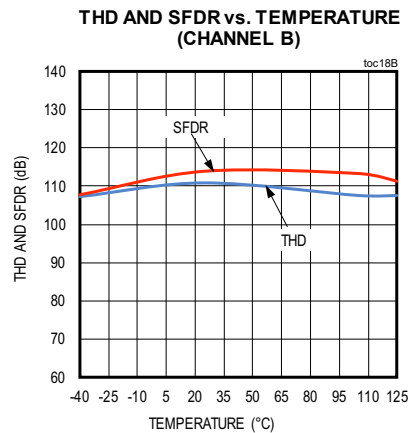
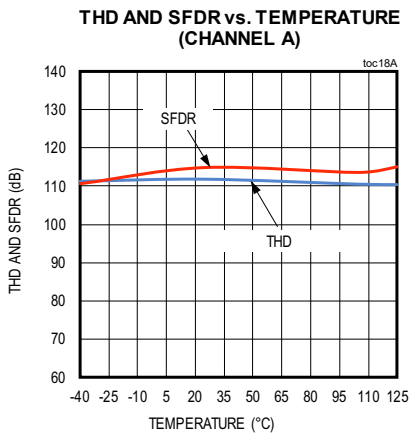
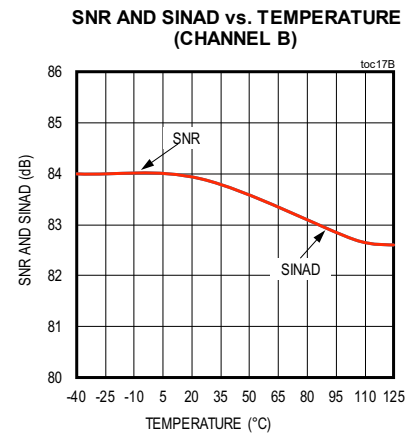
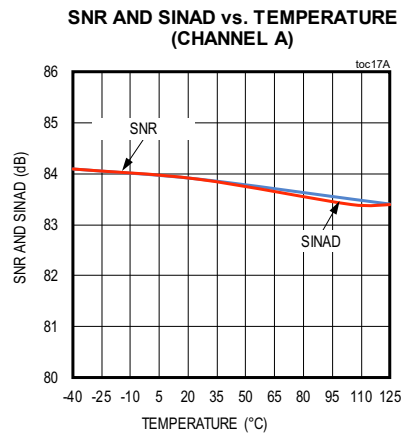
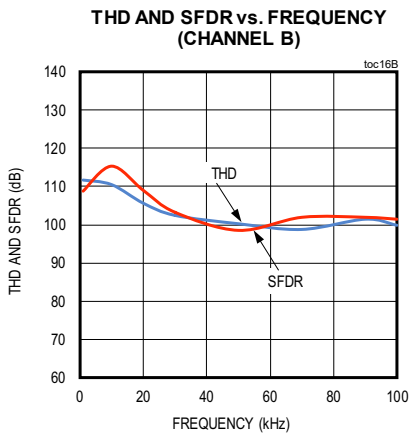
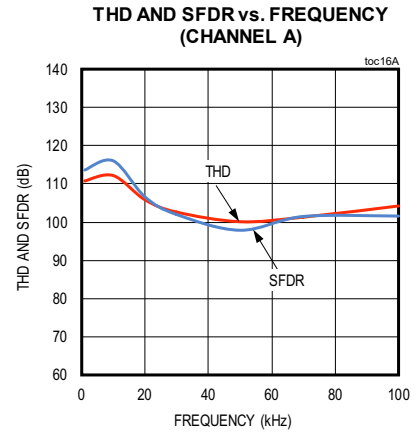
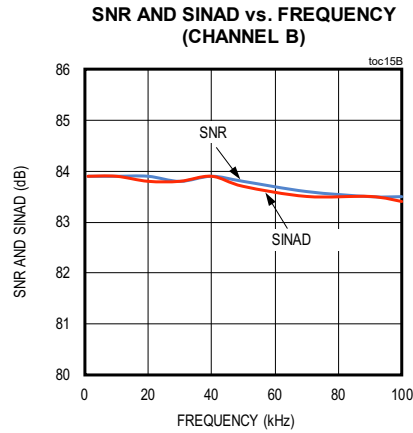
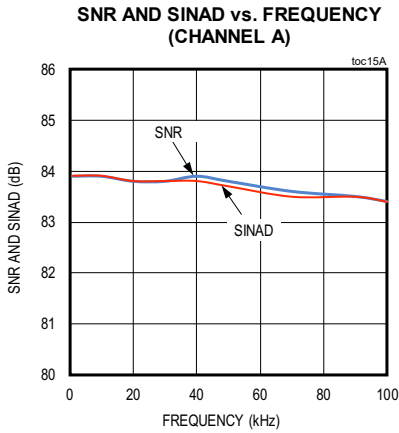
Typical Operating Characteristics—MAX11195 (continued)

($f_{SAMPLE} = 2\text{MSPS}$; $V_{AVDD} = 5.0\text{V}$, $V_{OVDD} = 1.8\text{V}$; $V_{REFIN/OUT} = 2.5\text{V}$ (Internal Reference); $T_A = T_{MIN}$ to T_{MAX} . Typical values are at $T_A = +25^\circ\text{C}$, unless otherwise noted.)



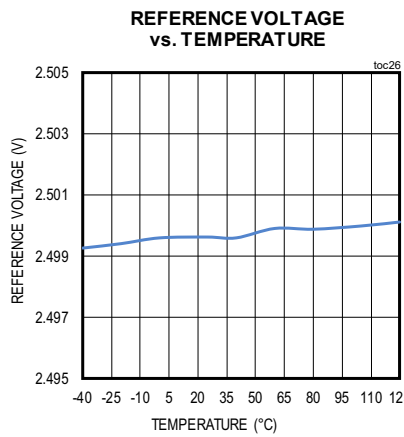
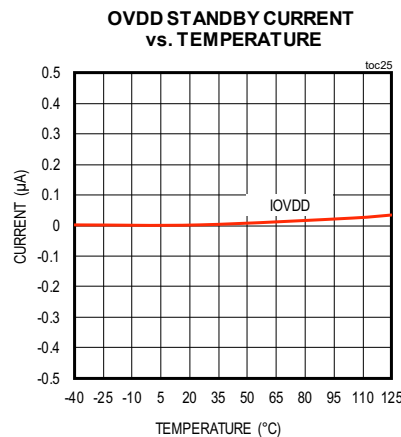
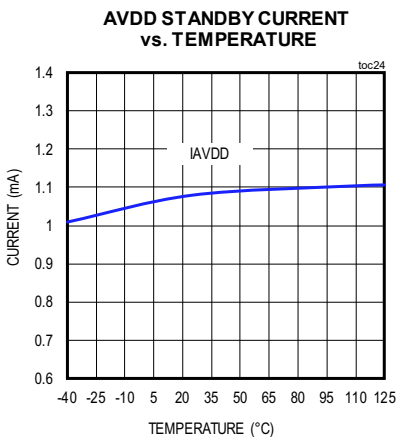
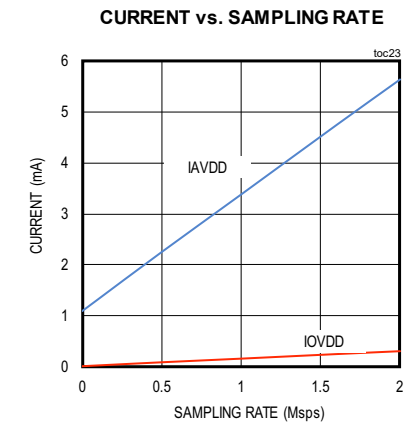
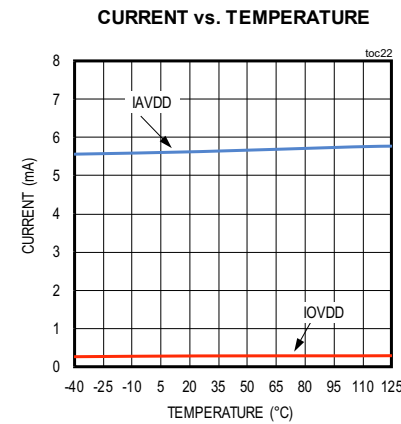
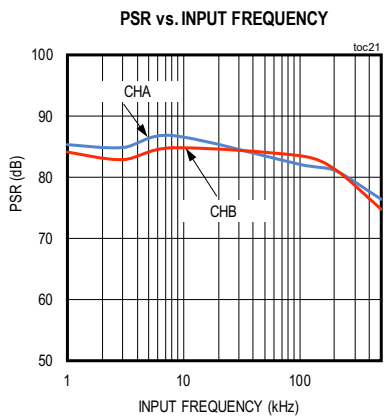
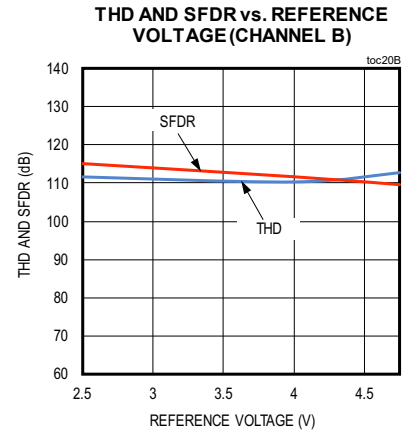
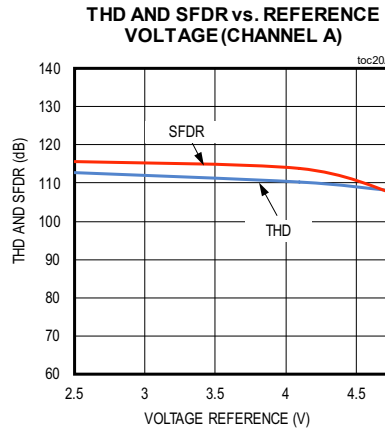
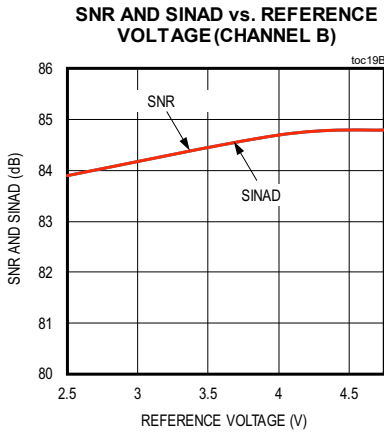
Typical Operating Characteristics—MAX11195 (continued)

($f_{SAMPLE} = 2\text{MSPS}$; $V_{AVDD} = 5.0\text{V}$, $V_{OVDD} = 1.8\text{V}$; $V_{REFIN/OUT} = 2.5\text{V}$ (Internal Reference); $T_A = T_{MIN}$ to T_{MAX} . Typical values are at $T_A = +25^\circ\text{C}$, unless otherwise noted.)



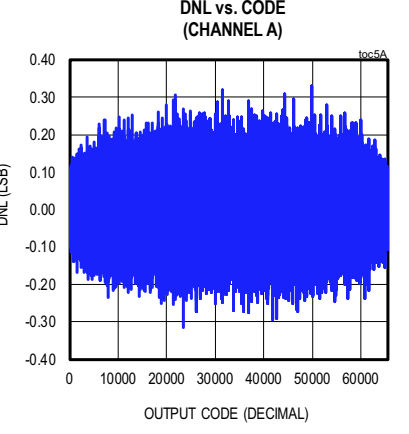
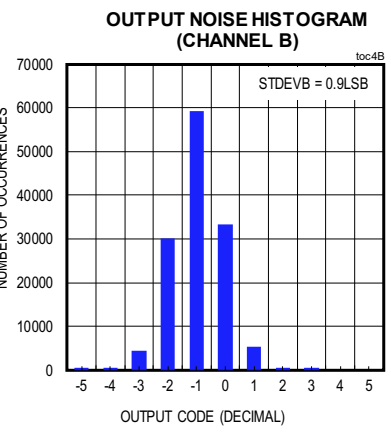
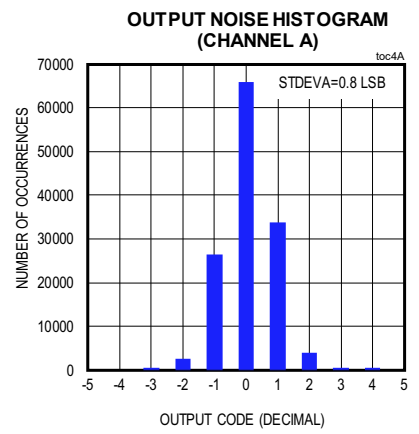
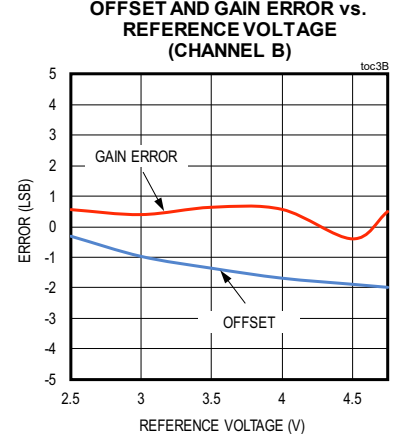
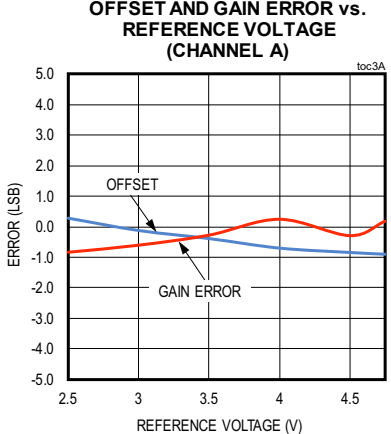
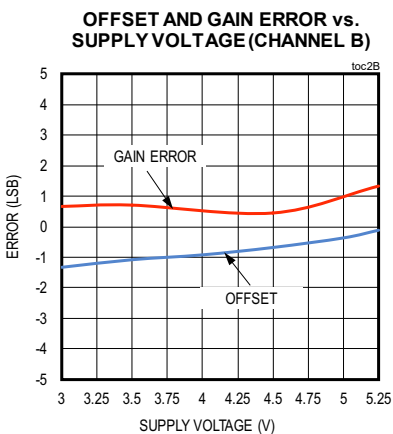
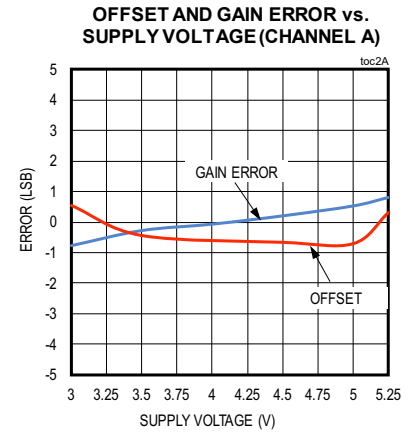
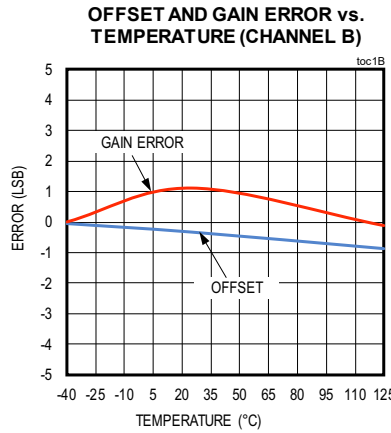
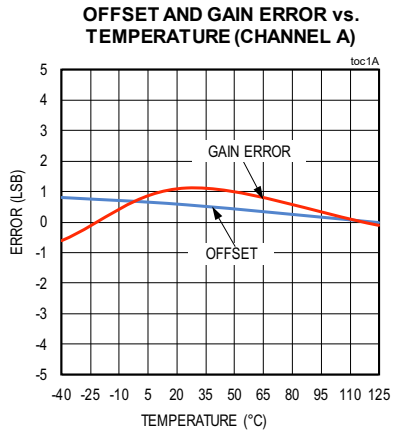
Typical Operating Characteristics—MAX11195 (continued)

($f_{SAMPLE} = 2\text{Mps}$; $V_{AVDD} = 5.0\text{V}$, $V_{OVDD} = 1.8\text{V}$; $V_{REFIN/OUT} = 2.5\text{V}$ (Internal Reference); $T_A = T_{MIN}$ to T_{MAX} . Typical values are at $T_A = +25^\circ\text{C}$, unless otherwise noted.)



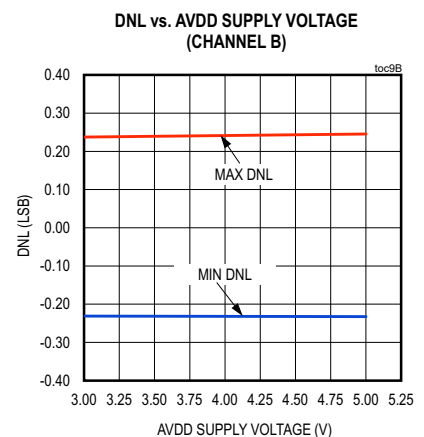
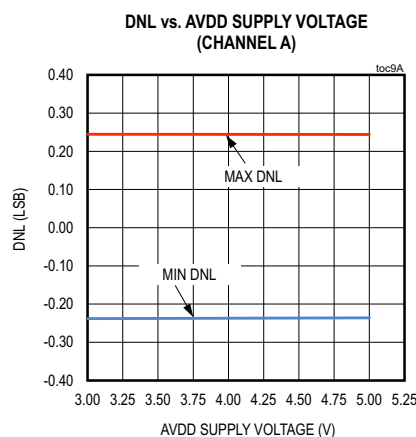
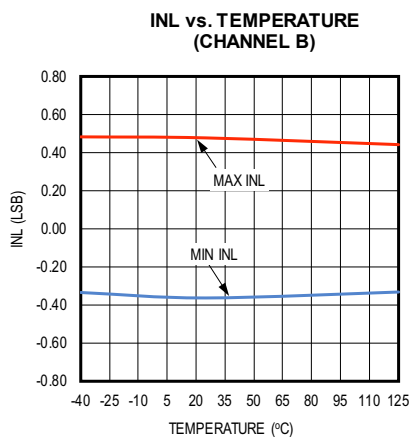
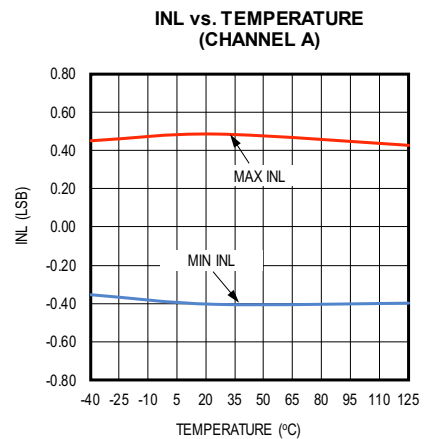
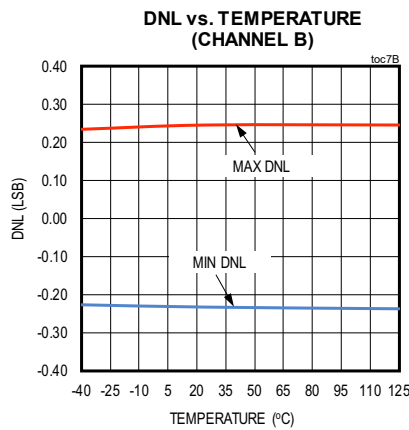
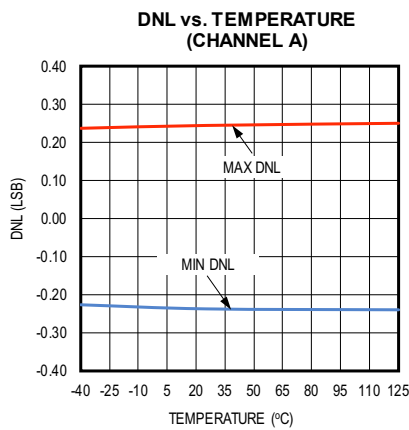
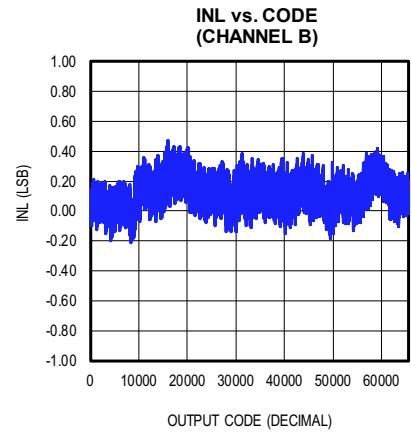
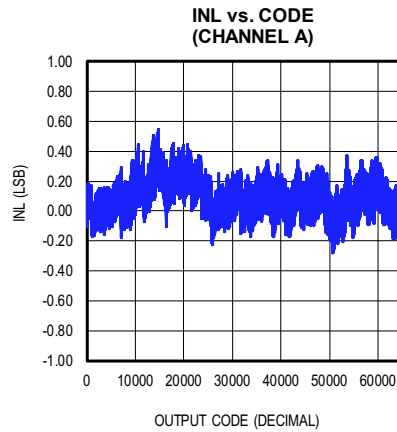
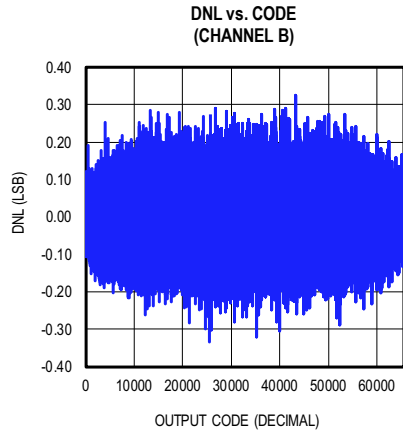
Typical Operating Characteristics—MAX11198

($f_{SAMPLE} = 2\text{MSPS}$; $V_{AVDD} = 5.0\text{V}$, $V_{OVDD} = 1.8\text{V}$; $V_{REFIN/OUT} = 2.5\text{V}$ (Internal Reference); $T_A = T_{MIN}$ to T_{MAX} . Typical values are at $T_A = +25^\circ\text{C}$, unless otherwise noted.)



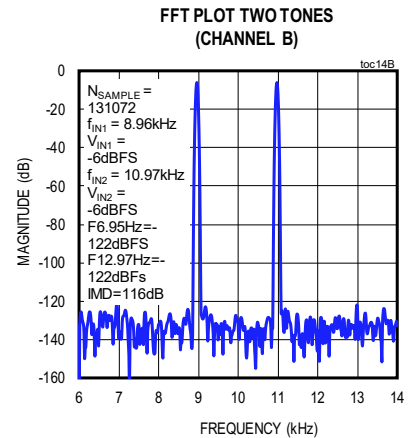
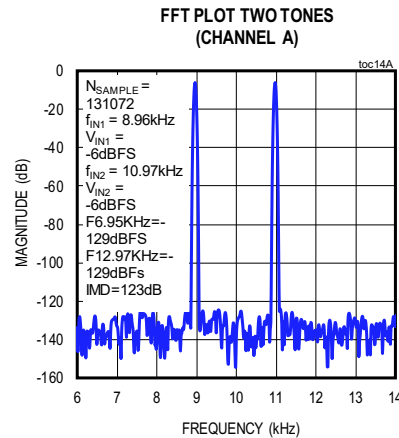
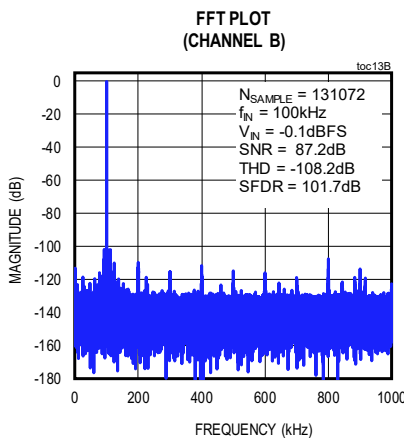
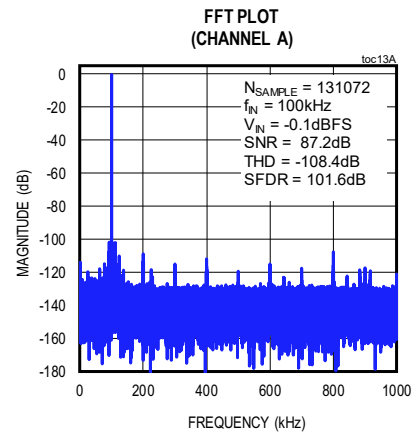
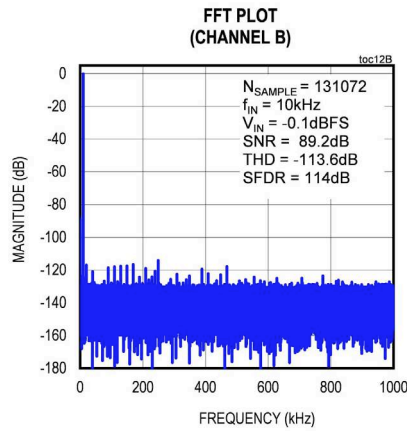
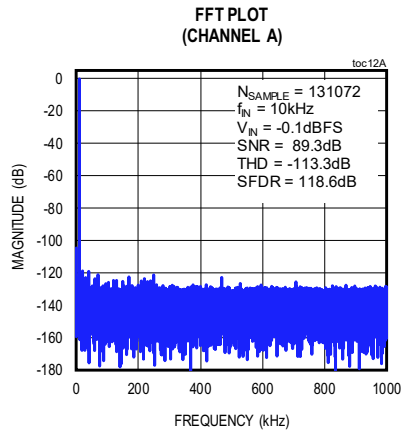
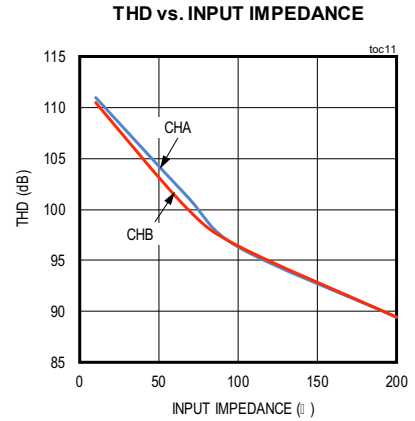
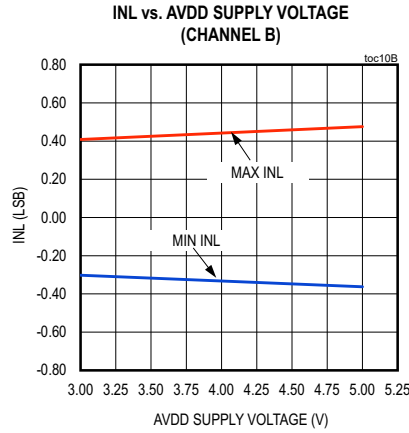
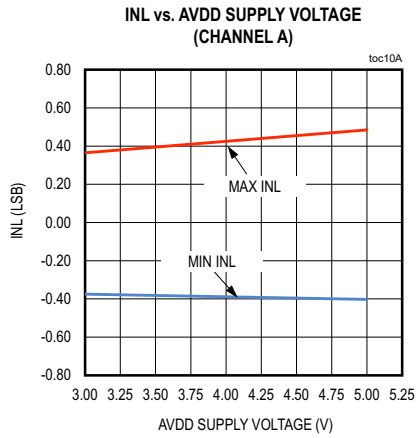
Typical Operating Characteristics—MAX11198 (continued)

($f_{SAMPLE} = 2\text{MSPS}$; $V_{AVDD} = 5.0\text{V}$, $V_{OVDD} = 1.8\text{V}$; $V_{REFIN/OUT} = 2.5\text{V}$ (Internal Reference); $T_A = T_{MIN}$ to T_{MAX} . Typical values are at $T_A = +25^\circ\text{C}$, unless otherwise noted.)



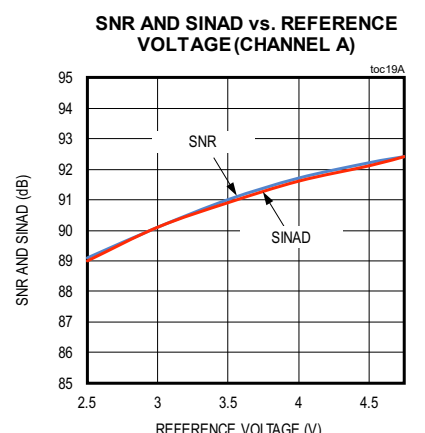
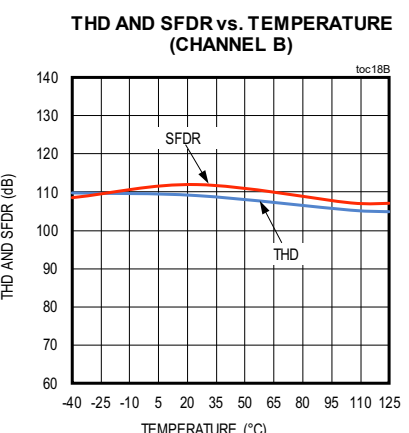
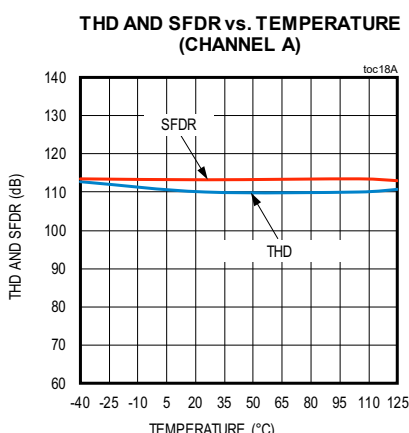
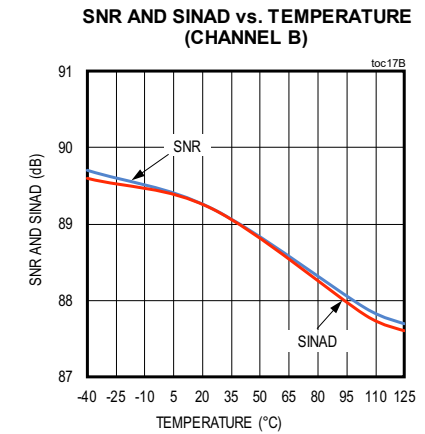
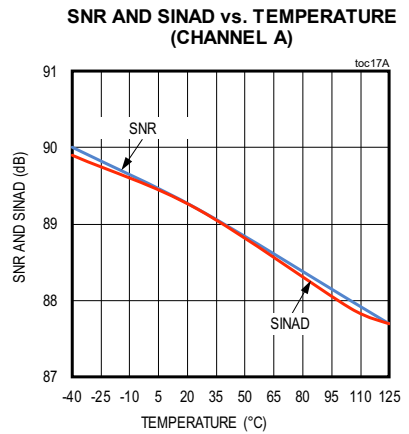
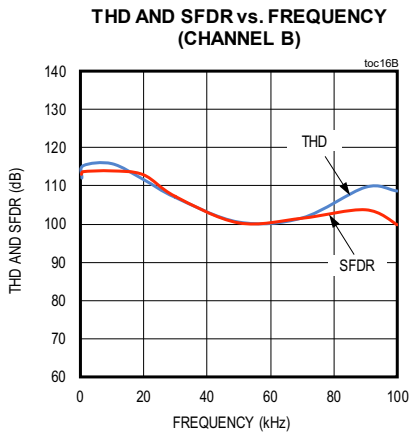
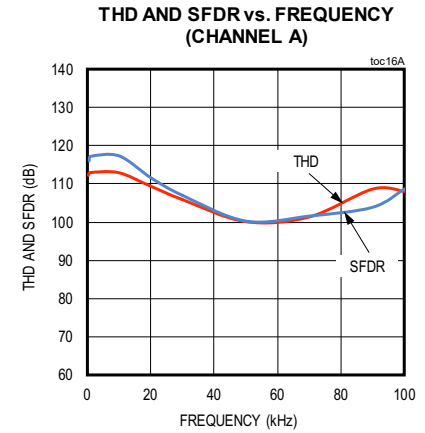
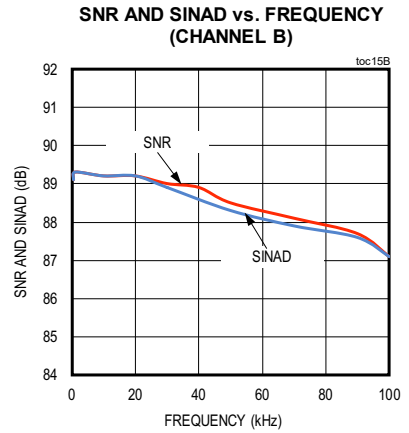
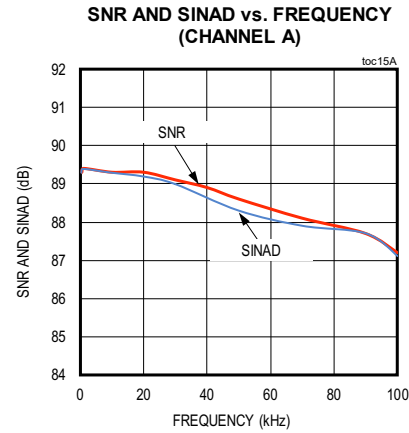
Typical Operating Characteristics—MAX11198 (continued)

($f_{SAMPLE} = 2\text{MSPS}$; $V_{AVDD} = 5.0\text{V}$, $V_{OVDD} = 1.8\text{V}$; $V_{REFIN/OUT} = 2.5\text{V}$ (Internal Reference); $T_A = T_{MIN}$ to T_{MAX} . Typical values are at $T_A = +25^\circ\text{C}$, unless otherwise noted.)



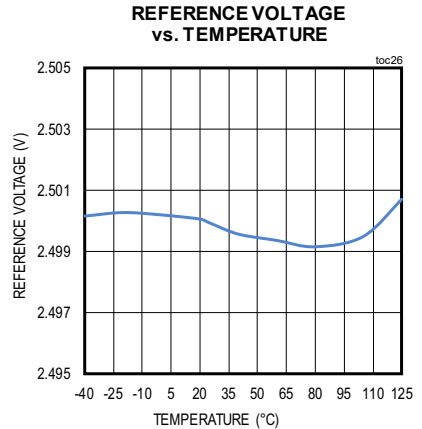
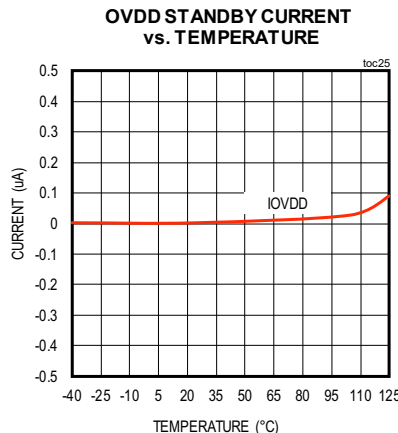
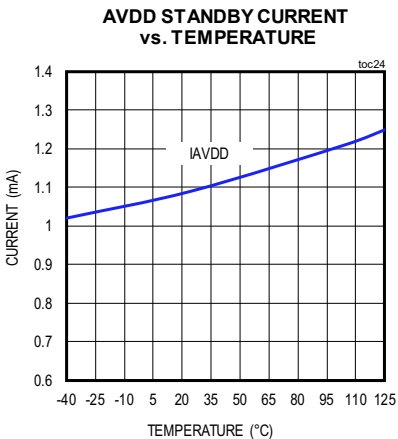
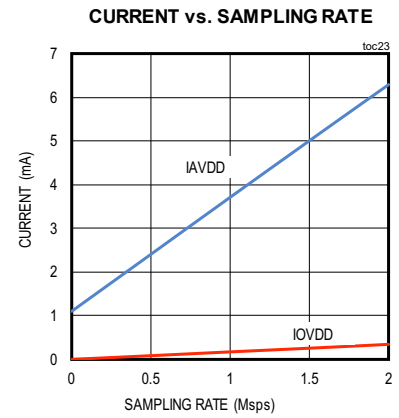
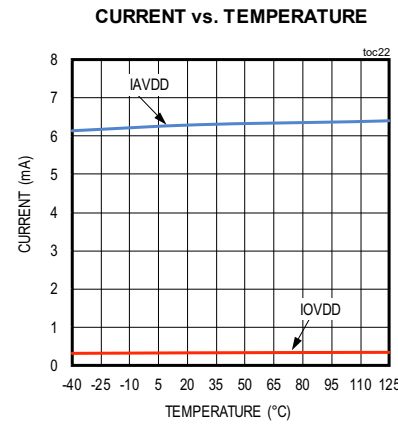
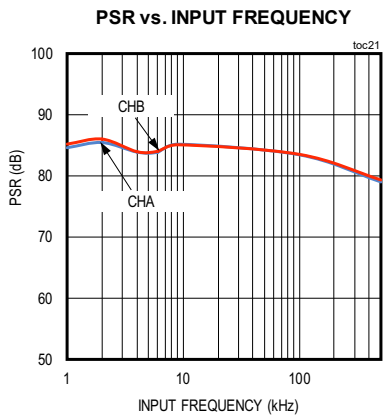
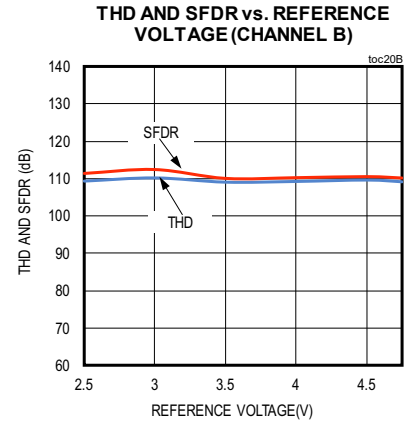
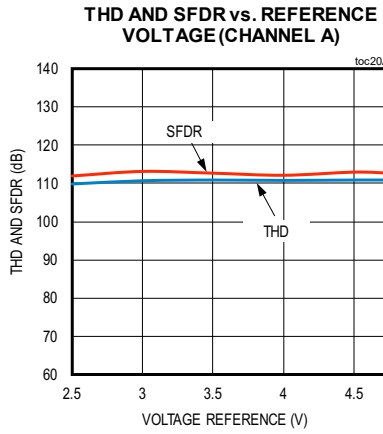
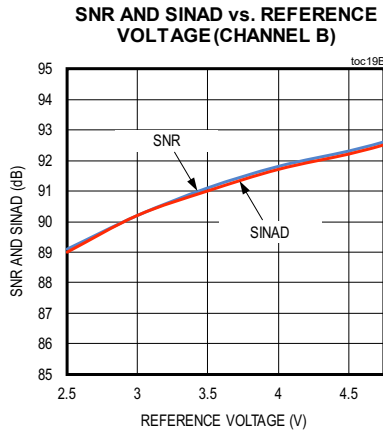
Typical Operating Characteristics—MAX11198 (continued)

($f_{SAMPLE} = 2\text{MSPS}$; $V_{AVDD} = 5.0\text{V}$, $V_{OVDD} = 1.8\text{V}$; $V_{REFIN/OUT} = 2.5\text{V}$ (Internal Reference); $T_A = T_{MIN}$ to T_{MAX} . Typical values are at $T_A = +25^\circ\text{C}$, unless otherwise noted.)



Typical Operating Characteristics—MAX11198 (continued)

($f_{SAMPLE} = 2\text{MSPS}$; $V_{AVDD} = 5.0\text{V}$, $V_{OVDD} = 1.8\text{V}$; $V_{REFIN/OUT} = 2.5\text{V}$ (Internal Reference); $T_A = T_{MIN}$ to T_{MAX} . Typical values are at $T_A = +25^\circ\text{C}$, unless otherwise noted.)



Pin Configuration

