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MAX11259

24-Bit, 6-Channel, 16ksps, 6.2nV/√Hz PGA, Delta-Sigma ADC with I²C Interface

General Description

The MAX11259 is a 6-channel, 24-bit delta-sigma ADC that achieves exceptional performance while consuming very low power. Sample rates up to 16ksps allow precision DC measurements. The MAX11259 communicates via an I²C-compatible serial interface and is available in a small (3mm x 3mm) WLP package.

The MAX11259 offers a 6.2nV/√Hz noise programmable gain amplifier (PGA) with gain settings from 1x to 128x. The integrated PGA provides isolation of the signal inputs from the switched capacitor sampling network. The PGA also enables the MAX11259 to interface directly with high-impedance sources without compromising available dynamic range.

The MAX11259 operates from a single 2.7V to 3.6V analog supply, or split ±1.8V analog supplies, allowing the analog input to be sampled below ground. The digital supply range is 1.7V to 2.0V or 2.0V to 3.6V, allowing communication with 1.8V, 2.5V, 3V, or 3.3V logic.

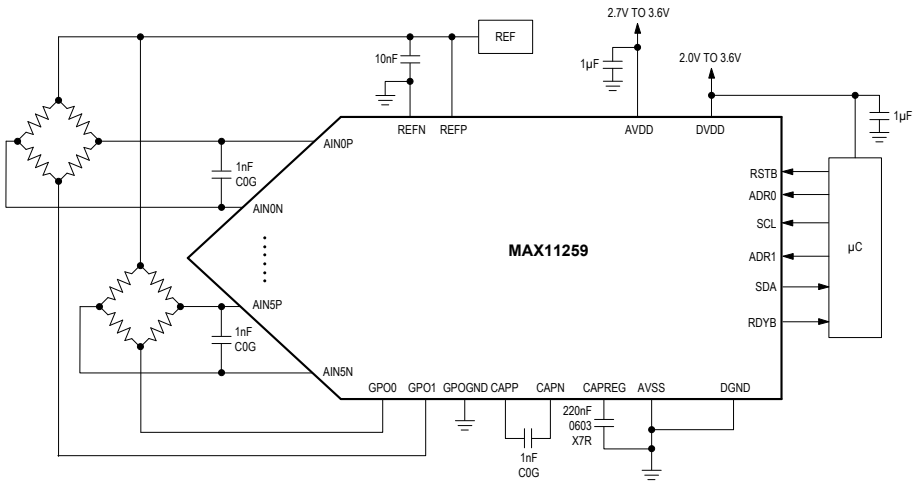
Applications

- Wearable Electronics
- Weigh Scales
- Pressure Sensors
- Battery-Powered Instrumentation

Benefits and Features

- High Resolution for Industrial Applications that Require a Wide Dynamic Range
  - 133dB SNR at 50sps
  - 124dB SNR at 1000sps
- Longer Battery Life for Portable Applications
  - 2.2mA Operating Mode Current
  - 1µA Sleep Current
- Single or Split Analog Supplies Provide Input Voltage Range Flexibility
  - 2.7V to 3.6V (Single Supply) or ±1.8V (Split Supply)
- Enables System Integration
  - Low Noise, 6.2nV/√Hz PGA with Gains of 1, 2, 4, 8, 16, 32, 64, 128
  - 6-Channel, Fully Differential Input
- Enables On-Demand Device and System Gain and Offset Calibration
  - User-Programmable Offset and Gain Registers
- Robust Performance in a Small Package
  - -40°C to +125°C Operating Temperature Range
  - WLP Package, 3mm x 3mm (6 x 6 Ball Array)

Typical Application Circuit



RESISTIVE BRIDGE MEASUREMENT CIRCUIT, I2C CONFIGURATION

maxim integrated™

Absolute Maximum Ratings

AVDD to AVSS .....-0.3V to +3.9V
AVDD to DGND .....-0.3V to +3.9V
DVDD to DGND.....-0.3V to +3.9V
AVSS to DGND .....-1.95V to +0.3V
DVDD to AVSS .....-0.3V to +3.9V
AVSS to GPOGND .....-1.95V to +0.3V
GPOGND to DGND.....-1.95V to +0.3V
AIN_P, AIN_N,REFP, REFN,
CAPP, CAPN to AVSS ..... -0.3V to the lower of +3.9V or (V_{AVDD} + 0.3V)
GPO_ to GPOGND ..... -0.3V to the lower of +3.9V or (V_{AVDD} + 0.3V)
CAPREG to AVSS .....-0.3V to +3.9V
CAPREG to DGND.....-0.3V to +2.1V
All Other Bumps to DGND ..... -0.3V to the lower of +3.9V or (V_{DVDD} + 0.3V)
Maximum Continuous Current into Any Bumps
Except GPOGND Bump.....±50mA
Maximum Continuous Current into
GPOGND Bump .....±100mA
Continuous Power Dissipation (T_A = +70°C)
WLP (derate 26.3mW/°C above +70°C) 2105mW
Operating Temperature Range..... -40°C to +125°C
Junction Temperature.....+150°C
Storage Temperature Range..... -55°C to +150°C
Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

WLP
Junction-to-Ambient Thermal Resistance (θ_{JA})(Note 2)...38°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Note 2: Refer to **Application Note 1891: *Wafer-Level Packaging (WLP) and its Applications*** for information about the thermal performance of WLP packaging.

Electrical Characteristics

(V_{AVDD} = 3.6V, V_{AVSS} = 0V, V_{DVDD} = 2.0V to 3.6V, V_{REFP} - V_{REFN} = V_{AVDD}, DATA RATE = 1ksps, PGA low-noise mode, single-cycle conversion mode (SCYCLE = 1). T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)(Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STATIC PERFORMANCE (Single-Cycle Conversion Mode)							
Noise Voltage (Referred to Input)	V_n	PGA gain of 128, single-cycle mode at 1ksps data rate	PGA low-noise mode		0.19		μV_{RMS}
			PGA low-power mode		0.26		
		PGA gain of 128, single-cycle mode at 12.8ksps data rate	PGA low-noise mode		0.83		
			PGA low-power mode		1.16		
Integral Nonlinearity	INL				3	15	ppm
Zero Error	Z_{ERR}	After system zero-scale calibration			1		µV
Zero Drift	Z_{Drift}				50		nV/°C
Full-Scale Error	FSE	After system full-scale calibration (Notes 4 and 5)			2		ppmFSR

Electrical Characteristics (continued)

(V_{AVDD} = 3.6V, V_{AVSS} = 0V, V_{DVDD} = 2.0V to 3.6V, V_{REFP} - V_{REFN} = V_{AVDD}, DATA RATE = 1ksps, PGA low-noise mode, single-cycle conversion mode (SCYCLE = 1). T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)(Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Full-Scale Error Drift	FSE_{Drift}			0.05		ppmFSR/°C
Common-Mode Rejection	CMR	DC rejection	110	130		dB
		50Hz/60Hz rejection (Note 6)	110	130		
		DC rejection with PGA gain 64	80	105		
		DC rejection with PGA gain 128		95		
AVDD, AVSS Supply Rejection Ratio	PSRRA	DC rejection	73	95		dB
		50Hz/60Hz rejection (Note 6)	75	95		
		DC rejection with PGA gain 128	65	75		
DVDD Supply Rejection Ratio	PSRRD	DC rejection	105	115		dB
		50Hz/60Hz rejection (Note 6)	105	115		
		DC rejection with PGA gain 128	90	110		
PGA						
Gain Setting			1		128	V/V
Noise-Spectral Density	NSD	Low-noise mode		6.2		nV/√Hz
		Low-power mode		10		
Gain Error, Not Calibrated	G_{ERR}	Gain = 1		0.75		%
		Gain = 2		1.2		
		Gain = 4		2		
		Gain = 8		3		
		Gain = 16		4.5		
		Gain = 32		6		
		Gain = 64		5.5		
		Gain = 128		2		
Output Voltage Range	$VOUT_{RNG}$		V_{AVSS} + 0.3		V_{AVDD} - 0.3	V
MUX						
Channel-to-Channel Isolation	ISO_{CH-CH}	DC		140		dB
GENERAL-PURPOSE OUTPUTS						
Resistance (On)	R_{ON}	GPO_ output current = 30mA, GPOGND connected to AVSS		3.5	10	Ω
Maximum Current (On)	I_{MAX}	Per output		30		mA
		Total from all outputs into GPOGND bump (Note 6)			90	mA

Electrical Characteristics (continued)

(V_{AVDD} = 3.6V, V_{AVSS} = 0V, V_{DVDD} = 2.0V to 3.6V, V_{REFP} - V_{REFN} = V_{AVDD}, DATA RATE = 1ksps, PGA low-noise mode, single-cycle conversion mode (SCYCLE = 1). T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)(Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Leakage Current (Off)	I_{leak1}	Current into the GPOGND bump with one individual GPO_ bump connected to 3V		0.4		nA
	I_{leak3}	Current into the GPOGND bump with all GPO_ bumps connected to 3V		13	160	
POWER-UP DELAYS (Note 6)						
Power-Up Time	T_{PUPSLP}	SLEEP state (full power-down) to LDO wake-up V_{AVDD} = 2.7V, V_{DVDD} = 2.0V, CAPREG = 220nF		23	50	µs
	T_{PUPSBY}	STANDBY state (analog blocks powered down, LDO on) to Active		4	8	
RSTB Fall to RDYB '1'	t_{R2}	RDYB transition from '0' to '1' on falling edge of RSTB, internal clock mode (Note 6)			300	ns
		RDYB transition from '0' to '1' on falling edge of RSTB, external clock mode, clock frequency = f_{CLK} (Note 6)			$2/f_{CLK}$	s
ANALOG INPUTS/REFERENCE INPUTS						
Common-Mode Input Voltage Range, V_{CM} = (V_{AIN_P} + V_{AIN_N})/2	CMI_{RNG}	Direct (PGA bypassed)	V_{AVSS}		V_{AVDD}	V
		PGA	V_{AVSS} + 0.4		V_{AVDD} - 1.3	
Input Voltage Range (AIN_P, AIN_N)	$V_{IN(RNG)}$	Direct (PGA bypassed)	V_{AVSS}		V_{AVDD}	V
		PGA	V_{AVSS} + 0.4		V_{AVDD} - 1.3	
Differential Input Voltage Range (AIN_P – AIN_N)	$V_{IN(DIFF)}$	Unipolar	0		V_{REF}	V
		Bipolar	$-V_{REF}$		$+V_{REF}$	
DC Input Leakage	I_{IN_LEAK}	SLEEP state enabled		±0.1		nA
Differential Input Conductance	G_{DIFF}	Direct (PGA bypassed) (Note 6)		±11.6		µA/V
Differential Input Current	I_{DIFF}	PGA enabled (Note 6)		±1.0		nA
Common-Mode Input Conductance	G_{CM}	Direct (PGA bypassed) (Note 6)		±1.0		µA/V
Common-Mode Input Current	I_{CM}	PGA enabled (Note 6)		±10		nA

Electrical Characteristics (continued)

(V_{AVDD} = 3.6V, V_{AVSS} = 0V, V_{DVDD} = 2.0V to 3.6V, V_{REFP} - V_{REFN} = V_{AVDD}, DATA RATE = 1ksps, PGA low-noise mode, single-cycle conversion mode (SCYCLE = 1). T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)(Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Reference Differential Input Resistance	R_{REF}	Active state		26		kΩ
Reference Differential Input Current	I_{REF_PD}	STANDBY and SLEEP state		±1		nA
Input Capacitance	C_{IN}	Direct (PGA bypassed)		2.5		pF
	CP_{GAIN}	PGA		0.25		
AIN_P, AIN_N Sampling Rate	f_S			4.096		MHz
Reference Voltage Range (REFP, REFN)	$V_{REF(RNG)}$	(Note 7)			V_{AVDD}	V
Differential Reference Voltage Range (REFP - REFN)	V_{REF}		1.5		V_{AVDD}	V
REFP, REFN Sampling Rate				4.096		MHz
SENSOR FAULT DETECT CURRENTS						
Current				1.1		µA
Initial Tolerance				±10		%
Drift				0.3		%/°C
DIGITAL SINC FILTER RESPONSE						
Bandwidth (-3dB)				0.203 x DATA RATE		Hz
Settling Time (Latency)				5/DATA RATE		s
LOGIC INPUTS						
Input Voltage Range	V_{IN}	For SDA and SCL bumps	0		V_{DVDD}	V
Input Current	$IDIGI_{LEAK}$	Leakage current			±1	µA
Input Low Voltage	V_{IL}				0.3 x V_{DVDD}	V
Input High Voltage	V_{IH}		0.7 x V_{DVDD}			V
Input Hysteresis	V_{HYS}			200		mV
GPIO Input Low Voltage	V_{IL_GPIO}				0.3	V
GPIO Input High Voltage	V_{IH_GPIO}		1.2			V
GPIO Input Hysteresis	V_{HYS_GPIO}			20		mV

Electrical Characteristics (continued)

(V_{AVDD} = 3.6V, V_{AVSS} = 0V, V_{DVDD} = 2.0V to 3.6V, V_{REFP} - V_{REFN} = V_{AVDD}, DATA RATE = 1ksps, PGA low-noise mode, single-cycle conversion mode (SCYCLE = 1). T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)(Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC OUTPUTS						
Output Voltage Range	V_{OUT}	For SDA bump	0		V_{DVDD}	V
Output Low Level	V_{OL}	I_{OL} = 1mA			0.4	V
Output High Level (RDYB, GPIO_)	V_{OH}	I_{OH} = 1mA	0.9 x V_{DVDD}			V
Floating State Leakage Current	$IDIGO_{LEAK}$				±10	µA
Floating State Output Capacitance	C_{DIGO}			9		pF
POWER REQUIREMENTS						
Negative Analog Supply Voltage	V_{AVSS}		-1.8		0	V
Positive Analog Supply Voltage	V_{AVDD}		V_{AVSS} + 2.7		V_{AVSS} + 3.6	V
Negative I/O Supply Voltage	V_{DGND}		0			V
Positive I/O Supply Voltage	V_{DVDD}	CAPREG not driven by external supply	2.0		3.6	V
		DVDD and CAPREG bumps connected together on the circuit board	1.7		2.0	
CAPREG Supply Voltage	V_{CAPREG}	Internal LDO enabled	1.8			V
		When CAPREG bump is driven externally, ensure it is connected directly to DVDD bump	1.7		2.0	
Analog Supply Current	$I_{AVDD(CNV)}$	Direct		2.2	3	mA
		PGA low-power mode		3.5	5.0	
		PGA low-noise mode		4.2	6.2	
DVDD Operating Current	$I_{DVDD(CNV)}$	V_{DVDD} = 2.0V, LDO enabled		0.65	1.1	mA
		V_{DVDD} = V_{CAPREG} = 2.0V, LDO disabled		0.58		
AVDD Sleep Current	$I_{AVDD(SLP)}$	V_{AVDD} = 3.6V, V_{AVSS} = 0V, V_{DVDD} = 2.0V		1		µA
DVDD Sleep Current	$I_{DVDD(SLP)}$	V_{DVDD} = 2.0V		0.3	4.5	µA
AVDD Standby Current	$I_{AVDD(SBY)}$	V_{AVDD} = 3.6V, V_{AVSS} = 0V, V_{DVDD} = 2.0V		1.5		µA
DVDD Standby Current	$I_{DVDD(SBY)}$	V_{DVDD} = 2.0V, LDO enabled		50	175	µA
		V_{DVDD} = V_{CAPREG} = 2.0V, LDO disabled		2.5		

Electrical Characteristics (continued)

(V_{AVDD} = 3.6V, V_{AVSS} = 0V, V_{DVDD} = 2.0V to 3.6V, V_{REFP} - V_{REFN} = V_{AVDD}, DATA RATE = 1ksps, PGA low-noise mode, single-cycle conversion mode (SCYCLE = 1). T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)(Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
UVLO Threshold Low to High	V_{LH}	AVDD, DVDD supply undervoltage lockout	0.75	1.2	1.7	V
		CAPREG supply undervoltage lockout	0.6	1.0	1.4	
UVLO Threshold High to Low	V_{HL}	AVDD, DVDD supply undervoltage lockout	0.6	1.1	1.6	V
		CAPREG supply undervoltage lockout	0.4	0.95	1.3	
UVLO Hysteresis	V_{HYS}	AVDD, DVDD supply undervoltage lockout		4		%
		CAPREG supply undervoltage lockout		5		
UVLO Delay Low to High or High to Low	T_{DEL}	AVDD, DVDD supply undervoltage lockout		10		µs
		CAPREG supply undervoltage lockout		3.5		
UVLO Glitch Suppression	T_P	AVDD, DVDD supply undervoltage lockout		10		ns
		CAPREG supply undervoltage lockout		10		

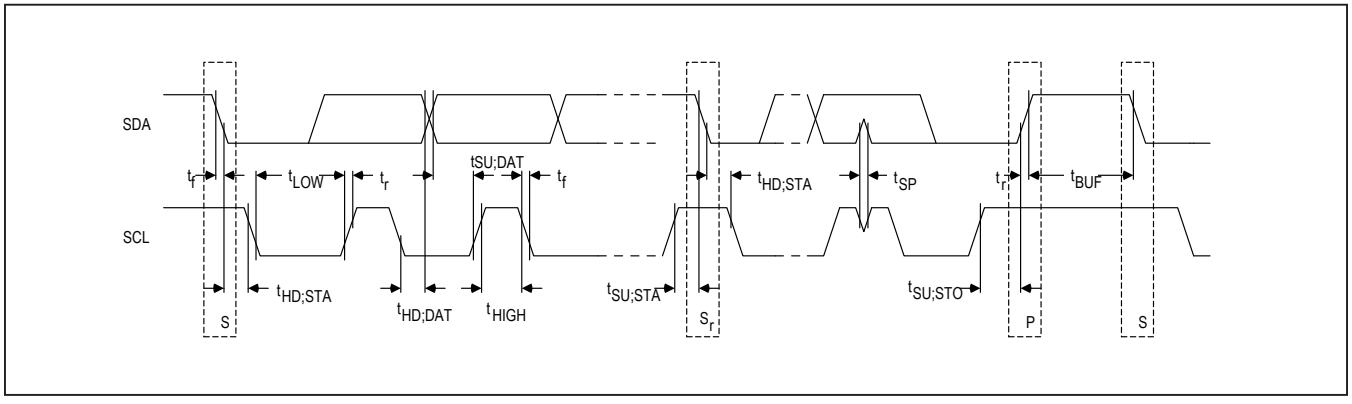


Figure 1. I²C Timing Diagram

I²C Timing Requirements

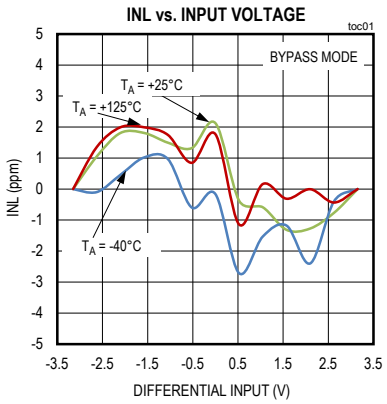
(V_{AVDD} = 3.6V, V_{AVSS} = 0V, V_{DVDD} = 1.7V to 3.6V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. For output bumps, C_{LOAD} = 20pF.)

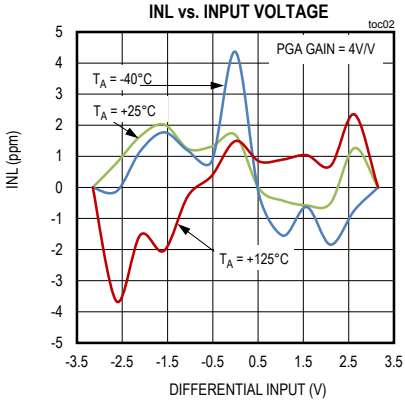
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Serial Clock Frequency	f_{SCL}	Note 6 applies to minimum value	0.1		1	MHz
Bus Free Time Between STOP and START Condition	t_{BUF}		0.5			µs
Hold Time (Repeated) START Condition (After This Period, First Clock Pulse Is Generated)	$t_{HD;STA}$		0.26			µs
SCL Pulse-Width Low	t_{LOW}		0.5			µs
SCL Pulse-Width High	t_{HIGH}		0.26			µs
Setup Time for Repeated START Condition	$t_{SU;STA}$		0.26			µs
Data Hold Time	$t_{HD;DAT}$		0			µs
Data Setup Time	$t_{SU;DAT}$		50			ns
SDA and SCL Receiving Rise Time	t_r	(Note 6)			120	ns
SDA and SCL Receiving Fall Time	t_f	(Note 6)	20 x V_{DVDD}/5.5		120	ns
SDA Transmitting Fall Time	t_f		20 x V_{DVDD}/5.5		120	ns
Setup Time for STOP Condition	$t_{SU;STO}$		0.26			µs
Bus Capacitance Allowed	C_b	(Note 6)			550	pF
Pulse Width of Suppressed Spike	t_{SP}			50		ns

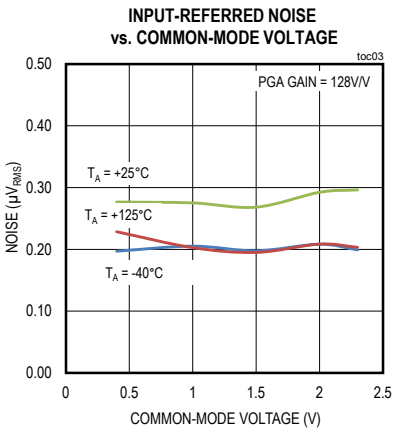
Note 3: Limits are 100% tested at T_A = +25°C, unless otherwise noted. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.
Note 4: Full-scale error includes errors from gain and offset or zero-scale error.
Note 5: ppmFSR is parts per million of full-scale range.
Note 6: These specifications are guaranteed by design, characterization, or I²C protocol.
Note 7: Reference common mode (V_{REFP} + V_{REFN})/2 ≤ (V_{AVDD} + V_{AVSS})/2 + 0.1V.

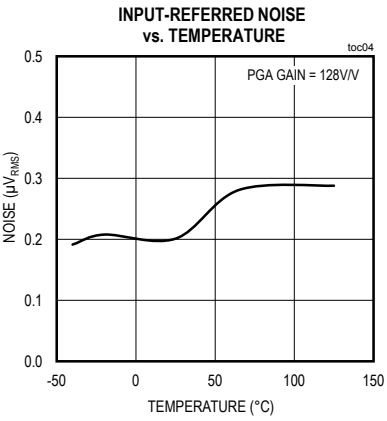
Typical Operating Characteristics

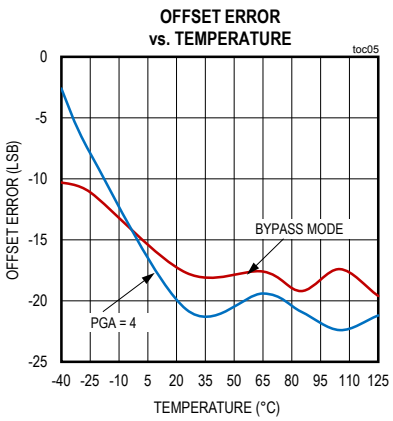
(V_{AVDD} = +3.6V, V_{AVSS} = 0V, V_{DVDD} = +2.0V, V_{REFP} - V_{REFN} = V_{AVDD}; T_A = T_{MIN} to T_{MAX}, LDO enabled, PGA enabled, unless otherwise noted. Data rate = 1ksps, single-cycle conversion mode (SCYCLE = 1) Typical values are at T_A = +25°C.)

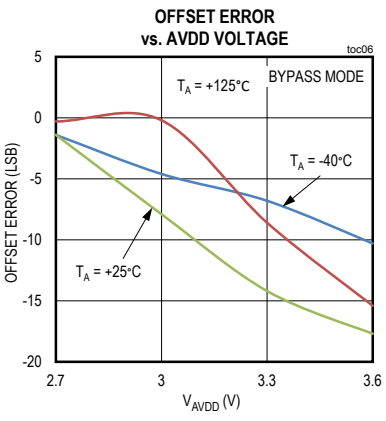


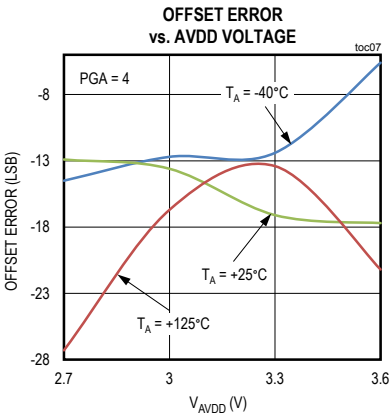


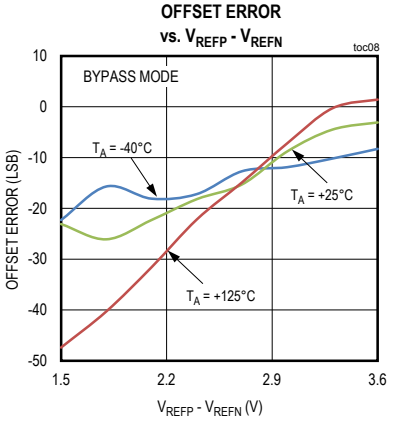


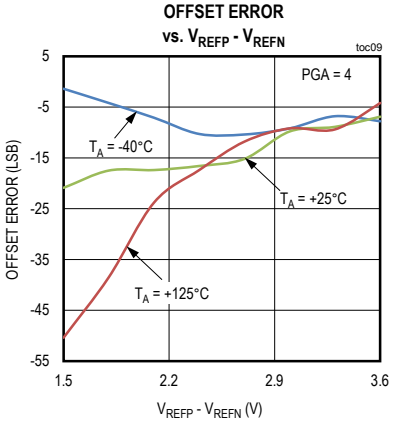








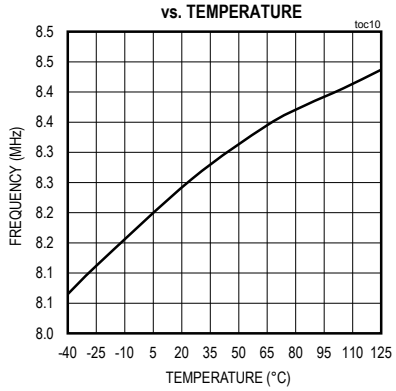




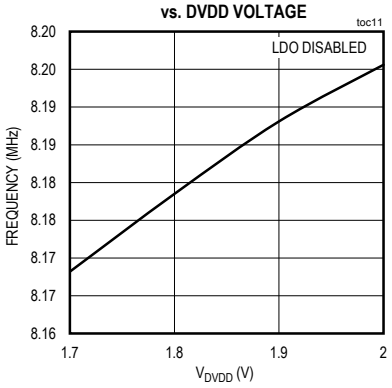
Typical Operating Characteristics (continued)

(V_{AVDD} = +3.6V, V_{AVSS} = 0V, V_{DVDD} = +2.0V, V_{REFP} - V_{REFN} = V_{AVDD}; T_A = T_{MIN} to T_{MAX}, LDO enabled, PGA enabled, unless otherwise noted. Data rate = 1ksps, single-cycle conversion mode (SCYCLE = 1) Typical values are at T_A = +25°C.)

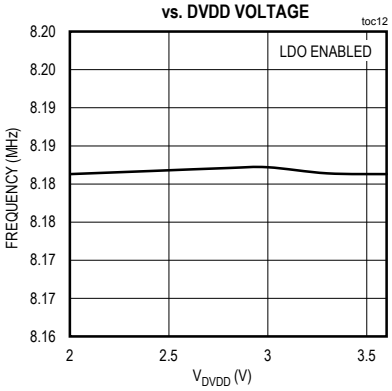
INTERNAL OSCILLATOR FREQUENCY vs. TEMPERATURE



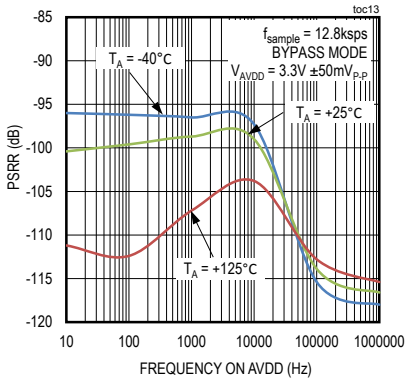
INTERNAL OSCILLATOR FREQUENCY vs. DVDD VOLTAGE



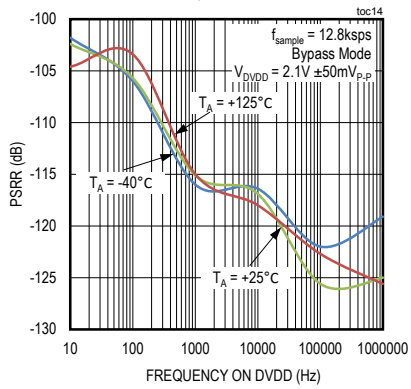
INTERNAL OSCILLATOR FREQUENCY vs. DVDD VOLTAGE



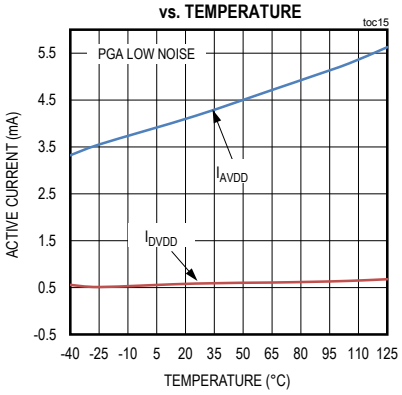
PSRR vs. FREQUENCY ON AVDD



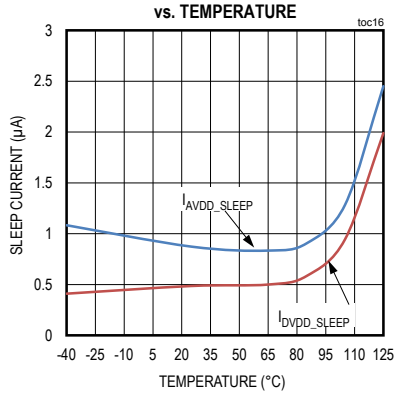
PSRR vs. FREQUENCY ON DVDD



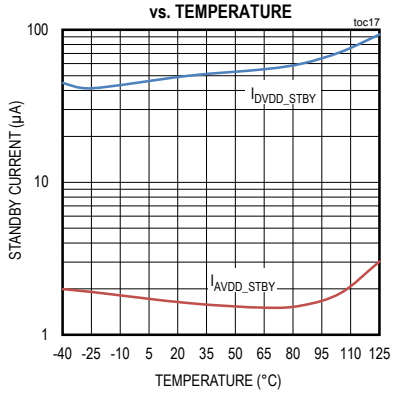
ACTIVE CURRENT vs. TEMPERATURE



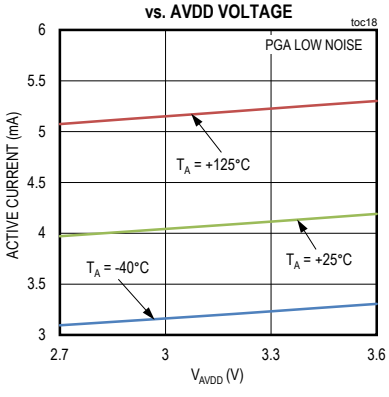
SLEEP CURRENT vs. TEMPERATURE



STANDBY CURRENT vs. TEMPERATURE



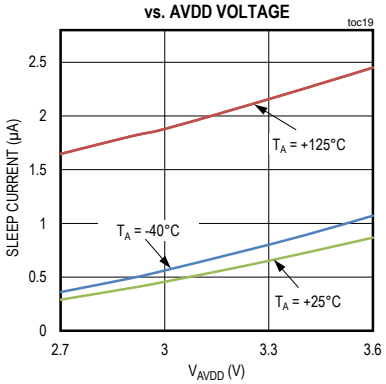
ACTIVE CURRENT vs. AVDD VOLTAGE



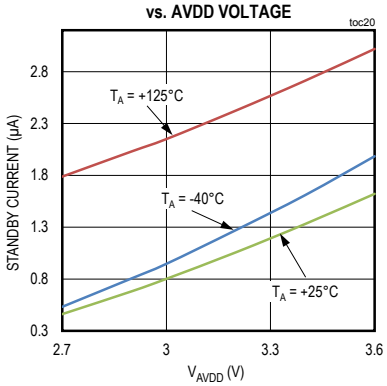
Typical Operating Characteristics (continued)

(V_{AVDD} = +3.6V, V_{AVSS} = 0V, V_{DVDD} = +2.0V, V_{REFP} - V_{REFN} = V_{AVDD}; T_A = T_{MIN} to T_{MAX}, LDO enabled, PGA enabled, unless otherwise noted. Data rate = 1ksps, single-cycle conversion mode (SCYCLE = 1) Typical values are at T_A = +25°C.)

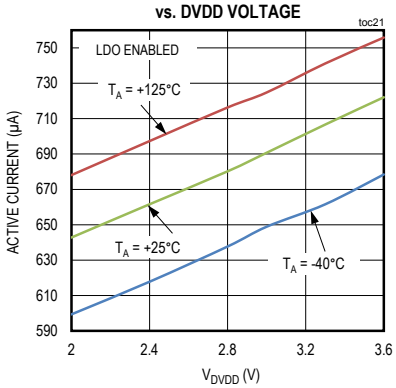
SLEEP CURRENT vs. AVDD VOLTAGE



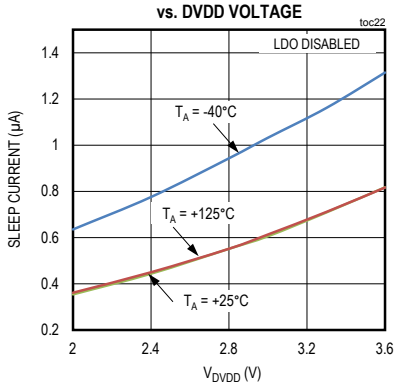
STANDBY CURRENT vs. AVDD VOLTAGE



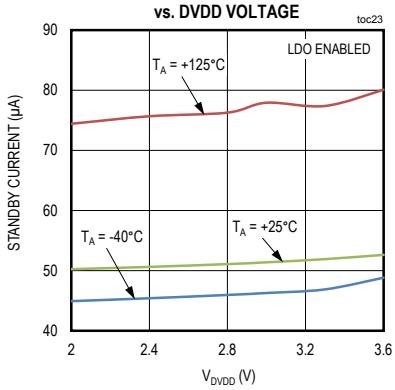
ACTIVE CURRENT vs. DVDD VOLTAGE



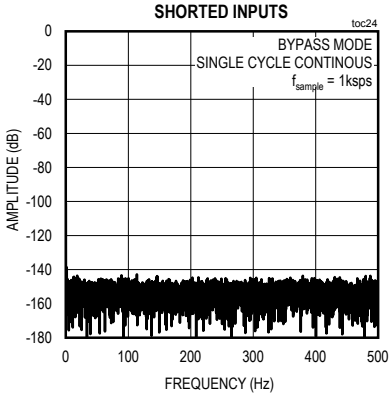
SLEEP CURRENT vs. DVDD VOLTAGE



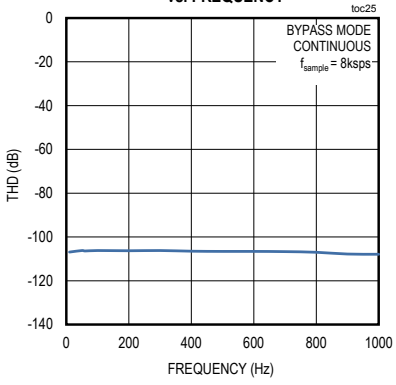
STANDBY CURRENT vs. DVDD VOLTAGE



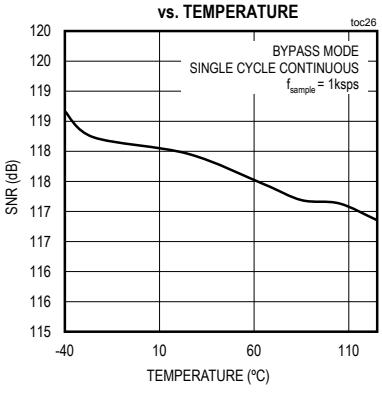
OUTPUT SPECTRUM SHORTED INPUTS



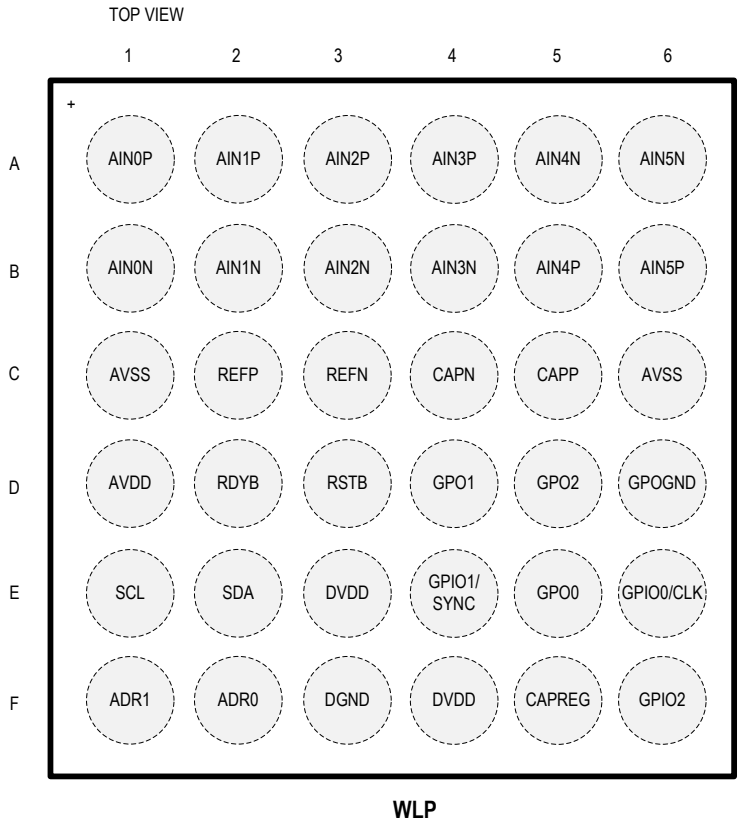
THD vs. FREQUENCY



SNR vs. TEMPERATURE



Bump Configuration



WLP

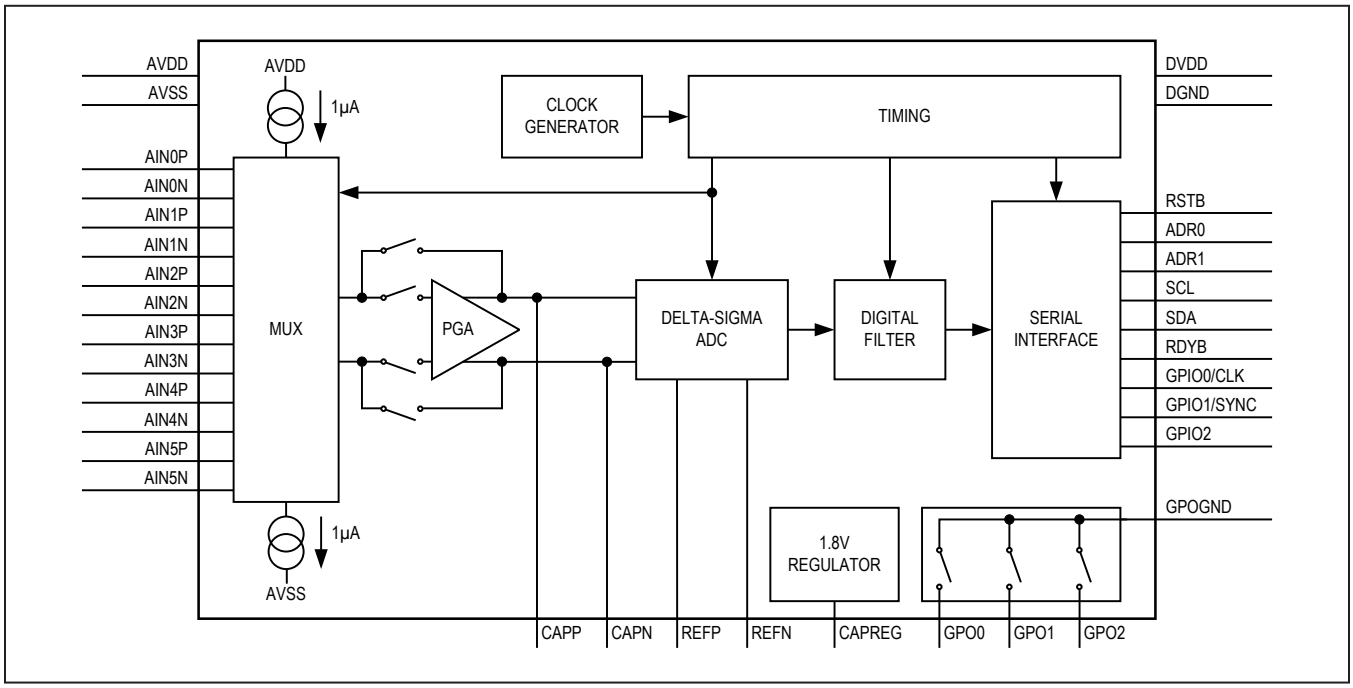
Bump Description

BUMP	NAME	FUNCTION
A1	AIN0P	Positive Analog Input 0
A2	AIN1P	Positive Analog Input 1
A3	AIN2P	Positive Analog Input 2
A4	AIN3P	Positive Analog Input 3
A5	AIN4N	Negative Analog Input 4
A6	AIN5N	Negative Analog Input 5
B1	AIN0N	Negative Analog Input 0
B2	AIN1N	Negative Analog Input 1
B3	AIN2N	Negative Analog Input 2
B4	AIN3N	Negative Analog Input 3
B5	AIN4P	Positive Analog Input 4
B6	AIN5P	Positive Analog Input 5

Bump Description (continued)

BUMP	NAME	FUNCTION
C1	AVSS	Analog Ground
C2	REFP	Positive Reference Input
C3	REFN	Negative Reference Input
C4	CAPN	PGA Filter Input. Connect 1nF C0G capacitor between CAPP and CAPN.
C5	CAPP	PGA Filter Input. Connect 1nF C0G capacitor between CAPP and CAPN.
C6	AVSS	Analog Ground
D1	AVDD	Positive Analog Supply
D2	RDYB	Active-Low Data Ready Output. RDYB goes low when a new conversion result is available in the data register. When a read operation of a full output word completes, RDYB returns high. RDYB is always driven.
D3	RSTB	Active-Low Power-On-Reset Input
D4	GPO1	Analog Switch Normally Open Terminal/General-Purpose Output 1. Register controlled, close position connects GPO1 to GPOGND. Current sink only.
D5	GPO2	Analog Switch Normally Open Terminal/General-Purpose Output 2. Register controlled, close position connects GPO2 to GPOGND. Current sink only.
D6	GPOGND	Analog Switch/General-Purpose Output, GND Terminal
E1	SCL	I²C Serial Clock Input
E2	SDA	I²C Serial Data
E3	DVDD	Digital Power Supply, 1.7V to 3.6V
E4	GPIO1/SYNC	Synchronization Input (default) or General-Purpose I/O. SYNC resets both the digital filter and the modulator. Connect SYNC from multiple MAX11259s in parallel to synchronize more than one ADC to an external trigger.
E5	GPO0	Analog Switch Normally Open Terminal/General-Purpose Output 0. Register controlled, close position connects GPO0 to GPOGND. Current sink only.
E6	GPIO0/ CLK	General-Purpose I/O (Default) or External Clock Signal for the Device. When external clock mode is selected, provide a digital clock signal at this bump. The MAX11259 is specified with a clock frequency of 8.192MHz. Clock frequencies below 8.192MHz are supported. The data rate and digital filter notch frequencies scale with the clock frequency.
F1	ADR1	I²C Address Select Line 1
F2	ADR0	I²C Address Select Line 0
F3	DGND	Digital Ground
F4	DVDD	Digital Power Supply, 1.7V to 3.6V
F5	CAPREG	1.8V Subregulator Output. Connects to DVDD when driven externally by a 1.8V supply. Connect a 220nF or larger capacitor between CAPREG and DGND.
F6	GPIO2	General-Purpose I/O

Functional Diagram



Detailed Description

The MAX11259 is a 24-bit delta-sigma ADC that achieves exceptional performance consuming minimal power. Sample rates up to 16ksps support precision DC measurements. The built-in sequencer supports scanning of selected analog channels, programmable conversion delay, and math operations to automate sensor monitoring.

The fourth order delta-sigma modulator is unconditionally stable and measures six differential input voltages. The modulator is monitored for overrange conditions, which are reported in the status register. The digital filter is a variable decimation-rate SINC filter with overflow monitoring reported in the status register.

The programmable gain differential amplifier (PGA) is low noise and is programmable from 1 to 128. The PGA buffers the modulator and provides a high-impedance input to the analog channels.

System Clock

The MAX11259 incorporates a highly stable internal oscillator that provides the system clock. The system clock is trimmed to 8.192MHz, providing digital and analog timing. The MAX11259 also supports an external clock mode.

Voltage Reference Inputs

The MAX11259 provides differential inputs REFP and REFN for an external reference voltage. Connect the external reference directly across the REFP and REFN bumps to obtain the differential reference voltage. The V_{REFP} voltage should always be greater than the V_{REFN} voltage, and the common-mode voltage range is between 0.75V and V_{AVDD} - 0.75V.

Analog Inputs

The MAX11259 measures six pairs of differential analog inputs (AIN_P, AIN_N) in direct connection or buffered through the PGA.

See the *CTRL2: Control Register 2 (Read/Write)* table for programming and enabling the PGA or direct connect mode. The default configuration is direct connect, with the PGA powered down.

Bypass/Direct Connect

The MAX11259 offers the option to bypass the PGA and route the analog inputs directly to the modulator. This option lowers the power of the device since the PGA is powered down.

Programmable Gain Amplifier (PGA)

The integrated PGA provides gain settings from 1x to 128x. (Figure 2). Direct connection is available to bypass the PGA and directly connect to the modulator. The PGA's absolute input voltage range is CMI_{RNG} and the PGA output voltage range is $VOUT_{RNG}$, as specified in the *Electrical Characteristics*.

Note that linearity and performance degrade when the specified input common-mode voltage of the PGA is exceeded. The input common-mode range and output common-mode range are shown in Figure 3. The following equations describe the relationship between the analog inputs and PGA output.

AINP = Positive input to the PGA

AINN = Negative input to the PGA

CAPP = Positive output of PGA

CAPN = Negative output of PGA

V_{CM} = Input common mode

GAIN = PGA gain

V_{REF} = ADC reference input voltage

$V_{IN} = V_{AINP} - V_{AINN}$

Note: Input voltage range is limited by the reference voltage as described by $V_{IN} \le \pm V_{REF}/GAIN$

$$V_{CM} = \frac{(V_{AINP} + V_{AINN})}{2}$$

$$V_{CAPP} = V_{CM} + GAIN \times (V_{AINP} - V_{CM})$$

$$V_{CAPN} = V_{CM} - GAIN \times (V_{CM} - V_{AINN})$$

Input Voltage Range

The ADC input range is programmable for bipolar ($-V_{REF}$ to $+V_{REF}$) or unipolar (0 to VREF) ranges. The U/$\overline{B}$ bit in the CTRL1 register configures the MAX11259 for unipolar or bipolar transfer functions.

Data Rates

Table 1 lists the available data rates for the MAX11259, RATE[3:0] setting of the conversion command (see the *Modes and Registers* section). The single-cycle mode has an overhead of 48 digital master clocks that is approximately 5.86µs for a typical digital master clock frequency of 8.192MHz. The single-cycle effective column contains the data rate values including the 48 clock startup delays. The 48 clocks are required to stabilize the modulator at startup. In continuous conversion mode, the output data rate is five times the single-cycle rate up to a maximum of 16ksps. During continuous conversions, the output sample data requires five 24-bit cycles to settle to a valid conversion from an input step, PGA gain changes, or a change of input channel through the multiplexer.

If self-calibration is used, 48 additional master clocks are required to process the data per conversion. Likewise, system calibration takes an additional 48 master clocks to complete.

If both self and system calibration are used, it takes an additional 80 master clocks to complete. If self and/or system calibration are used, the effective data rate will be reduced by these additional clock cycles per conversion.

Noise Performance

The MAX11259 provides exceptional noise performance. SNR is dependent on data rate, PGA gain, and power mode. Bandwidth is reduced at low data rates; both noise and SNR are improved proportionally. Tables 2 and 3 summarize the noise performance for both single-cycle and continuous operation versus data rate, PGA gain, and power mode.

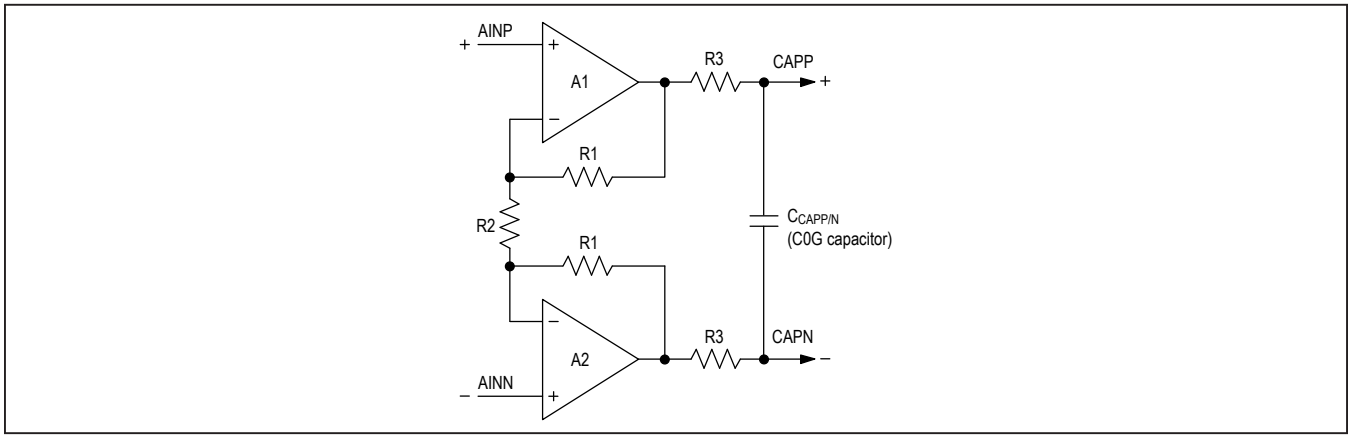


Figure 2. Simplified Equivalent Diagram of the PGA

Table 1. Available Programmable Data Rates

	DATA RATE (sps)				
RATE[3:0]	**CONTINUOUS**	**SINGLE CYCLE**	**CONVERSION ONLY**	**CONVERSION PLUS SELF-CALIBRATION***	**CONVERSION PLUS SELF-CALIBRATION PLUS SYSTEM CALIBRATION***
0000	1.9	50	50.01	49.99	49.98
0001	3.9	62.5	62.51	62.48	62.47
0010	7.8	100	99.98	99.92	99.88
0011	15.6	125	124.95	124.86	124.80
0100	31.2	200	199.80	199.57	199.41
0101	62.5	250	249.66	249.29	249.05
0110	125	400	398.98	398.05	397.44
0111	250	500	498.34	496.89	495.93
1000	500	800	796.11	792.41	789.97
1001	1000	1000	991.86	986.13	982.35
1010	2000	1600	1578.72	1564.26	1554.77
1011	4000	2000	1974.16	1951.60	1936.84
1100	8000	3200	3114.26	3058.48	3022.39
1101	16000**	4000	3895.78	3808.89	3753.08
1110	Not available	6400	6135.27	5922.49	5788.64
1111	Not available	12800	11776.90	11017.10	10562.79

**The effective data rate is lower when the calibration is enabled due to additional MAC (multiply/accumulate) operations required after the conversion is complete to perform the calibration adjustment.*
***Only supported in Fast Mode Plus.*

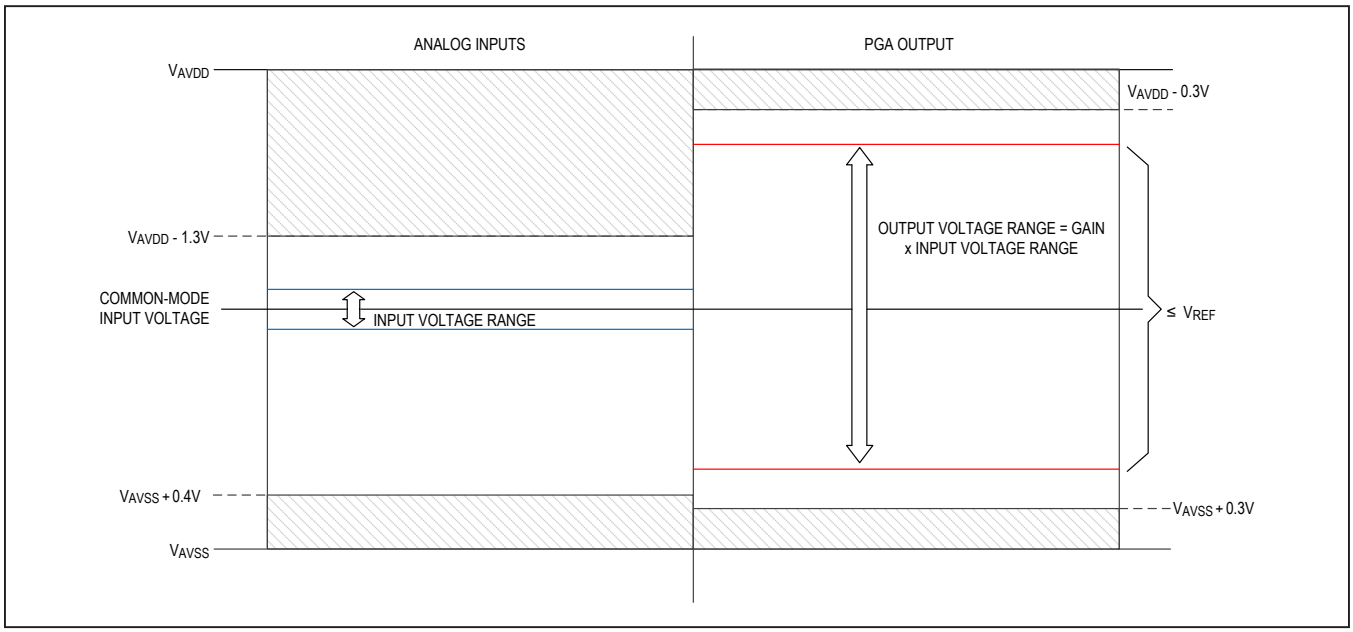


Figure 3. Analog Input Voltage Range Compared to PGA Output Range

Table 2. Noise vs. PGA Mode and Gain (Single-Cycle Conversion)

	SINGLE-CYCLE CONVERSION MODE INPUT-REFERRED NOISE VOLTAGE (μV_{RMS}) VS. PGA GAIN SETTING															
DATA RATE (sps)	**1**		**2**		**4**		**8**		**16**		**32**		**64**		**128**	
	LP	**LN**	**LP**	**LN**	**LP**	**LN**	**LP**	**LN**	**LP**	**LN**	**LP**	**LN**	**LP**	**LN**	**LP**	**LN**
50	0.81	0.58	0.38	0.27	0.18	0.13	0.10	0.07	0.09	0.07	0.08	0.06	0.08	0.06	0.08	0.06
62.5	0.88	0.63	0.48	0.34	0.21	0.15	0.12	0.09	0.09	0.07	0.08	0.06	0.08	0.05	0.08	0.05
100	1.18	0.84	0.61	0.44	0.30	0.21	0.17	0.12	0.12	0.08	0.09	0.07	0.09	0.07	0.10	0.07
125	1.24	0.89	0.59	0.42	0.31	0.22	0.18	0.13	0.12	0.08	0.10	0.07	0.10	0.07	0.10	0.07
200	1.38	0.99	0.68	0.49	0.35	0.25	0.21	0.15	0.15	0.10	0.12	0.08	0.11	0.08	0.11	0.08
250	1.38	0.99	0.72	0.52	0.39	0.28	0.23	0.16	0.16	0.11	0.13	0.09	0.12	0.09	0.12	0.09
400	1.63	1.16	0.85	0.61	0.45	0.32	0.27	0.19	0.19	0.14	0.16	0.12	0.15	0.11	0.16	0.11
500	1.79	1.28	0.93	0.66	0.48	0.34	0.29	0.21	0.21	0.15	0.18	0.13	0.17	0.12	0.18	0.13
800	2.12	1.51	1.10	0.79	0.61	0.43	0.36	0.26	0.27	0.20	0.24	0.17	0.23	0.16	0.23	0.16
1,000	2.38	1.70	1.25	0.89	0.69	0.49	0.41	0.29	0.31	0.22	0.27	0.19	0.26	0.18	0.26	0.19
1,600	3.21	2.29	1.67	1.19	0.89	0.64	0.56	0.40	0.41	0.29	0.36	0.26	0.35	0.25	0.35	0.25
2,000	3.76	2.69	1.95	1.39	1.04	0.74	0.65	0.47	0.48	0.34	0.43	0.30	0.41	0.29	0.42	0.30
3,200	4.41	3.15	2.28	1.63	1.25	0.89	0.78	0.55	0.58	0.41	0.51	0.36	0.49	0.35	0.49	0.35
4,000	5.18	3.70	2.68	1.91	1.48	1.06	0.91	0.65	0.69	0.49	0.60	0.43	0.58	0.41	0.59	0.42
6,400	7.34	5.24	3.83	2.73	2.08	1.48	1.29	0.92	0.98	0.70	0.86	0.61	0.81	0.58	0.83	0.59
12,800	10.84	7.74	5.59	3.99	3.01	2.15	1.85	1.32	1.37	0.98	1.23	0.88	1.17	0.83	1.16	0.83

LP = Low Power, LN = Low Noise

Table 3. Noise vs. PGA Mode and Gain (Continuous Conversion)

DATA RATE (sps)	CONTINUOUS CONVERSION MODE INPUT-REFERRED NOISE VOLTAGE (μV_{RMS}) VS. PGA GAIN SETTING															
	1		2		4		8		16		32		64		128	
	LP	LN	LP	LN	LP	LN	LP	LN	LP	LN	LP	LN	LP	LN	LP	LN
15.6	0.45	0.32	0.20	0.14	0.11	0.08	0.06	0.04	0.04	0.03	0.03	0.02	0.03	0.02	0.03	0.02
31.2	0.58	0.41	0.26	0.18	0.13	0.10	0.08	0.06	0.05	0.04	0.04	0.03	0.04	0.03	0.04	0.03
62.5	0.68	0.48	0.34	0.25	0.18	0.13	0.10	0.07	0.07	0.05	0.06	0.04	0.06	0.04	0.06	0.04
125	0.86	0.61	0.44	0.32	0.23	0.16	0.14	0.10	0.10	0.07	0.08	0.06	0.08	0.06	0.08	0.06
250	1.14	0.82	0.56	0.40	0.30	0.22	0.18	0.13	0.14	0.10	0.11	0.08	0.11	0.08	0.11	0.08
500	1.47	1.05	0.76	0.54	0.41	0.29	0.25	0.18	0.19	0.13	0.16	0.11	0.16	0.11	0.16	0.11
1000	1.99	1.42	1.03	0.73	0.56	0.40	0.35	0.25	0.26	0.19	0.23	0.16	0.21	0.15	0.22	0.16
2000	2.73	1.95	1.40	1.00	0.76	0.54	0.47	0.34	0.36	0.26	0.31	0.22	0.30	0.21	0.30	0.21
4000	3.68	2.63	1.86	1.33	1.03	0.73	0.64	0.45	0.49	0.35	0.42	0.30	0.40	0.28	0.41	0.29
8000	4.57	3.26	2.36	1.69	1.30	0.93	0.81	0.58	0.61	0.43	0.53	0.38	0.52	0.37	0.52	0.37
16000	5.22	3.73	2.66	1.90	1.48	1.06	0.93	0.67	0.68	0.49	0.61	0.44	0.58	0.41	0.60	0.43

LP = Low Power, LN = Low Noise

I²C Protocol

The I²C-compatible serial interface consists of the standard I²C bumps: SCL and SDA. The SCL and the SDA bumps are bidirectional lines, connected to a positive supply voltage via a current source or a pullup resistor. The data is clocked into the MAX11259 from the SDA bump on the rising edge of SCL. Data is clocked out of the MAX11259 on the SDA bump on the falling edge of SCL. The SCL/SDA have an open-drain pad for wired-AND connection on the bus. Data on the bus can be transferred at rates of up to 1Mbit/s since the MAX11259 supports the Fast Mode Plus protocol. Each device on the I²C bus is recognized by a unique device address and can operate as a transmitter and a receiver. The interface is backward-compatible with standard mode and fast mode.

Due to the variety of different devices (bipolar, CMOS, NMOS) that can be connected to the I²C bus, the input reference levels are set as 30% and 70% of V_{DD}. The data on the SDA line must be stable during high period of SCL. The HIGH or LOW state of the data line can only change when the clock line is LOW for a normal byte transfer except for START and STOP conditions.

All transactions begin with a START(S) and are terminated by a STOP(P). A HIGH to LOW transaction on the SDA line while SCL is HIGH defines a START condition. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition. The START and STOP are always generated by the I²C Master. The MAX11259 has a circuit to detect the START and STOP conditions. Every byte on the SDA line must be 8 bits long. The number of bytes that can be transmitted is unrestricted. Each byte must be followed by an acknowledge (ACK). Data is transferred with MSB first. The MAX11259 always sends out an ACK in response to master's request for reading or writing data which means the interface is always ready and it does not hold the master in wait state. If the MAX11259 receives a not acknowledge (NACK) from the master it will reset the I²C interface and wait for another START condition.

SCL (Serial Clock)

The SCL bump synchronizes data communication between the host device and the MAX11259. Data is latched into the MAX11259 on the rising edge of SCL and data is shifted out of the MAX11259 after the falling edge of SCL.

RDYB (Data Ready)

RDYB indicates the ADC conversion status and the availability of the conversion result. When RDYB is low, a conversion result is available. When RDYB is high, a con-

version is in progress and the data for the current conversion is not available. RDYB is driven high after a complete read of the data register. RDYB resets to high four master clock cycles prior to the next DATA register update.

If data was read, then RDYB transitions from high to low at the output data rate. If the previous data was not read, then the RDYB transitions from low to high for four master clock cycles and then transitions from high to low. In continuous mode, RDYB remains high for the first four conversion results and on the 5th result, RDYB goes low.

For sequencer mode 2 and sequencer mode 3, the RDYB behavior for a multichannel conversion can be controlled by the SEQ:RDYBEN bit. The default value of SEQ:RDYBEN is ‘0’. When set to ‘0’, RDYB behaves the same for multichannel conversion and single channel operation. The RDYB toggles high to low after each channel is ready to update its corresponding data register. After the channel data is read, the RDYB will reset back to ‘1’. If the channel data is not read and the next channel is ready to update its data, the RDYB will toggle low to high four cycles before the data update (similar to a single channel operation), and then toggle high to low indicating the new channel’s conversion data is available. If ‘N’ channels are enabled, RDYB will toggle high to low ‘N’ times. If SEQ:RDYBEN is set to ‘1’, the RDYB event for each channel is suppressed. The RDYB toggles high to low when the last channel is ready to update its corresponding data register and a single high to low transition happens.

The STAT:SRDY[5:0] bits get set to ‘1’ when their corresponding channel finishes converting, irrespective of the RDYBEN setting for sequencer modes 2 and 3. The conversion status is available by reading the STAT:MSTAT bit. This stays high as long as the modulator is converting.

See Figure 4 for timing of RDYB.

SDA (Serial Data Input/Output)

The SDA line is considered an input when the master is transmitting the data to the MAX11259. The SDA line will be used as an output when the MAX11259 has data to be sent onto the I2C bus during a register read by the host master.

The slave in the MAX11259 implements mandatory requirements as specified in I2C standard, which are detections of START and STOP conditions and support for ACK/NACK. This slave supports 7-bit addressing and does not support the general call address.

I2C Sequence: The master needs to send out the first byte with a valid device address. The last bit of the first byte is a R/W bit and the master needs to send a '0' in this bit. The device will ignore a '1' sent in this bit. This is followed by a COMMAND BYTE for the MAX11259 as described in the command structure. The MAX11259 then responds to the command request depending on the MODE bit in the command.

Writing a Command to the MAX11259 for Conversion/Calibration/Power-Down

1) I2C START

2) I2C WRITE

a. Send Device Address with a '0' in bit 8 indicating the master will send a command byte followed by the device address. (8’b0110000_0)

b. Check Acknowledge

c. Send Command byte to convert/power down / calibrate (8’b10_01_xxxx)

d. Check acknowledge

3) I2C STOP

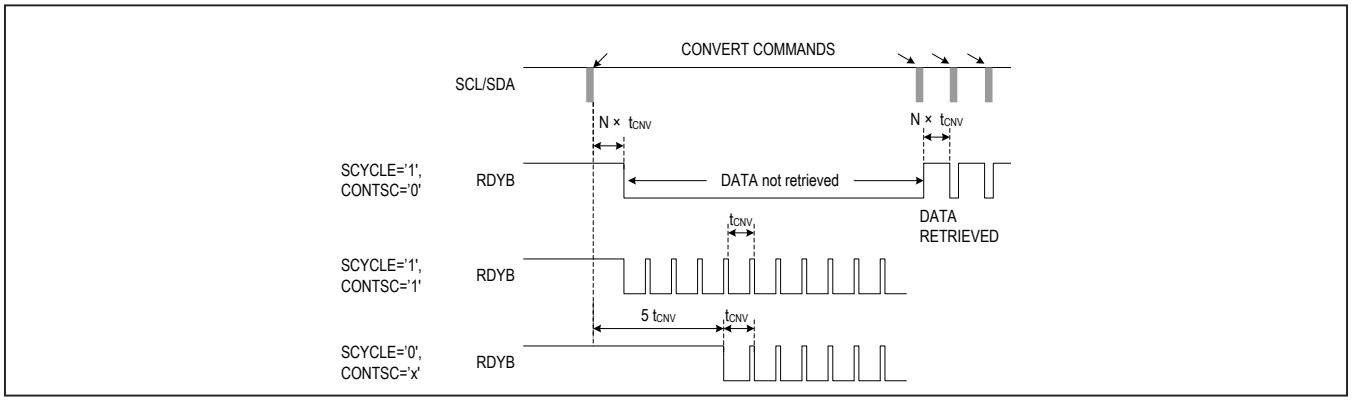


Figure 4. Timing of RDYB in All Conversion Configurations: Single-Cycle, Single-Cycle Continuous and Continuous. In sequencer mode 1 and in sequencer modes 2 and 3, with SEQ:RDYBEN=’0’ N = 1. In sequencer modes 2 and 3 with SEQ:RDYBEN=’1’ N = number of active channels.

Sequence to Execute I²C Write Operation

1) I²C START

2) I²C WRITE

a. Send Device Address with a '0' in bit 8 indicating the master will send a command byte followed by the device address. (8'b0110000_0)

b. Check Acknowledge

c. Send Command byte to Write registers (8'b11_reg_addr[4:0]_0)

d. Check acknowledge

e. Send 8-bit register data MSB first

f. Check Acknowledge

g. …

h. Check Acknowledge

3) I²C STOP

Sequence to Execute I²C Read Operation

1) I²C START

2) I²C WRITE

a. Send Device Address with a '0' in bit 8 indicating the master will send a command byte followed by the device address. (8'b0110000_0)

b. Check Acknowledge

c. Send Command byte to Read registers (8'b11_reg_addr[4:0]_1)

d. Check Acknowledge

3) I²C Repeat START

4) I²C WRITE

a. Send Device Address with a '1' in bit 8 indicating the master will read the register data out.

b. Check Acknowledge

5) I²C READ

a. Receive 8 bits of Data

b. Send Acknowledge

c. …

d. Receive 8 bits of Data

e. Send Not Acknowledge

6) I²C STOP

I²C Timing Characteristics

The I²C timing diagram is shown in Figure 1. The bus timing requirements are specified in *I2C Timing Requirements* table. The data is sampled on the positive edge of SCL and launched on negative edge of SCL for ACK and DATA reads. This gives a sufficient hold time for the master to sample the data.

I²C Device Addressing Scheme

The I²C slave has a 7-bit long device address. The device address is followed by a R/$\overline{W}$ bit which is low for a write command and high for a read command.

The first three most significant bits of the device address are always 011. Slave address bits A[4:1] correspond by the matrix in Table 4 to the states of the device address bumps AD0 and AD1.

The AD0 and AD1 bumps can be connected to any of the three signals: DGND, DVDD, and SDA giving 3 possible addresses for each bump allowing up to 9 devices connected to the bus (see Figure 5).

Modes and Registers

The MAX11259 interface operates in two fundamental modes, either to issue a conversion command or to access registers. The mode of operation is selected by a command byte. Every I²C transaction to the MAX11259 starts with a command byte. The command byte begins with the MSB (B7) set to '1'. The next bit (B6) determines whether a conversion command is sent or register read/write access is requested.

Command Byte

The conversion command sets the mode of operation (conversion, calibration, or power-down) as well as the conversion speed of the MAX11259. The register read/write command specifies the register address as well as the direction of the access (read or write).

Channel Sequencing

Changing SEQUENCER Modes

Mode Exit (See Table 9. Register Map for Register Definitions)

To exit any of the three sequencer modes at any time program the following sequence:

1) Issue a power-down command to exit the conversion process to STANDBY or SLEEP, as defined in CTRL1:PD[1:0]:

a. Write a conversion command byte (see Table 5. Command Byte Definition) and set MODE[1:0] of the command byte to '01'

2) Wait for STAT:PDSTAT[1:0] = '01' (SLEEP) or STAT:PDSTAT[1:0] = '10' (STANDBY).

Note: For all sequencer modes, the default exit state upon completion of all conversions is SLEEP. In

Table 4. I²C Device Address Mapping

ADDRESS PINS		DEVICE ADDRESS							
AD1	AD0	A7	A6	A5	A4	A3	A2	A1	A0
DGND	DGND	0	1	1	0	0	0	0	~W/R
DGND	DVDD				0	0	0	1	~W/R
DGND	SDA				0	0	1	1	~W/R
DVDD	DGND				0	1	0	0	~W/R
DVDD	DVDD				0	1	0	1	~W/R
DVDD	SDA				0	1	1	1	~W/R
SDA	DGND				1	1	0	0	~W/R
SDA	DVDD				1	1	0	1	~W/R
SDA	SDA				1	1	1	1	~W/R

Note: *Up to 9 devices can be selected on the I²C bus using the above addressing scheme.*

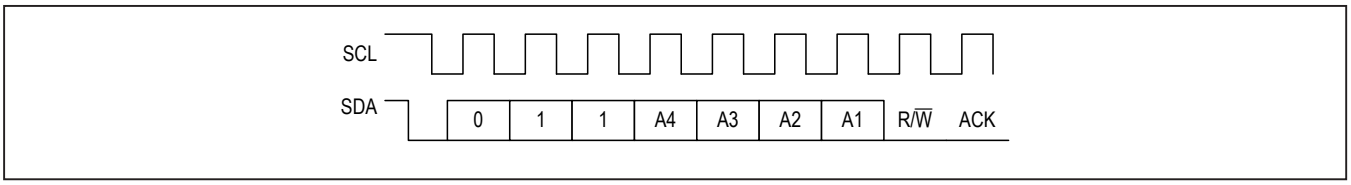


Figure 5. I²C Address Selection Byte Timing

sequencer mode 1, however, continuous conversion operation (CTRL1:SCYCLE='0') and continuous single-cycle conversion operation (CTRL1:SCYCLE='1' and CTRL1:CONTSC='1') are running continuously and must be terminated with the Mode Exit sequence.

Mode Change

To change sequencer modes or to update the SEQ register, program the following sequence:

1) Perform Sequencer Mode Exit (see the *Mode Exit* section).
2) Set up the following registers: SEQ, CTRL1.
   a. Set SEQ:MODE[1:0] to select the new sequencer mode
   b. Set CTRL1:PD[1:0] to STANDBY or SLEEP state to set the desired exit state if a conversion command with MODE[1:0] set to '01' is issued during the conversion.
3) Write the command byte (see Table 5).
   a. Set MODE[1:0] of the command byte to '11' (sequencer mode)
4) Wait for STAT:PDSTAT[1:0] = '00' to confirm conversion mode.

SEQUENCER MODE 1—Single-Channel Conversion with GPO Control and MUX Delays

This mode is used for single-channel conversions where the sequencer is disabled. Figure 6 illustrates the timing. To support high-impedance source networks, the conversion delay (SEQ:MDREN) feature must be enabled. The states of the GPO and GPIO bumps are configured using the GPO_DIR and GPIO_CTRL registers and can be modified anytime during mode 1 operation. The values of the CHMAP0/CHMAP1 registers and DELAY:GPO[7:0] bits are ignored in this mode.

Programming Sequence

Mode Entry

1) Set up the following registers: SEQ, DELAY, CTRL1, GPO_DIR, GPIO_CTRL.
   a. SEQ:MODE[1:0] = '00' for sequencer mode 1
   b. SEQ:MUX[2:0] to select the channel for conversion

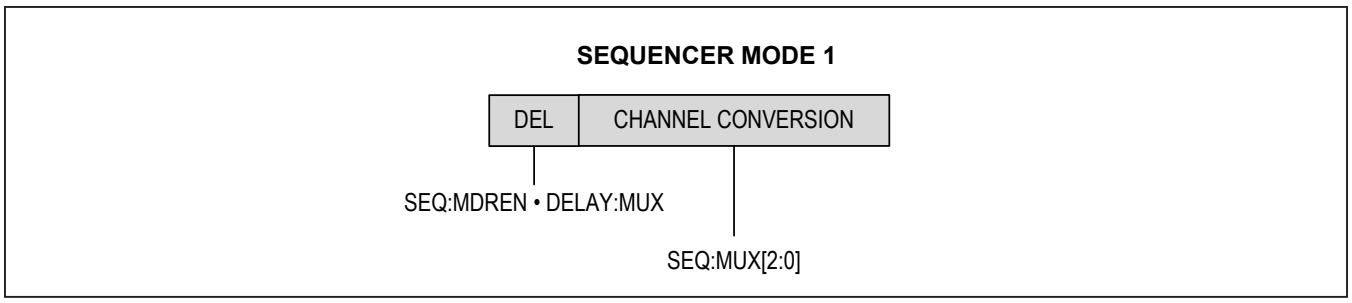


Figure 6. Sequencer Mode 1 Timing Diagram

Table 5. Command Byte Definition

	B7 (MSB)	B6	B5	B4	B3	B2	B1	B0
Conversion Command	1	0	MODE1	MODE0	RATE3	RATE2	RATE1	RATE0
Register Read/Write	1	1	RS4	RS3	RS2	RS1	RS0	R/$\overline{W}$

Table 6. Command Byte Decoding

BIT NAME	DESCRIPTION		
MODE[1:0]	The MODE bits are used to set the functional operation of the MAX11259 according to the following decoding.		
	MODE1	**MODE0**	**DESCRIPTION**
	0	0	Unused
	0	1	Power-down performed based on the CTRL1:PD[1:0] setting
	1	0	Calibration performed based on the CTRL1:CAL[1:0] setting
	1	1	Sequencer mode. The operation is based on the configuration of the SEQ register
RATE[3:0]	These bits determine the conversion speed of the MAX11259. The decoding is shown in Table 1.		
RS[4:0]	Register address as shown in Table 9.		
R/$\overline{W}$	The R/$\overline{W}$ bit enables either a read or a write access to the address specified in RS[4:0]. If R/$\overline{W}$ is set to '0', then data is written to the register. If the R/$\overline{W}$ bit is set to '1', then data is read from the register.		

c. Enable SEQ:MDREN to delay conversion start to allow for input settling. Set DELAY:MUX[7:0] to the desired conversion delay

d. Set CTRL1:SCYCLE for either single cycle (no latency) or continuous conversion

e. If single-cycle conversion is selected, set CTRL1:CONTSC to '1' if continuous single-cycle conversion is desired

f. Set CTRL1:PD[1:0] to STANDBY or SLEEP state to set the desired exit state if a conversion command with MODE[1:0] set to '01' is issued during the conversion

g. Set register GPO_DIR and, if desired, GPIO_CTRL to enable or disable the desired GPO and GPIO bumps

2) Write a conversion command (see Table 5, Command Byte Definition).

   a. Set data rate using bits RATE[3:0] of the command byte

   b. Set MODE[1:0] of the command byte to '11' for sequencer mode

3) Monitor RDYB for availability of conversion results in the DATA register (See Figure 4 for RDYB timing).

Mode Exit

1) In single-cycle conversion mode (CTRL1:SCYCLE ='1') the sequencer exits into SLEEP state.

2) In continuous conversion mode (CTRL1: SCYCLE='0' or (CTRL:SCYCLE='1' and CTRL1:CONTSC ='1')), conversions continue nonstop until the mode is exited. To interrupt and exit continuous conversion or con-

tinuous single-cycle conversion follow the *Changing SEQUENCER Modes—Mode Exit* section to put the part into STANDBY or SLEEP state based on CTRL1:PD[1:0] set in step 1(f) of *Mode Entry* section.

Changing Input Channel During Continuous Single-Cycle Conversion in Mode 1

1) Issue a conversion command with MODE[1:0] set to '01' to exit the conversion process to STANDBY or SLEEP state (see the *Changing SEQUENCER Modes—Mode Exit* section).
2) Monitor STAT:PDSTAT = '10' or '01' to confirm exit to STANDBY or SLEEP state.
3) Set SEQ:MUX[2:0] to select the new channel for conversion
4) Write a conversion command (see Table 5) and set MODE[1:0] of command byte to '11'

SEQUENCER MODE 2 – Multichannel Scan with GPO Control and MUX Delays

This mode is used to sequentially convert a programmed set of channels in a preset order. Figure 7 illustrates the timing.

The states of the GPO and GPIO bumps are configured using the GPO_DIR and GPIO_CTRL registers and can be modified anytime during mode 2 operation. In mode 2, register bits CHMAP0:CHn_ORD[2:0], CHMAP1:CHn_ORD[2:0], CHMAP0:CHn_EN, and CHMAP1:CHn_EN are used to select channels and conversion order. Bits DELAY:GPO[7:0], CHMAP0:CHn_GPO[2:0], CHMAP0:CHn_GPOEN, CHMAP1:CHn_GPO[2:0], and CHMAP1:CHn_GPOEN are ignored in this mode. The bit CTRL1:CONTSC is ignored and bit CTRL1:SCYCLE = '0' is invalid in this mode.

Programming Sequence

Mode Entry

1) Set up the following registers: SEQ, CHMAP0, CHMAP1, DELAY, GPO_DIR, GPIO_CTRL, CTRL1
   a. SEQ:MODE[1:0] = '01' for sequencer mode 2
   b. If desired set SEQ:RDYBEN to '1' to signal data ready only when all channel conversions are completed
   c. Enable SEQ:MDREN to delay conversion start to allow for input settling. Set DELAY:MUX[7:0] to the desired conversion delay
   d. Set CHMAP0 and CHMAP1 to select the channels and channel order for conversion
   e. Set CTRL1:PD[1:0] to STANDBY or SLEEP state to set the desired exit state if a conversion command with MODE[1:0] set to '01' is issued during the conversion
   f. Set register GPO_DIR and GPIO_CTRL to enable or disable the desired GPO and GPIO bumps
   g. Set CTRL1:SCYCLE = '1' for single-cycle conversion mode
2) Write a conversion command (see Table 5).
   a. Set data rate using bits RATE[3:0] of the command byte
   b. Set MODE[1:0] of the command byte to '11'
3) Monitor RDYB (if SEQ:RDYBEN='0') and bits STAT:SRDY[5:0] for availability of per channel conversion results in DATA[x] registers.

Mode Exit

1) This mode exits to SLEEP state upon completion of sequencing all channels
2) To interrupt current sequencing perform mode exit, see the *Changing SEQUENCER Modes—Mode Exit* section. This device is put in STANDBY or SLEEP state based on CTRL1:PD[1:0] set in step 1(e) of *Mode Entry* section.

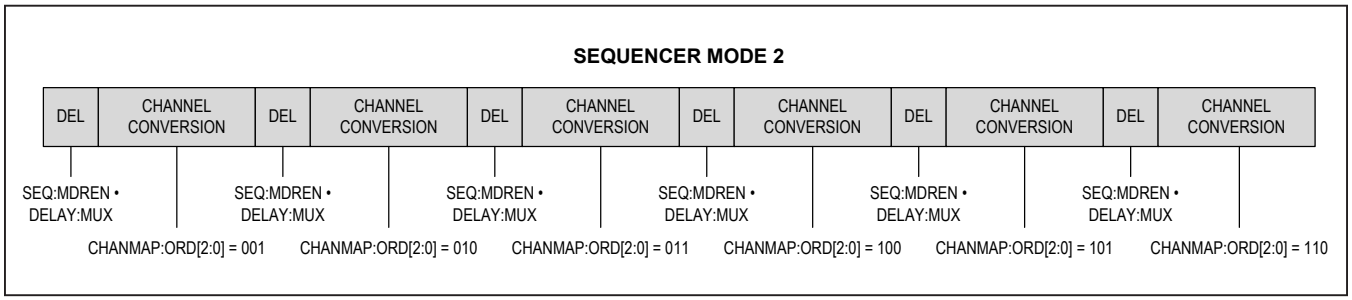


Figure 7. Sequencer Mode 2 Timing Diagram

SEQUENCER MODE 3 – Scan, With Sequenced GPO Controls

This mode is used to sequentially convert a programmed set of channels in a preset order and sequence the GPO/GPIO bumps concurrently. The GPO/GPIO bumps are used to bias external circuitry such as bridge sensors; the common reference (GPOGND) is typically ground. After all channel conversions have completed, the MAX11259 automatically powers down into SLEEP mode. Figure 8 illustrates the Sequencer Mode 3 timing diagram for a three-channel scan. As long as CTRL3:GPO_MODE is set to '1', registers GPO_DIR and GPIO_CTRL are ignored in this mode, as the GPO/GPIO bumps are controlled by the sequencer.

If CTRL3:GPO_MODE is set to '0', the GPO/GPIO bumps are directly controlled by the GPO_DIR and GPIO_CTRL registers and are not controlled by the sequencer.

Programming Sequence

Mode Entry

1) Set up the following registers: SEQ, CHMAP0, CHMAP1, DELAY, CTRL1, CTRL3
   a. SEQ:MODE[1:0]='10' for sequencer mode 3
   b. If desired, set SEQ:RDYBEN to '1' to signal data ready only when all channel conversions are completed
   c. Enable SEQ:MDREN if conversion start is to be delayed to allow for input settling. Set DELAY:MUX[7:0] to the desired conversion delay
   d. Set CTRL3:GPO_MODE to '1' to enable GPO/GPIO sequencing
   e. Set CHMAP0 and CHMAP1 to enable the channels for conversion and to set the channel conversion order. Map the corresponding GPO/GPIO bumps to a channel.
   f. Enable SEQ:GPODREN to add a delay before the multiplexer selects this channel for conversion. Set DELAY:GPO to a delay value sufficient for the bias to settle.
   g. Set CTRL1:PD[1:0] to STANDBY or SLEEP state to set the desired exit state if a conversion command with MODE[1:0] set to '01' is issued during the conversion
   h. Set CTRL1:SCYCLE = '1' for single conversion mode
2) Write the conversion command (see Table 5)
   a. Set the data rate using bits RATE[3:0] of the command byte

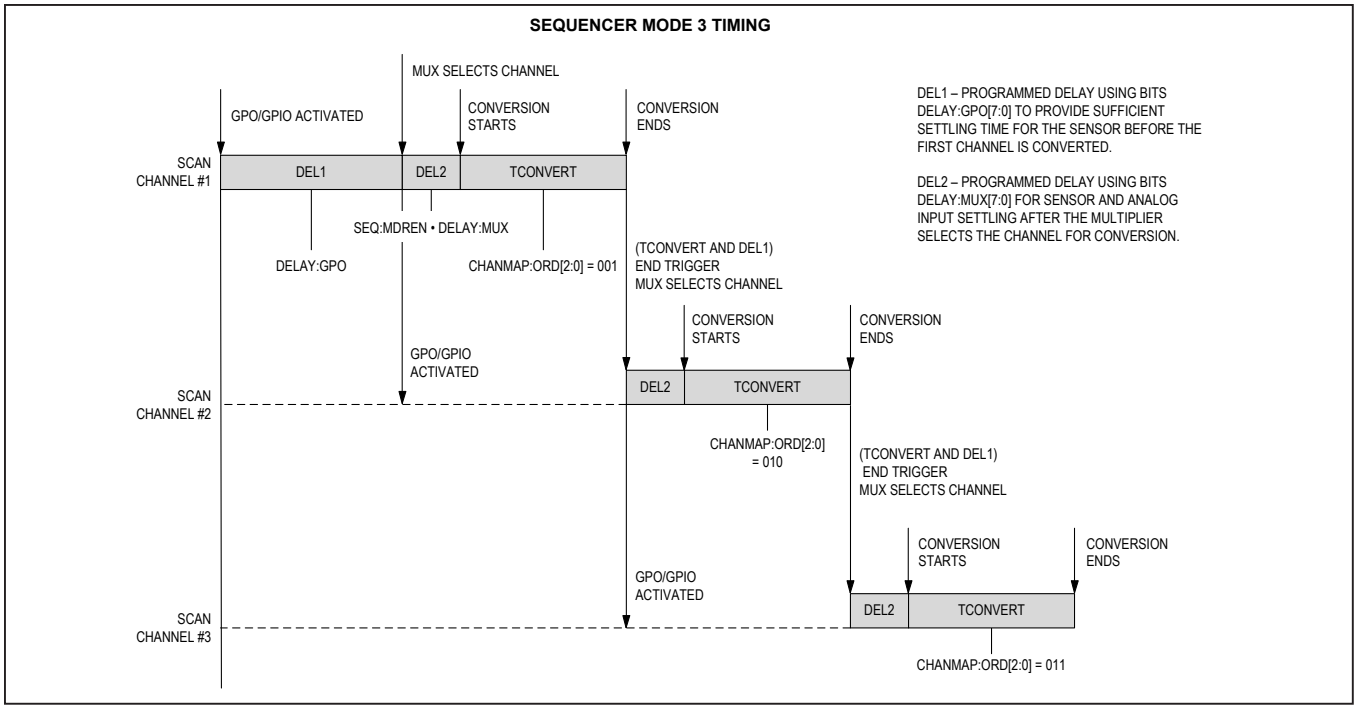


Figure 8. Sequencer Mode 3 Timing Diagram for a Three-Channel Scan

b. Set MODE[1:0] of command byte to '11'

3) Monitor RDYB (if SEQ:RDYBEN = '0') and bits STAT:SRDY[5:0] for availability of per channel conversion results in DATA[x] registers.

Mode Exit

1) This mode exits to SLEEP state upon completion of sequencing all channels and GPO/GPIO bumps.

2) To interrupt the current sequencing, perform mode exit. See the *Changing SEQUENCER Modes—Mode Exit* section. This puts the part in STANDBY or SLEEP state based on CTRL1:PD[1:0] set in step 1(g) of Mode Entry.

The bit CTRL1:CONTSC is ignored and bit CTRL1:SCYCLE = '0' is invalid in this mode.

Operating Examples—From Full Power-Down to Mode 3

In this example, channels 0, 1, and 2 are configured for conversion in mode 3. Channel 0 is configured last in the scan order and the GPIO0 is mapped to this channel. Channel 1 is configured first in the scan order and GPO1 is mapped to this channel. Channel 2 is configured second in the scan order and GPO0 is mapped to this channel. Channels 0, 1, and 2 are enabled for scan and GPO/GPIO switching is also enabled. The RDYBEN is not set which generates a RDYB transition after each channel is converted. The PGA is configured for a gain of 128 and the data rate is 6,400sps in single-cycle mode. The MUX delays are enabled for all used channels and the GPO/GPIO delays are disabled. Reference *I²C Command Sequence* section.

Error Checking Sequencer Mode 3

The MAX11259 perform checks on registers CHMAP0 and CHMAP1. Error flags are set when invalid values are set:

STAT:GPOERR is set when more than one input channel is mapped to the same GPO/GPIO bump.

STAT:ORDERR is set when CHn_ORD is set as '000' or '111' and channel n is enabled using CHMAPx:CHn_EN.

Supplies and Power-On Sequence

The MAX11259 requires two power supplies, AVDD and DVDD. These power supplies can be sequenced in any order. The analog supply (AVDD) powers the analog inputs and the modulator. The DVDD supply powers the I²C interface. The low-voltage core logic can either be powered by the integrated LDO (default) or via DVDD. Figure 9 shows the two possible schemes. CAPREG denotes the internally generated supply voltage. If the LDO is used, the DVDD operating voltage range is from 2.0V to 3.6V. If the core logic is directly powered by DVDD (DVDD and CAPREG connected together), the DVDD operating voltage range is from 1.7V to 2.0V

Power-On Reset and Undervoltage Lockout

A global power-on reset (POR) is triggered until AVDD, DVDD, and CAPREG cross a minimum threshold voltage (V_{LH}), as shown in Figure 10.

To prevent ambiguous power-supply conditions from causing erratic behavior, voltage detectors monitor AVDD, DVDD, and CAPREG and hold the MAX11259 in reset when supplies fall below V_{HL} (see Figure 10). The analog undervoltage lockout (AVDD UVLO) prevents the ADC from converting when AVDD falls below V_{HL}. The CAPREG UVLO resets and prevents the low-voltage digital logic from operating at voltages below V_{HL}. DVDD UVLO thresholds supersede CAPREG thresholds when CAPREG is externally driven. Figure 11 shows a flow diagram of the POR sequence. Glitches on supplies AVDD, DVDD, and CAPREG for durations shorter than T_P are suppressed without triggering POR or UVLO. For glitch durations longer than T_P, POR is triggered within T_{DEL} seconds. See the *Electrical Characteristics* table for values of V_{LH}, V_{HL}, T_P, and T_{DEL}.