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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

General Description

The MAX11261PMB peripheral module (Pmod™) provides the necessary hardware to interface to the MAX11261, a 24-bit, 6-channel, 16ksps, integrated PGA delta-sigma ADC to any system that utilizes Pmod-compatible expansion ports configurable for I²C communication. The peripheral module includes a graphical user interface (GUI) that provides communication from the target device to the PC through the USB2PMB2#. The peripheral module can operate in multiple modes:

Using USB2PMB2# Adapter: In "standalone" mode, the peripheral module is connected to the PC through a USB2PMB2# adapter board and performs a subset of the complete peripheral module functions with limitations for sample rate, sample size, and no support for coherent sampling.

User-Supplied I²C Mode: The peripheral module provides a 12-pin Pmod-style header for user-supplied I²C interface to connect the signals for SCL, SDA, RSTB, and RDYB.

Ordering Information **appears at end of data sheet.**

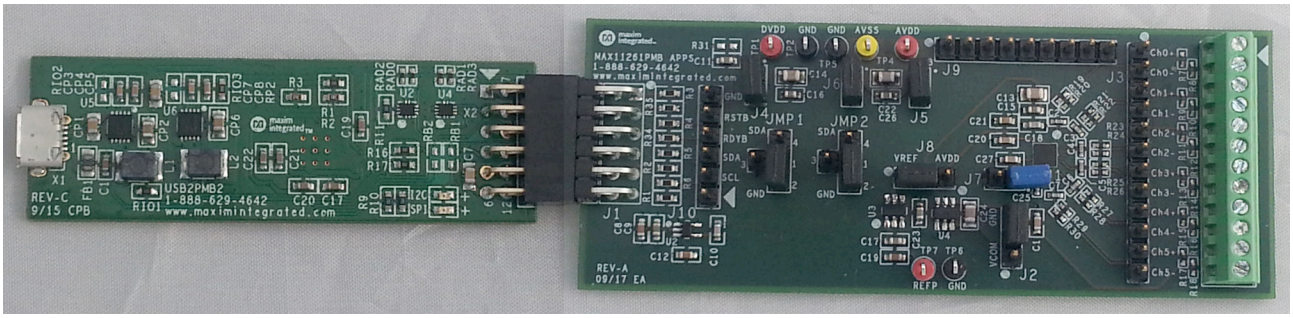
The peripheral module includes Windows XP®, Windows® 7, Windows 8.1, and Windows 10-compatible software for exercising the features of the IC. The peripheral module GUI allows different sample sizes, adjustable sampling rates, internal or external reference options, and graphing software that includes the FFT and histogram of the sampled signals.

The peripheral module can be powered by a local +3.3V supply and comes installed with a MAX11261ENX+ in a 36-bump wafer-level package (WLP).

Features

- Various Sample Sizes and Sample Rates
- Time Domain, Frequency Domain, and Histogram Plotting
- On-Board Voltage Reference (MAX6071)
- Proven PCB Layout
- Fully Assembled and Tested

MAX11261 EV Board Photo



Windows are registered trademarks and registered service marks of Microsoft Corporation.

maxim integrated™

Quick Start

Required Equipment

- MAX11261PMB1 EV kit (includes micro-USB cable)
- USB2PMB2 USB to I²C interface board
- Windows PC

Note: In the following sections, software-related items are identified by bolding. Text in **bold** refers to items directly from the EV kit software. Text in **bold and underlined** refers to items from the Windows operating system.

Procedure

The EV kit is fully assembled and tested. Follow the steps below to verify board operation:

1) Visit http://www.maximintegrated.com and search for MAX11261 product page. Click on the **Design Resources** tab. The software associated with this part will be listed under **Software**.
2) Connect the MAX11261PMB1 board to the USB-2PMB2 board.
3) Connect the USB cable from the PC to the USB2PMB2 board. Windows may require some time to install its device driver.
4) Open the EV kit GUI, MAX11261EVKit.exe and select **Device→MAX11261PMB** option (or **MAX11261PMB**).
5) In the center of the **Configuration** tab, inside the **Delta-Sigma Modulator** block, set **Conversion Mode** to **Single Continuous** and then click **Convert** and **Read All**. The status will be updated with the measurement data. See Figure 1.
6) On the **Scope** tab, click **Capture**. A data sample is collected and plotted on the graph. The frequency spectrum can be viewed on the **FFT** tab. The Scope, DMM, Histogram, and FFT tabs support data capture for Single Continuous mode.
7) In the center of the **Configuration** tab, inside the **Delta-Sigma Modulator** block, set **Conversion Mode** to **Continuous** and then click **Convert** and **Read All**.
8) On the **Scope** tab, click **Capture**. A data sample is collected and plotted on the graph. The frequency spectrum can be viewed on the **FFT** tab. The Single Continuous and Continuous modes support different sets of sample rates. The Scope, DMM, Histogram, and FFT tabs support data capture for Continuous mode.
9) In the center of the **Configuration** tab, inside the **Delta-Sigma Modulator** block, set C**onversion Mode** to **Single Cycle** and then click **Convert** and **Read All**. (**Note:** The Scope, DMM, Histogram, and FFT tabs do not support data capture for Single Cycle mode, so the **Capture** button will be disabled in this mode.)
10) In the **Scan Mode** tab, inside **Read Data** group, click **Scan** to ensure that the Conversion mode has been set to Single Cycle.
11) In the **Sequence Settings** group, click **Enable All Channels** to configure channels CH0-CH5 to be scanned in order, with GPO0-5 assigned to individual channels. The channels can be scanned in any order, and the GPO's can be assigned in any order.
12) Set **Sequence Mode** to **Mode 2** or **Mode 3**, then click **Scan** to perform a scan and **Read Data** to read the data. Mode 2 and Mode 3 perform a single scan each time Scan is clicked, but Mode 4 scans perpetually until another mode is selected.
13) Set **Sequence Mode** to **Mode 4**, click T**ouch Detect Demo** then click **Scan**. The registers will be configured for comparator mode 10 to trigger on a level change exceeding ±4096 LSB. Whenever the RDYB interrupt is asserted, the GUI will read the data and update its display.

Detailed Description of Software

The main window of the peripheral module software contains seven tabs: Configuration, Scope, DMM, Histogram, FFT, Scan Mode, and Registers. The Configuration tab provides control for the ADC configuration including calibration and data capture. The other six tabs are used for evaluating the data captured by the ADC.

The Scope, DMM, Histogram, and FFT tabs support data capture for Continuous and Single Continuous conversion modes (Sequence Mode 1). When in Single Cycle mode, the Capture button is disabled.

The Scan Mode tab supports data capture for Conversion Mode = Single Cycle, Sequence Mode = Mode 1, 2, 3, or 4.

Evaluating Single Conversions (Sequence Mode 1)

In the **Configuration** tab, when **Conversion Mode** is set to **Single Cycle** or **Single Continuous**, conversions can be performed by clicking **Convert** followed by **Read Data** and **Status**.

Note: The Scope, DMM, Histogram, and FFT tabs require using **Continuous** or **Single Continuous** Conversion Mode instead of Single Cycle mode.

Evaluating Continuous Conversions (SEQ Mode 1)

In SEQ Mode 1, with Continuous conversion, the Scope, Histogram, and FFT tabs can be used to capture data.

Evaluating I2C SCLK Rates

Different I2C clock rates can be selected from the menu **Options→I2C→SCLK Rate**. Be sure to set the SEQ register SIF_FREQ bits to the right range for the selected clock rate.

Evaluating I2C Voltage Levels

Different I2C voltage levels can be selected from the menu **Options→I2C→Voltage**. When selecting 1.8V operation, install a shunt at J7 and disable the CAPREG LDO.

Evaluating Sequence Modes 2 (01) and 3 (10)

In Single Cycle Conversion mode, Sequence Mode 2 (01) and Mode 3 (10) can be evaluated using the Scan Mode tab.

In the **Scan Mode** tab, inside **Read Data** group, click **Scan** to ensure that the Conversion mode has been set to Single Cycle.

In the **Sequence Settings** group, click **Enable All Channels** to configure channels CH0-CH5 to be scanned in order, with GPO0-5 assigned to individual channels. The channels can be scanned in any order, and the GPO's can be assigned in any order.

Set **Sequence Mode** to **Mode 2 (01)** or **Mode 3 (10)**; then click **Scan** to perform a scan and **Read Dat**a to read the data. Mode 2 and mode 3 perform a single scan each time **Scan** is clicked.

Evaluating Sequence Mode 4 (11)

In Single Cycle Conversion mode, Sequence Mode 4 (11) can be evaluated using the Scan Mode tab.

In the **Scan Mode** tab, inside **Read Data** group, click **Scan** to ensure that the Conversion mode has been set to Single Cycle.

In the **Sequence Settings** group, click **Touch Detect Demo** to configure channels CH0-CH5 to be scanned in order, with GPO0-5 assigned to individual channels, set CMP mode 10, and set the limit registers to default values. The channels can be scanned in any order, and the GPO's can be assigned in any order.

Set **Sequence Mode** to **Mode 4 (11)**; then click **Scan** to perform a scan and **Read Data** to read the data.

Mode 4 scans perpetually until another mode is selected.

When Mode 4 is active, the software responds to RDYB hardware pin low, by performing **Read Data** and clearing the interrupt status. The channel Out-of-Range status bit indicates that a touch event happened on that channel (the internal high-pass filtered data exceeded the configured threshold).

ADC Calibration

Two types of software calibration for offset and gain are available: self-calibration and system calibration. The primary mode for calibration is using the drop-down list to select a calibration mode, followed by clicking the **Calibrate** button. The checkboxes for **Self Offset**, **Self Gain**, **System Offset**, and **System Gain** allow for the user to enable or disable the calibration values. The calibration values can also be changed manually by entering a hex value in the numeric box.

Evaluating the PGA (Programmable Gain Amplifier)

Using the internal PGA requires performing System Offset / System Gain calibration.

On the **Configuration** Tab, under **Calibration**, make sure "**Internal Values**" is selected instead of "Interface Values".

Self Offset/Gain, **Calibrate**, **Read All**; verify that Self Offset and Self Gain values have changed slightly.

After selecting Input Path = PGA 1V/V: On the **Configuration** Tab, under **Calibration**, make sure **System Offset** and **System Gain** are checked (enabled).

Apply 0.0V to the input, select **System Offset** and **Calibrate**. Then **Read All** and verify the System Offset value changed.

Apply full-scale 2.490V to the input, select **System Gain** and **Calibrate**. Then **Read All** and verify the System Offset value changed. Note: if the Status register shows Data Overrange or Sys Gain Overrange, you will need to slightly reduce the fullscale input voltage and try again.

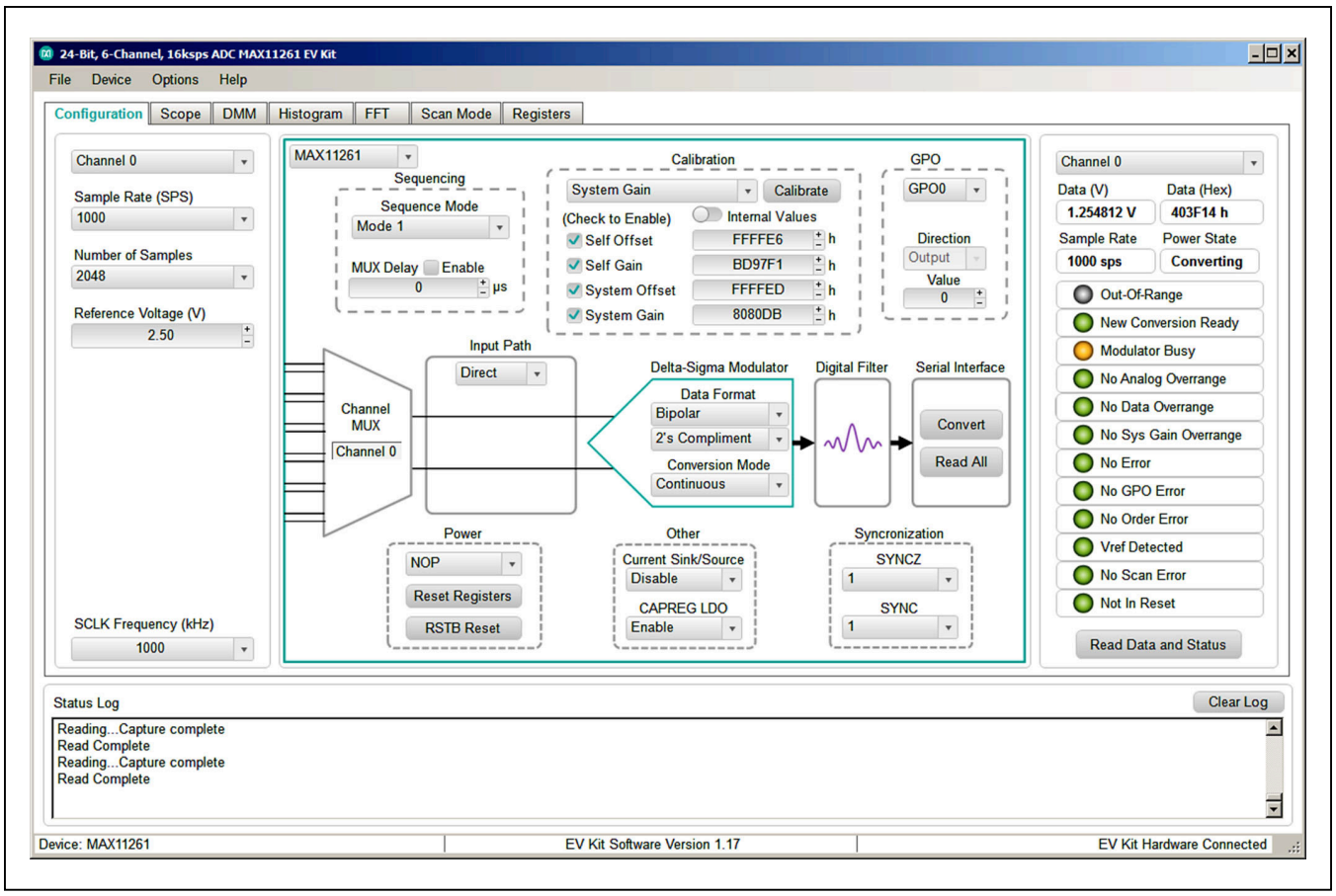


Figure 1. MAX11261 EV Kit Configuration Window

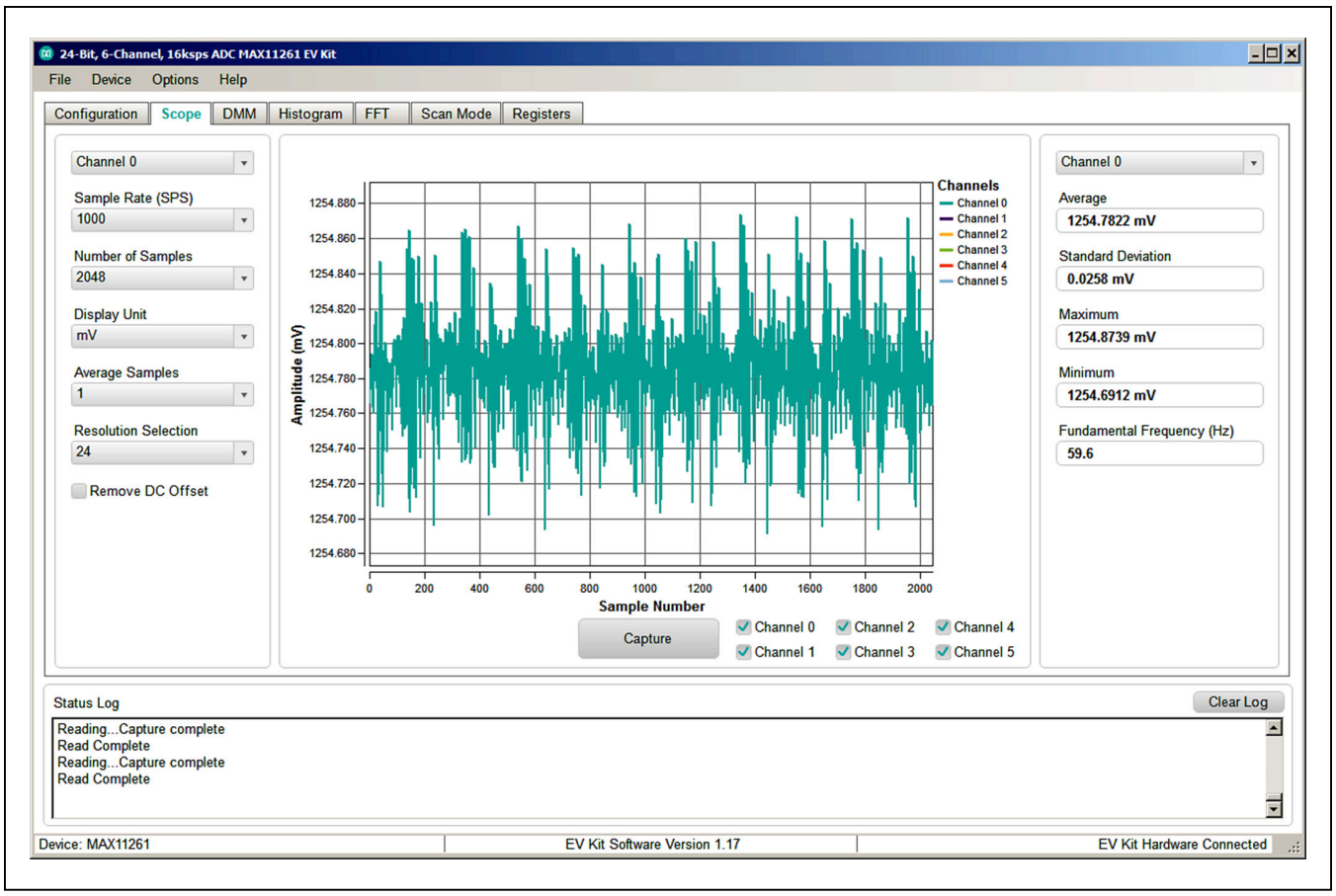


Figure 2. MAX11261 EV Kit Scope Window

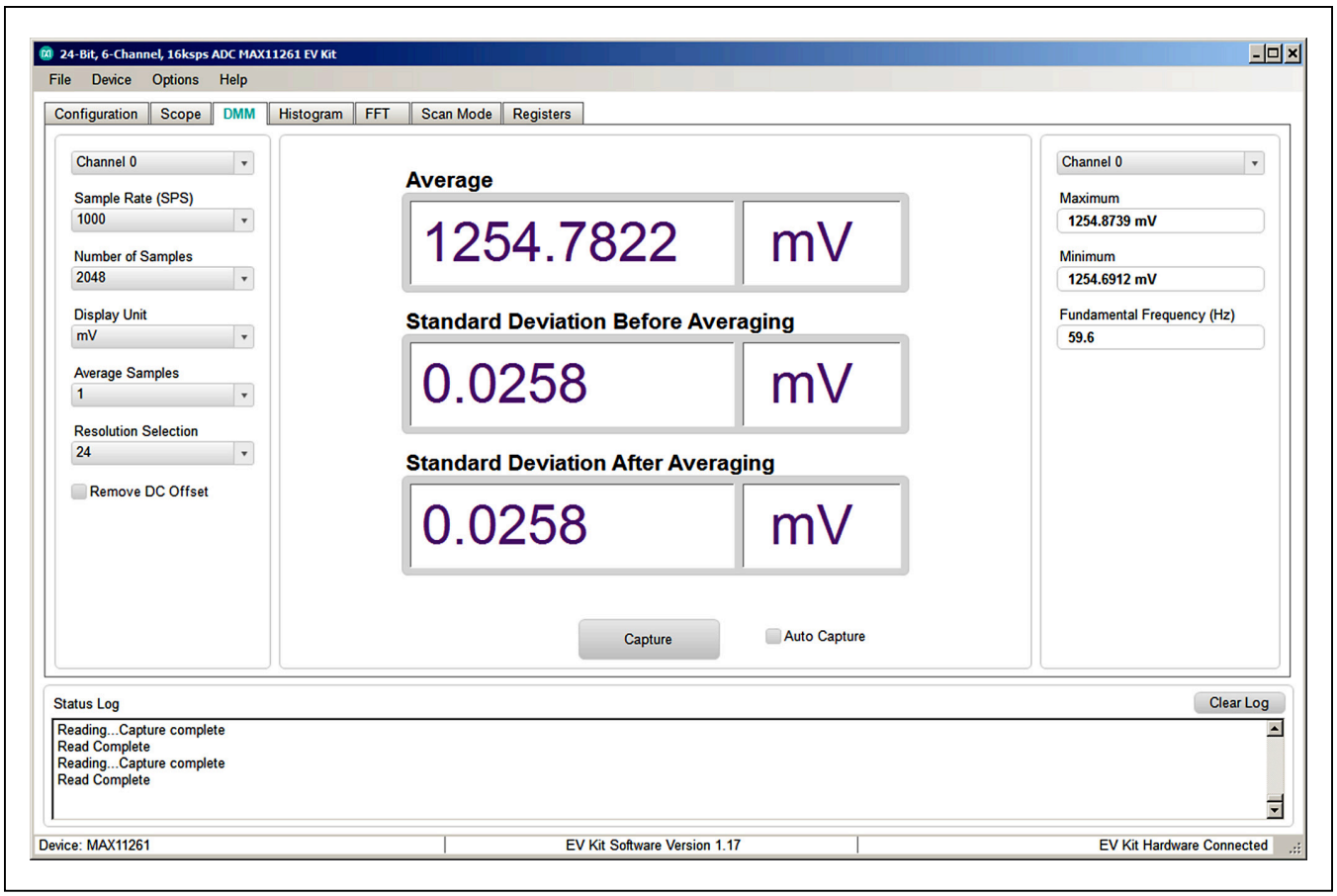


Figure 3. MAX11261 EV Kit DMM Window

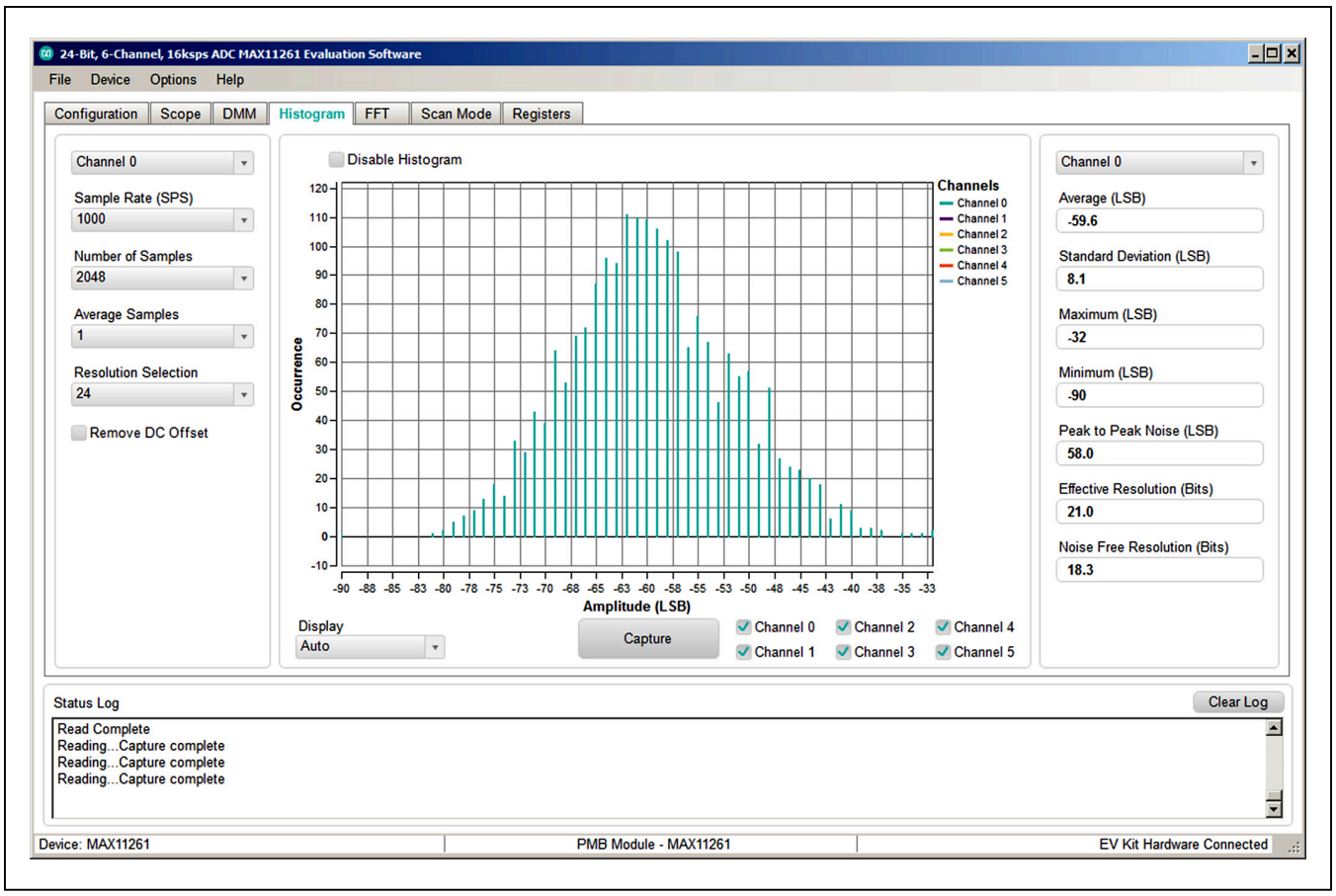


Figure 4. MAX11261 EV Kit Histogram Window

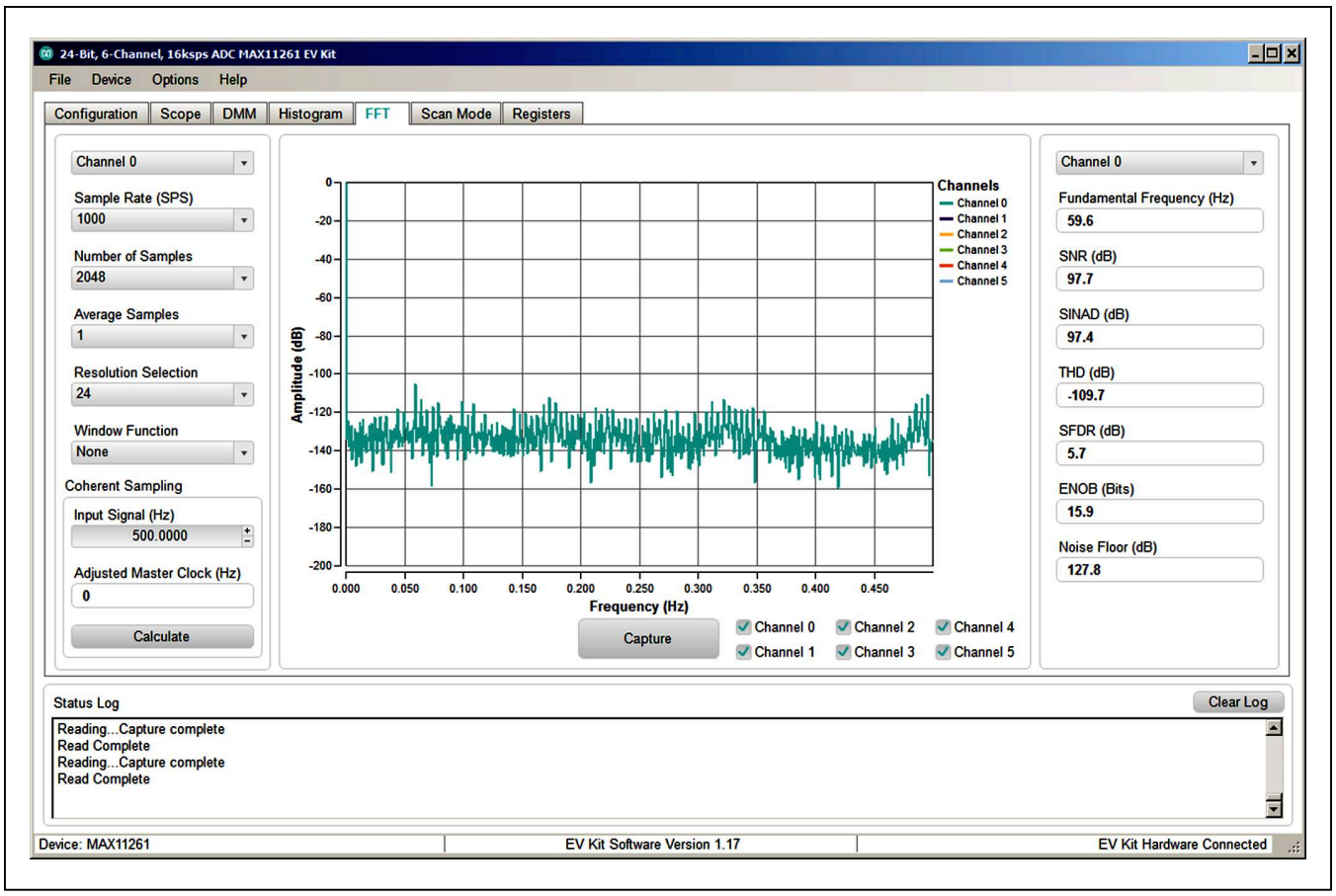


Figure 5. MAX11261 EV Kit FFT Window

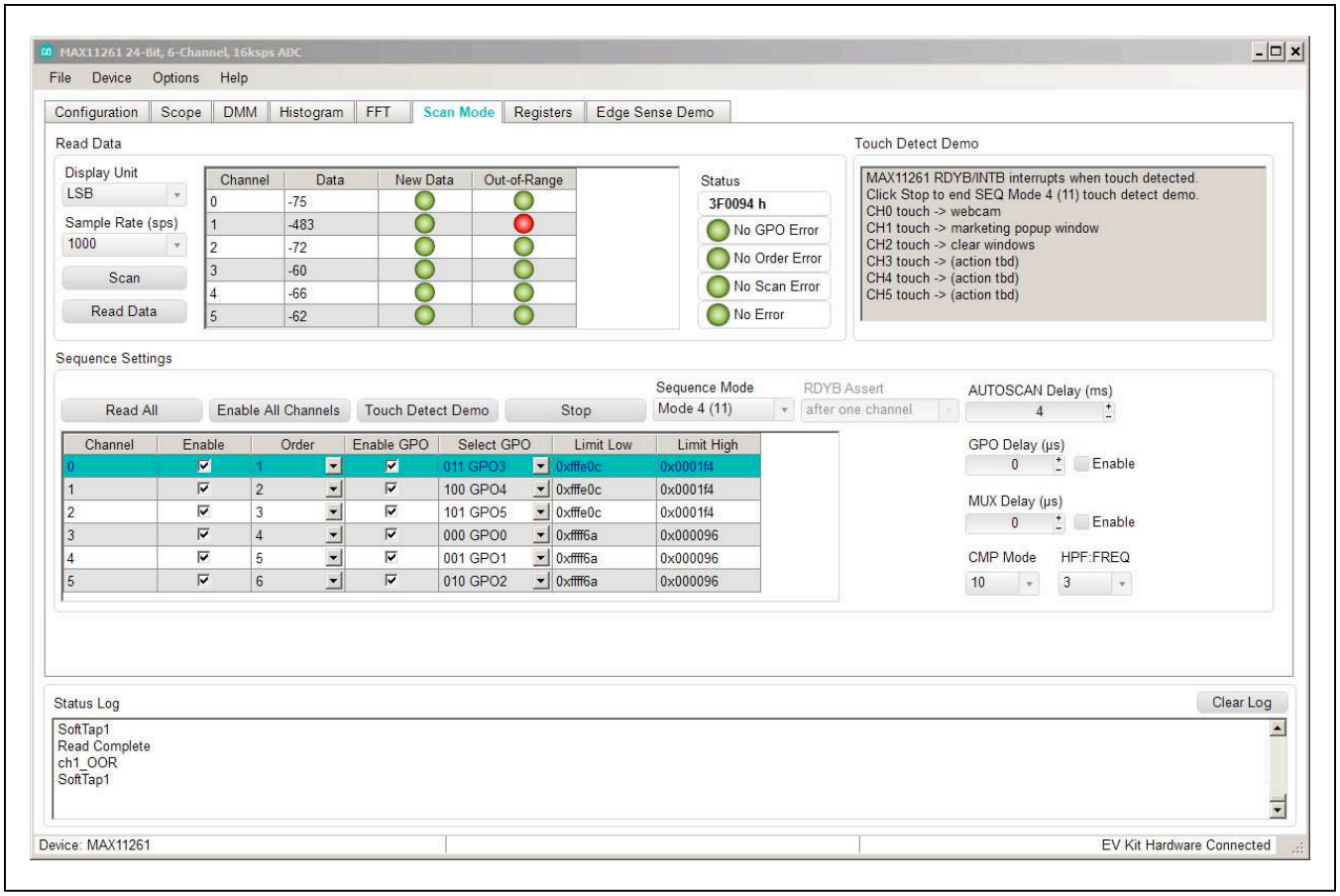


Figure 6. MAX11261 EV Kit Scan Mode Window

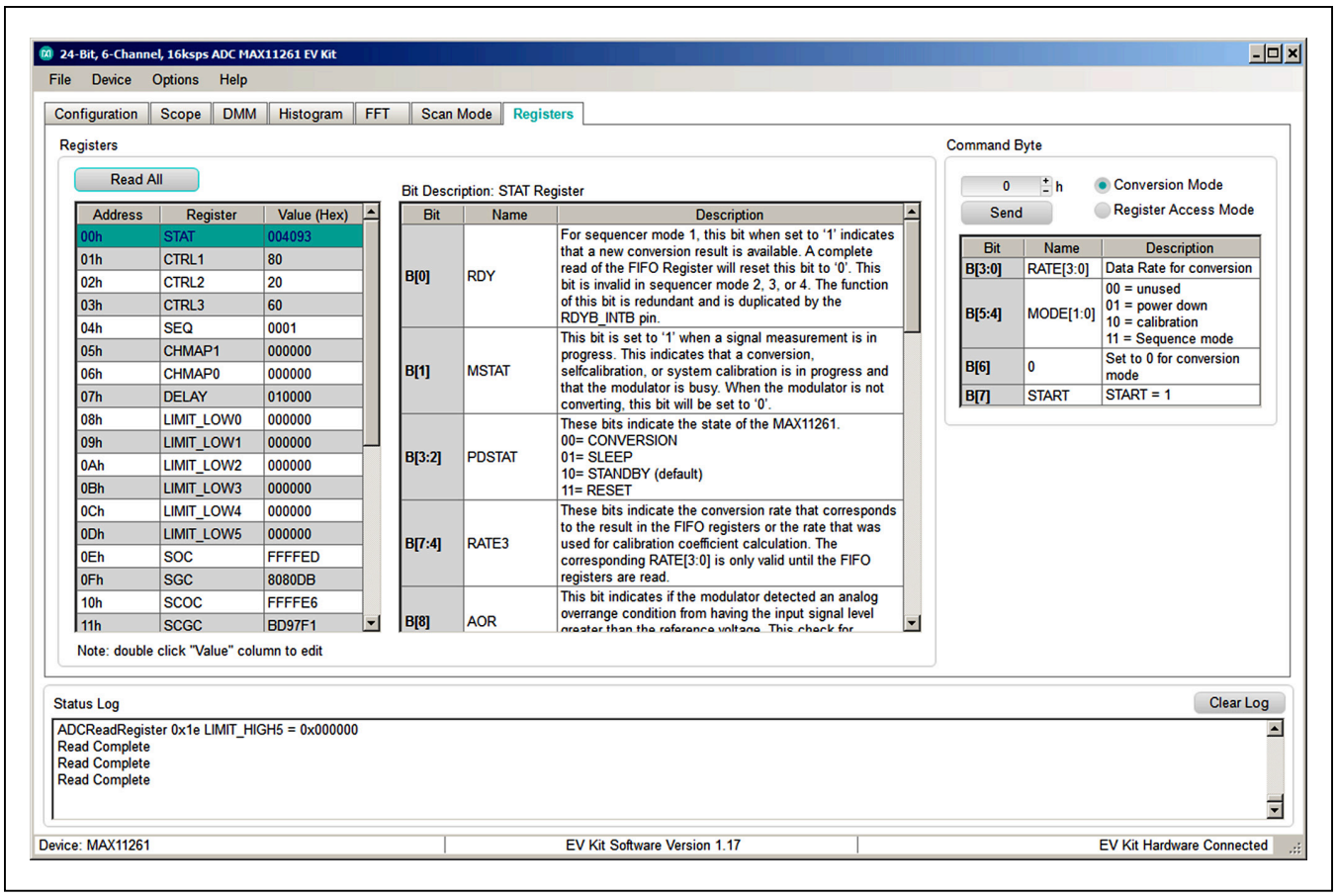


Figure 7. MAX11261 EV Kit Registers Window

Detailed Description of Hardware

U1, the MAX11261, is a 6-channel, 24-bit delta-sigma ADC with I2C Interface. Connect analog inputs to header J3 or terminal block J11 (these are equivalent). Set the common-mode level using jumper J2. Open-drain digital output control signals GPO[0:5] are provided on header J9 along with the SYNC and RDYB signals.

U2, the MAX8610, is a low-dropout linear regulator that provides the 3.0V AVDD supply.

U3 and U4 are MAX6071, which provides the 2.500V V_{REF} reference voltage and the 1.250V V_{COM} common-mode voltage.

The EV kit includes the USB2PMB2 master for all I^2C communication. Header J10 provides probe access to the signals on the PMOD interface connector J1.

Table 1. Jumper Functions

JUMPER	STATE	FUNCTION
JMP1/JMP2	1-2*/1-2*	Select address 0x30
	1-2/1-3	Select address 0x31
	1-2/1-4	Select address 0x33
	1-3/1-2	Select address 0x34
	1-3/1-3	Select address 0x35
	1-3/1-4	Select address 0x37
	1-4/1-2	Select address 0x3C
	1-4/1-3	Select address 0x3D
	1-4/1-4	Select address 0x3F
J2	1-2	Use MAX6071 as VCOM
	2-3*	Use GND as VCOM
J4	1-2*	Select +3.3V for DVDD
	Open	Select user-provided supply for DVDD at J4-1
J5	1-2*	Select +3.0V for AVDD
	Open	Select user-provided supply for DVDD at J5-1
J6	1-2*	Select GND for AVSS
	Open	Select user-provided supply for AVSS at J6-1
J7	Open*	Use internal 1.8V subregulator if DVDD ≥ 2.0V
	1-2	Use DVDD for internal logic if DVDD ≤ 2.0V
J8	1-2*	Select VREF from the on-board MAX6071 as the voltage reference
	2-3	Select AVDD as the voltage reference

**Default*
J1 is the PMOD header
J3 is an input header
J9 is the GP0[0:5]/SYNC/RDYB header
J10 is the SCL/SDA/RDYB/RSTB header
J11 is an input terminal block

Ordering Information

PART	TYPE
MAX11261SYS1#	EV Kit

#Denotes RoHS compliant.

MAX11261 EV Kit Bill of Materials

ITEM	QTY	REF DES	Var Status	MAXINV	MFG PART #	MFG	VALUE	DESCRIPTION
1	7	C1, C8, C12, C19-C21, C27	Pref	20-0001U-BA46	C1608X7R1V105K080AC	TDK	1UF	CAPACITOR; SMT (0603); CERAMIC CHIP; 1UF; 35V; TOL=10%; TG=-55 DEGC TO +125 DEGC; TC=X7R
2	7	C2-C7, C25	Pref	20-1000P-27	GRM1555C1H102JA01; C1005C0G1H102J050	MURATA; TDK	1000PF	CAPACITOR; SMT (0402); CERAMIC CHIP; 1000PF; 50V; TOL=5%; TG=-55 DEGC TO +125 DEGC
3	7	C9, C11, C15-C17, C23, C26	Pref	20-000U1-91	C0603C104K5RAC; C1608X7R1H104K	KEMET; TDK	0.1UF	CAPACITOR; SMT (0603); CERAMIC CHIP; 0.1UF; 50V; TOL=10%; TG=-55 DEGC TO +125 DEGC; TC=X7R;NOTE: NOT RECOMMENDED FOR NEW DESIGN USE 20-000u1-01
4	2	C10, C18	Pref	20-00U01-R0	C1608C0G1E103J	TDK	0.01UF	CAPACITOR; SMT (0603); CERAMIC CHIP; 0.01UF; 25V; TOL=5%; MODEL=; TG=-55 DEGC TO +125 DEGC; TC=C0G
5	4	C13, C14, C22, C24	Pref	20-004U7-63	C2012X7R1E475K125AB	TDK	4.7UF	CAPACITOR; SMT (0805); CERAMIC CHIP; 4.7UF; 25V; TOL=10%; MODEL=; TG=-55 DEGC TO +125 DEGC; TC=X7R
6	1	J1	Pref	01-TSW10608SDRA12P-17	TSW-106-08-S-D-RA	SAMTEC	TSW-106-08-S-D-RA	CONNECTOR; THROUGH HOLE; DOUBLE ROW; RIGHT ANGLE; 12PINS; THIS PART IS DEDICATED FOR PMOD PERIPHERAL BOARD
7	2	J2, J8	Pref	01-PCC03SAAN3P-21	PCC03SAAN	SULLINS	PCC03SAAN	CONNECTOR; MALE; THROUGH HOLE; BREAKAWAY; STRAIGHT THROUGH; 3PINS; -65 DEGC TO +125 DEGC
8	1	J3	Pref	01-PBC12SAAN12P-21	PBC12SAAN	SULLINS ELECTRONICS CORP.	PBC12SAAN	CONNECTOR; MALE; THROUGH HOLE; BREAKAWAY; STRAIGHT; 12PINS; -65 DEGC TO +125 DEGC
9	4	J4-J7	Pref	01-PCC02SAAN2P-21	PCC02SAAN	SULLINS	PCC02SAAN	CONNECTOR; MALE; THROUGH HOLE; BREAKAWAY; STRAIGHT THROUGH; 2PINS; -65 DEGC TO +125 DEGC
10	1	J9	Pref	01-PBC09SAAN9P-21	PBC09SAAN	SULLINS ELECTRONICS CORP	PBC09SAAN	CONNECTOR; MALE; THROUGH HOLE; BREAKAWAY; STRAIGHT; 9PINS; -65 DEGC TO +125 DEGC
11	1	J10	Pref	01-PBC06SAAN6P-21	PBC06SAAN	SULLINS ELECTRONICS CORP.	PBC06SAAN	CONNECTOR; MALE; THROUGH HOLE; BREAKAWAY; STRAIGHT; 6PINS; -65 DEGC TO +125 DEGC
12	1	J11	Pref	01-OSTVN12A15012P-25	OSTVN12A150	ON-SHORE TECHNOLOGY INC	OSTVN12A150	CONNECTOR; FEMALE; THROUGH HOLE; SCREW TYPE; GREEN TERMINAL BLOCK; RIGHT ANGLE; 12PINS
13	2	JMP1, JMP2	Pref	01-222840434P-21	22-28-4043	MOLEX	22-28-4043	CONNECTOR; MALE; THROUGH HOLE; FLAT VERTICAL BREAKAWAY; STRAIGHT; 4PINS
14	8	R1-R6, R34, R35	Pref	80-0028R-24	ERJ-3EKF28R0V	PANASONIC	28	RESISTOR; 0603; 28 OHM; 1%; 100PPM; 0.10W; THICK FILM
15	12	R7-R18	Pref	80-0001M-23	CRCW04021M00FK	VISHAY DALE	1M	RESISTOR; 0402; 1M; 1%; 100PPM; 0.0625W; THICK FILM
16	12	R19-R30	Pref	80-0010R-23	CRCW040210R0FK; 9C04021A10R0FL	VISHAY DALE	10	RESISTOR; 0402; 10 OHM; 1%; 100PPM; 0.0625W; THICK FILM
17	1	R31	Pref	80-0100K-24	CRCW06031003FK; ERJ-3EKF1003	VISHAY DALE/PANASONIC	100K	RESISTOR; 0603; 100K; 1%; 100PPM; 0.10W; THICK FILM
18	2	R32, R33	Pref	80-002K2-24	CRCW06032K20FK	VISHAY DALE	2.2K	RESISTOR, 0603, 2.2K OHM, 1%, 100PPM, 0.10W, THICK FILM
19	7	SU1-SU7	Pref	02-JMPFS1100B-00	SX1100-B	KYCON	SX1100-B	TEST POINT; JUMPER; STR; TOTAL LENGTH=0.24IN; BLACK; INSULATION=PBT;PHOSPHOR BRONZE CONTACT=GOLD PLATED
20	3	TP1, TP3, TP7	Pref	02-TPMINI5000-00	5000	KEYSTONE	N/A	TEST POINT; PIN DIA=0.1IN; TOTAL LENGTH=0.3IN; BOARD HOLE=0.04IN; RED; PHOSPHOR BRONZE WIRE SILVER PLATE FINISH; RECOMMENDED FOR BOARD THICKNESS=0.062IN; NOT FOR COLD TEST
21	3	TP2, TP5, TP6	Pref	02-TPMINI5001-00	5001	KEYSTONE	N/A	TEST POINT; PIN DIA=0.1IN; TOTAL LENGTH=0.3IN; BOARD HOLE=0.04IN; BLACK; PHOSPHOR BRONZE WIRE SILVER PLATE FINISH; RECOMMENDED FOR BOARD THICKNESS=0.062IN; NOT FOR COLD TEST

MAX11261 EV Kit Bill of Materials (continued)

22	1	TP4	Pref	02-TPMINI5004-00	5004	KEYSTONE	N/A	TEST POINT; PIN DIA=0.1IN; TOTAL LENGTH=0.3IN; BOARD HOLE=0.04IN; YELLOW; PHOSPHOR BRONZE WIRE SILVER PLATE FINISH; RECOMMENDED FOR BOARD THICKNESS=0.062IN; NOT FOR COLD TEST
23	1	U1	Pref	00-SAMPLE-01	MAX11261ENX+	MAXIM	MAX11261ENX+	EVKIT PART - IC; MAX11261ENX+; 6-CHANNEL; 24-BIT; DELTA-SIGMA ADC; PACKAGE OUTLINE DRAWING: 21-0742; PACKAGE CODE: N362B2+2
24	1	U2	Pref	10-MAX8510EXK30-X	MAX8510EXK30+	MAXIM	MAX8510EXK30+	IC; VREG; ULTRA-LOW-NOISE; HIGH PSRR; LOW-DROPOUT; 0.12A LINEAR REGULATOR; SC70-5
25	1	U3	Pref	10-MAX6071AAUT25-U	MAX6071AAUT25+	MAXIM	MAX6071AAUT25+	IC; VREF; LOW NOISE; HIGH-PRECISION SERIES VOLTAGE REFERENCE; SOT23-6
26	1	U4	Pref	10-MAX6071AAUT12-U	MAX6071AAUT12+	MAXIM	MAX6071AAUT12+	IC; VREF; LOW-NOISE; HIGH-PRECISION SERIES VOLTAGE REFERENCE; SOT23-6
27	1	PCB	-	N/A	MAX11261PMB_APPS_A	MAXIM	PCB	PCB:MAX11261PMB_APPS_A
TOTAL	94							

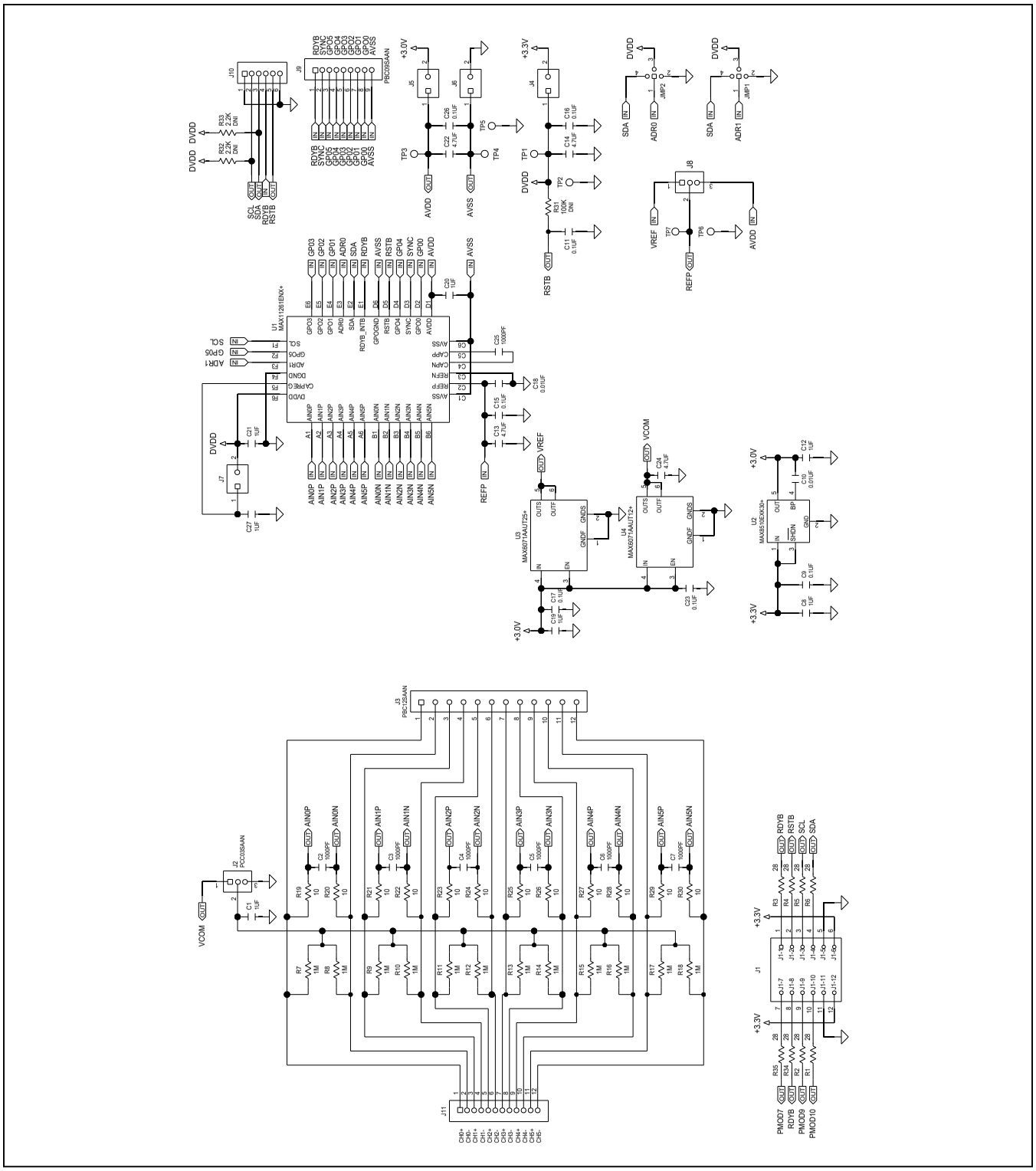
DO NOT PURCHASE(DNP)

ITEM	QTY	REF DES	Var Status	MAXINV	MFG PART #	MFG	VALUE	DESCRIPTION
TOTAL	0							

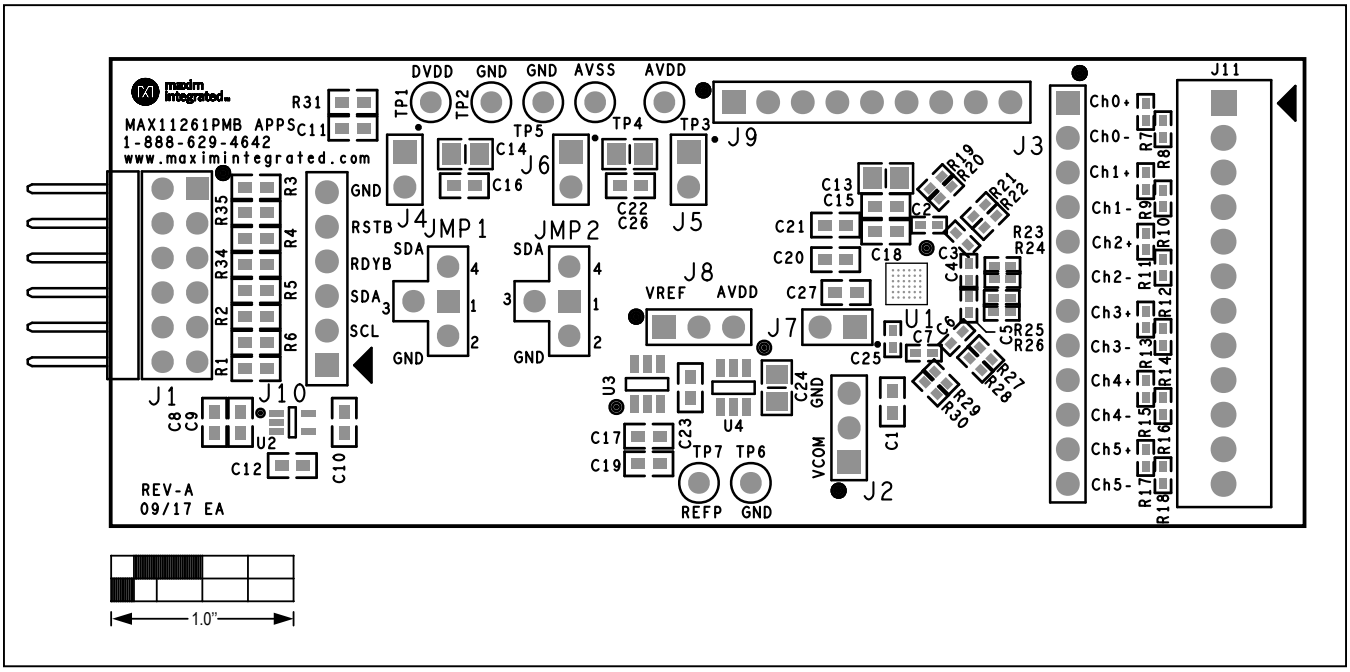
PACKOUT (These are purchased parts but not assembled on PCB and will be shipped with PCB)

ITEM	QTY	REF DES	Var Status	MAXINV	MFG PART #	MANUFACTURER	VALUE	DESCRIPTION
1	1	PACKOUT_BOX	Pref	88-00711-SML	88-00711-SML	N/A	N/A	BOX;SMALL BROWN 9 3/16X7X1 1/4 - PACKOUT
2	1	PACKOUT_BOX	Pref	87-02162-00	87-02162-00	N/A	N/A	ESD BAG;BAG;STATIC SHIELD ZIP 4inX6in;W/ESD LOGO - PACKOUT
3	1	PACKOUT_BOX	Pref	85-MAXKIT-PNK	85-MAXKIT-PNK	N/A	N/A	PINK FOAM;FOAM;ANTI-STATIC PE 12inX12inX5MM - PACKOUT
4	1	PACKOUT_BOX	Pref	EVINSERT	EVINSERT	N/A	N/A	WEB INSTRUCTIONS FOR MAXIM DATA SHEET
5	1	PACKOUT_BOX	Pref	85-84003-006	85-84003-006	N/A	N/A	LABEL(EV KIT BOX) - PACKOUT
TOTAL	5							

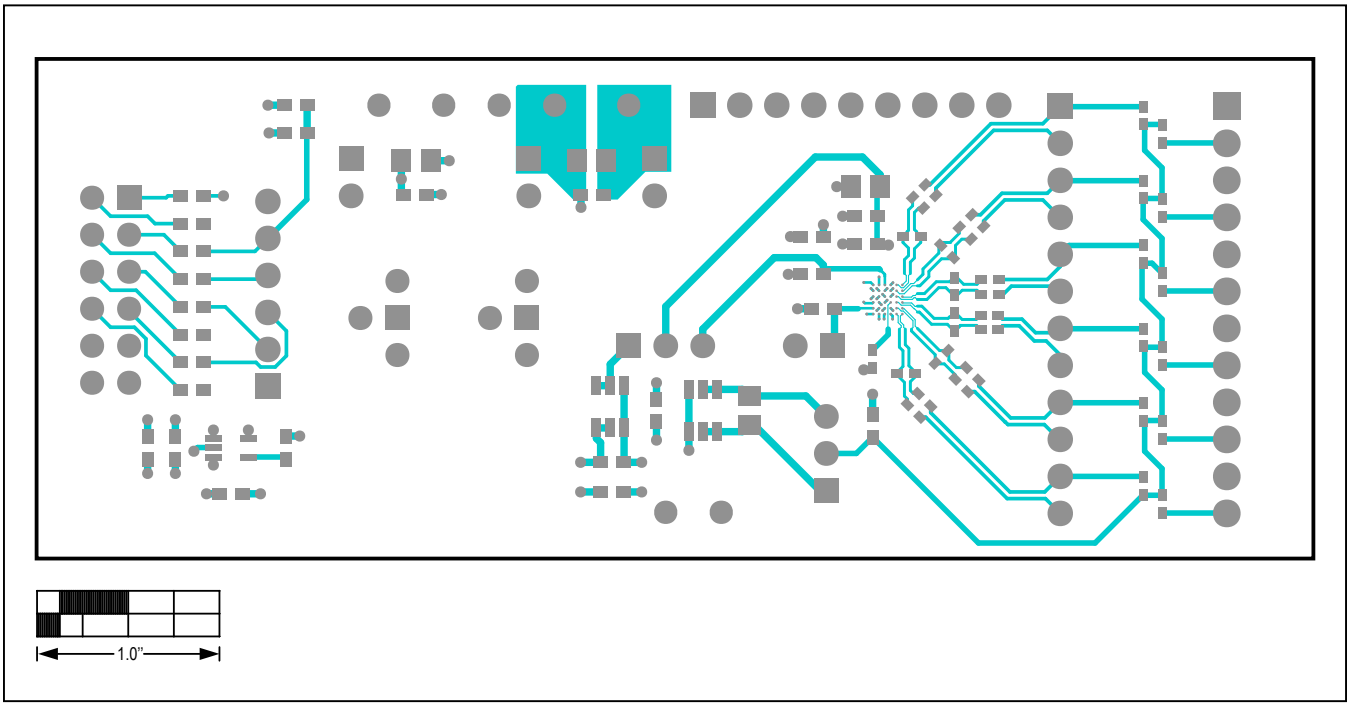
MAX11261 EV Kit Schematic



MAX11261 EV Kit PCB Layout Diagrams

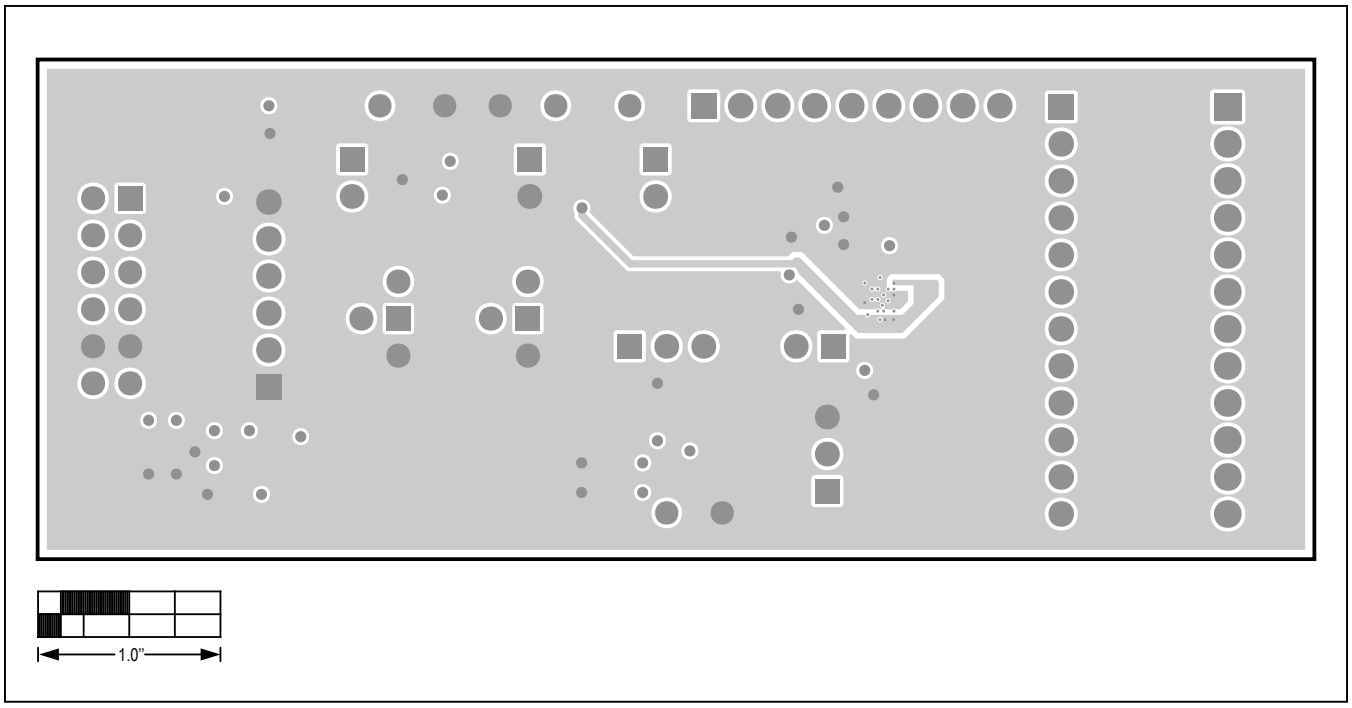


MAX11261 EV PCB Top Silkscreen

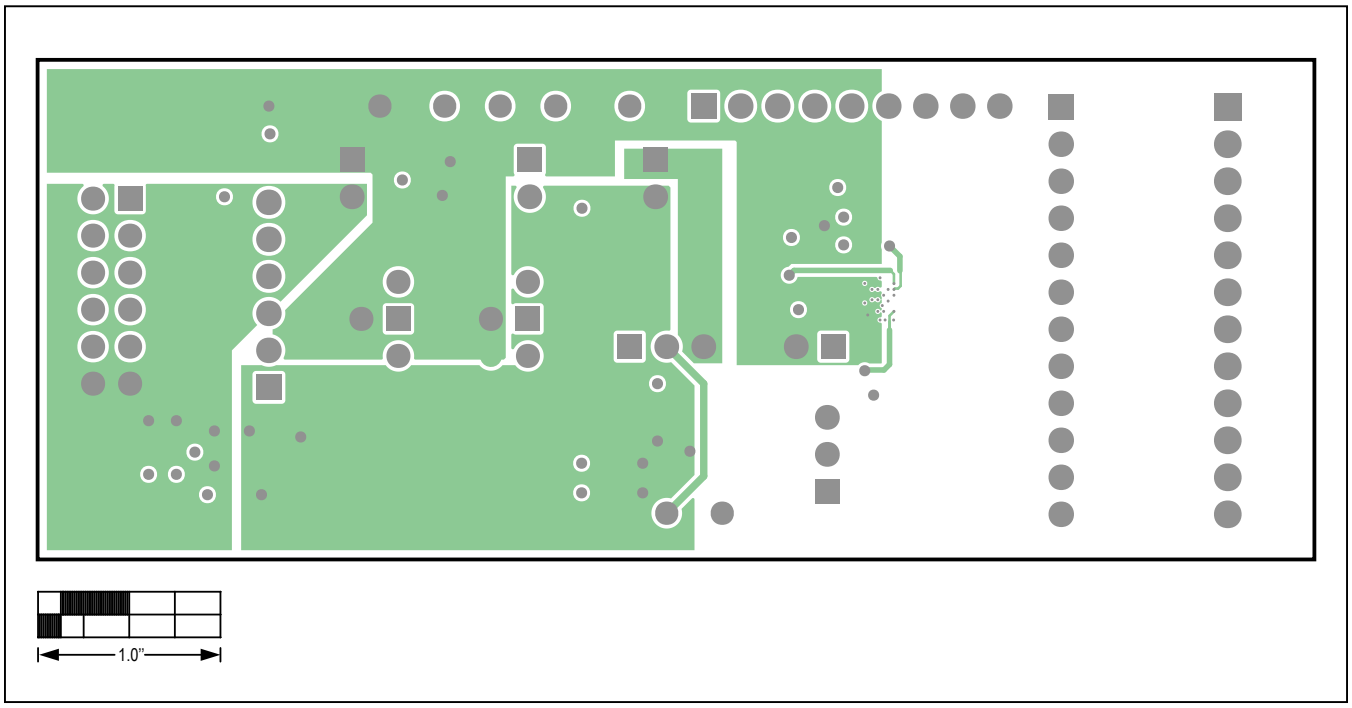


MAX11261EV PCB Top Layer

MAX11261 EV Kit PCB Layout Diagrams (continued)

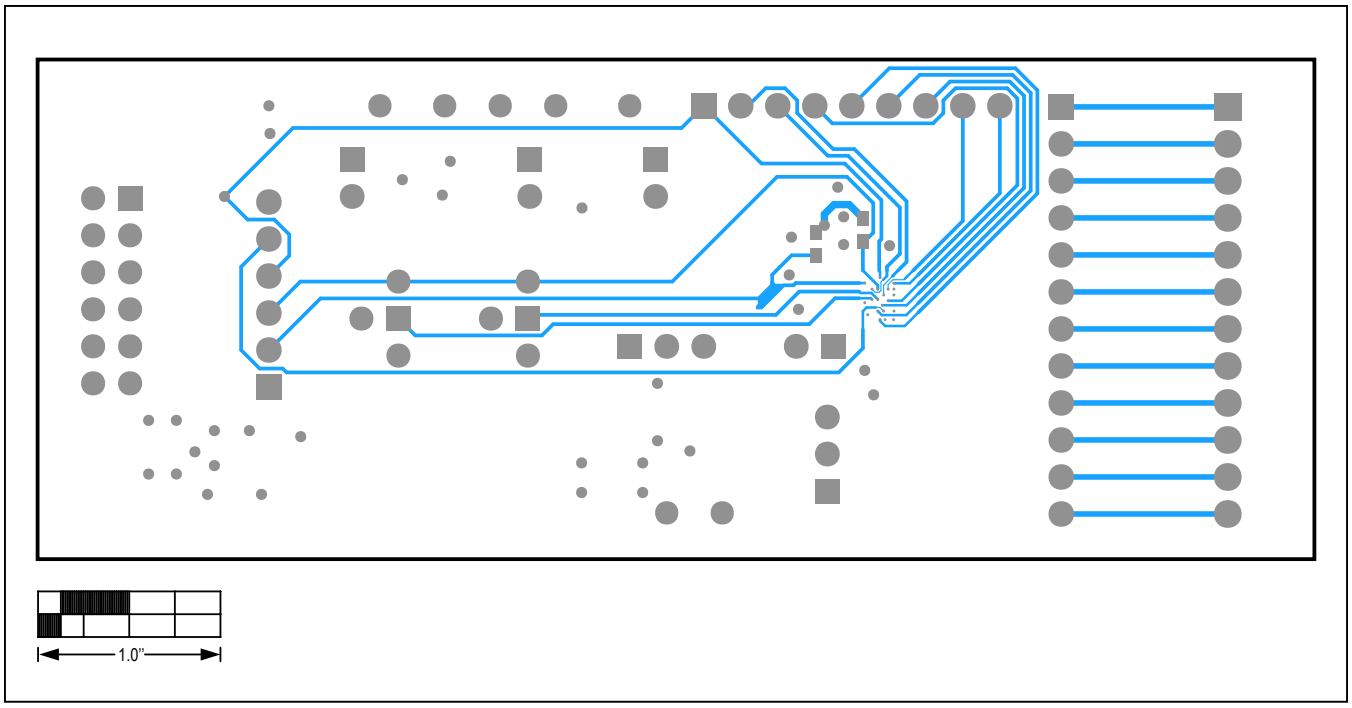


MAX11261EV PCB Layer 2

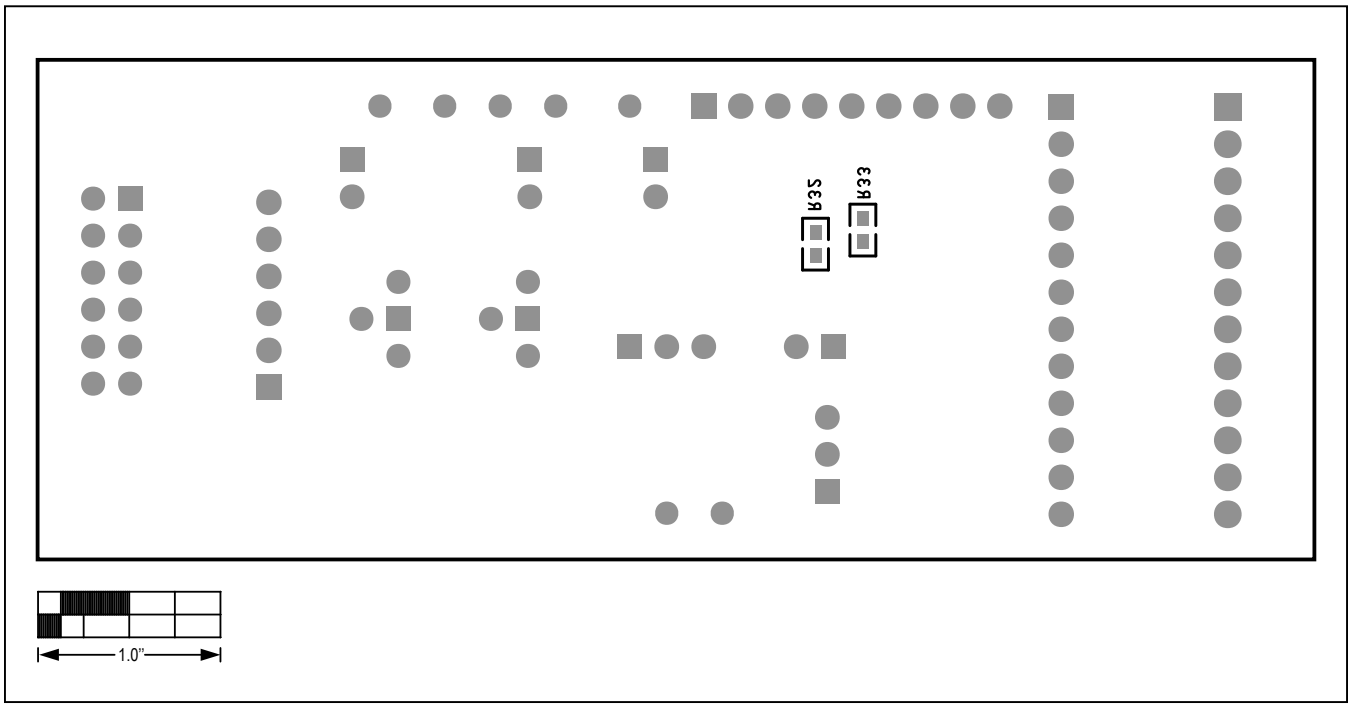


MAX11261EV PCB Layer 3

MAX11261 EV Kit PCB Layout Diagrams (continued)



MAX11261EV PCB Layer 2



MAX11261EV PCB Bottom Silkscreen

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	3/18	Initial release	—

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