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MAX11311

PIXI, 12-Port Programmable Mixed-Signal I/O with 12-Bit ADC, 12-Bit DAC, Analog Switches, and GPIO

General Description

The MAX11311 integrates a PIXI™, 12-bit, multichannel, analog-to-digital converter (ADC) and a 12-bit, multichannel, buffered digital-to-analog converter (DAC) in a single integrated circuit. This device offers 12 mixed-signal high-voltage, bipolar ports, which are configurable as an ADC analog input, a DAC analog output, a general-purpose input (GPI), a general-purpose output (GPO), or an analog switch terminal. One internal and two external temperature sensors track junction and environmental temperature. Adjacent pairs of ports are configurable as a logic-level translator for open-drain devices or an analog switch.

PIXI ports provide highly flexible hardware configuration for 12-bit mixed-signal applications. The MAX11311 is best suited for applications that demand a mixture of analog and digital functions. Each port is individually configurable with up to four selectable voltage ranges within -10V to +10V.

The MAX11311 allows for the averaging of 2, 4, 8, 16, 32, 64, or 128 ADC samples from each ADC-configured port to improve noise performance. A DAC-configured output port can drive up to 25mA. The GPIO ports can be programmed to user-defined logic levels, and a GPI coupled with a GPO forms a logic-level translator.

Internal and external temperature measurements monitor programmable conditions of minimum and maximum temperature limits, using the interrupt to notify the host if one or more conditions occur. The temperature measurement results are made available through the serial interface.

The MAX11311 features an internal, low-noise 2.5V voltage reference and provides the option to use external voltage references with separate inputs for the DAC and ADC. The device uses a 4-wire, 20MHz, SPI-compatible serial interface, operating from a 5V analog supply and a 1.8V to 5.0V digital supply. The PIXI port supply voltages operate from a wide range of -12.0V to +12.0V.

The MAX11311 is available in a 32-pin TQFN, 5mm x 5mm package or a 48-pin TQFP, 7mm x 7mm package specified over the -40°C to +105°C temperature range.

Applications

- Base Station RF Power Device Bias Controllers
- System Supervision and Control
- Power-Supply Monitoring
- Industrial Control and Automation
- Control for Optical Components

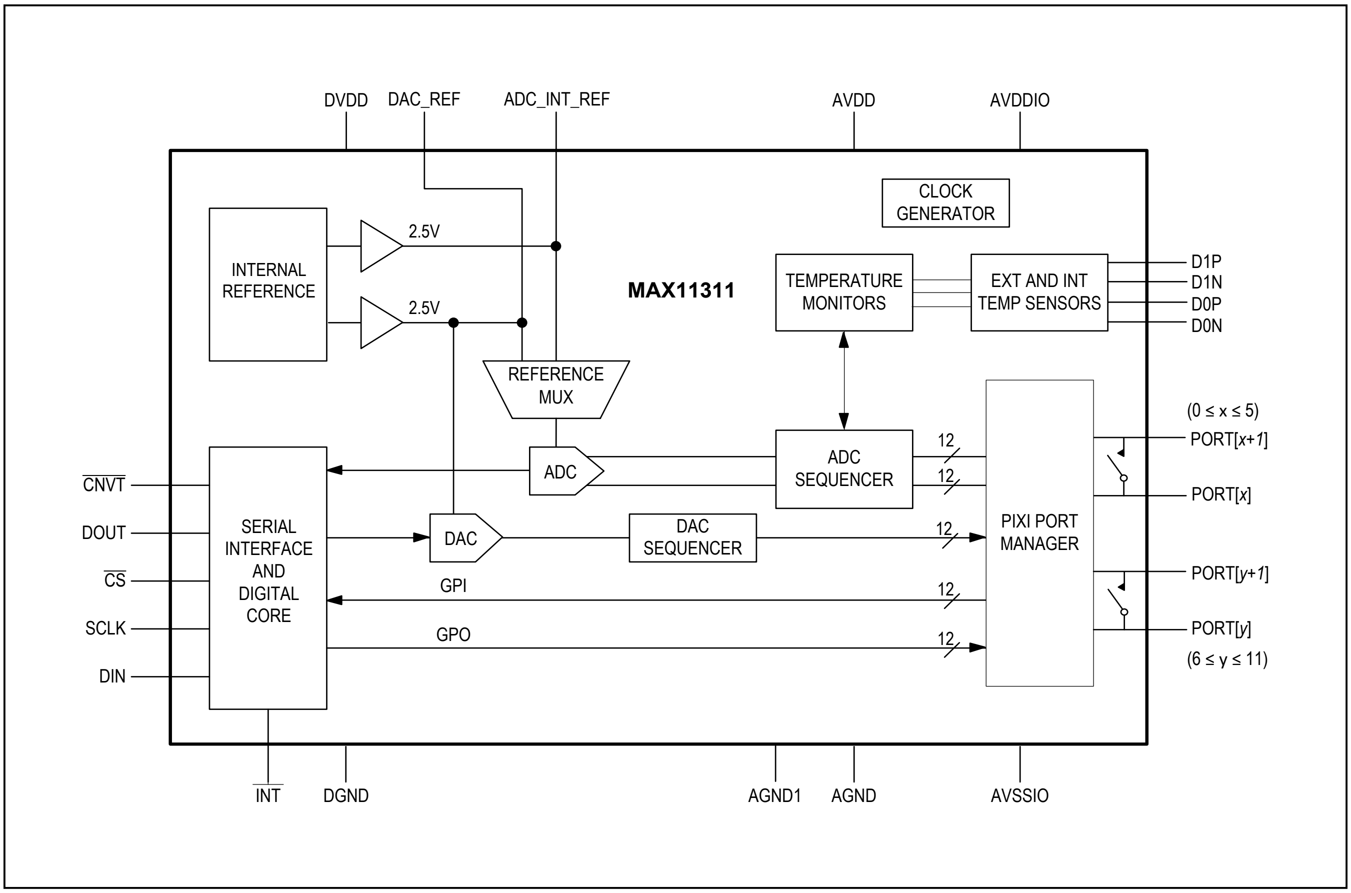
Benefits and Features

- 12 Configurable Mixed-Signal Ports Maximize Design Flexibility Across Platforms
  - Up to 12 12-Bit ADC Inputs
    - Single-Ended, Differential, or Pseudo-Differential Range Options: 0 to 2.5V, ±5V, 0 to +10V, -10V to 0V
    - Programmable Sample Averaging Per ADC Port
    - Unique Voltage Reference for Each ADC PIXI Port
  - Up to 12 12-Bit DAC Outputs
    - Range Options: ±5V, 0 to +10V, -10V to 0V
    - 25mA Current Drive Capability with Overcurrent Protection
  - Up to 12 General-Purpose Digital I/Os
    - 0 to +5V GPI Input Range
    - 0 to +2.5V GPI Programmable Threshold Range
    - 0 to +10V GPO Programmable Output Range
    - Logic-Level Shifting Between Any Two Pins
  - 60Ω Analog Switch Between Adjacent PIXI Ports
  - Internal/External Temperature Sensors, ±1°C Accuracy
- Adapts to Specific Application Requirements and Allows for Easy Reconfiguration as System Needs Change
- Configurability of Functions Enables Optimized PCB Layout
- Reduces BOM Cost with Fewer Components in Small Footprint
  - 25mm^2 32-Pin TQFN

Ordering Information ***appears at end of data sheet.***

19-8455; Rev 0; 12/15

Functional Diagram



Absolute Maximum Ratings

DVDD to DGND..-0.3V to +6V
AVDD to AGND ....-0.3V to +6V
AVDDIO to AVSSIO ....-0.3V to +25V
AVDDIO to AGND..-0.3V to +17V
AVSSIO to AGND ....-14V to +0.3V
AGND to AGND1 ....-0.3V to +0.3V
AGND to DGND ....-0.3V to +0.3V
AGND1 to DGND ....-0.3V to +0.3V
(PORT0 to PORT11) to AGND ....max of (V_{AVSSIO} - 0.3V) or -14V to min of (V_{AVDDIO} + 0.3V) or +17V
(PORT0 to PORT11) to AGND (GPI and Bidirectional Level Translator Modes).....-0.3V to the min of (V_{AVDD} + 0.3V) or +6V
($\overline{CNVT}$, DOUT) to DGND... -0.3V to the min of (V_{DVDD} + 0.3V) or +6V
($\overline{CS}$, SCLK, DIN, $\overline{INT}$) to DGND.............................-0.3V to +6V
DAC and ADC Reference Pins to AGND (DAC_REF, ADC_INT_REF).. -0.3V to the min of (V_{AVDD} + 0.3V) or +4V
Temperature Sensor Pins (D0N, D0P, D1N, D1P) to AGND.................... -0.3V to the min of (V_{AVDD} + 0.3V) or +6V
Current into Any PORT Pin 100mA
Current into Any Other Pin Except Supplies and Ground 50mA
Continuous Power Dissipation (T_A = +70°C) (Multilayer board)
TQFN (derate 34.5mW/°C above +70°C) 2758.6mW
Operating Temperature Range......................... -40°C to +105°C
Storage Temperature Range .... -65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C
Soldering Temperature (reflow) ....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

TQFN
Junction-to-Case Thermal Resistance (θ_{JC}).............1.7°C/W
Junction-to-Ambient Thermal Resistance (θ_{JA}) ....29°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Electrical Characteristics

ADC Electrical Specifications

(V_{AVDD} = 4.75V to 5.25V, V_{DVDD} = 3.3V, V_{AVDDIO} = +12.0V, V_{AGND} = V_{DGND} = 0V, V_{AVSSIO} = -2.0V, V_{DACREF} = 2.5V, V_{ADCREF} = 2.5V (Internal), f_S = 400ksps, 10V analog input range set to range 1 (0 to +10V). T_A = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY (Note 3)						
Resolution			12			Bits
Integral Nonlinearity	INL				±2.5	LSB
Differential Nonlinearity	DNL	No missing codes over temperature			±1	LSB
Offset Error				±0.5	±8	LSB
Offset Error Drift				±0.002		LSB/ºC
Gain Error					±11	LSB
Gain Error Drift				±0.01		LSB/ºC
Channel-to-Channel Offset Matching				1		LSB
Channel-to-Channel Gain Matching				2		LSB

Electrical Characteristics (continued)

ADC Electrical Specifications

(V_{AVDD} = 4.75V to 5.25V, V_{DVDD} = 3.3V, V_{AVDDIO} = +12.0V, V_{AGND} = V_{DGND} = 0V, V_{AVSSIO} = -2.0V, V_{DACREF} = 2.5V, V_{ADCREF} = 2.5V (Internal), f_S = 400ksps, 10V analog input range set to range 1 (0 to +10V). T_A = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DYNAMIC PERFORMANCE (Single-Ended Inputs)						
Signal-to-Noise Plus Distortion	SINAD	f_S = 400ksps, f_{IN} = 10kHz		70		dB
Signal to Noise	SNR	f_S = 400ksps, f_{IN} = 10kHz		71		dB
Total Harmonic Distortion	THD	f_S = 400ksps, f_{IN} = 10kHz		-75		dB
Spurious-Free Dynamic Range	SFDR	f_S = 400ksps, f_{IN} = 10kHz		75		dB
Crosstalk		f_S = 100ksps, f_{IN} = 10kHz		-85		dB
DYNAMIC PERFORMANCE (Differential Inputs)						
Signal-to-Noise Plus Distortion	SINAD	f_S = 400ksps, f_{IN} = 10kHz		71		dB
Signal to Noise	SNR	f_S = 400ksps, f_{IN} = 10kHz		72		dB
Total Harmonic Distortion	THD	f_S = 400ksps, f_{IN} = 10kHz		-82		dB
Spurious-Free Dynamic Range	SFDR	f_S = 400ksps, f_{IN} = 10kHz		82		dB
Crosstalk		f_S = 100ksps, f_{IN} = 10kHz		-85		dB
CONVERSION RATE						
Throughput (Note 4)		ADCCONV[1:0] = 00		200		ksps
		ADCCONV[1:0] = 01		250		
		ADCCONV[1:0] = 10		333		
		ADCCONV[1:0] = 11		400		
Acquisition Time	t_{ACQ}	ADCCONV[1:0] = 00		3.5		µs
		ADCCONV[1:0] = 01		2.5		
		ADCCONV[1:0] = 10		1.5		
		ADCCONV[1:0] = 11		1.0		
ANALOG INPUT (All Ports)						
Absolute Input Voltage (Note 5)	V_{PORT}	Range 1	0		10	V
		Range 2	-5		+5	
		Range 3	-10		0	
		Range 4	0		2.5	
Input Resistance		Range 1, 2, 3	70	100	130	kΩ
		Range 4	50	75	100	kΩ

REF Electrical Specifications

(V_{AVDD} = 4.75V to 5.25V, V_{DVDD} = 3.3V, V_{AVDDIO} = +12.0V, V_{AGND} = V_{DGND} = 0V, V_{AVSSIO} = -2.0V, V_{DACREF} = 2.5V, V_{ADCREF} = 2.5V (Internal), f_S = 400ksps, 10V analog input range set to range 1 (0 to +10V). T_A = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ADC INTERNAL REFERENCE						
Reference Output Voltage		Internal references at T_A = +25°C	2.494	2.5	2.506	V
REF Output Tempco (Note 6)	$T_{C\text{-}VREF}$			±10	±25	ppm/°C
Capacitor Bypass at ADC_INT_REF			4.7		10	μF
DAC INTERNAL REFERENCE						
Reference Output Voltage		Internal references at T_A = +25°C	2.494	2.5	2.506	V
REF Output Tempco (Note 6)	$T_{C\text{-}VREF}$			±10	±25	ppm/°C
Capacitor Bypass at DAC_REF			4.7		10	μF
DAC EXTERNAL REFERENCE						
Reference Input Range			1.25		2.5	V

GPIO Electrical Specifications

(V_{AVDD} = 5.0V, V_{DVDD} = 3.3V, V_{AVDDIO} = +12.0V, V_{AGND} = V_{DGND} = 0V, V_{AVSSIO} = -2.0V, V_{DACREF} = 2.5V, V_{ADCREF} = 2.5V (Internal), f_S = 400ksps, 10V analog input range set to range 1 (0 to +10V). T_A = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
GPIO EXCEPT IN BIDIRECTIONAL LEVEL TRANSLATION MODE						
Programmable Input Logic Threshold	V_{ITH}		0.3		V_{DACREF}	V
Input High Voltage	V_{IH}		V_{ITH} + 0.3			V
Input Low Voltage	V_{IL}				V_{ITH} - 0.3	V
Hysteresis				±30		mV
Programmable Output Logic Level	V_{OLVL}		0		4 x V_{DACREF}	V
Propagation Delay from GPI Input to GPO Output in Unidirectional Level Translating Mode		Midscale threshold, 5V logic swing		2		μs
BIDIRECTIONAL LEVEL TRANSLATION PATH AND ANALOG SWITCH						
Input High Voltage	V_{IH}		1			V
Input Low Voltage	V_{IL}				0.2	V
On-Resistance		From V_{AVSSIO} +2.50V to V_{AVDDIO} - 2.50V			60	Ω

GPIO Electrical Specifications (continued)

(V_{AVDD} = 4.75V to 5.25V, V_{DVDD} = 3.3V, V_{AVDDIO} = +12.0V, V_{AGND} = V_{DGND} = 0V, V_{AVSSIO} = -2.0V, V_{DACREF} = 2.5V, V_{ADCREF} = 2.5V (Internal), f_S = 400ksps, 10V analog input range set to range 1 (0 to +10V). T_A = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay		10kΩ pullup resistors to rail in each side. Midvoltage to midvoltage when driving side goes from high to low			1	µs
ANALOG SWITCH						
Turn-On Delay		(Note 7)			400	ns
Turn-Off Delay		(Note 7)			400	ns
On-Time Duration		(Note 7)	1			µs
Off Time Duration		(Note 7)	1			µs
On-Resistance		From V_{AVSSIO} +2.50V to V_{AVDDIO} - 2.50V			60	Ω

DAC Electrical Specifications

(V_{AVDD} = 4.75V to 5.25V, V_{DVDD} = 3.3V, V_{AVDDIO} = +12.0V, V_{AGND} = V_{DGND} = 0V, V_{AVSSIO} = -2.0V, V_{DACREF} = 2.5V, V_{ADCREF} = 2.5V (Internal), f_S = 400ksps, 10V analog input range set to range 1 (0 to +10V). T_A = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY						
Resolution	N		12			Bits
Output Range (Note 5)	V_{PORT}	Range 1	0		+10	V
		Range 2	-5		+5	
		Range 3	-10		0	
Integral Linearity Error	INL	From code 100 to code 3996		±0.5	±1.5	LSB
Differential Linearity Error	DNL			±0.5	±1	LSB
Offset Voltage		At code 100			±20	LSB
Offset Voltage Tempco				15		ppm/°C
Gain Error		From code 100 to code 3996	-0.6		+0.6	% of FS
Gain Error Tempco		From code 100 to code 3996		4		ppm of FS/°C
Power-Supply Rejection Ratio	PSRR			0.4		mV/V
DYNAMIC CHARACTERISTICS						
Output Voltage Slew Rate	SR			1.6		V/µs
Output Settling Time		To ±1 LSB, from 0 to full scale, output load capacitance of 250pF (Note 7)		40		µs
Settling Time After Current-Limit Condition				6		µs
Noise		f = 0.1Hz to 300kHz		3.8		mV_{P-P}

DAC Electrical Specifications (continued)

(V_{AVDD} = 4.75V to 5.25V, V_{DVDD} = 3.3V, V_{AVDDIO} = +12.0V, V_{AGND} = V_{DGND} = 0V, V_{AVSSIO} = -2.0V, V_{DACREF} = 2.5V, V_{ADCREF} = 2.5V (Internal), f_S = 400ksps, 10V analog input range set to range 1 (0 to +10V). T_A = -40ºC to +105ºC, unless otherwise noted. Typical values are at T_A = +25ºC.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TRACK-AND-HOLD						
Digital Feedthrough				5		nV·s
Hold Step		(Note 6)		1	6	mV
Droop Rate		(Note 6)		0.3	15	mV/s

Interface Digital IO Electrical Specifications

(V_{AVDD} = 5.0V, V_{DVDD} = 1.62V to 5.50V, V_{AVDDIO} = +12.0V, V_{AGND} = V_{DGND} = 0V, V_{AVSSIO} = -2.0V, V_{DACREF} = 2.5V, V_{ADCREF} = 2.5V (Internal), f_S = 400ksps, 10V analog input range set to range 1 (0 to +10V). T_A = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SPI IO DC SPECIFICATION						
Input High Voltage (DIN, SCLK, $\overline{CS}$, $\overline{CNVT}$)		V_{DVDD} = 2.50V to 5.50V	0.7 x V_{DVDD}			V
		V_{DVDD} = 1.62V to 2.50V	0.85 x V_{DVDD}			V
Input Low Voltage (DIN, SCLK, $\overline{CS}$, $\overline{CNVT}$)		V_{DVDD} = 2.50V to 5.50V			0.3 x V_{DVDD}	V
		V_{DVDD} = 1.62V to 2.50V			0.15 x V_{DVDD}	V
Input Leakage Current (DIN, SCLK, $\overline{CS}$, $\overline{CNVT}$, $\overline{INT}$)		Input voltage at DVDD	-10		+10	µA
Input Capacitance (DIN, SCLK, $\overline{CS}$, $\overline{CNVT}$)				10		pF
Output High Voltage (DOUT)		I_{SRC} = 5mA, V_{DVDD} = 2.50V to 5.50V	V_{DVDD} - 0.5			V
		I_{SRC} = 2mA, V_{DVDD} = 1.62V to 2.50V	V_{DVDD} - 0.3			V
Output Low Voltage (DOUT, $\overline{INT}$)		I_{SNK} = 5mA, V_{DVDD} = 2.50V to 5.50V			0.4	V
		I_{SNK} = 2mA, V_{DVDD} = 1.62V to 2.50V			0.2	V
Output Leakage Current (DOUT)			-10		+10	µA

Interface Digital IO Electrical Specifications (continued)

(V_{AVDD} = 5.0V, V_{DVDD} = 1.62V to 5.50V, V_{AVDDIO} = +12.0V, V_{AGND} = V_{DGND} = 0V, V_{AVSSIO} = -2.0V, V_{DACREF} = 2.5V, V_{ADCREF} = 2.5V (Internal), f_S = 400ksps, 10V analog input range set to range 1 (0 to +10V). T_A = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SPI TIMING REQUIREMENTS (See Figures 1 and 2)						
SCLK Frequency	f_{SCLK}	V_{DVDD} = 2.50V to 5.50V			20	MHz
		V_{DVDD} = 1.62V to 2.50V			10	MHz
SCLK Clock Period	t_{CP}	V_{DVDD} = 2.50V to 5.50V	50			ns
		V_{DVDD} = 1.62V to 2.50V	100			ns
SCLK Pulse-Width High	t_{CH}		10			ns
SCLK Pulse-Width Low	t_{CL}	V_{DVDD} = 2.50V to 5.50V	25			ns
		V_{DVDD} = 1.62V to 2.50V	65			ns
$\overline{CS}$ Low to First SCLK Rise Setup	t_{CSS0}		5			ns
24th SCLK Rising Edge to $\overline{CS}$ Rising Edge	t_{CSS1}		5			ns
SCLK Rise to $\overline{CS}$ Low	t_{CSH0}		5			ns
$\overline{CS}$ Pulse-Width High	t_{CSW}		50			ns
DIN to SCLK Setup	t_{DS}		5			ns
DIN Hold After SCLK	t_{DH}		5			ns
DOUT Transition Valid After SCLK Fall	t_{DOT}	V_{DVDD} = 2.50V to 5.50V			23	ns
		V_{DVDD} = 1.62V to 2.50V			55	ns
$\overline{CS}$ Rise to DOUT Disable	t_{DOD}	C_{LOAD} = 20pF			50	ns

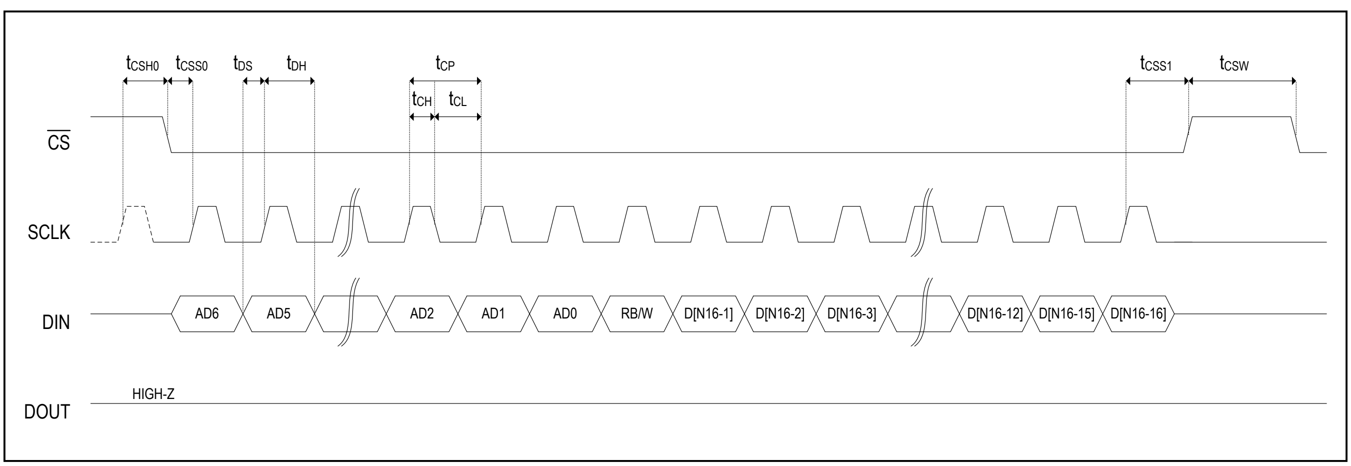


Figure 1. SPI Write Timing (N = Number of Words Written; N > 1 for Burst Mode)

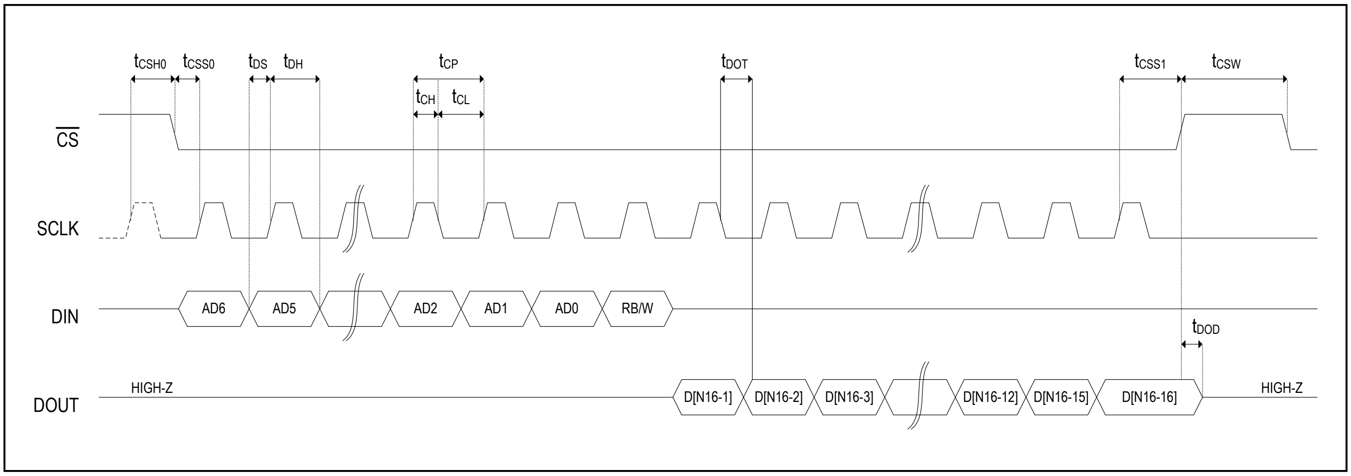


Figure 2. SPI Read Timing (N = Number of Words Written; N > 1 for Burst Mode)

Internal and External Temperature Sensor Specifications

(V_{AVDD} = 4.75V to 5.25V, V_{DVDD} = 3.3V, V_{AVDDIO} = +12.0V, V_{AGND} = V_{DGND} = 0V, V_{AVSSIO} = -2.0V, V_{DACREF} = 2.5V, V_{ADCREF} = 2.5V (Internal), f_S = 400ksps, 10V analog input range set to range 1 (0 to +10V). T_A = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ACCURACY						
Accuracy of Internal Sensor (Note 6,8)		0°C ≤ T_J ≤ +80°C		±0.3	±2.0	°C
		-40°C ≤ T_J ≤ +125°C		±0.7	±5	°C
Accuracy of External Sensor (Note 6,8)		0°C ≤ T_{RJ} ≤ +80°C		±0.3	±2.0	°C
		-40°C ≤ T_{RJ} ≤ +150°C		±1.0	±5	°C
Temperature Measurement Resolution				0.125		°C
External Sensor Junction Current	High			68		µA
	Low			4		µA
External Sensor Junction Current	High	Series resistance cancellation mode		136		µA
	Low	Series resistance cancellation mode		8		µA
Remote Junction Current Conversion Ratio				17		
D0N/D1N Voltage (Internally Generated)		Internally Generated		0.5		V

Power Supply Specifications

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{AVDD}			4.75		5.25	V
V_{DVDD}			1.62		5.50	V
V_{AVDDIO}			V_{AVDD}		15.75	V
V_{AVSSIO}			-12.0		0	V
V_{AVDDIO} to V_{AVSSIO}			V_{AVDD}		24	V
I_{AVDD}		All ports in high-impedance mode		14	18	mA
		LPEN = 1		11		mA
		All ports in ADC-related modes		17		mA
		All ports in DAC-related modes		18		mA
I_{DVDD}		Serial interface in idle mode			2	µA
I_{AVDDIO}		All ports in mode 0			150	µA
I_{AVSSIO}		All ports in mode 0	-400			µA

Recommended VDDIO/VSSIO Supply Selection

		ADC RANGE			
		-10V TO 0V	-5V TO +5V	0V TO +10V	0 TO 2.5V
DAC RANGE	-10V TO 0V	V_{AVDDIO} = +5V V_{AVSSIO} = -12V	V_{AVDDIO} = +5V V_{AVSSIO} = -12V	V_{AVDDIO} = +10V V_{AVSSIO} = -12V	V_{AVDDIO} = +5V V_{AVSSIO} = -12V
	-5V TO +5V	V_{AVDDIO} = +7V V_{AVSSIO} = -10V	V_{AVDDIO} = +7V V_{AVSSIO} = -7V	V_{AVDDIO} = +10V V_{AVSSIO} = -7V	V_{AVDDIO} = +7V V_{AVSSIO} = -7V
	0V TO +10V	V_{AVDDIO} = +12V V_{AVSSIO} = -10V	V_{AVDDIO} = +12V V_{AVSSIO} = -5V	V_{AVDDIO} = +12V V_{AVSSIO} = -2V	V_{AVDDIO} = +12V V_{AVSSIO} = -2V

The values of V_{AVDDIO} and V_{AVSSIO} supply voltages depend on the application circuit and the device configuration.

V_{AVDDIO} needs to be the maximum of those four values:

- If one or more ports are in mode 3, 4, 5, 6, or 10 (DAC-related modes), V_{AVDDIO} must be set, at minimum, to the value of the largest voltage driven by any of the ports set in those modes. For improved linearity, it is recommended to set V_{AVDDIO} 2.0V above the largest voltage value.
- If one or more ports are in mode 7, 8, or 9 (ADC-related modes), V_{AVDDIO} must be set, at minimum, to the value of the largest voltage applied to any of the ports set in those modes.
- If one or more ports are in mode 11 or 12 (Analog switch-related modes), V_{AVDDIO} must be set, at minimum, to 2.0V above the value of the largest voltage applied to any of the ports functioning as analog switch terminals.
- V_{AVDDIO} cannot be set lower than V_{AVDD}.

V_{AVSSIO} needs to be the minimum of those four values:

- If one or more ports are in mode 3, 4, 5, 6, or 10 (DAC-related modes), V_{AVSSIO} must be set, at maximum, to the value of the lowest voltage driven by any of the ports set in those modes. For improved linearity, it is recommended to set V_{AVSSIO} 2.0V below the lowest voltage value.
- If one or more ports are in mode 7, 8, or 9 (ADC-related modes), V_{AVSSIO} must be set, at maximum, to the value of the lowest voltage applied to any of the ports set in those modes.

Recommended VDDIO/VSSIO Supply Selection (continued)

- If one or more ports are in mode 11 or 12 (Analog Switch-related modes), V_{AVSSIO} must be set, at maximum, to 2.0V below the value of the lowest voltage applied to any of the ports functioning as analog switch terminals.
- V_{AVSSIO} cannot be set higher than V_{AGND}.

For example, the MAX11311 can operate with only one voltage supply of 5V (±5%) connected to AVDD, AVDDIO, and DVDD, and one ground of 0V connected to AGND, DGND, and AVSSIO. However, the level of performance presented in the electrical specifications requires the setting of the supplies connected to AVDDIO and AVSSIO as previously described.

Common PIXI Electrical Specifications

(V_{AVDD} = 4.75V to 5.25V, V_{DVDD} = 3.3V, V_{AVDDIO} = +12.0V, V_{AGND} = V_{DGND} = 0V, V_{AVSSIO} = -2.0V, V_{DACREF} = 2.5V, V_{ADCREF} = 2.5V (Internal), f_S = 400ksps, 10V analog input range set to range 1 (0 to +10V). T_A = -40°C to +105°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PIXI PORTS						
Input Capacitance		All PIXI ports		20		pF
Input Resistance		All PIXI input ports except ADC mode	50	75	100	kΩ
Startup Time		Between stable supplies and accessing registers			100	ms
HIGH-VOLTAGE OUTPUT DRIVER CHARACTERISTICS						
Maximum Output Capacitance					250	pF
Output Low Voltage, DAC Mode		Sinking 25mA, V_{AVSSIO} = 0V, AVDDIO = 10V			V_{AVSSIO} + 1.0	V
Output High Voltage, DAC Mode		Sourcing 25mA, V_{AVSSIO} = 0V, V_{AVDDIO} = 10V	V_{AVDDIO} - 1.5			V
Output Low Voltage, GPO Mode		Sinking 2mA, V_{AVSSIO} = 0V, V_{AVDDIO} = 10V			V_{AVSSIO} + 0.4	V
Output High Voltage, GPO Mode		Sourcing 2mA, V_{AVSSIO} = 0V, V_{AVDDIO} = 10V	V_{AVDDIO} – 0.4			V
Current Limit		Short to AVDDIO		75		mA
		Short to AVSSIO		75		mA

Note 2: Electrical specifications are production tested at T_A = +25°C. Specifications over the entire operating temperature range are guaranteed by design and characterization. Typical specifications are at T_A = +25°C.

Note 3: DC accuracy specifications are tested for single-ended ADC inputs only.

Note 4: The effective ADC sample rate for port X configured in mode 6, 7, or 8 is:
[ADC sample rate per ADCCONV]/(([number of ports in modes 6,7,8] + [1 if TMPSEL ≠ 000]) x [$2^{\text{\# OF SAMPLES for port X}}$])

Note 5: See the *Recommended VDDIO/VSSIO Supply Selection* table for each range. For ports in modes 6, 7, 8, or 9, the voltage applied to those ports must be within the limits of their selected input range, whether in single-ended or differential mode.

Note 6: Specification is guaranteed by design and characterization.

Note 7: Switch controlled by GPI-configured port. One switch terminal connected to 0V, the other terminal connected to 5V through a 5mA current source. Timing is measured at the 2.5V transition point. Turn-on and turn-off delays are measured from the edge of the control signal to the 2.5V transition point. Turn-on and turn-off durations are measured between control signal transitions.

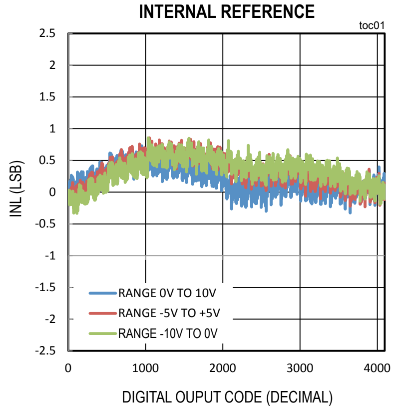
Note 8: In DAC-related modes, the rate, at which PIXI ports configured in mode 1, 3, 4, 5, 6, or 10 are refreshed, is as follows:
1/(40µs x [number of ports in modes 1, 3, 4, 5, 6, 10])

Note 9: Typical (TYP) values represent the errors at the extremes of the given temperature range.

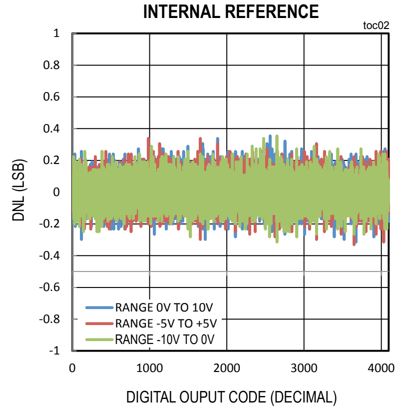
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

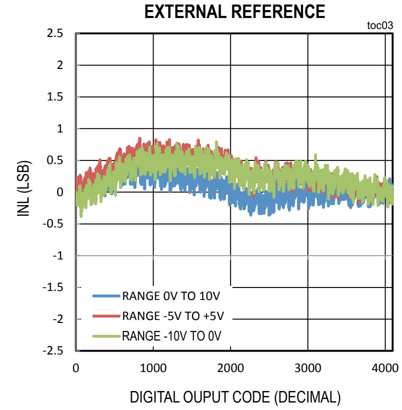
ADC INTEGRAL NONLINEARITY vs. DIGITAL OUTPUT CODE INTERNAL REFERENCE



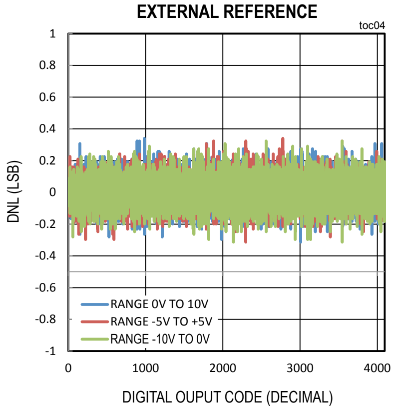
ADC DIFFERENTIAL NONLINEARITY vs. DIGITAL OUTPUT CODE INTERNAL REFERENCE



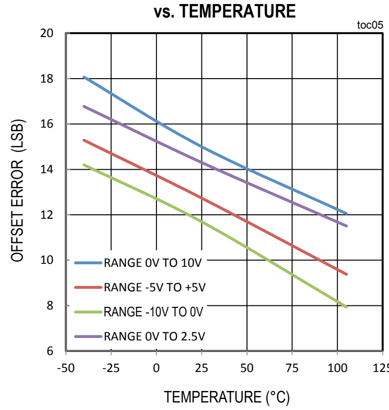
ADC INTEGRAL NONLINEARITY vs. DIGITAL OUTPUT CODE EXTERNAL REFERENCE



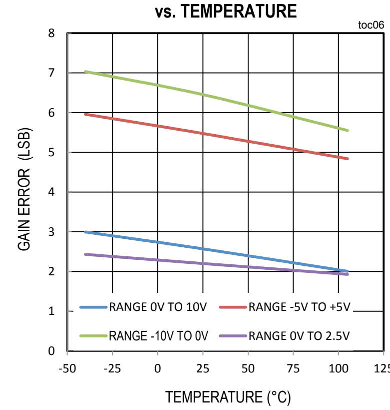
ADC DIFFERENTIAL NONLINEARITY vs. DIGITAL OUTPUT CODE EXTERNAL REFERENCE



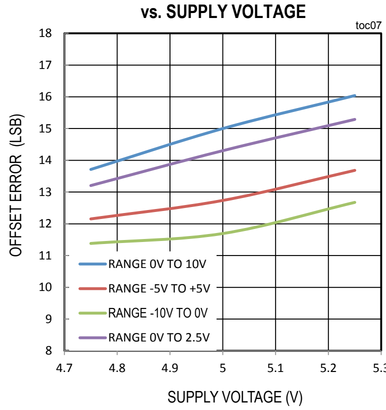
ADC OFFSET ERROR vs. TEMPERATURE



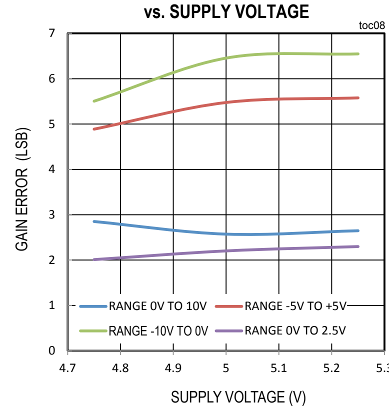
ADC GAIN ERROR vs. TEMPERATURE



ADC OFFSET ERROR vs. SUPPLY VOLTAGE



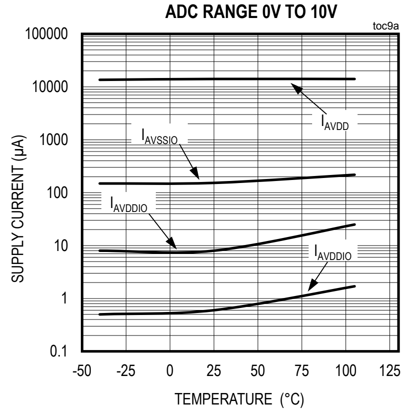
ADC GAIN ERROR vs. SUPPLY VOLTAGE



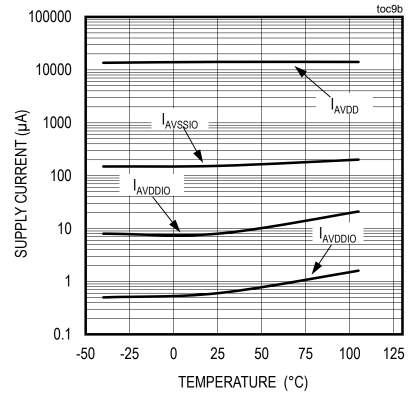
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

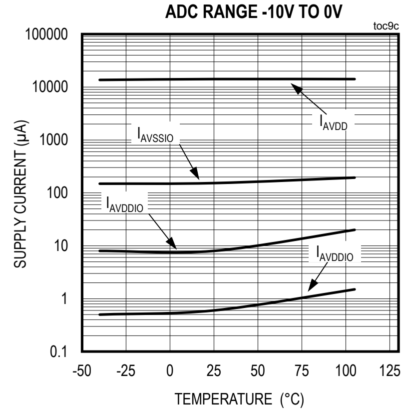
SUPPLY CURRENT
vs. TEMPERATURE
ADC RANGE 0V TO 10V



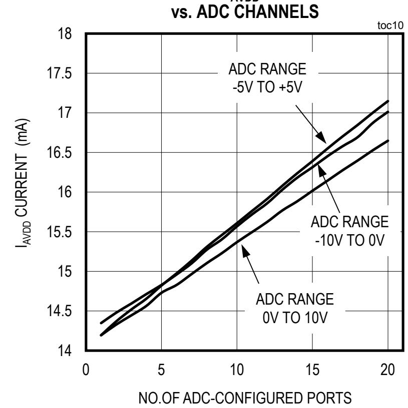
SUPPLY CURRENT
vs. TEMPERATURE
ADC RANGE -5V TO +5V



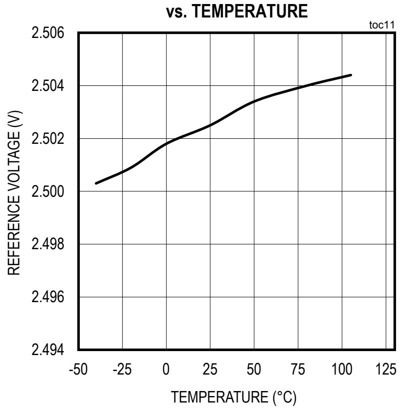
SUPPLY CURRENT
vs. TEMPERATURE
ADC RANGE -10V TO 0V



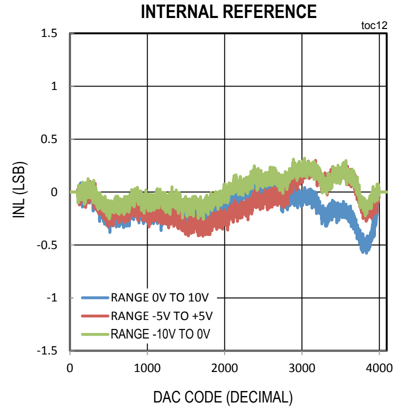
I_{AVDD}
vs. ADC CHANNELS



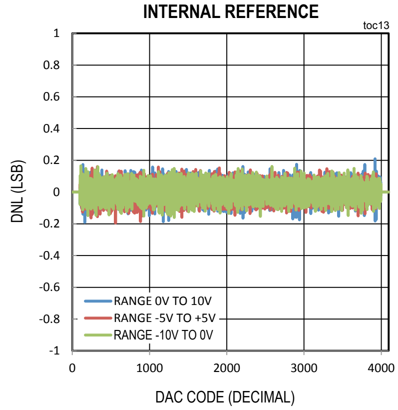
ADC INTERNAL REFERENCE
vs. TEMPERATURE



DAC INTEGRAL NONLINEARITY
vs. DIGITAL CODE
INTERNAL REFERENCE

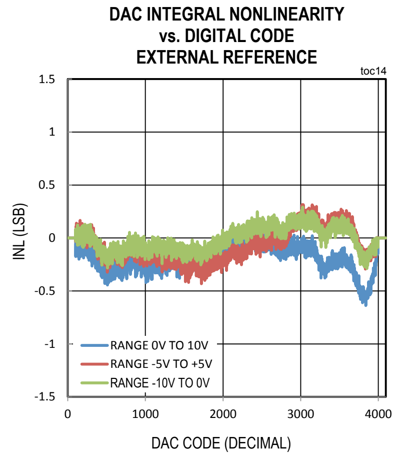


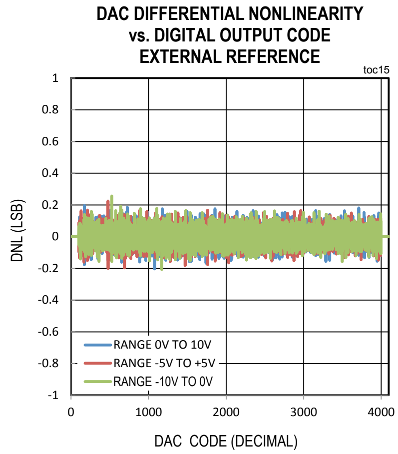
DAC DIFFERENTIAL NONLINEARITY
vs. DIGITAL OUTPUT CODE
INTERNAL REFERENCE

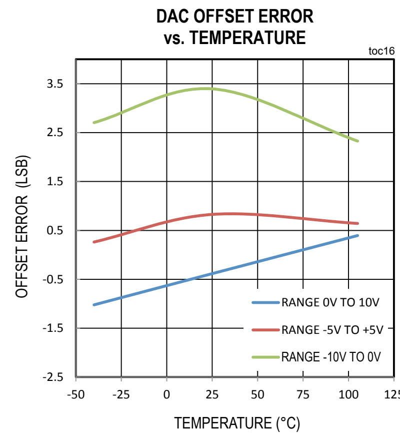


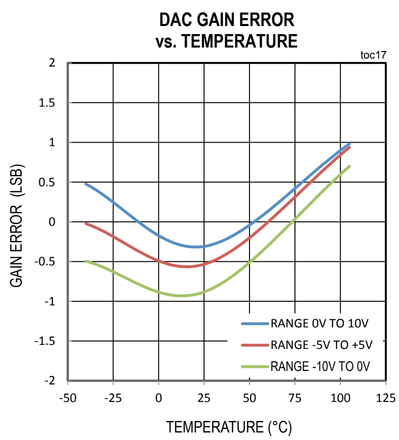
Typical Operating Characteristics (continued)

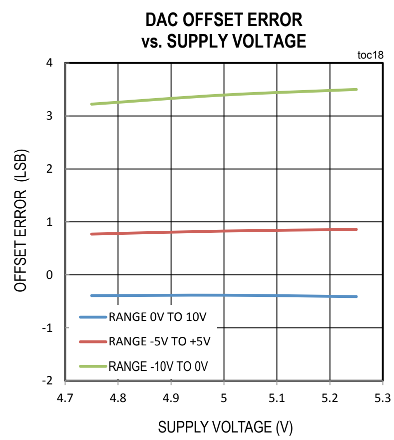
(T_A = +25°C, unless otherwise noted.)

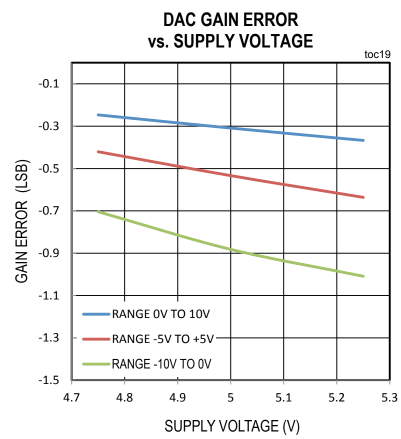


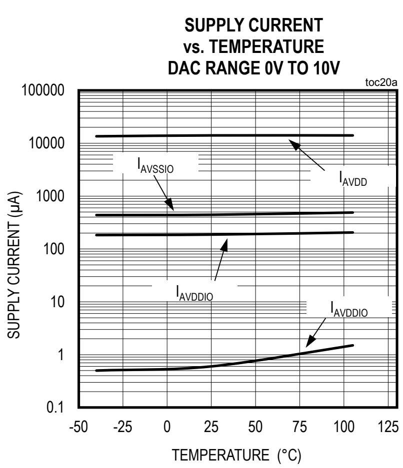


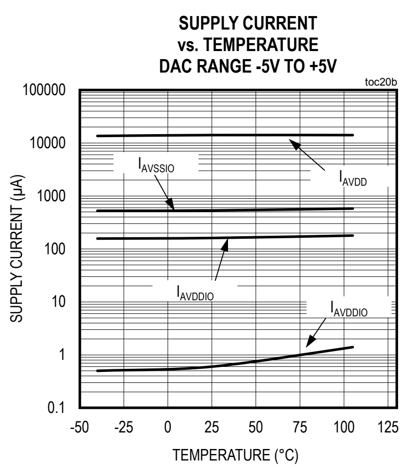


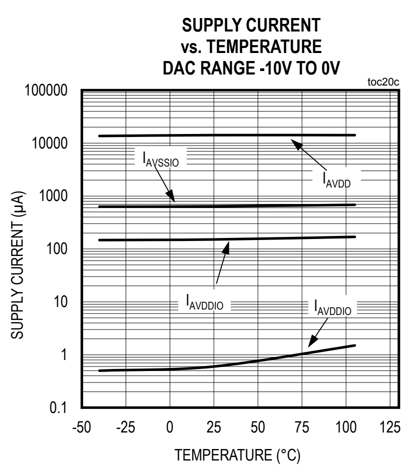








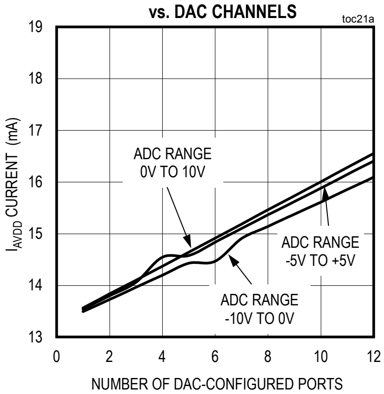




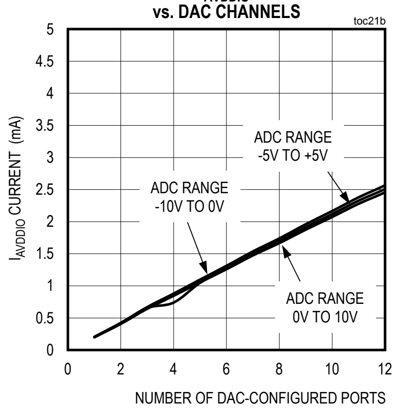
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

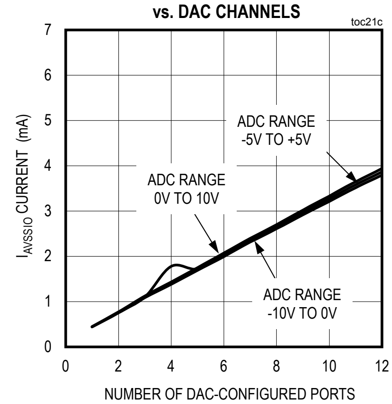
I_{AVDD} vs. DAC CHANNELS



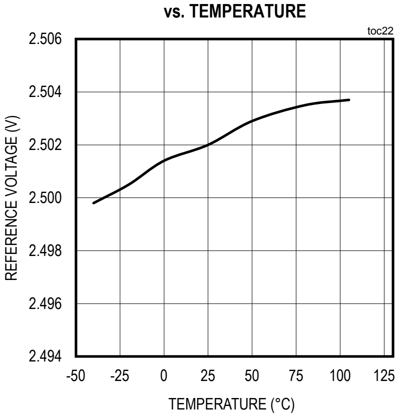
I_{AVDDIO} vs. DAC CHANNELS



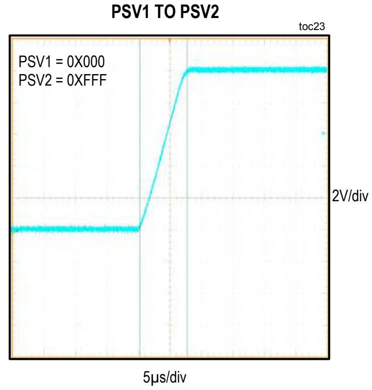
I_{AVSSIO} vs. DAC CHANNELS



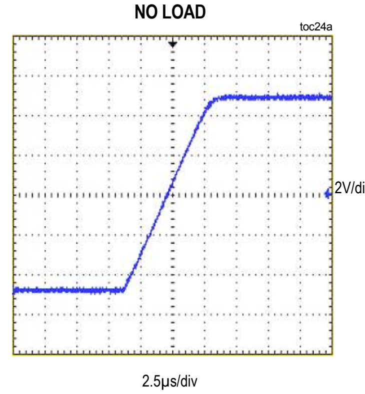
DAC INTERNAL REFERENCE vs. TEMPERATURE



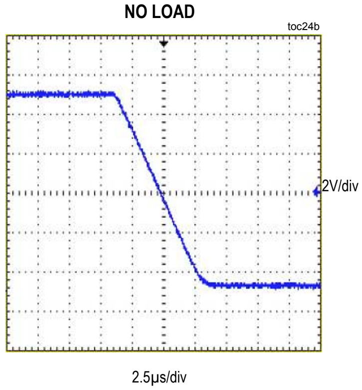
DAC SETTLING TIME CHANGE FROM PSV1 TO PSV2



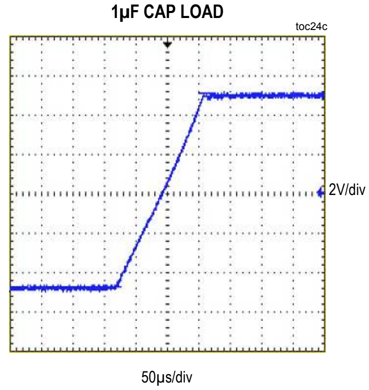
DAC SETTLING TIME CHANGE FROM MIN TO MAX NO LOAD



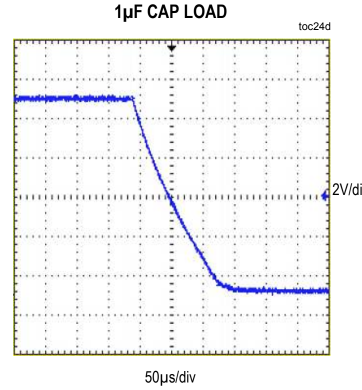
DAC SETTLING TIME CHANGE FROM MAX TO MIN NO LOAD



DAC SETTLING TIME CHANGE FROM MIN TO MAX 1μF CAP LOAD



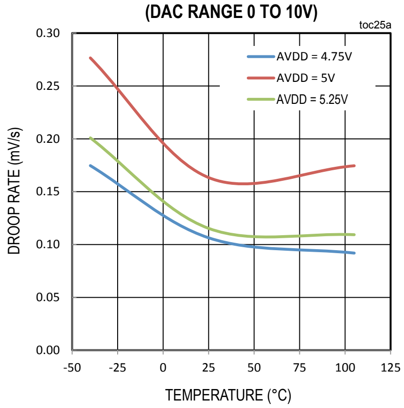
DAC SETTLING TIME CHANGE FROM MAX TO MIN 1μF CAP LOAD



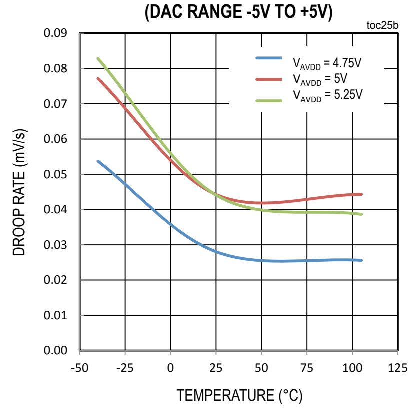
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

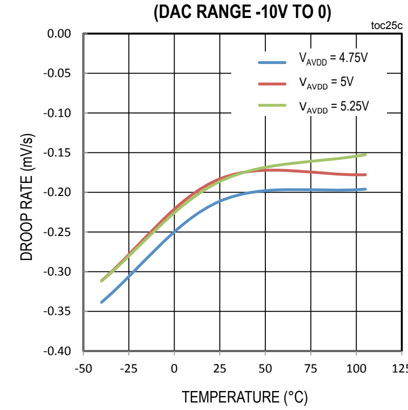
DAC DROOP RATE
vs. TEMPERATURE
(DAC RANGE 0 TO 10V)



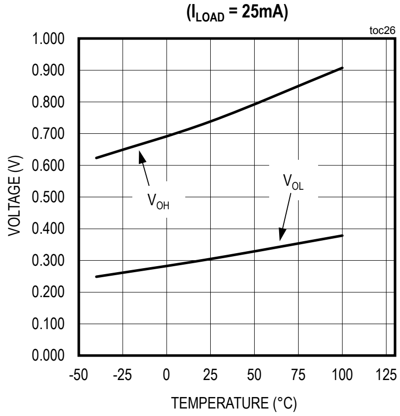
DAC DROOP RATE
vs. TEMPERATURE
(DAC RANGE -5V TO +5V)



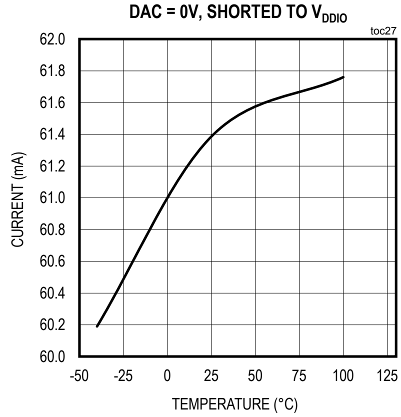
DAC DROOP RATE
vs. TEMPERATURE
(DAC RANGE -10V TO 0)



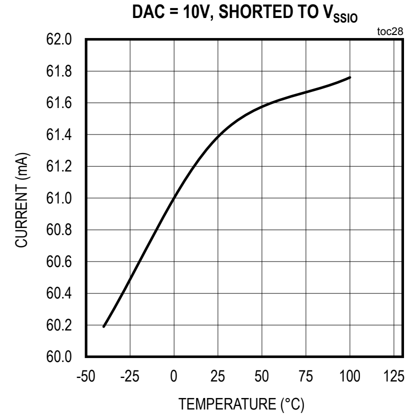
DAC V_{OH} AND V_{OL}
vs. TEMPERATURE
(I_{LOAD} = 25mA)



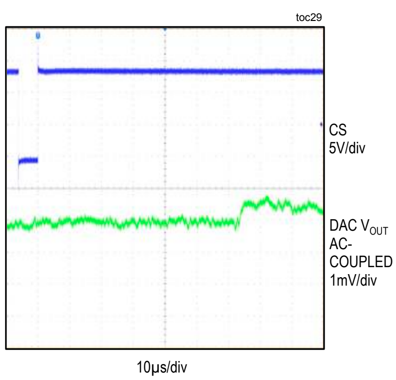
DAC DRIVE CURRENT LIMIT
vs. TEMPERATURE
DAC = 0V, SHORTED TO V_{DDIO}



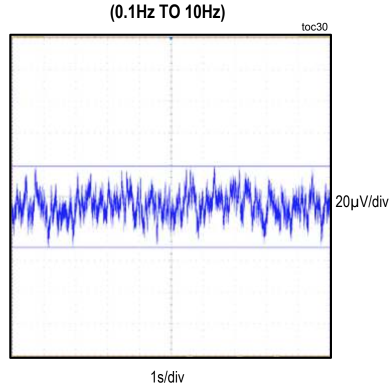
DAC DRIVE CURRENT LIMIT
vs. TEMPERATURE
DAC = 10V, SHORTED TO V_{SSIO}



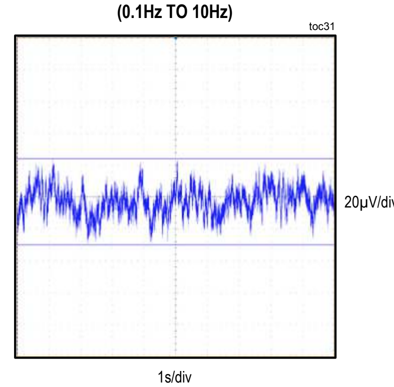
MAJOR-CODE TRANSITION GLITCH
DAC CODE FROM 0x7FF TO 0x800



DAC OUTPUT NOISE
INTERNAL REFERENCE
(0.1Hz TO 10Hz)

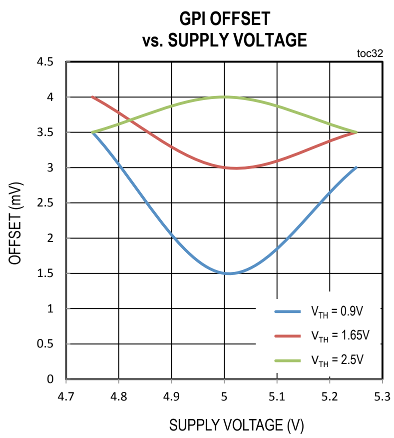


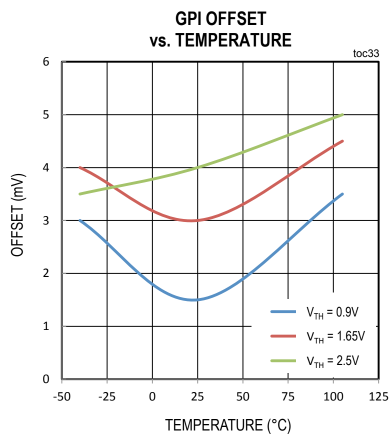
DAC OUTPUT NOISE
EXTERNAL REFERENCE
(0.1Hz TO 10Hz)

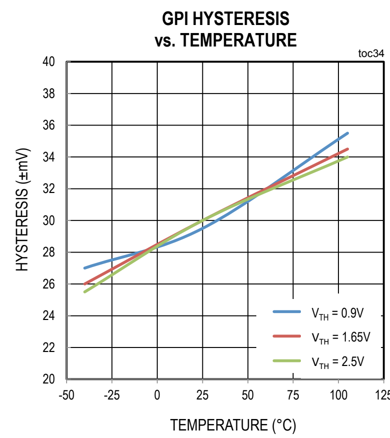


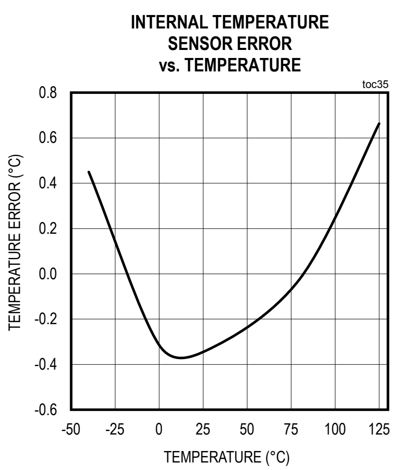
Typical Operating Characteristics (continued)

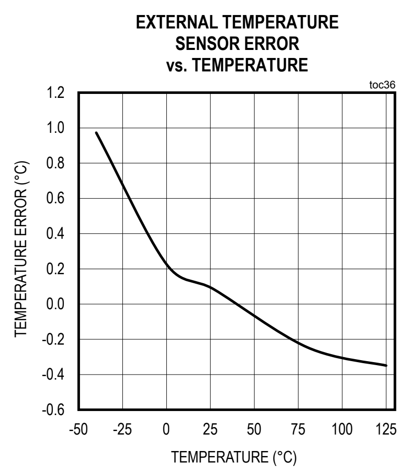
(T_A = +25°C, unless otherwise noted.)



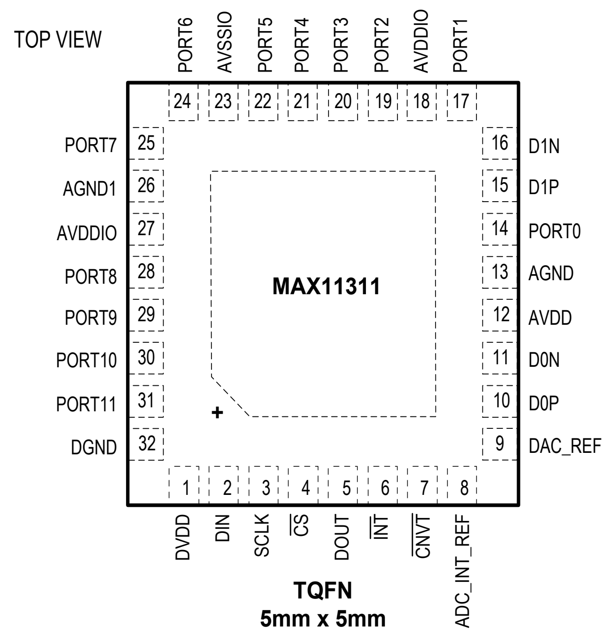








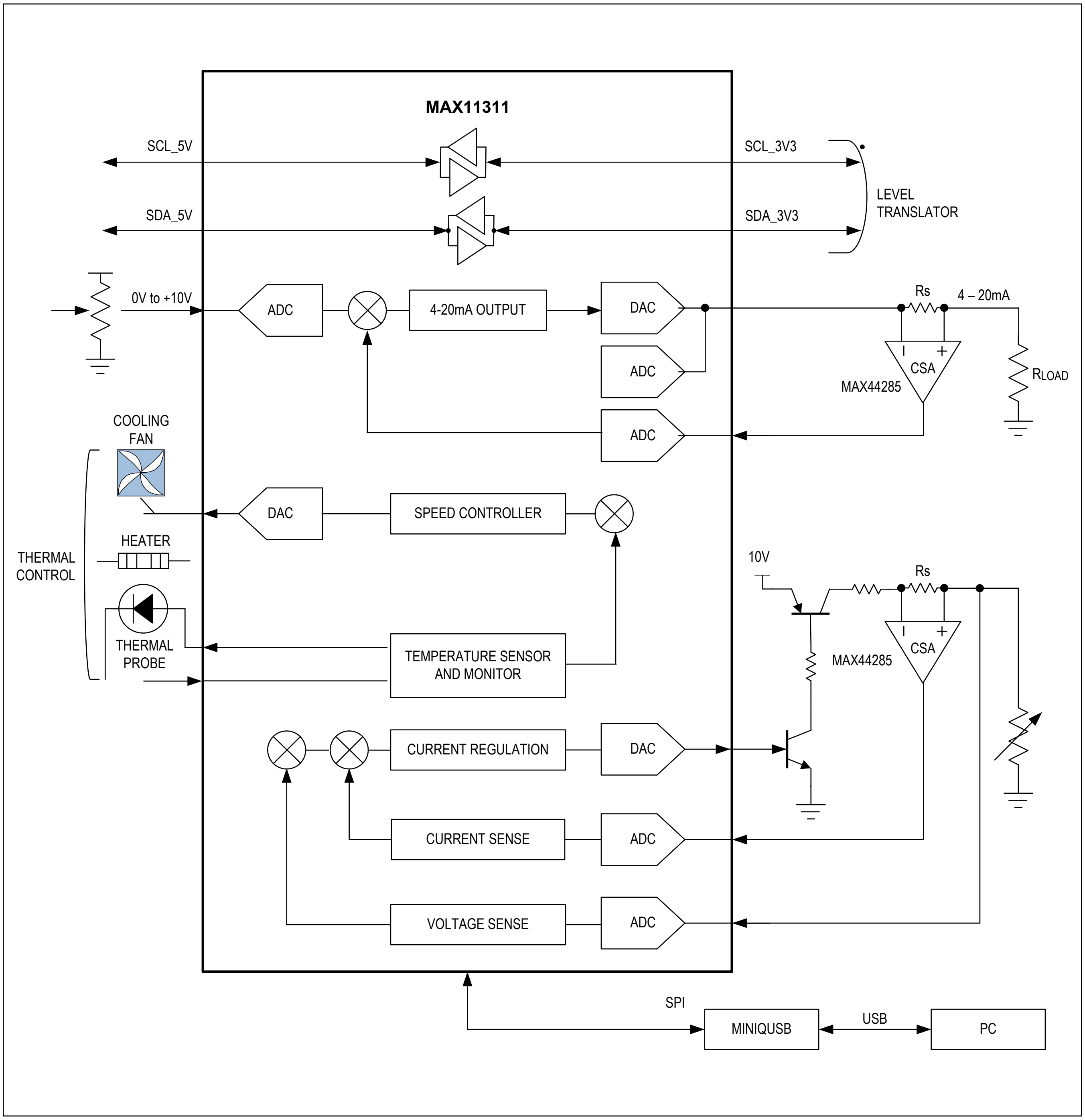
Pin Configurations



Pin Description

PIN	NAME	FUNCTION
1	DVDD	Positive Digital Supply
2	DIN	Serial Interface Data Input
3	SCLK	Serial Interface Clock Input
4	CSB	Serial Interface Chip-Select. Active-low.
5	DOUT	Serial Interface Data Output
6	$\overline{\text{INT}}$	Interrupt Open-Drain Output. Active-low.
7	$\overline{\text{CNVT}}$	ADC Trigger Control Input. Active-low.
8	ADC_INT_REF	ADC Internal Voltage Reference Output. Connect a bypass capacitor at this pin (4.7µF to 10µF).
9	DAC_REF	DAC External/Internal Voltage Reference Input. Connect a bypass capacitor at this pin (4.7µF to 10µF).
10	D0P	1st External Temperature Sensor Positive Input
11	D0N	1st External Temperature Sensor Negative Input
12	AVDD	Positive Analog Supply
13	AGND	Analog Ground
14	PORT0	Configurable Mixed-Signal Port 0
15	D1P	2nd External Temperature Sensor Positive Input
16	D1N	2nd External Temperature Sensor Negative Input
17	PORT1	Configurable Mixed-Signal Port 1
18,27	AVDDIO	Analog Positive Supply For Mixed-Signal Ports. Connect both pins to AVDDIO.
19	PORT2	Configurable Mixed-Signal Port 2
20	PORT3	Configurable Mixed-Signal Port 3
21	PORT4	Configurable Mixed-Signal Port 4
22	PORT5	Configurable Mixed-Signal Port 5
23	AVSSIO	Analog Negative Supply for Mixed-Signal Ports.
24	PORT6	Configurable Mixed-Signal Port 6
25	PORT7	Configurable Mixed-Signal Port 7
26	AGND1	Analog Ground
28	PORT8	Configurable Mixed-Signal Port 8
29	PORT9	Configurable Mixed-Signal Port 9
30	PORT10	Configurable Mixed-Signal Port 10
31	PORT11	Configurable Mixed-Signal Port 11
32	DGND	Digital Ground
—	EP	Exposed Pad. Connect EP to AVSSIO.

Application Circuits



Control and Monitoring Solution

Detailed Description

Functional Overview

The MAX11311 has 12 configurable mixed-signal I/O ports. Each port is independently configured as a DAC output, an ADC input, a GPI, a GPO, or an analog switch terminal. User-controllable parameters are available for each of those configurations. The device offers one internal and two external temperature sensors. The serial interface operates as a SPI Mode 0 interface.

The DAC is used to drive out a voltage defined by the DAC data register of the DAC-configured ports. The DAC uses either an internal or external voltage reference. The selection of the voltage reference is set for all the ports and cannot be configured on a port-by-port basis.

The ADC converts voltages applied to the ADC-configured ports. The ADC can operate in single-ended mode or in differential mode, by which any two ports can form a differential pair. The port configured as the negative input of the ADC can be used by more than one differential ADC input pairs. The ADC uses an internal voltage reference. In some configurations, the ADC uses the DAC voltage reference. The ADC voltage reference selection can be configured on a port-by-port basis.

Interrupts provide the host with the occurrence of user-selected events through the configuration of an interrupt mask register.

ADC Operations

The ADC is a 12-bit, low-power, successive approximation analog-to-digital converter, capable of sampling a single input at up to 400ksps. The ADC's conversion rate can be programmed to 400ksps, 333ksps, 250ksps, or 200ksps. The default conversion rate setting is 200ksps. Each ADC-configured port can be programmed for one of four input voltage ranges: 0V to +10V, -5V to +5V, -10V to 0V, and 0V to +2.5V. The ADC uses the internal ADC 2.5V voltage reference, or, in some cases, the DAC voltage reference. The voltage reference can be selected on a port-by-port basis.

ADC Control

The ADC can be triggered using an external signal $\overline{\text{CNVT}}$ or from a control bit. $\overline{\text{CNVT}}$ is active-low and must remain low for a minimal duration of 0.5µs to trigger a conversion. Four configurations are available:

- Idle mode (default setting).
- Single sweep mode. The ADC sweeps sequentially the ADC-configured ports, from the lowest index port to the highest index port, once $\overline{\text{CNVT}}$ is asserted.
- Single conversion mode. The ADC performs a single conversion at the current port in the series of ADC-configured ports when $\overline{\text{CNVT}}$ is asserted.
- Continuous sweep mode. The ADC continuously sweeps the ADC-configured ports. The $\overline{\text{CNVT}}$ port has no effect in this mode.

ADC Averaging Function

ADC-configured ports can be configured to average blocks of 2, 4, 8, 16, 32, 64, or 128 conversion results. The corresponding ADC data register is updated only when the averaging is completed, thus decreasing the throughput proportionally. If the number of samples to average is modified for a given port, the content of the ADC data register for that port is cleared before starting to average the new block of samples.

ADC Mode Change

When users change the ADC active mode (continuous sweep, single sweep, or single conversion), the ADC data registers are reset. However, ADC data registers retain content when the ADC is changed to idle mode.

ADC Configurations

The ADC can operate in single-ended, differential, or pseudo-differential mode. In single-ended mode, the PIXI port is the positive input to the ADC while the negative input is grounded internally (Figure 3). In differential mode (Figure 4), any pair of PIXI ports can be configured as inputs to the differential ADC. In pseudo-differential mode (Figure 5), one PIXI port produces the voltage applied to the negative input of the ADC while another PIXI port forms the positive input.

The ADC data format is straight binary in single-ended mode, and two's complement in differential and pseudo-differential modes.

DAC Operations

The MAX11311 uses a 12-bit DAC, which operates at the rate of 40µs per port. Since up to 12 ports can be configured in DAC-related modes, the minimum refresh rate per port is 2.083kHz.

No external component is required to set the offset and gain of the DAC drivers. The PIXI port driver features a wide output voltage range of ±10V and high current capability with dedicated power supplies (AVDDIO, AVSSIO).

The DAC uses either the internal or external voltage reference. Unlike the ADC, the DAC voltage reference cannot be configured on a port-by-port basis. DAC mode configuration is illustrated in Figure 6.

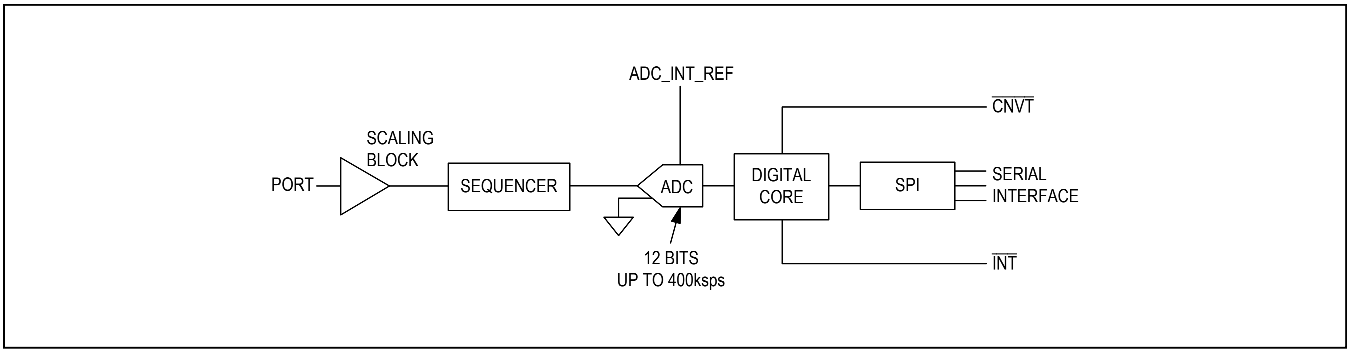


Figure 3. ADC with Single-Ended Input

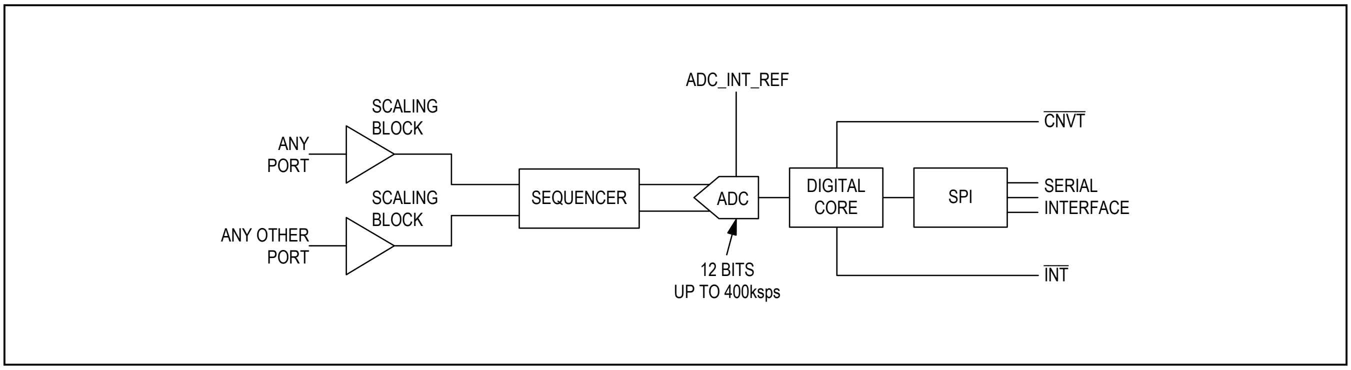


Figure 4. ADC with Differential Inputs

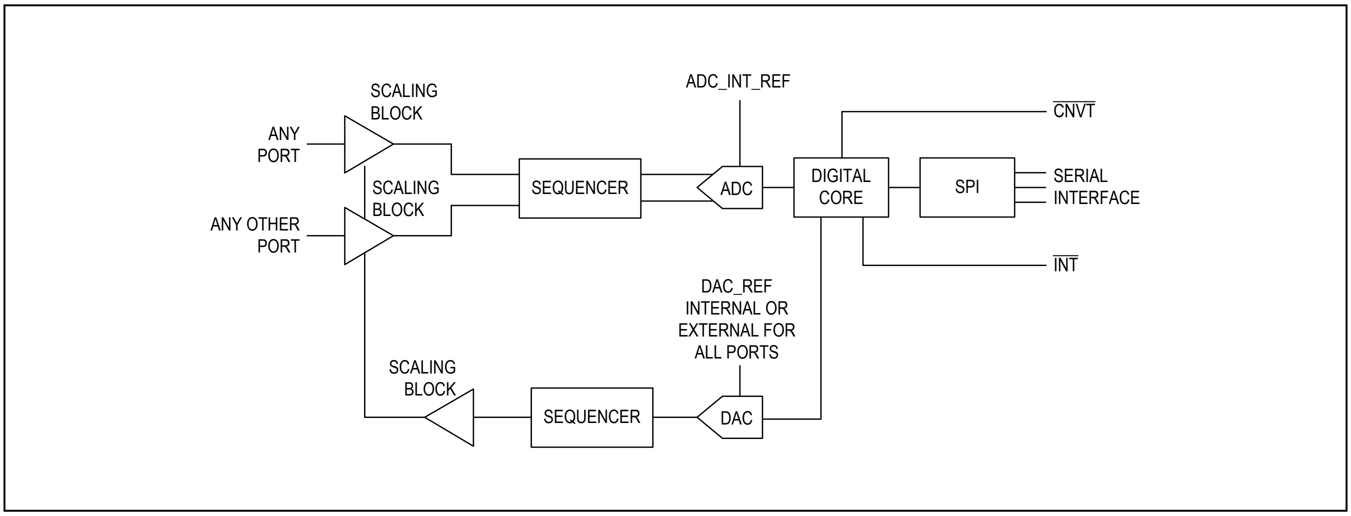


Figure 5. ADC with Pseudo-Differential Input Set by DAC

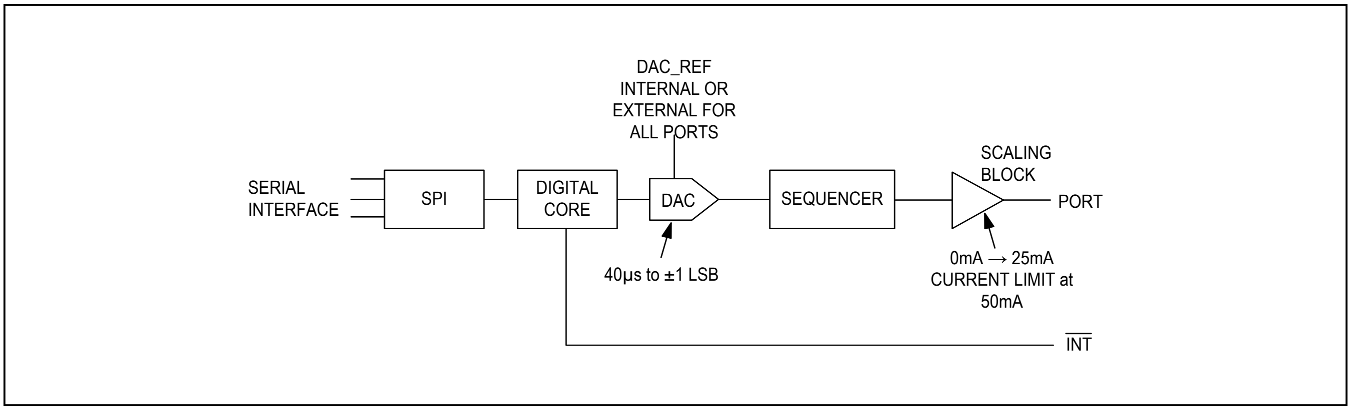


Figure 6. DAC Configuration

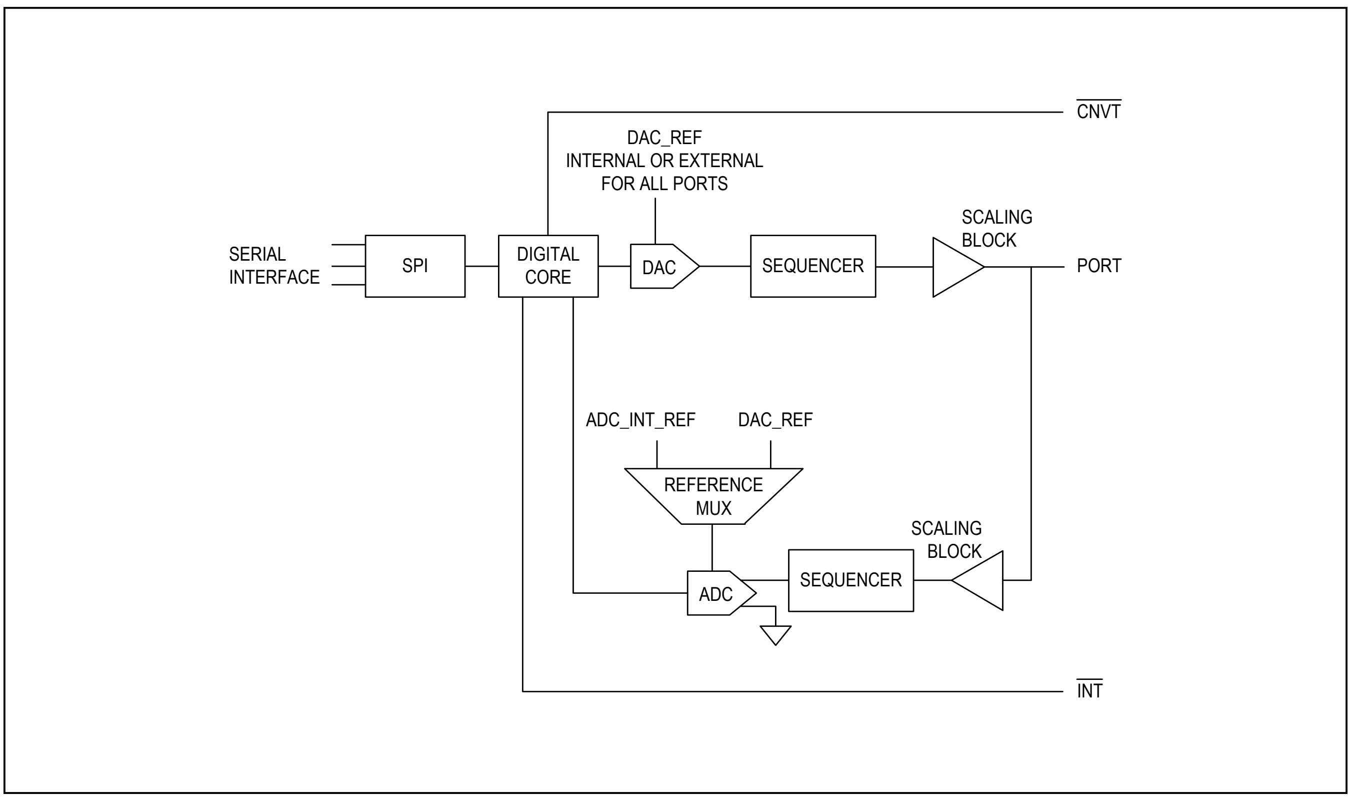


Figure 7. DAC Configuration with ADC Monitoring

DAC operations can be monitored by the ADC. In such a mode, the ADC samples the DAC-configured port to allow the host to monitor that the voltage at the port is within expectations given the accuracy of the ADC and DAC. This ADC monitoring mode is shown in Figure 7.

By default, the DAC updates the DAC-configured ports sequentially. However, users can configure the DAC so that its sequence can jump to update the port that just received new data to convert. After having updated this port, the DAC continues its default sequence from that port. In that mode, users should allow a minimum of 80μs between DAC data register updates for subsequent jump operations.

In addition to port-specific DAC data registers, the host can also use the same data for all DAC-related ports using one of two preset DAC data registers.

All DAC output drivers are protected by overcurrent limit circuitry. In case of overcurrent, the MAX11311 generates an interrupt. Detailed status registers are offered to the host to determine which ports are current limited.

General-Purpose Input and Output

Each PIXI port can be configured as a GPI or a GPO. The GPI threshold (Figure 8) is adjusted by setting the DAC data register of that GPI port to the corresponding voltage. If the DAC data register is set at 0x0FFF, the GPI threshold is the DAC reference voltage. The amplitude of the input signal must be contained within 0V to V_{AVDD}. The GPI-configured port can be set to detect rising edges, falling edges, either rising or falling edges, or none.

When a port is configured as GPO (Figure 9), the amplitude of its logic-one level is set by its DAC data register. If the DAC data register is set at 0x0FFF, the GPO logic-one level is four times the DAC reference voltage. The logic-zero level is always 0V. The host can set the logic state of GPO-configured ports through the corresponding GPO data registers.

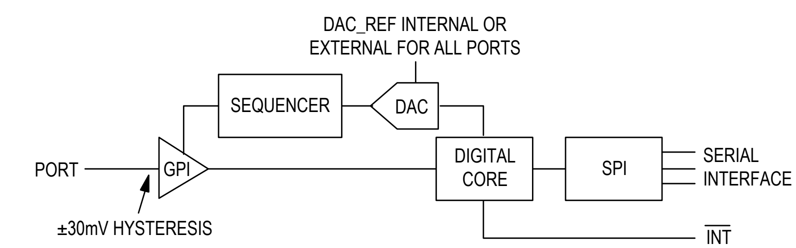


Figure 8. GPI Mode

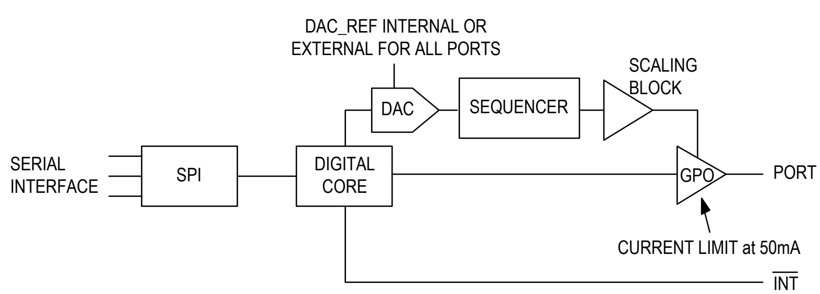


Figure 9. GPO Mode

Unidirectional and Bidirectional Level Translator Operations

By combining GPI- and GPO-configured ports, unidirectional level translator paths can be formed. The signaling at the input of the path can be different from the signaling at the end (Figure 10). For example, a unidirectional path could convert a signal from 1.8V logic level to 3.3V logic level.

The unidirectional path configuration allows for the transmission of signals received on a GPI-configured port to one or more GPO-configured ports.

Pairs of adjacent PIXI ports can also form bidirectional level translator paths that are targeted to operate with open-drain drivers (Figure 11). In this configuration, adjacent PIXI ports must be from the same six-channel group: PORT0 to PORT5 or PORT6 to PORT11. When used as a bidirectional level translator, the pair of PIXI ports must be accompanied with external pullup resistors to meet proper logic levels.

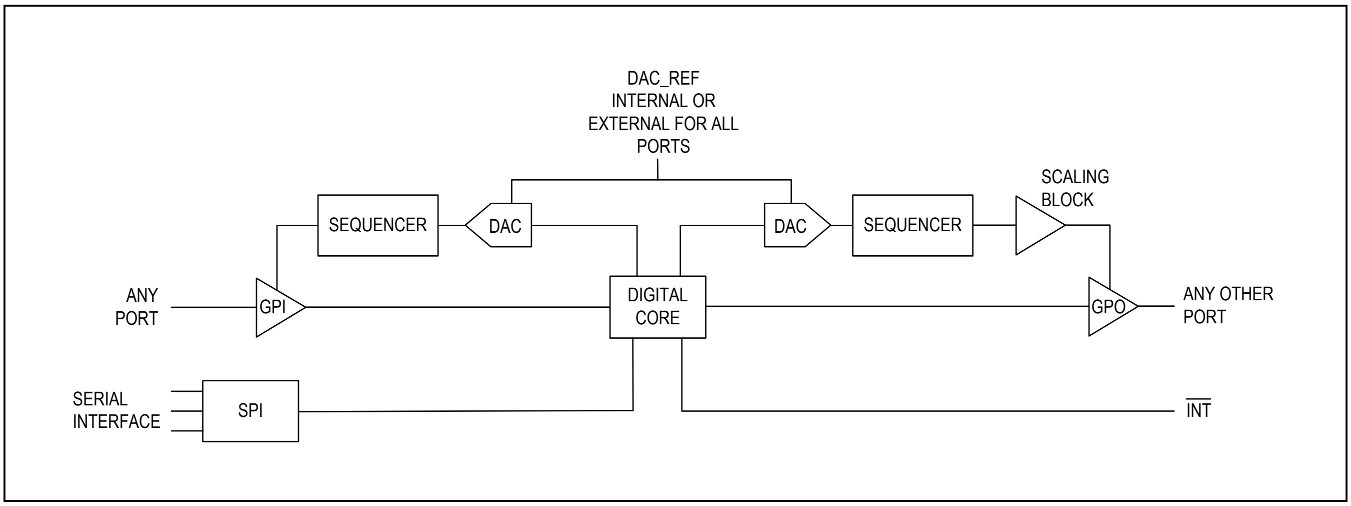


Figure 10. Unidirectional Level Translator Path Mode

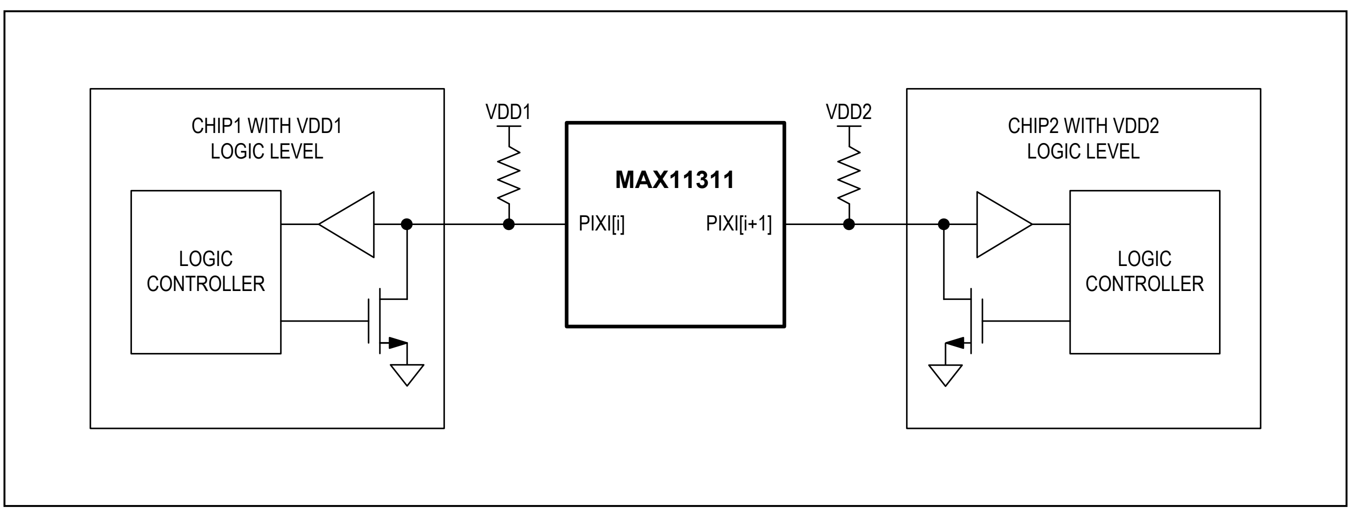


Figure 11. Bidirectional Level Translation Application Diagram