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maxim integrated™

MAX11359A

16-Bit Data-Acquisition System with ADC, DAC, UPIOs, RTC, Voltage Monitors, and Temp Sensor

General Description

The MAX11359A smart data-acquisition systems (DAS) is based on a 16-bit, sigma-delta analog-to-digital converter (ADC) and system-support functionality for a microprocessor (µP)-based system. The device integrates an ADC, DAC, operational amplifiers, internal selectable-voltage reference, temperature sensors, analog switches, a 32kHz oscillator, a real-time clock (RTC) with alarm, a high-frequency-locked loop (FLL) clock, four user-programmable I/Os, an interrupt generator, and 1.8V and 2.7V voltage monitors in a single chip.

The MAX11359A has dual 10:1 differential input multiplexers (muxes) that accept signal levels from 0 to AVDD. An on-chip 1x to 8x programmable-gain amplifier (PGA) allows measuring low-level signals and reduces external circuitry required.

The MAX11358B operates from a single +1.8V to +3.6V supply and consumes only 1.4mA in normal mode and only 6.1µA in sleep mode. The MAX11385B has one DACs with two uncommitted op amp.

The serial interface is compatible with either SPI/QSPI™ or MICROWIRE®, and is used to power up, configure, and check the status of all functional blocks.

The MAX11359A is available in a space-saving, 40-pin TQFN package and is specified over the commercial (0°C to +70°C) and the extended (-40°C to +85°C) temperature ranges.

Applications

Battery-Powered and Portable Devices
Electrochemical and Optical Sensors
Medical Instruments
Industrial Control
Data-Acquisition Systems

QSPI is a trademark of Motorola, Inc.
MICROWIRE is a registered trademark of National Semiconductor Corp.

Features

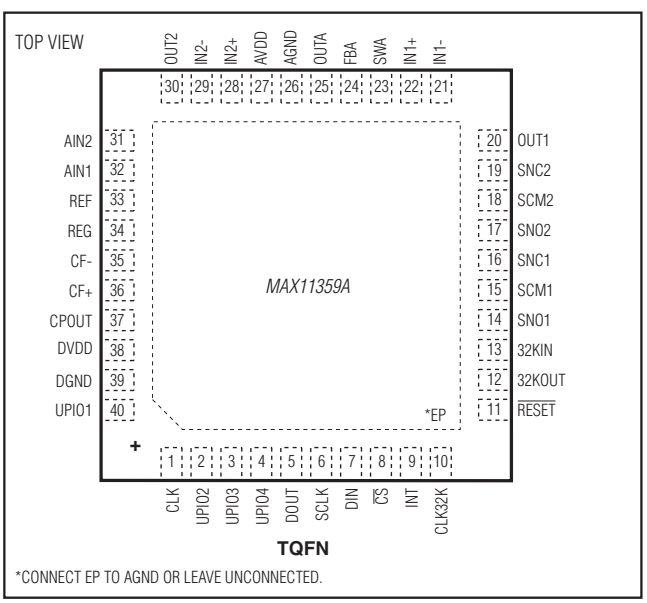
- **+1.8V to +3.6V Single-Supply Operation**
- **Multichannel 16-Bit Sigma-Delta ADC**
  - **10sps to 512sps Programmable Conversion Rate**
  - **Self and System Offset and Gain Calibration**
  - **PGA with Gains of 1, 2, 4, or 8**
  - **Unipolar and Bipolar Modes**
  - **10-Input Differential Multiplexer**
- **10-Bit Force-Sense DACs**
- **Uncommitted Op Amps**
- **Dual SPDT Analog Switches**
- **Selectable References**
  - **1.25V, 1.996V and 2.422V**
- **Internal Charge Pump**
- **System Support**
  - **Real-Time Clock and Alarm Register**
  - **Internal/External Temperature Sensor**
  - **Internal Oscillator with Clock Output**
  - **User-Programmable I/O and Interrupt Generator**
  - **V_{DD} Monitors**
- **SPI/QSPI/MICROWIRE, 4-Wire Serial Interface**
- **Space-Saving (6mm x 6mm x 0.75mm), 40-Pin TQFN Package**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX11359AETL+	-40°C to +85°C	40 TQFN-EP**
MAX11359ACTL+*	0°C to +70°C	40 TQFN-EP**

+Denotes a lead(Pb)-free/RoHS–compliant package.
**Future product—contact factory for availability.*
***EP = Exposed pad.*

Pin Configuration



For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maximintegrated.com.

19-4594; Rev 1; 1/12

ABSOLUTE MAXIMUM RATINGS

AVDD to AGND .....-0.3V to +4V
DVDD to DGND .....-0.3V to +4V
AVDD to DVDD .....-4V to +4V
AGND to DGND.....-0.3V to +0.3V
CLK32K to DGND .....-0.3V to (V_{DVDD} + 0.3V)
UPIO_ to DGND.....-0.3V to +4V
Digital Inputs to DGND .....-0.3V to +4V
Analog Inputs to AGND.....-0.3V to (V_{AVDD} + 0.3V)
Digital Output to DGND… .....-0.3V to (V_{DVDD} + 0.3V)
Analog Outputs to AGND.....-0.3V to (V_{AVDD} + 0.3V)
Continuous Current Into Any Pin.....50mA
Continuous Power Dissipation (T_A = +70°C)
40-Pin TQFN (derate 25.6mW/°C above +70°C) 2051.3mW
Operating Temperature Range
MAX11358_ _CTL+.....0°C to +70°C
MAX11358_ _ETL+ .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{AVDD} = V_{DVDD} = +1.8V to +3.6V, V_{REF} = +1.25V, external reference, CLK32K = 32.768kHz (external clock), C_{REG} = 10µF, C_{CPOUT} = 10µF, 10µF between CF+ and CF-, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ADC DC ACCURACY						
Noise-Free Resolution		Data rate = 10sps, PGA gain = 2; data rate = 10sps to 60sps, PGA gain = 1; no missing codes, Table 1 (Note 2)	16			Bits
Conversion Rate		No missing codes, Table 1	10		512	sps
Output Noise		No missing codes		Table 1		μV_{RMS}
Integral Nonlinearity	INL	Unipolar mode, V_{AVDD} = 3V, PGA gain = 1, T_A = +25°C, data rate = 50sps		±0.004		%FSR
Unipolar Offset Error or Bipolar Zero Error (Note 3)		Uncalibrated		±1.0		%FSR
		PGA gain = 1, calibrated, T_A = +25°C, data rate = 50sps			±0.003	
Unipolar Offset-Error or Bipolar Zero-Error Temperature Drift (Note 4)		Bipolar		±2.0		µV/°C
		Unipolar		±10		
Gain Error (Notes 3, 5)		Uncalibrated		±0.6		%FSR
		PGA = 1, calibrated, data rate = 50sps		±0.003		
Gain-Error Temperature Coefficient		(Notes 4, 6)		±1.0		ppm/°C
DC Positive Power-Supply Rejection Ratio	PSRR	PGA gain = 1, unipolar mode, measured by full-scale error with V_{AVDD} = 1.8V to 3.6V		73		dB
ADC ANALOG INPUTS (AIN1, AIN2)						
DC Input Common-Mode Rejection Ratio	CMRR	PGA gain = 1, unipolar mode		85		dB

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{DVDD} = +1.8V to +3.6V, V_{REF} = +1.25V, external reference, CLK32K = 32.768kHz (external clock), C_{REG} = 10µF, C_{CPOUT} = 10µF, 10µF between CF+ and CF-, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Normal-Mode 60Hz Rejection Ratio		PGA gain = 1, unipolar mode, data rate = 50sps (Note 2)	100			dB
Normal-Mode 50Hz Rejection Ratio		Data rate = 10sps or 50sps, PGA gain = 1, unipolar mode (Note 2)	100			dB
Absolute Input Range		Internal temperature sensor disabled (Figure 26)	V_{AGND}		V_{AVDD}	V
Differential Input Range		Unipolar mode	-0.05/ Gain		V_{REF}/ Gain	V
		Bipolar mode	-V_{REF}/ Gain		V_{REF}/ Gain	
DC Input Current (Note 7)		ADC not in measurement mode, mux enabled, $T_A \le +55°C$, inputs = +0.1V to (V_{AVDD} - 0.1V)			±1	nA
		T_A = +85°C			±5	
Input Sampling Capacitance	C_{IN}			5		pF
Input Sampling Rate	f_{SAMPLE}			21.84		kHz
External Source Impedance at Input		(Table 3)		Table 3		kΩ
FORCE-SENSE DAC (R_L = 10kΩ and C_L = 200pF, FBA = OUTA, unless otherwise noted)						
Resolution		Guaranteed monotonic	10			Bits
Differential Nonlinearity	DNL	Code 3Dhex to 3FF hex			±1	LSB
Integral Nonlinearity	INL	Code 3Dhex to 3FF hex			±4	LSB
Offset Error		Reference to code 52 hex			±20	mV
Offset-Error Tempco				±4.4		µV/°C
Gain Error		Excludes offset and voltage reference error			±5	LSB
Gain-Error Tempco		Excludes offset and reference drift		±1		ppm/°C
Input Leakage Current at SWA/B		SWA switches open (Notes 7, 8)			±1	nA
Input Leakage Current at FBA/B		V_{FBA} = +0.3V to (V_{AVDD} - 0.3V) (Note 7), T_A = -40°C to +85°C			±1	nA
		V_{FBA} = +0.3V to (V_{AVDD} - 0.3V) (Note 7), T_A = 0°C to +70°C			±600	pA
		V_{FBA} = +0.3V to (V_{AVDD} - 0.3V) (Note 7), T_A = 0°C to +50°C			±400	
DAC Output Buffer Leakage Current		DAC buffer disabled (Note 7)			±75	nA
Input Common-Mode Voltage		At FBA	0		V_{AVDD} - 0.35	V
Line Regulation		V_{AVDD} = +1.8V to +3.6V, T_A = +25°C		40	175	µV/V
Load Regulation		I_{OUT} = ±2mA, C_L = 1000pF (Note 2)			0.5	µV/µA
Output Voltage Range			V_{AGND}		V_{AVDD}	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{DVDD} = +1.8V to +3.6V, V_{REF} = +1.25V, external reference, CLK32K = 32.768kHz (external clock), C_{REG} = 10µF, C_{CPOUT} = 10µF, 10µF between CF+ and CF-, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Slew Rate		52 hex to 3FF hex code swing rising or falling, R_L = 10kΩ, C_L = 100pF			40		V/ms
Output-Voltage Settling Time		10% to 90% rising or falling to ±0.5 LSB			65		µs
Input Voltage Noise		Referred to FBA, excludes reference noise	f = 0.1Hz to 10Hz		80		$µV_{P-P}$
			f = 10Hz to 10kHz		200		
Output Short-Circuit Current		OUTA shorted to AGND			20		mA
		OUTA shorted to AVDD			15		
Input-Output SWA/SWB Switch Resistance		Between SWA and OUTA, HFCK enabled				150	Ω
SWA/SWB Switch Turn-On/Off Time		HFCK enabled			100		ns
Power-On Time		Excluding reference			18		µs
EXTERNAL REFERENCE (REF)							
Input Voltage Range				V_{AGND}		V_{AVDD}	V
Input Resistance		DAC on, internal REF and ADC off			2.5		MΩ
DC Input Leakage Current		Internal REF, DAC, and ADC off (Note 7)				100	nA
INTERNAL VOLTAGE REFERENCE (C_{REF} = 4.7µF)							
Reference Output Voltage	V_{REF}	V_{AVDD} ≥ +1.8V, T_A = +25°C		1.238	1.251	1.264	V
		V_{AVDD} ≥ +2.2V, T_A = +25°C		1.976	1.996	2.016	
		V_{AVDD} ≥ +2.7V, T_A = +25°C		2.349	2.422	2.495	
Output-Voltage Temperature Coefficient (Note 7)	TC	V_{REF} = 1.251V			15	50	ppm/°C
		V_{REF} = 1.996V, 2.422V				65	
Output Short-Circuit Current	I_{RSC}	REF shorted to AGND			18		mA
		REF shorted to AVDD			90		µA
Line Regulation		T_A = +25°C				100	µV/V
Load Regulation		T_A = +25°C, V_{REF} = 1.25V	I_{SOURCE} = 0 to 500µA			1.2	µV/µA
			I_{SINK} = 0 to 50µA		1.7		

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{DVDD} = +1.8V to +3.6V, V_{REF} = +1.25V, external reference, CLK32K = 32.768kHz (external clock), C_{REG} = 10µF, C_{CPOUT} = 10µF, 10µF between CF+ and CF-, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Long-Term Stability		(Note 9)			35		ppm/ 1000hrs
Output Noise Voltage		f = 0.1Hz to 10Hz, V_{AVDD} = 3V			50		μV_{P-P}
		f = 10Hz to 10kHz, V_{AVDD} = 3V			400		
Turn-On Settling Time		Buffer only, settle to 0.1% of final value			100		µs
TEMPERATURE SENSOR							
Temperature Measurement Resolution		ADC resolution is 16-bit, 10sps			0.11		°C/LSB
Internal Temperature-Sensor Measurement Error		Internal voltage reference, four-current calibration, and stored calibration coefficients	T_A = 0°C to +50°C		±0.5		°C
			T_A = -40°C to +85°C		±1		
External Temperature-Sensor Measurement Error (Note 10)		T_A = +25°C			±0.50		°C
		T_A = 0°C to +50°C			±0.5		
		T_A = -40°C to +85°C			±1.0		
Temperature Measurement Noise					0.18		$°C_{RMS}$
Temperature Measurement Power-Supply Rejection Ratio					0.2		°C/V
OP AMP (R_L = 10kΩ connected to V_{AVDD}/2)							
Input Offset Voltage	V_{OS}	V_{CM} = 0.5V				±15	mV
Offset-Error Tempco					3		µV/°C
Input Bias Current (Note 7)	I_{BIAS}	IN1+, IN2+, IN3+	T_A = -40°C to +85°C		0.006	±1	nA
			T_A = 0°C to +70°C		4	±300	pA
			T_A = 0°C to +50°C		2	±200	
		IN1-, IN2-, IN3-	T_A = -40°C to +85°C		0.025	±1	nA
			T_A = 0°C to +70°C		20	±600	pA
			T_A = 0°C to +50°C			±400	
Input Offset Current	I_{OS}	$V_{IN1\_}$, $V_{IN2\_}$ = +0.3V to (V_{AVDD} - 0.3V) (Note				±1	nA
Input Common-Mode Voltage Range	CMVR			0		V_{AVDD} - 0.35	V
Common-Mode Rejection Ratio	CMRR	0 ≤ V_{CM} ≤ 75mV			60		dB
		75mV < V_{CM} ≤ V_{AVDD} - 0.35V, T_A = +25°C		60	75		

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{DVDD} = +1.8V to +3.6V, V_{REF} = +1.25V, external reference, CLK32K = 32.768kHz (external clock), C_{REG} = 10µF, C_{CPOUT} = 10µF, 10µF between CF+ and CF-, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Power-Supply Rejection Ratio	PSRR	V_{AVDD} = +1.8V to +3.6V, T_A = +25°C		76.5	100		dB
Large-Signal Voltage Gain	A_{VOL}	100mV ≤ $V_{OUT\_}$ ≤ V_{AVDD} - 100mV (Note 11)		90	116		dB
Maximum Current Drive	ΔV_{OUT}	Sourcing	I_{SOURCE} = 10µA			0.005	V
			I_{SOURCE} = 50µA			0.025	
			I_{SOURCE} = 100µA			0.05	
			I_{SOURCE} = 500µA			0.25	
			I_{SOURCE} = 2mA			0.5	
		Sinking	I_{SINK} = 10µA			0.005	
			I_{SINK} = 50µA			0.025	
			I_{SINK} = 100µA			0.05	
			I_{SINK} = 500µA			0.25	
			I_{SINK} = 2mA			0.5	
Gain Bandwidth Product	GBW	Unity-gain configuration, C_L = 1nF			80		kHz
Phase Margin		Unity-gain configuration, C_L = 1nF (Note 11)			60		Degrees
Output Slew Rate	SR	C_L = 200pF			0.04		V/µs
Input Voltage Noise		Unity-gain configuration	f = 0.1Hz to 10Hz		80		μV_{P-P}
			f = 10Hz to 10kHz		200		
Output Short-Circuit Current		$V_{OUT\_}$ shorted to AGND			20		mA
		$V_{OUT\_}$ shorted to AVDD			15		
Power-On Time					15		µs
SPDT SWITCHES (SNO_, SNC_, SCM_, HFCK enabled)							
On-Resistance	R_{ON}	$V_{SCM\_}$ = 0V	T_A = 0°C to +50°C			45	Ω
		$V_{SCM\_}$ = 0.5V	T_A = 0°C to +50°C			50	
		$V_{SCM\_}$ = 0.5V to V_{AVDD}				150	
SNO_, SNC_ Off-Leakage Current	$I_{SNO\_(OFF)}$ $I_{SNC\_(OFF)}$	$V_{SNO\_}$, $V_{SNC\_}$ = +0.5V, +1.5V; $V_{SCM\_}$ = +1.5V, +0.5V (Note 7)	T_A = -40°C to +85°C			±1	nA
			T_A = 0°C to +70°C			±600	pA
			T_A = 0°C to +50°C			±400	
SCM_ Off-Leakage Current	$I_{SCM\_(OFF)}$	$V_{SNO\_}$, $V_{SNC\_}$ = +0.5V, +1.5V; $V_{SCM\_}$ = +1.5V, +0.5V (Note 7)	T_A = -40°C to +85°C			±2	nA
			T_A = 0°C to +70°C			±1.2	
			T_A = 0°C to +50°C			±0.8	
SCM_ On-Leakage Current	$I_{SCM\_(ON)}$	$V_{SNO\_}$, $V_{SNC\_}$ = +0.5V, +1.5V, or unconnected; $V_{SCM\_}$ = +1.5V, +0.5V (Note 7)	T_A = -40°C to +85°C			±2	nA
			T_A = 0°C to +70°C			±1.2	
			T_A = 0°C to +50°C			±0.8	
Input Voltage Range				V_{AGND}		V_{AVDD}	V
Turn-On/Off Time	t_{ON}/t_{OFF}	Break-before-make			100		ns

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{DVDD} = +1.8V to +3.6V, V_{REF} = +1.25V, external reference, CLK32K = 32.768kHz (external clock), C_{REG} = 10µF, C_{CPOUT} = 10µF, 10µF between CF+ and CF-, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Capacitance		SNO_, SNC_, or SCM_ = AVDD or AGND; switch connected to enabled mux input		5		pF
CHARGE PUMP (10µF at REG and 10µF external capacitor between CF+ and CF-)						
Maximum Output Current	I_{OUT}		10			mA
Output Voltage		No load	3.2	3.3	3.6	V
		I_{OUT} = 10mA	3.0			
Output Voltage Ripple		10µF external capacitor between CPOUT and DGND, I_{OUT} = 10mA, excluding ESR of external capacitor			50	mV
Load Regulation		I_{OUT} = 10mA, excluding ESR of external capacitor		15	20	mV/mA
REG Input Voltage Range		Internal linear regulator disabled	1.6		1.8	V
REG Input Current		Linear regulator off, charge pump off		3		nA
CPOUT Input Voltage Range		Charge pump disabled	1.8		3.6	V
CPOUT Input Leakage Current		Charge pump disabled		2		nA
SIGNAL-DETECT COMPARATOR						
Differential Input-Detection Threshold Voltage		TSEL[2:0] = 0 hex		0		mV
		TSEL[2:0] = 4 hex		50		
		TSEL[2:0] = 5 hex		100		
		TSEL[2:0] = 6 hex		150		
		TSEL[2:0] = 7 hex		200		
Differential Input-Detection Threshold Error				±10		mV
Common-Mode Input Voltage Range			V_{AGND}		V_{AVDD}	V
Turn-On Time				50		µs
VOLTAGE MONITORS						
DVDD Monitor Supply Voltage Range		For valid reset	1.0		3.6	V
Trip Threshold (V_{DVDD} Falling)			1.80	1.85	1.90	V
DVDD Monitor Timeout Reset Period				1.5		s
DVDD Monitor Hysteresis		HYSE bit set to logic 1		200		mV
		HYSE bit set to logic 0		35		

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{DVDD} = +1.8V to +3.6V, V_{REF} = +1.25V, external reference, CLK32K = 32.768kHz (external clock), C_{REG} = 10µF, C_{CPOUT} = 10µF, 10µF between CF+ and CF-, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DVDD Monitor Turn-On Time				5		ms
CPOUT Monitor Supply Voltage Range			1.0		3.6	V
CPOUT Monitor Trip Threshold			2.7	2.8	2.9	V
CPOUT Monitor Hysteresis				35		mV
CPOUT Monitor Turn-On Time				5		ms
Internal Power-On Reset Voltage					1.7	V
32kHz Oscillator (32KIN, 32KOUT)						
Clock Frequency		V_{DVDD} = 2.7V		32.768		kHz
Stability		V_{DVDD} = 1.8V to 3.6V, excluding crystal		25		ppm
Oscillator Startup Time				1500		ms
Crystal Load Capacitance				6		pF
LOW-FREQUENCY CLOCK INPUT/OUTPUT (CLK32K)						
Output Clock Frequency				32.768		kHz
Absolute Input to Output Clock Jitter		Cycle to cycle		5		ns
Input to Output Rise/Fall Time		10% to 90%, 30pF load		5		ns
Input Duty Cycle			40		60	%
Output Duty Cycle				43		%
HIGH-FREQUENCY CLOCK OUTPUT (CLK)						
FLL Output Clock Frequency		f_{OUT} = f_{FLL}	4.8660	4.9152	4.9644	MHz
		f_{OUT} = f_{FLL}/2, power-up default	2.4330	2.4576	2.4822	MHz
		f_{OUT} = f_{FLL}/4	1.2165	1.2288	1.2411	MHz
		f_{OUT} = f_{FLL}/8	608.25	614.4	620.54	kHz
Absolute Clock Jitter		Cycle to cycle, FLL off		0.15		ns
		Cycle to cycle, FLL on		1		ns
Rise and Fall Time	t_R/t_F	10% to 90%, 30pF load			10	ns
Duty Cycle		f_{OUT} = 4.9152MHz	40		60	%
		f_{OUT} = 2.4576MHz, 1.2288MHz, 614.4kHz	45		55	%
Uncalibrated CLK Frequency Error		FLL calibration not performed			±35	%
DIGITAL INPUTS (SCLK, DIN, $\overline{CS}$, UPIO_, CLK32K)						
Input High Voltage	V_{IH}		0.7 x V_{DVDD}			V
Input Low Voltage	V_{IL}				0.3 x V_{DVDD}	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{DVDD} = +1.8V to +3.6V, V_{REF} = +1.25V, external reference, CLK32K = 32.768kHz (external clock), C_{REG} = 10µF, C_{CPOUT} = 10µF, 10µF between CF+ and CF-, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
UPIO_ Input High Voltage		DVDD supply voltage	0.7 x V_{DVDD}			V
		CPOUT supply voltage	0.7 x V_{CPOUT}			
UPIO_ Input Low Voltage		DVDD supply voltage			0.3 x V_{DVDD}	V
		CPOUT supply voltage			0.3 x V_{CPOUT}	
Input Hysteresis	V_{HYS}	V_{DVDD} = 3.0V		200		mV
Input Current	I_{IN}	V_{IN} = V_{DGND} or DVDD (Note 7)		±0.01	±100	nA
Input Capacitance		V_{IN} = V_{DGND} or DVDD		10		pF
UPIO_ Input Current		V_{IN} = DVDD or V_{CPOUT}, pullup enabled		±0.01	1	µA
		V_{IN} = DVDD or V_{CPOUT} or 0V, pullup disabled			1	
UPIO_ Pullup Current		V_{IN} = 0, pullup enabled, unconnected UPIO inputs are pulled up to DVDD or CPOUT with pullup enabled	0.5	2	5	µA
DIGITAL OUTPUTS (DOUT, $\overline{RESET}$, UPIO_, CLK32K, INT, CLK)						
Output Low Voltage	V_{OL}	I_{SINK} = 1mA			0.4	V
Output High Voltage	V_{OH}	I_{SOURCE} = 500µA	0.8 x V_{DVDD}			V
DOUT Three-State Leakage Current	I_L			±0.01	±1	µA
DOUT Three-State Output Capacitance	C_{OUT}			15		pF
$\overline{RESET}$ Output Low Voltage	V_{OL}	I_{SINK} = 1mA			0.4	V
$\overline{RESET}$ Output Leakage Current		Open-drain output, $\overline{RESET}$ deasserted			0.1	µA
UPIO_ Output Low Voltage	V_{OL}	I_{SINK} = 1mA, UPIO_ referenced to DVDD			0.4	V
		I_{SINK} = 4mA, UPIO_ referenced to CPOUT			0.4	
UPIO_ Output High Voltage	V_{OH}	I_{SOURCE} = 500µA, UPIO_ referenced to DVDD	0.8 x V_{DVDD}			V
		I_{SOURCE} = 4mA, UPIO_ referenced to CPOUT	V_{CPOUT} - 0.4			
POWER REQUIREMENT						
Analog Supply Voltage Range	AVDD		1.8		3.6	V
Digital Supply Voltage Range	DVDD		1.8		3.6	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{DVDD} = +1.8V to +3.6V, V_{REF} = +1.25V, external reference, CLK32K = 32.768kHz (external clock), C_{REG} = 10µF, C_{CPOUT} = 10µF, 10µF between CF+ and CF-, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Total Supply Current	I_{MAX}	Everything on, charge pump unloaded, no digital pins, sinking/sourcing current, e.g., $\overline{RST}$, UPIO, and CLK32K, max internal temp-sensor current, clock output buffers unloaded, ADC at 512sps	V_{AVDD} = V_{DVDD} = 3.6V		1.36	2.0	mA
			V_{AVDD} = V_{DVDD} = 3.3V		1.15	1.7	
	I_{NORMAL}	All on except charge pump and temp sensor, ADC at 512sps, CLK output buffer enabled, clock output buffers unloaded			1.17	1.3	
Sleep-Mode Supply Current	I_{SLEEP}	T_A = -45°C to +85°C	V_{AVDD} = V_{DVDD} = 3.0V			6.5	µA
			V_{AVDD} = V_{DVDD} =			9	
		T_A = +25°C	V_{AVDD} = V_{DVDD} = 3.0V		4.42		
			V_{AVDD} = V_{DVDD} = 3.6V		5.56		
Shutdown Supply Current	I_{SHDN}	All off	T_A = -40°C to +85°C			4	µA
			T_A = +25°C		1.6		

Note 1: Devices are production tested at T_A = +25°C and T_A = +85°C. Specifications to T_A = -40°C are guaranteed by design.

Note 2: Guaranteed by design or characterization.

Note 3: The offset and gain errors are corrected by self-calibration or system calibration. For accurate calibrations, perform calibration at the lowest rate. The calibration error is therefore in the order of peak-to-peak noise for the selected rate.

Note 4: Eliminate drift errors by recalibration at the new temperature.

Note 5: The gain error excludes reference error, offset error (unipolar), and zero error (bipolar).

Note 6: Gain-error drift does not include unipolar offset drift or bipolar zero-error drift. It is effectively the drift of the part if zero-scale error is removed.

Note 7: These specifications are obtained from characterization during design or from initial product evaluation. Not production tested or guaranteed.

Note 8: V_{OUTA} = +0.5V or +1.5V, V_{SWA} = +1.5V or +0.5V, T_A = 0°C to +50°C.

Note 9: Long-term stability is characterized using five to six parts. The bandgaps are turned on for 1000hrs at room temperature with the parts running continuously. Daily measurements are taken and any obvious outlying data points are discarded.

Note 10: All of the stated temperature accuracies assume that 1) the external diode characteristic is precisely known (i.e., ideal) and 2) the ADC reference voltage is exactly equal to 1.25V. Any variations to this known reference characteristic and voltage caused by temperature, loading, or power supply results in errors in the temperature measurement. The actual temperature calculation is performed externally by the microcontroller (µC).

Note 11: Values based on simulation results and are not production tested or guaranteed.

Table 1. Output Noise (Notes 12, 13, and 14)

RATE (sps)	OUTPUT NOISE (μV_{RMS})			
	GAIN = 1	GAIN = 2	GAIN = 4	GAIN = 8
10	1.684	1.684	1.684	1.684
40	3.178	3.178	3.178	3.178
50	3.234	3.234	3.234	3.234
60	3.307	3.307	3.307	3.307
200	55.336	55.336	55.336	55.336
240	104.596	104.596	104.596	104.596
400	587.138	587.138	587.138	587.138
512	983.979	983.979	983.979	983.979

Note 12: V_{REF} = ±1.25V, bipolar mode, V_{IN} = 1.24912V, PGA gain = 1, T_A = +85°C.
Note 13: C_{IN} = 5pF, op-amp noise is considered to be the same as the switching noise. The increase in the op amp's noise contribution is due to a large input swing (0 to 3.6V).
Note 14: Assume ±3 sigma peak-to-peak variation; noise-free resolution means no code flicker at given bits' LSB.

Table 2. Peak-to-Peak Resolution

RATE (sps)	PEAK-TO-PEAK RESOLUTION (Bits)			
	GAIN = 1	GAIN = 2	GAIN = 4	GAIN = 8
10	17.49	17.49	17.49	17.49
40	16.57	16.57	16.57	16.57
50	16.55	16.55	16.55	16.55
60	16.51	16.51	16.51	16.51
200	12.45	12.45	12.45	12.45
240	11.53	11.53	11.53	11.53
400	9.04	9.04	9.04	9.04
512	8.30	8.30	8.30	8.30

Table 3. Maximum External Source Impedance Without 16-Bit Gain Error

PARAMETER	EXTERNAL CAPACITANCE (pF)					
	0 (Note 15)	50	100	500	1000	5000
Resistance (kΩ)	350	60	30	10	4	1

Note 15: 2pF parasitic capacitance is assumed, which represents pad and any other parasitic capacitance.

TIMING CHARACTERISTICS (Figures 1 and 20)

(V_{AVDD} = V_{AVDD} = +1.8V to +3.6V, external V_{REF} = +1.25V, CLK32K = 32.768kHz (external clock), C_{REG} = 10µF, C_{CPOUT} = 10µF, 10µF between CF+ and CF-, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLK Operating Frequency	f_{SCLK}		0		10	MHz
SCLK Cycle Time	t_{CYC}		100			ns
SCLK Pulse-Width High	t_{CH}		40			ns
SCLK Pulse-Width Low	t_{CL}		40			ns
DIN to SCLK Setup	t_{DS}		30			ns
DIN to SCLK Hold	t_{DH}		0			ns
SCLK Fall to DOUT Valid	t_{DO}	C_L = 50pF, Figure 2			40	ns
$\overline{CS}$ Fall to Output Enable	t_{DV}	C_L = 50pF, Figure 2			48	ns
$\overline{CS}$ Rise to DOUT Disable	t_{TR}	C_L = 50pF, Figure 2			48	ns
$\overline{CS}$ to SCLK Rise Setup	t_{CSS}		20			ns
$\overline{CS}$ to SCLK Rise Hold	t_{CSH}		0			ns
DVDD Monitor Timeout Period	t_{DSLP}	(Note 16)		1.5		s
Wake-Up (WU) Pulse Width	t_{WU}	Minimum pulse width required to detect a wake-up event		1		µs
Shutdown Delay	t_{DPU}	The delay for $\overline{SHDN}$ to go high after a valid wake-up event		1		µs
HFCK Turn-On Time	t_{DFON}	The turn-on time for the high-frequency clock and FLL (FLLE = 1) (Note 17)			10	ms
		If FLLE = 0, the turn-on time for the high-frequency clock (Note 18)			10	µs
CRDY to $\overline{INT}$ Delay	t_{DFI}	The delay for CRDY to go low after the HFCK clock output has been enabled (Note 19)		7.82		ms
HFCK Disable Delay	t_{DFOF}	The delay after a shutdown command has asserted and before HFCK is disabled (Note 20)		1.95		ms
$\overline{SHDN}$ Assertion Delay	t_{DPD}	(Note 21)		2.93		ms

Note 16: The delay for the sleep voltage monitor output, $\overline{RESET}$, to go high after V_{DD} rises above the reset threshold. This is largely driven by the startup of the 32kHz oscillator.

Note 17: It is gated by an AND function with three inputs—the external $\overline{RESET}$ signal, the internal DV_{DD} monitor output, and the external $\overline{SHDN}$ signal. The time delay is timed from the internal LOV_{DD} going high or the external $\overline{RESET}$ going high, whichever happens later. HFCK always starts in the low state.

Note 18: If FLLE = 0, the internal signal CRDY is not generated by the FLL block and $\overline{INT}$ or INT are deasserted.

Note 19: CRDY is used as an interrupt signal to inform the µC that the high-frequency clock has started. Only valid if FLLE = 1.

Note 20: t_{DFOF} gives the µC time to clean up and go into sleep-override mode properly.

Note 21: t_{DPD} is greater than the HFCK delay for the MAX11358B/MAX11359A to clean up before losing power.

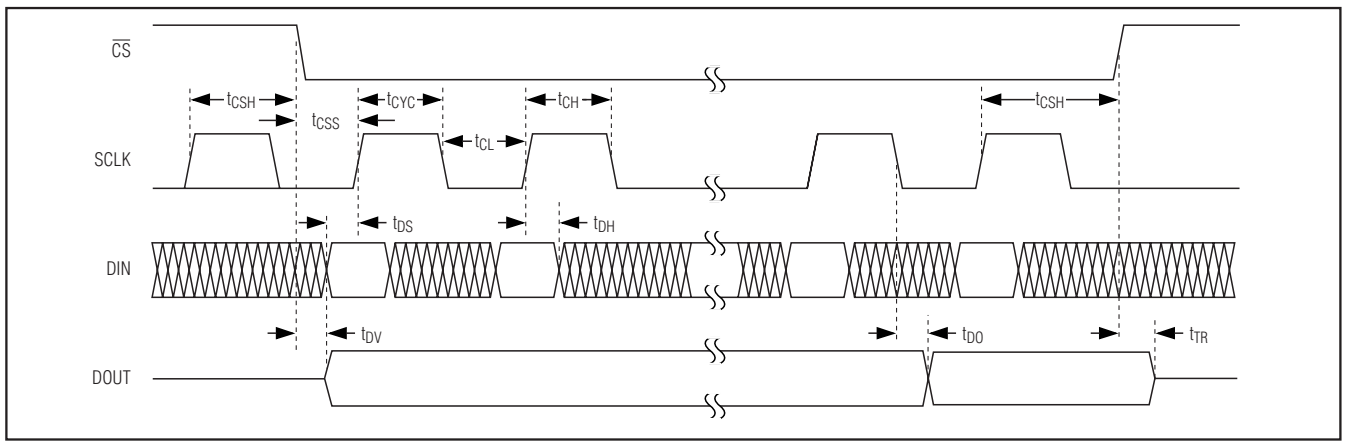


Figure 1. Detailed Serial-Interface Timing

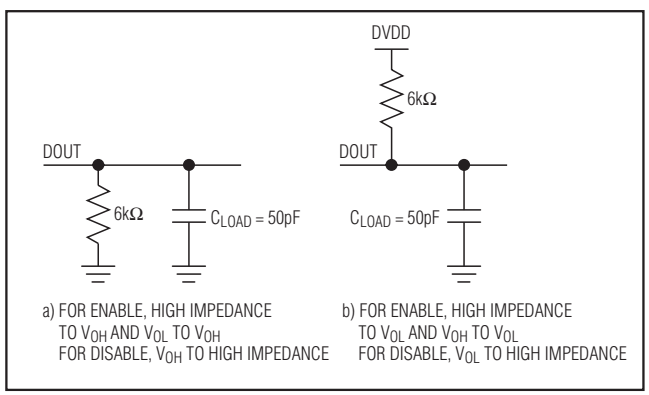
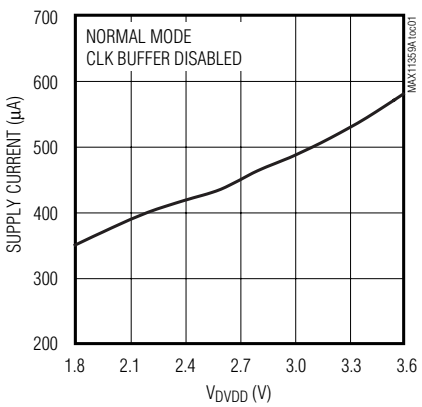


Figure 2. DOUT Enable and Disable Time Load Circuits

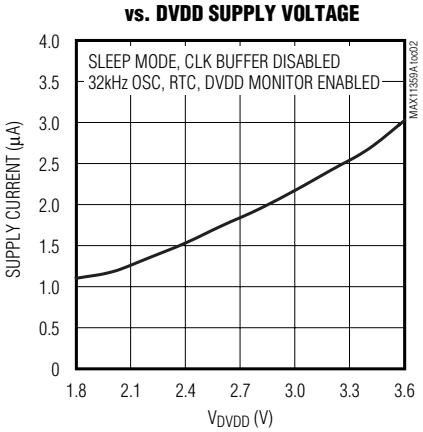
Typical Operating Characteristics

(V_{DVDD} = V_{AVDD} = 1.8V, V_{REF} = +1.25V, C_{CPOUT} = 10µF, T_A = +25°C, unless otherwise noted.)

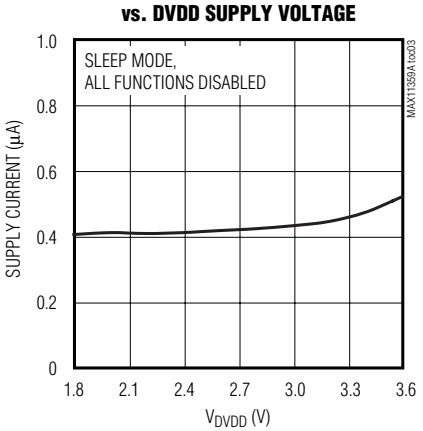
DVDD SUPPLY CURRENT vs. DVDD SUPPLY VOLTAGE



DVDD SUPPLY CURRENT vs. DVDD SUPPLY VOLTAGE



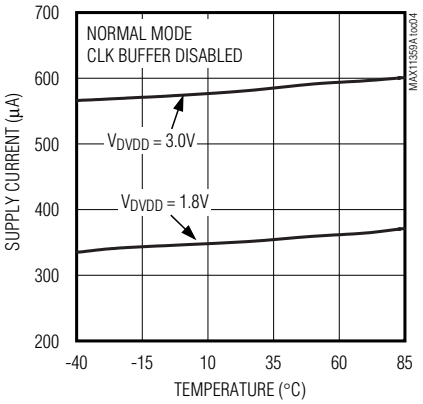
DVDD SUPPLY CURRENT vs. DVDD SUPPLY VOLTAGE



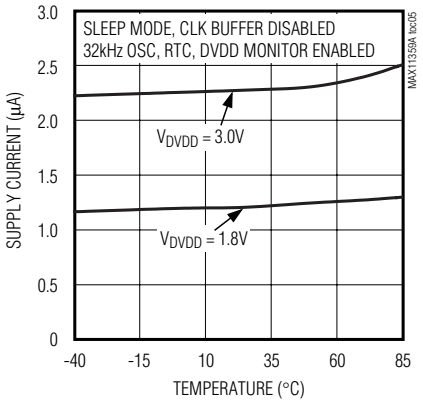
Typical Operating Characteristics (continued)

(V_{DVDD} = V_{AVDD} = 1.8V, V_{REF} = +1.25V, C_{CPOUT} = 10µF, T_A = +25°C, unless otherwise noted.)

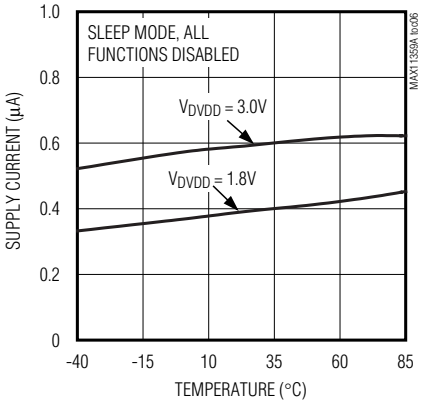
DVDD SUPPLY CURRENT vs. TEMPERATURE



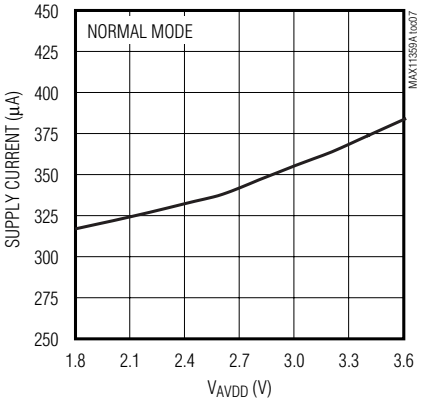
DVDD SUPPLY CURRENT vs. TEMPERATURE



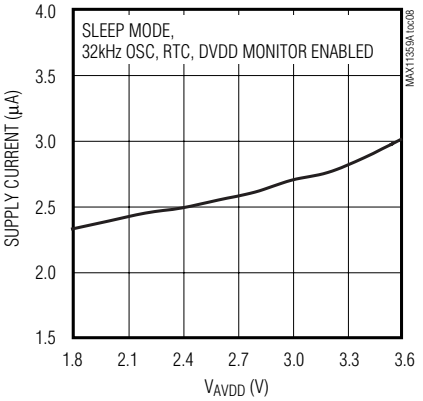
DVDD SUPPLY CURRENT vs. TEMPERATURE



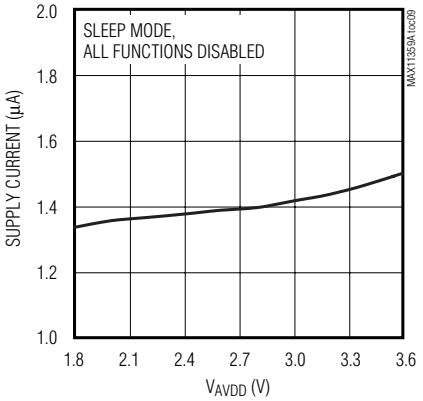
AVDD SUPPLY CURRENT vs. AVDD SUPPLY VOLTAGE



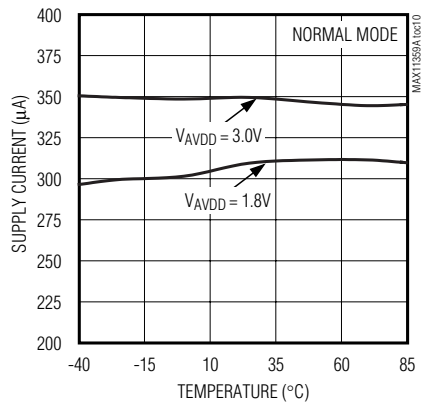
AVDD SUPPLY CURRENT vs. AVDD SUPPLY VOLTAGE



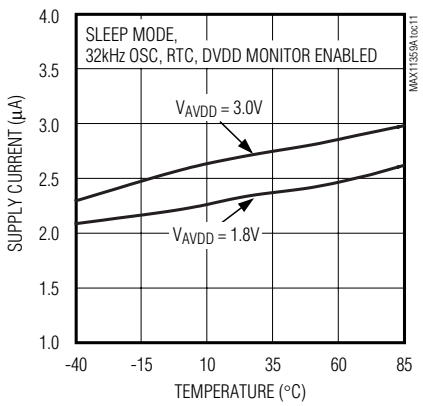
AVDD SUPPLY CURRENT vs. AVDD SUPPLY VOLTAGE



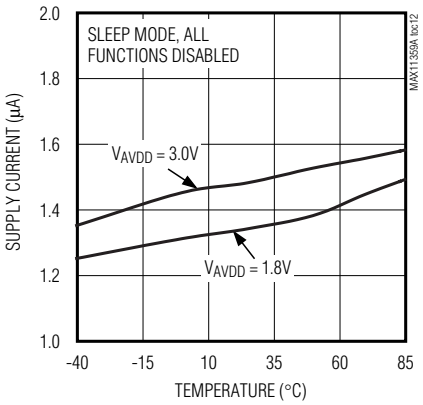
AVDD SUPPLY CURRENT vs. TEMPERATURE



AVDD SUPPLY CURRENT vs. TEMPERATURE



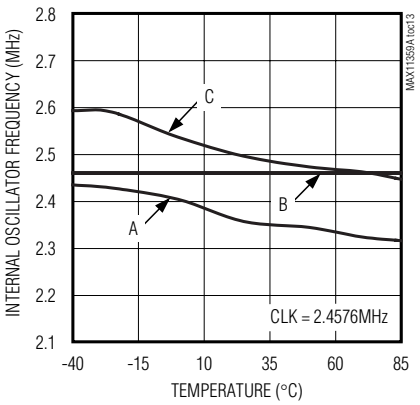
AVDD SUPPLY CURRENT vs. TEMPERATURE



Typical Operating Characteristics (continued)

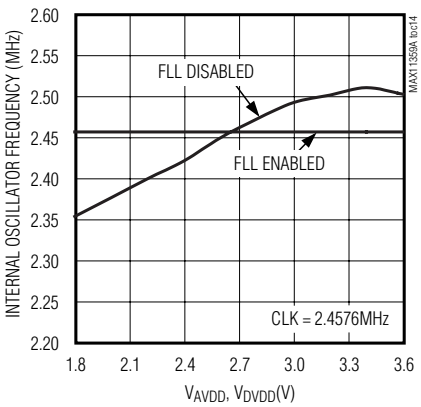
(V_{DVDD} = V_{AVDD} = 1.8V, V_{REF} = +1.25V, C_{CPOUT} = 10µF, T_A = +25°C, unless otherwise noted.)

INTERNAL OSCILLATOR FREQUENCY vs. TEMPERATURE

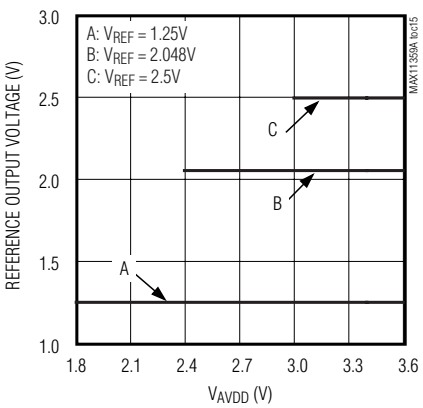


A: FLL DISABLED; V_{AVDD}, V_{DVDD} = 1.8V
B: FLL ENABLED
C: FLL DISABLED; V_{AVDD}, V_{AVDD} = 3.0V

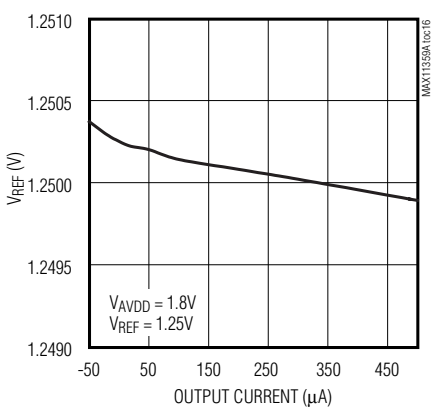
INTERNAL OSCILLATOR FREQUENCY vs. SUPPLY VOLTAGE



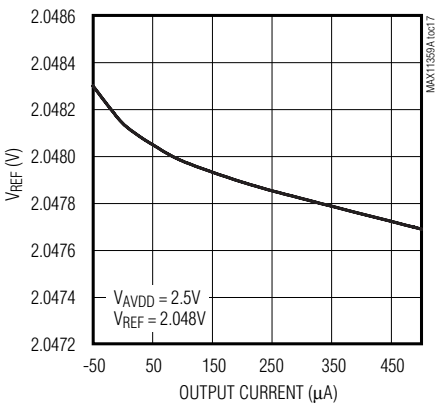
REFERENCE OUTPUT VOLTAGE vs. SUPPLY VOLTAGE



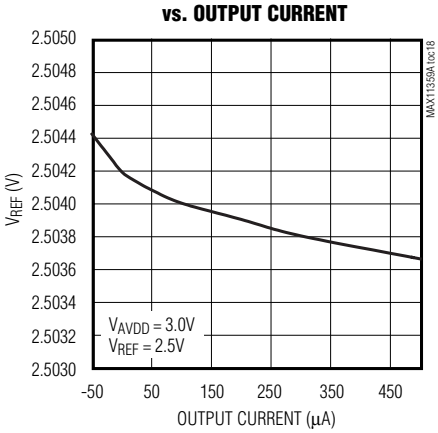
REFERENCE OUTPUT VOLTAGE vs. OUTPUT CURRENT



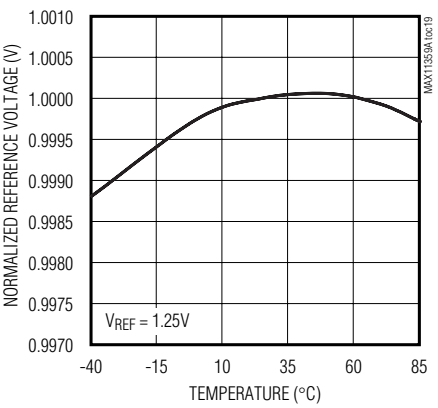
REFERENCE OUTPUT VOLTAGE vs. OUTPUT CURRENT



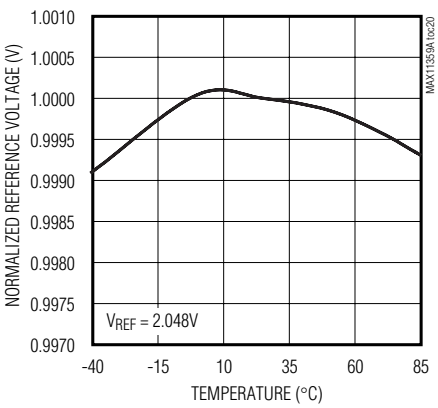
REFERENCE OUTPUT VOLTAGE vs. OUTPUT CURRENT



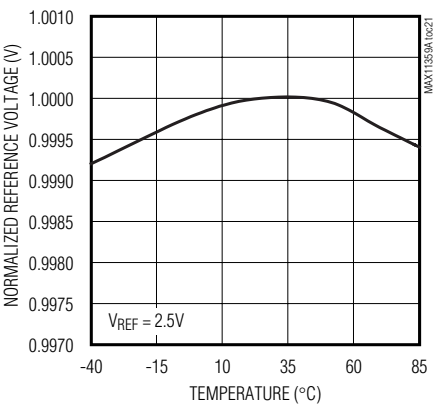
NORMALIZED REFERENCE OUTPUT VOLTAGE vs. TEMPERATURE



NORMALIZED REFERENCE OUTPUT VOLTAGE vs. TEMPERATURE



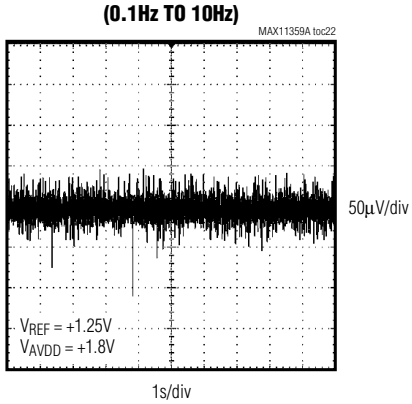
NORMALIZED REFERENCE OUTPUT VOLTAGE vs. TEMPERATURE



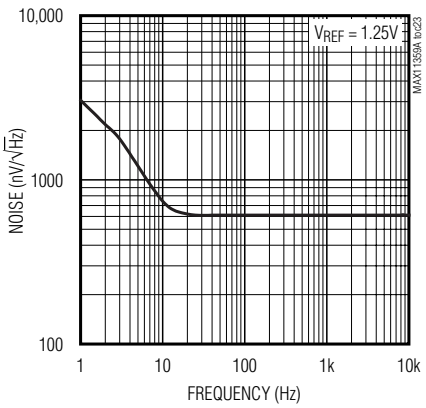
Typical Operating Characteristics (continued)

(V_{DVDD} = V_{AVDD} = 1.8V, V_{REF} = +1.25V, C_{CPOUT} = 10µF, T_A = +25°C, unless otherwise noted.)

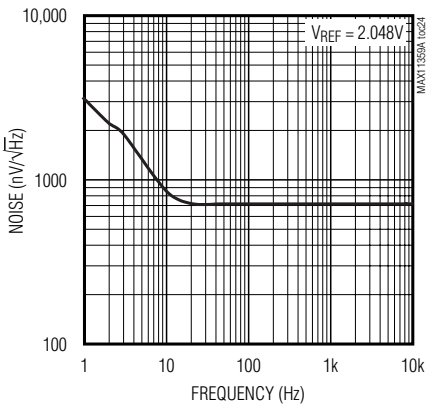
REFERENCE VOLTAGE OUTPUT NOISE (0.1Hz TO 10Hz)



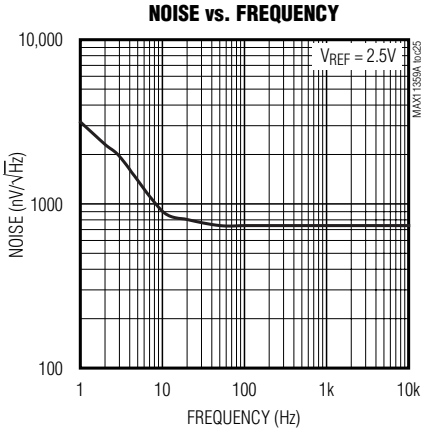
REFERENCE VOLTAGE OUTPUT NOISE vs. FREQUENCY



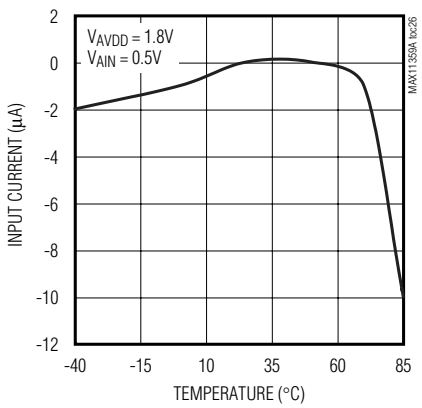
REFERENCE VOLTAGE OUTPUT NOISE vs. FREQUENCY



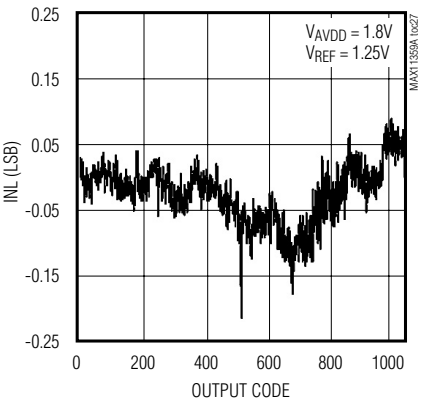
REFERENCE VOLTAGE OUTPUT NOISE vs. FREQUENCY



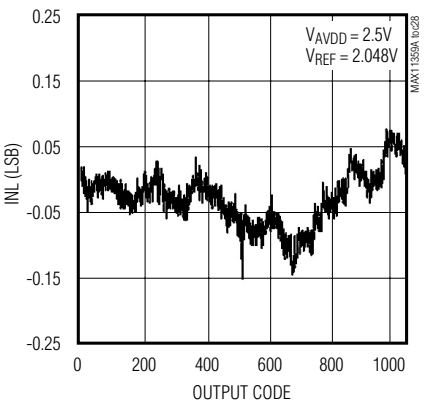
ADC MUX INPUT DC CURRENT vs. TEMPERATURE



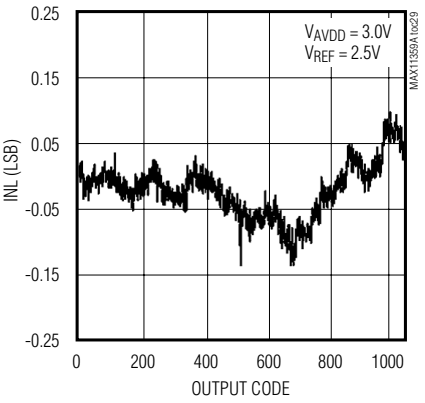
DAC INL vs. OUTPUT CODE



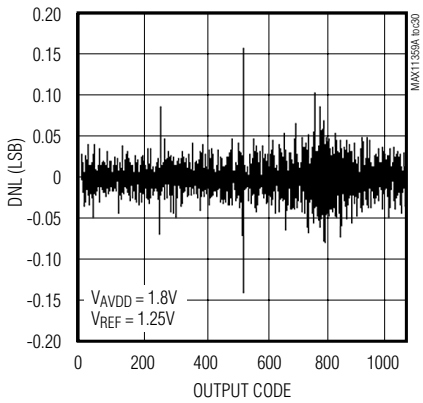
DAC INL vs. OUTPUT CODE



DAC INL vs. OUTPUT CODE



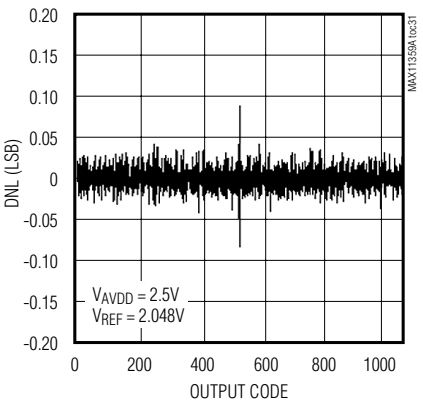
DAC DNL vs. OUTPUT CODE



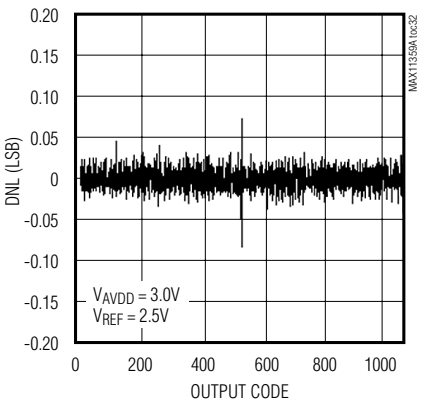
Typical Operating Characteristics (continued)

(V_{DVDD} = V_{AVDD} = 1.8V, V_{REF} = +1.25V, C_{CPOUT} = 10µF, T_A = +25°C, unless otherwise noted.)

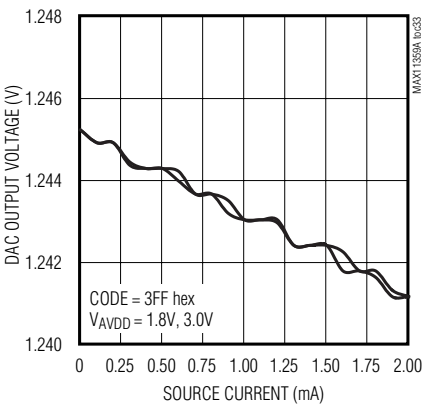
DAC DNL vs. OUTPUT CODE



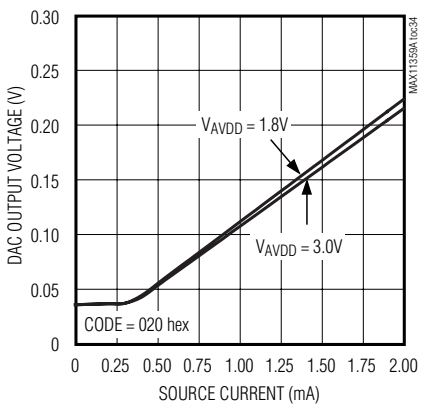
DAC DNL vs. OUTPUT CODE



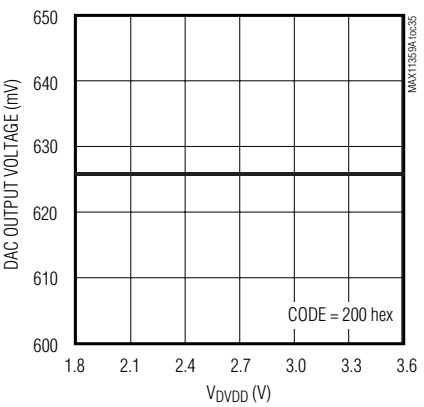
DAC OUTPUT VOLTAGE vs. OUTPUT SOURCE CURRENT



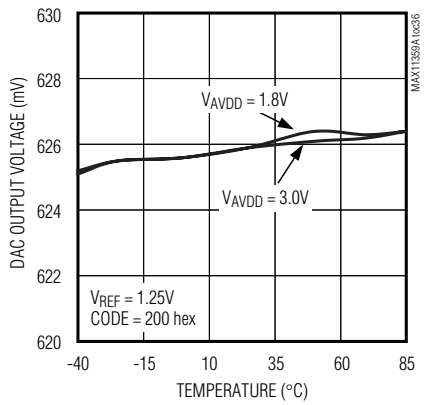
DAC OUTPUT VOLTAGE vs. OUTPUT SINK CURRENT



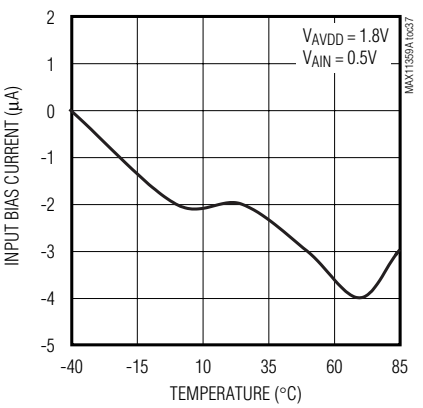
DAC OUTPUT VOLTAGE vs. ANALOG SUPPLY VOLTAGE



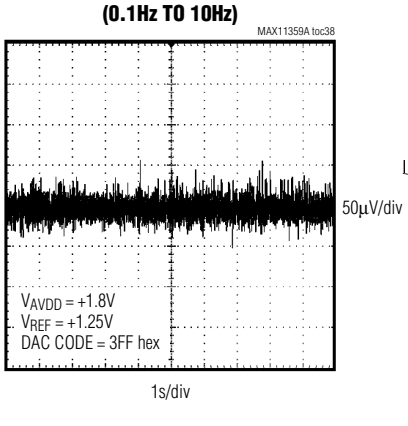
DAC OUTPUT VOLTAGE vs. TEMPERATURE



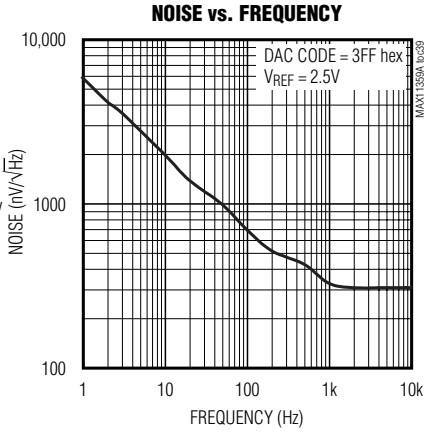
DAC FBA/B INPUT BIAS CURRENT vs. TEMPERATURE



DAC OUTPUT NOISE (0.1Hz TO 10Hz)



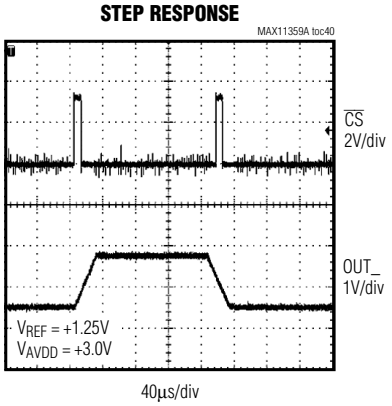
DAC OUTPUT NOISE vs. FREQUENCY



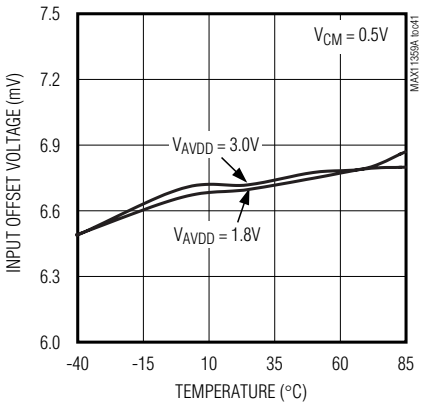
Typical Operating Characteristics (continued)

(V_{DVDD} = V_{AVDD} = 1.8V, V_{REF} = +1.25V, C_{CPOUT} = 10µF, T_A = +25°C, unless otherwise noted.)

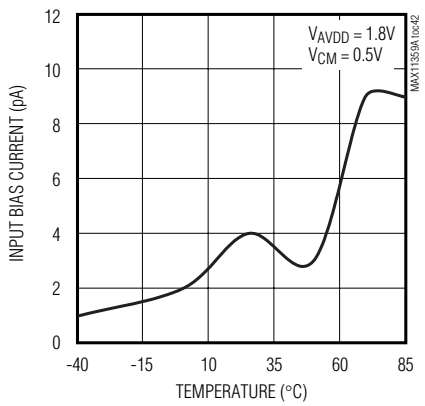
DAC LARGE-SIGNAL OUTPUT STEP RESPONSE



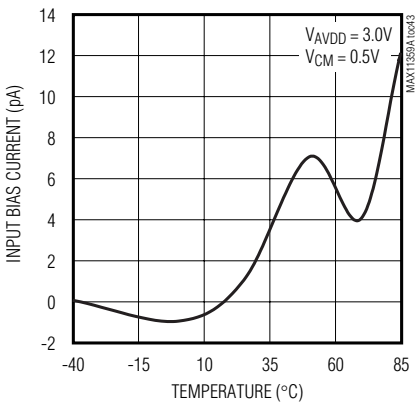
OP-AMP INPUT OFFSET VOLTAGE vs. TEMPERATURE



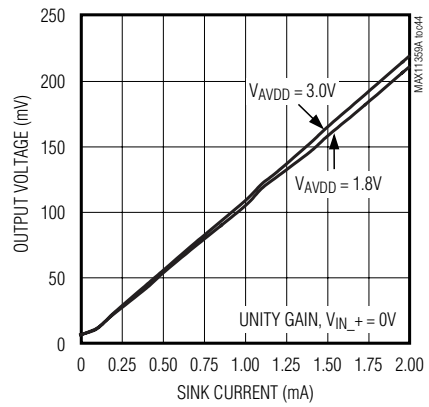
OP-AMP INPUT BIAS CURRENT vs. TEMPERATURE



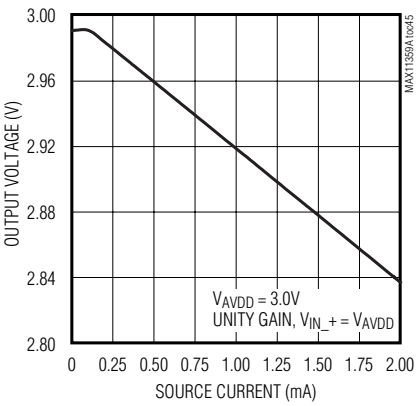
OP-AMP INPUT BIAS CURRENT vs. TEMPERATURE



OP-AMP OUTPUT VOLTAGE vs. OUTPUT SINK CURRENT



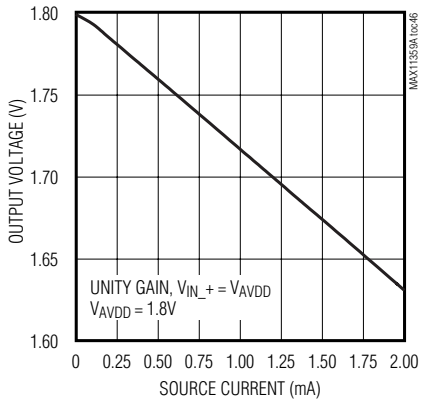
OP-AMP OUTPUT VOLTAGE vs. OUTPUT SOURCE CURRENT



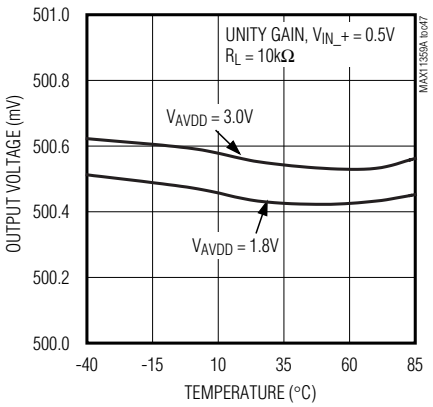
Typical Operating Characteristics (continued)

(V_{DVDD} = V_{AVDD} = 1.8V, V_{REF} = +1.25V, C_{CPOUT} = 10µF, T_A = +25°C, unless otherwise noted.)

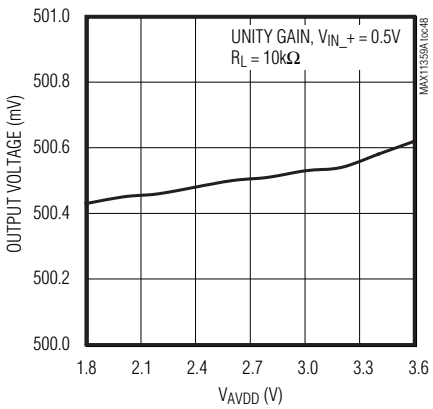
OP-AMP OUTPUT VOLTAGE vs. OUTPUT SOURCE CURRENT



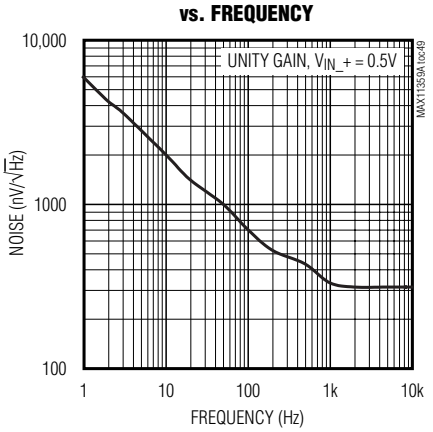
OP-AMP OUTPUT VOLTAGE vs. TEMPERATURE



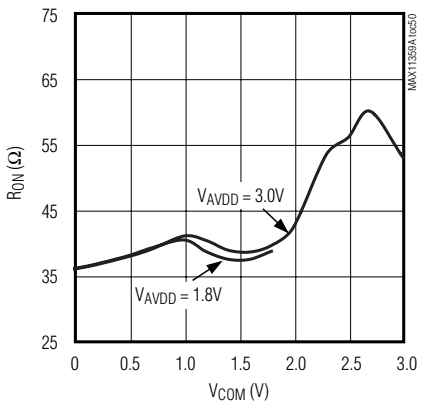
OP-AMP OUTPUT VOLTAGE vs. AV_{DD} SUPPLY VOLTAGE



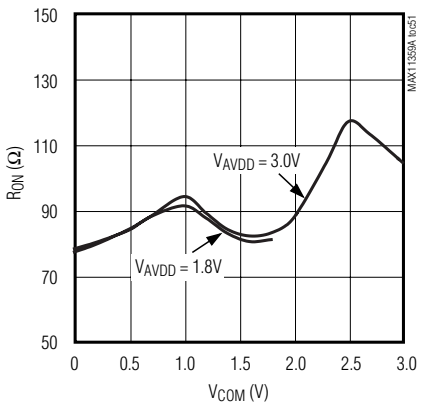
OP-AMP OUTPUT NOISE vs. FREQUENCY



SPDT ON-RESISTANCE vs. V_{COM} VOLTAGE



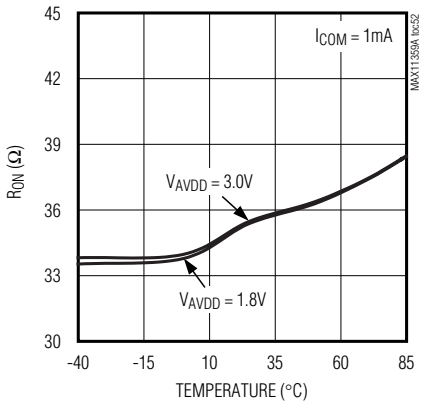
SPST ON-RESISTANCE vs. V_{COM} VOLTAGE



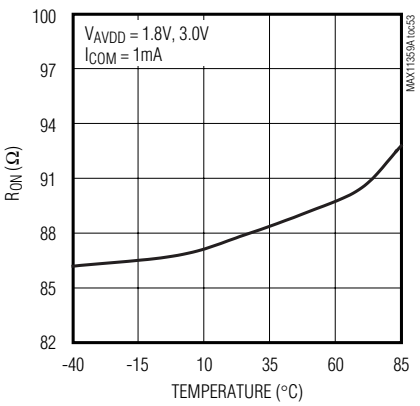
Typical Operating Characteristics (continued)

(V_{DVDD} = V_{AVDD} = 1.8V, V_{REF} = +1.25V, C_{CPOUT} = 10µF, T_A = +25°C, unless otherwise noted.)

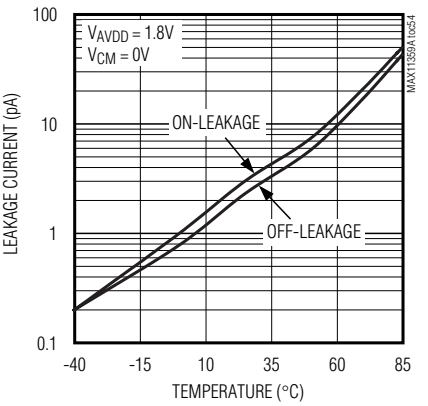
SPDT ON-RESISTANCE vs. TEMPERATURE



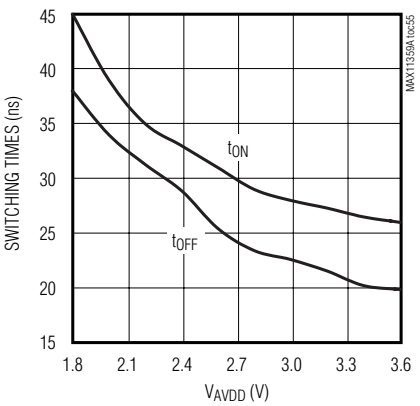
SPST ON-RESISTANCE vs. TEMPERATURE



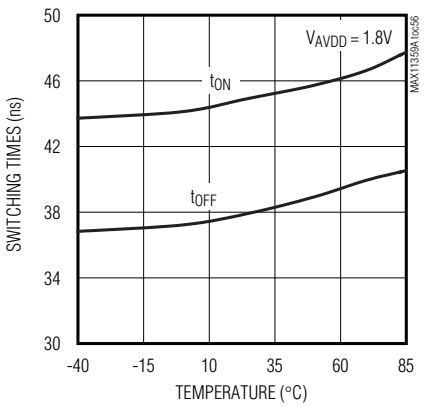
SPDT/SPST ON-/OFF-LEAKAGE CURRENT vs. TEMPERATURE



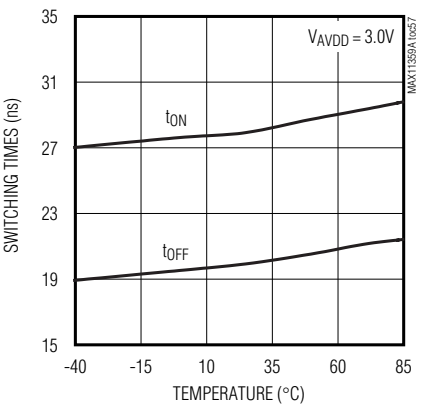
SPDT/SPST SWITCHING TIME vs. AVDD SUPPLY VOLTAGE



SPDT/SPST SWITCHING TIME vs. TEMPERATURE



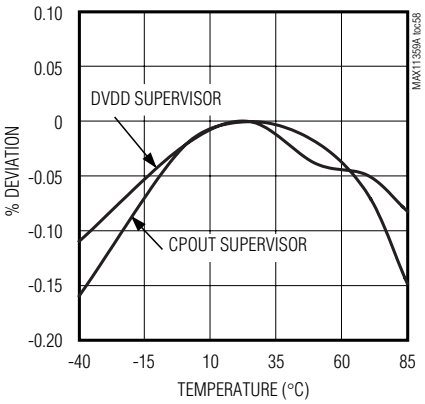
SPDT/SPST SWITCHING TIME vs. TEMPERATURE



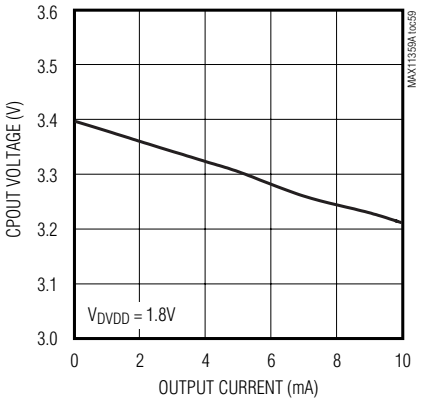
Typical Operating Characteristics (continued)

(V_{DVDD} = V_{AVDD} = 1.8V, V_{REF} = +1.25V, C_{CPOUT} = 10µF, T_A = +25°C, unless otherwise noted.)

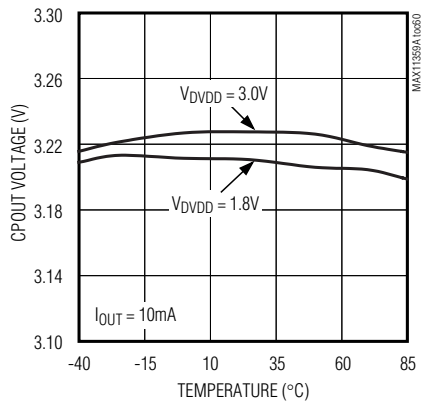
VOLTAGE SUPERVISOR THRESHOLD vs. TEMPERATURE



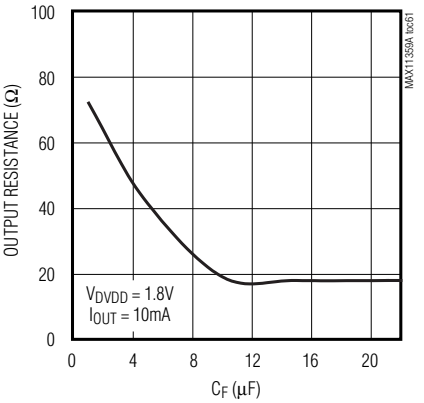
CHARGE-PUMP OUTPUT VOLTAGE vs. OUTPUT CURRENT



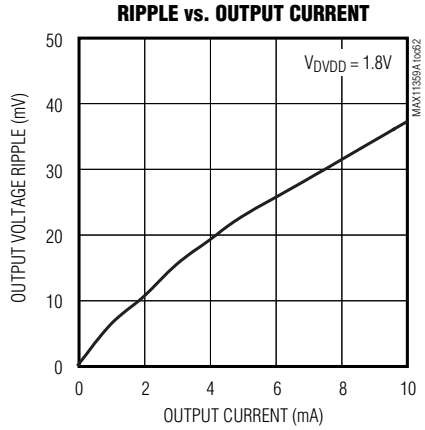
CHARGE-PUMP OUTPUT VOLTAGE vs. TEMPERATURE



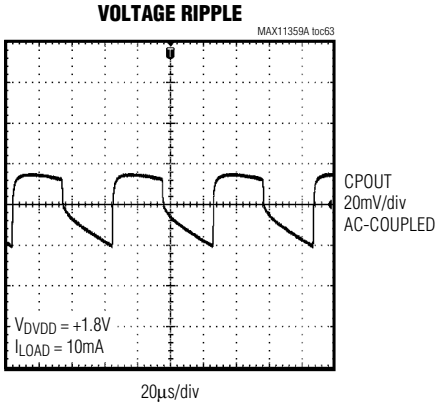
CHARGE-PUMP OUTPUT RESISTANCE vs. CAPACITANCE



CHARGE-PUMP OUTPUT VOLTAGE RIPPLE vs. OUTPUT CURRENT



CHARGE-PUMP OUTPUT VOLTAGE RIPPLE



Pin Description

PIN	NAME	FUNCTION
1	CLK	Clock Output. Default is 2.457MHz output clock for µC.
2	UPIO2	User-Programmable Input/Output 2. See the *UPIO2_CTRL Register* section for functionality.
3	UPIO3	User-Programmable Input/Output 3. See the *UPIO3_CTRL Register* section for functionality.
4	UPIO4	User-Programmable Input/Output 4. See the *UPIO4_CTRL Register* section for functionality.
5	DOUT	Serial-Data Output. Data is clocked out on SCLK's falling edge. High impedance when $\overline{CS}$ is high. When UPIO/SPI passthrough mode is enabled, DOUT mirrors the state of UPIO1.
6	SCLK	Serial-Clock Input. Clocks data in and out of the serial interface.
7	DIN	Serial-Data Input. Data is clocked in on SCLK's rising edge.
8	$\overline{CS}$	Active-Low Chip-Select Input. Data is not clocked into DIN unless $\overline{CS}$ is low. When $\overline{CS}$ is high, DOUT is high impedance. High impedance when $\overline{CS}$ is high. When UPIO/SPI passthrough mode is enabled, DOUT mirrors the state of UPIO1.
9	INT	Programmable Active-High/Low Interrupt Output. ADC, UPIO wake-up, alarm, and voltage-monitor events.
10	CLK32K	32kHz Clock Input/Output. Outputs 32kHz clock for µC. Can be programmed as an input by enabling the IO32E bit to accept an external 32kHz input clock. The RTC, PWM, and watchdog timer always use the internal 32kHz clock derived from the 32kHz crystal.
11	$\overline{RESET}$	Active-Low Open-Drain Reset Output. Remains low while DVDD is below the 1.8V voltage threshold, and stays low for a timeout period (t_{DSLP}) after DVDD rises above the 1.8V threshold. $\overline{RESET}$ also pulses low when the watchdog timer times out and holds low during POR until the 32kHz oscillator stabilizes.
12	32KOUT	32kHz Crystal Output. Connect external 32kHz watch crystal between 32KIN and 32KOUT.
13	32KIN	32kHz Crystal Input. Connect external 32kHz watch crystal between 32KIN and 32KOUT or drive with CMOS level as shown in Figure 25.
14	SNO1	Analog Switch 1 Normally Open Terminal. Analog input to mux.
15	SCM1	Analog Switch 1 Common Terminal. Analog input to mux.
16	SNC1	Analog Switch 1 Normally Closed Terminal. Analog input to mux (open on POR).
17	SNO2	Analog Switch 2 Normally Open Terminal. Analog input to mux.
18	SCM2	Analog Switch 2 Common Terminal. Analog input to mux (open on POR).
19	SNC2	Analog Switch 2 Normally Closed Terminal. Analog input to mux.
20	OUT1	Amplifier 1 Output. Analog input to mux.
21	IN1-	Amplifier 1 Inverting Input. Analog input to mux.
22	IN1+	Amplifier 1 Noninverting Input
23	SWA	DACA SPST Shunt Switch Input. Connects to OUTA through a SPST switch.
24	FBA	DACA Force-Sense Feedback Input. Analog input to mux.

Pin Description (continued)

PIN	NAME	FUNCTION
25	OUTA	DACA Force-Sense Output. Analog input to mux.
26	AGND	Analog Ground
27	AVDD	Analog Supply Voltage. Also ADC reference voltage during AVDD measurement. Bypass to AGND with 10µF and 0.1µF capacitors in parallel as close to the pin as possible.
28	IN2+	Amplifier 2 Noninverting Input
29	IN2-	Amplifier 2 Inverting Input. Analog input to mux.
30	OUT2	Amplifier 2 Output. Analog input to mux.
31	AIN2	Analog Input 2. Analog input to mux. Inputs have internal programmable current source for external temperature measurement.
32	AIN1	Analog Input 1. Analog input to mux. Inputs have internal programmable current source for external temperature measurement.
33	REF	Reference Input/Output. Output of the reference buffer amplifier or external reference input. Disabled at power-up to allow external reference. Reference voltage for ADC and DAC.
34	REG	Linear Voltage-Regulator Output. Charge-pump-doubler input voltage. Bypass REG with a 10µF capacitor to DGND for charge-pump regulation.
35	CF-	Charge-Pump Flying Capacitor Terminals. Connect an external 10µF (typ) capacitor between CF+ and CF-.
36	CF+	
37	CPOUT	Charge-Pump Output. Connect an external 10µF (typ) reservoir capacitor between CPOUT and DGND. There is a low threshold diode between DVDD and CPOUT. When the charge pump is disabled, CPOUT is pulled up within 300mV (typ) of DVDD.
38	DVDD	Digital Supply Voltage. Bypass to DGND with 10µF and 0.1µF capacitors in parallel as close to the pin as possible.
39	DGND	Digital Ground. Also ground for cascaded linear voltage regulator and charge-pump doubler.
40	UPIO1	User-Programmable Input/Output 1. See the *UPIO1_CTRL Register* for functionality.
—	EP	Exposed Pad. Leave unconnected or connect to AGND.

Detailed Description

The MAX11359A DAS features a multiplexed differential 16-bit ADC, 10-bit force-sense DACs, an RTC with an alarm, a selectable bandgap voltage reference, a signal-detect comparator, 1.8V and 2.7V voltage monitors, and wake-up control circuitry, all controlled by a 4-wire serial interface (See Figure 3 for the functional diagram).

The DAS directly interfaces to various sensor outputs and, once configured, provides the stimulus, signal conditioning, and data conversion, as well as µP support. See the *Applications* section for sample MAX11359A applications.

The 16-bit ADC features programmable continuous conversion rates as shown in Table 4, and gains of 1, 2, 4, and 8 (Table 5) to suit applications with different power

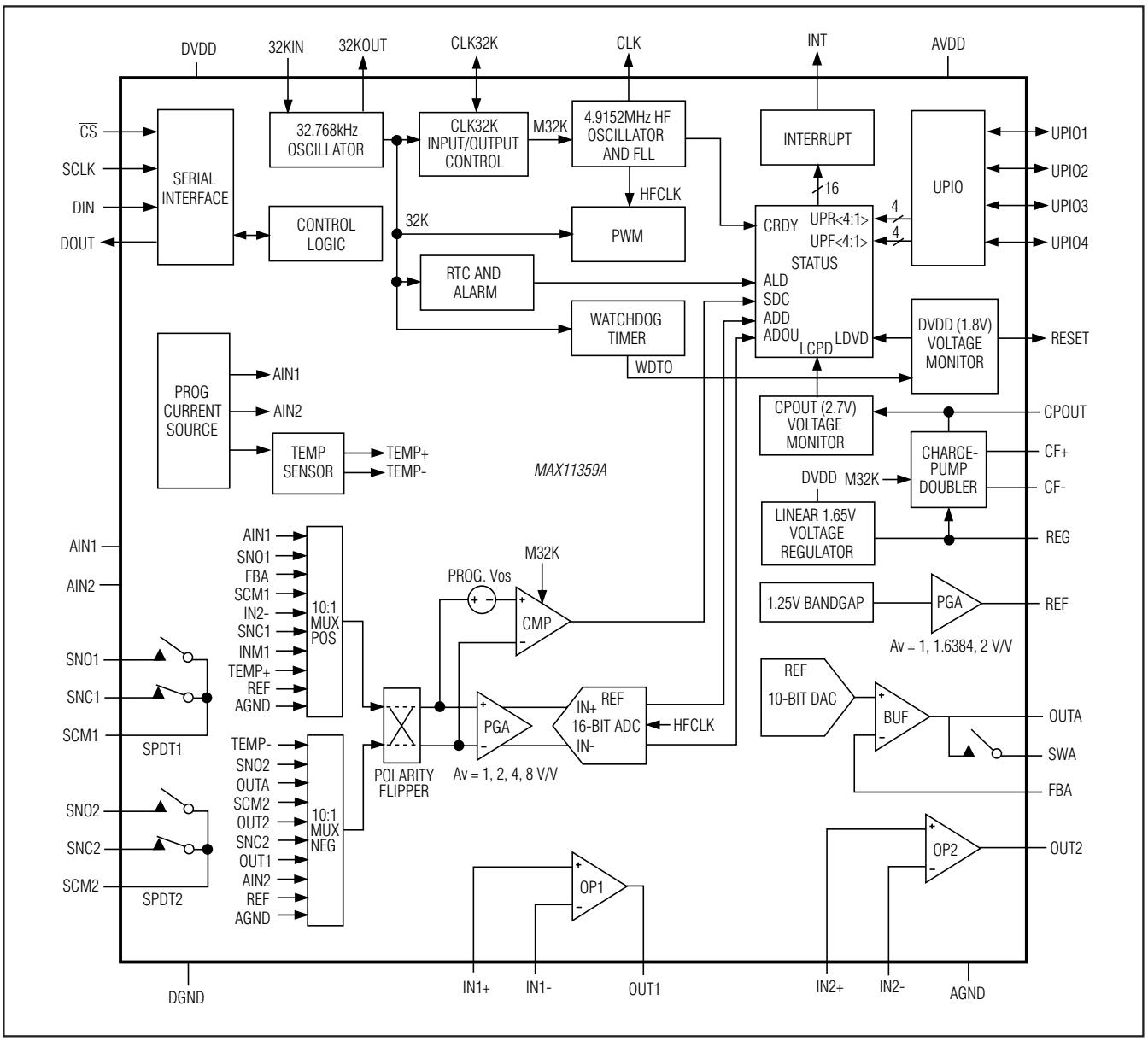


Figure 3. MAX11358B Functional Diagram

and dynamic range constraints. The force-sense DAC provides 10-bit resolution for precise sensor applications. The ADC and DACs both utilize a low-drift 1.25V internal bandgap reference for conversions and full-scale range setting. The RTC has a 138-year range and provides an alarm function that can be used to wake up the system or cause an interrupt at a predefined time. The power-supply voltage monitor detects when DVDD falls below a trip threshold voltage of +1.8V and asserts $\overline{\text{RESET}}$. The MAX11359A uses a 4-wire serial interface to communicate directly between SPI, QSPI, or MICROWIRE devices for system configuration and readback functions.

Analog-to-Digital Converter (ADC)

The MAX11359A includes a sigma-delta ADC with programmable conversion rate, a PGA, and a dual 10:1 input mux. When performing continuous conversions at 10sps or single conversions at the 40sps setting (effectively 10sps due to four sample sigma-delta settling), the ADC has 16-bit noise-free resolution. The noise-free resolution drops to 10 bits at the maximum sampling rate of 512sps. Differential inputs support unipolar (between 0 and V_{REF}) and bipolar (between $\pm V_{REF}$) modes of operation. **Note:** Avoid combinations of input signal and PGA gains that exceed the reference range at the ADC input. The ADOU bit in the status register indicates if the ADC has overranged or underranged.

Zero-scale and full-scale calibrations remove offset and gain errors. Direct access to gain and zero-scale calibration registers allows system-level offset and gain calibration. The zero-scale adjustment register allows intentional positive offset skewing to preserve unipolar-mode resolution for signals that have a slight negative offset (i.e., unipolar clipping near zero can be removed). Perform ADC calibration whenever the ADC configuration, temperature, or AVDD changes. The ADC-done status can be programmed to provide an interrupt on INT or on any UPIO_.

PGA Gain

An integrated PGA provides four selectable gains: +1V/V, +2V/V, +4V/V, and +8V/V to maximize the dynamic range of the ADC. Bits GAIN1 and GAIN0 set the gain (see the *ADC Register* for more information). The PGA gain is implemented in the digital filter of the ADC.

ADC Modulator

The MAX11359A performs analog-to-digital conversions using a single-bit, 3rd-order, switched-capacitor sigma-delta modulator. The sigma-delta modulation converts the input signal into a digital pulse train whose average duty cycle represents the digitized signal information. The pulse train is then processed by a digital decimation filter. The modulator provides 2nd-order frequency shaping of the quantization noise resulting from the single-bit quantizer. The modulator is fully differential for maximum signal-to-noise ratio and minimum susceptibility to power-supply noise.

Signal-Detect Comparator

INT asserts (and remains asserted) within 30µs when the differential voltage on the selected analog inputs exceeds the signal-detect comparator trip threshold. The signal-detect comparator's differential input trip threshold (i.e., offset) is user selectable and can be programmed to the following values: 0mV, 50mV, 100mV, 150mV, or 200mV.

Analog Inputs

The ADC provides two external analog inputs: AIN1 and AIN2. The rail-to-rail inputs accept differential or single-ended voltages, or external temperature-sensing diodes. The unused op amps, switches, or DAC inputs and output pins can also be used as rail-to-rail analog inputs if the associated function is disabled.

Analog Input Protection

Internal protection diodes clamp the analog inputs to AVDD and AGND, and allow the channel input to swing from (V_{AVDD} - 0.3V) to (V_{AVDD} + 0.3V). For accurate conversions near full scale, the inputs must not exceed AV_{DD} by more than 50mV or be lower than AGND by 50mV. If the inputs exceed (V_{AGND} - 0.3V) to (V_{AVDD} + 0.3V), limit the current to 50mA.

Analog Mux

The MAX11359A includes a dual 10:1 mux for the positive and negative inputs of the ADC. Figure 3 illustrates which signals are present at the inputs of each mux for the MAX11359A. The MUXP[3:0] and MUXN[3:0] bits of the mux register select the input to the ADC and the signal-detect comparator (Tables 8 and 9). See the mux register description in the *Register Definitions* section for multiplexer functionality. The POL bit of the ADC register swaps the polarity of mux output signals to the ADC.