### imall

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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832 Email & Skype: info@chipsmall.com Web: www.chipsmall.com Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



### Evaluates: MAX11905

### **General Description**

The MAX11905 differential evaluation kit (EV kit) demonstrates the MAX11905, 20-bit, 1.6Msps, single-channel, fully differential SAR ADC with internal reference buffers. The EV kit uses the MAX44205, a low-noise fully differential operational amplifier. The EV kit includes a graphical user interface (GUI) that provides communication from Avnet's ZedBoard™ development board for the Xilinx Zynq®-7000 SoC. The ZedBoard, not included with the EV kit, must be purchased through Avnet, Inc.

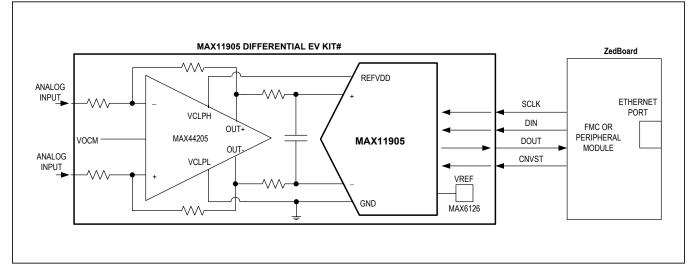
The ZedBoard communicates with the PC through an Ethernet cable using Windows XP<sup>®</sup>-, Windows Vista<sup>®</sup>-, Windows<sup>®</sup> 7-, or Windows 8/8.1-compatible software.

The EV kit comes with the MAX11905ETP+ installed.

### **Features**

- Peripheral Module and FMC Connector for Interface
- 75MHz SPI Clock Capability through FMC Connector
- 37.5MHz SPI Clock Capability through Peripheral Module Connector
- Sync In and Sync Out for Coherent Sampling
- On-Board Input Buffer (MAX44205)
- On-Board +3.0V Reference Voltage (MAX6126)
- Windows XP-, Windows Vista-, Windows 7-, and Windows 8/8.1-Compatible Software

Ordering Information appears at end of data sheet.



### System Block Diagram

ZedBoard is a trademark of Avnet, Inc.

Zynq is a registered trademark of Xilinx, Inc.

Windows, Windows XP, and Windows Vista are registered trademarks and registered service marks of Microsoft Corporation.



### Evaluates: MAX11905

### **Quick Start**

### **Required Equipment**

- MAX11905 differential EV kit with SD card
- ZedBoard development board (includes Micro-USB A-to-B cables)
- Windows PC
- Ethernet cable
- +5V DC power supply
- ±5V dual DC power supply
- Signal generator with differential outputs (e.g., Audio Precision 2700 series)
- Soldering iron and 2-pin, 2.54 header

**Note:** In the following sections, software-related items are identified by bolding. Text in **bold** refers to items directly from the EV kit software. Text in **bold and underlined** refers to items from the Windows operating system.

### Procedure

The EV kit is fully assembled and tested. Follow the steps below to verify board operation:

- 1) Download the LabVIEW<sup>®</sup> Run-Time Engine 2013 from www.ni.com/download/labview-run-time-engine-2013/4059/en/.
- Visit <u>www.maximintegrated.com/evkitsoftware</u> to download the latest version of the EV kit software, 11905EVKit.ZIP. Save the EV kit software to a temporary folder and uncompress the ZIP file.
- 3) Solder the 2-pin header on J18-3V3 of the ZedBoard.
- Connect the Ethernet cable from the PC to the Zed-Board and configure the Internet Protocol Version 4 (TCP/IPv4) properties in the local area connection to IP address 192.168.1.2 and the subnet mask to 255.255.255.0.

- 5) Connect the USB cable from the PC to the Zed-Board's USB programming connector (J17).
- Verify that the ZedBoard's jumpers JP7, JP8, and JP11 have shunts installed at the GND position, and JP9 and JP10 at the 3V3 position.
- 7) Move the shunt of J18 of the ZedBoard from 1V8 to the 3V3 position.
- 8) Insert the SD card with the boot image (BOOT.bin).
- 9) Verify that all jumpers on the EV kit are in their default positions, as shown in Table 1.
- Connect the ZedBoard to J2 on the EV kit for FMC connection. If the peripheral module is used, the ZedBoard's JA1 connector must be connected to J1 on the EV kit.
- Connect the positive terminal of the +5V supply to the +5V test point and the negative terminal to the GND test point.
- 12) Connect the +5V of the dual supply to the VS+ test point, the -5V supply to the VS- test point, and the ground to the GND test point.
- The configuration of the op amp is gain of 0.5. Set the signal generator to 11.95V<sub>P-P</sub> and 10kHz to the INP and INM SMA connectors or test points on the EV kit.
- 14) Turn on the power to the ZedBoard.
- 15) Turn on all power supplies.
- 16) Enable the function generator.
- 17) Open the EV kit GUI, MAX11905EVKit.exe.
- Verify that the IP Address is 192.168.1.10, the port is 6001, and that the status bar displays TCP/IP Connection to Zedboard is successful and Connected to ZedBoard (MISO = 1).
- 19) Click on the **Set** button within the **Configuration** tab.
- 20) Click on the FFT tab (Figure 6) and start capturing data.

LabVIEW is a registered trademark of National Instruments Corporation.

### Table 1. Jumper Descriptions (JU1–JU14)

JUMPER	SHUNT POSITION	DESCRIPTION
JU1	Installed	Connects to 49.9Ω termination.
	Not installed*	Apply negative end of the differential signal at the INM test point or SMA connector.
JU2	Installed	Connects to 49.9Ω termination.
	Not installed*	Apply positive end of the differential signal at the INP test point or SMA connector.
JU3	1-2*	Connects to VOCM to REF/2.
	2-3	Connects to VOCM to GND.
JU4	Installed*	DVDD supply connects to the on-board +1.8V LDO
	Not installed	User-supplied DVDD. Apply +1.8V at the DVDD test point.
11.15	1-2*	REFIN connects to the on-board +3.0V reference.
JU5	2-3	User-supplied REFIN. Apply reference voltage at the EXT_REFIN test point.
	1-2	Do not use
JU6	2-3*	OVDD supply connects to the on-board +3.3V LDO
	Not installed	User-supplied OVDD. Apply +3.3V at the OVDD test point.
11.17	Installed*	AVDD supply connects to the on-board +1.8V LDO
JU7	Not installed	User-supplied AVDD. Apply +1.8V at the jumper JU7-2 pin.
11.10	Installed*	REFVDD supply connects to the on-board +3.3V LDO.
JU8	Not installed	User-supplied REFVDD. Apply +3.3V at the JU9-2 pin.
	2-3, 5-6, 8-9, 11-12*	Connects the SPI signals coming from the peripheral module or FMC connectors to the MAX11905.
JU9	Not installed	User-supplied SPI. Connect the SPI signals at the SCLK, CNVST, DIN, and DOUT test points.
11.14.0	Installed	Disables the line driver.
JU10	Not installed*	Enables the line driver.
JU11	Installed*	Input common mode voltage set to REF/2.
3011	Not installed	Input common mode voltage set GND.
	1-2*	VCLPH set to MAX11905's REFVDD supply.
JU12	2-3	VCLPH set to MAX44205's VS+ supply.
JU13	1-2*	VCLPL set to GND.
3013	2-3	VCLPL set to MAX44205's VS- supply.
11.11.4	1-2*	SHDN pulled to VS+ and set to normal operation.
JU14	2-3	SHDN pulled to GND and set to shutdown mode.

\*Default position.

### **General Description of Software**

The main window of the MAX11905 EV kit software contains five tabs: **Configuration**, **Scope**, **DMM**, **Histogram**, and **FFT**. The **Configuration** tab sheet provides control to communicate with the ZedBoard, SPI, and the IC registers. The other four tabs are used for evaluating the IC's high-speed ADC.

### **Configuration Tab**

When all connections are made on the system and are fully powered, the **Configuration** tab sheet displays the correct IP address, port, and the lower status bar displays as shown <u>Figure 1</u>. These are all indicators that the system and GUI are ready for communication.

Before proceeding, connect the connector used on the ZedBoard to either the FMC or PMOD connector on the EV kit. If the FMC connector is used, all SCLK frequencies are applicable. If the PMOD connector is used, the maximum allowed frequency is 37.5MHz. For the **Clock Source** selection, the ZedBoard internal clock is always a valid option. If the external clock is selected, an external

clock must be applied at the DCLK\_IN SMA on the EV kit. The **Sync-Out CLK (10MHz)** checkbox is used to synchronize the signal generator with a 10MHz input. See the *Sync Input and Sync Output* section for more information. Once the above configurations are completed, adjust to the desired sampling rate, reference voltage, and number of samples, and then click on the **Set** button.

Also in this tab sheet are the IC register controls. The Mode register is accessible using the controls on the **MAX11905 Mode Register Configuration** group box in the center, or the **Mode** control on the right. All other registers are read-only and are updated by clicking on the appropriate **Read** button. The first and second REF must be shorted on the board to use the REF controls. first REF BUF and second REF BUF are internally set to the same value. The GUI forces these two controls to the same value, regardless of the user's choice.

The **Reset** button resets the firmware, as well as the device. It sends 0x8000 to the Mode register and causes the device to do a power-on reset. The **Set** button needs to be clicked to save the current screen settings.

Configuration Scope DMM	Histogram FFT	 
IP address 192.168.1.10 Clock Source 2 edBoard Internal External Sync-In Sync-Out CLK (10MHz) SCLK Frequency (MHz) 75 Sampling Rate (SPS) 1000000 CNVST HIGH (ns)	Reference Voltage (V)       Number of Samples         3       65536         MAX11905 Mode Register Configuration         MAX11905 Mode Register Configuration         Off/On         Data Format         2's Complement/Offset Binary         Ist REF BUF         Enable/Disable         POR Pass         2nd REF BUF         Enable/Disable         OUT Driver Strength	MAX11905 Registers Write Mode Write MAX11905 Registers Read Mode 0 Read Result 0 Read
0 CNVST LOW (ns) 0 MXX11905 Firmware V4.2 Software v1.0	Save to File Reset Set	Chip ID Chip ID Read Connected to Zedboard (MISO = 1)

Figure 1. MAX11905 EV Kit Main Window (Configuration Tab)

### Evaluates: MAX11905

### Scope Tab

The **Scope** tab sheet is used to capture data and display it in the time domain. Sampling rate and number of samples can also be set in this tab if they were not adjusted appropriately in other tabs. The **Display Unit** drop-down list allows counts and voltages. Once the desired configuration is set, click on the **Capture** button. The right side of the tab sheet displays details of the waveform, such as average, standard deviation, maximum, minimum, and fundamental frequency.

Figure 2 displays the ADC data when differential sinusoidal are applied at the inputs on the EV kit.

### **DMM** Tab

The DMM tab sheet provides the typical information as a digital multimeter. Once the desired configuration is set, click on the **Capture** button.

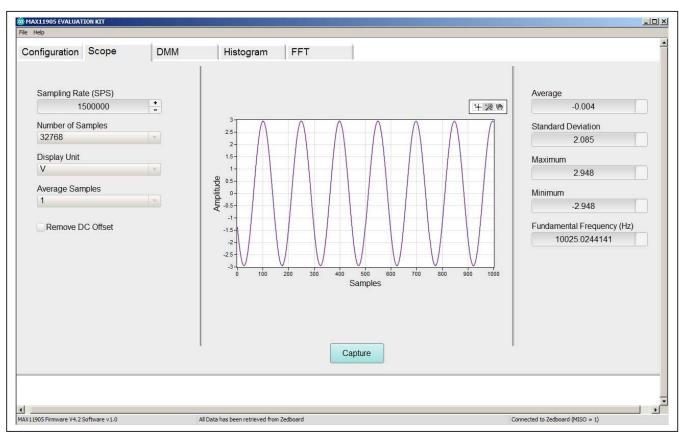


Figure 2. MAX11905 EV Kit Main Window (Scope Tab)

### Evaluates: MAX11905

Figure 3 displays the numerical value when the inputs on the EV kit are shorted to ground using the jumpers (JU1 and JU2). See Table 1 for shunt settings.

### **Histogram Tab**

The **Histogram** tab sheet is used to capture the histogram of the data. Sampling rate and number of samples can also be set in this tab if they were not adjusted appropriately in other tabs. Make sure that the number of samples do not exceed 524,288; otherwise, data capturing is longer than expected. Once the desired configuration is set, click on the **Capture** button. The right side of the tab sheet displays details of the histogram such as average, standard deviation, maximum, minimum, peak-to-peak noise, effective resolution, and noise-free resolution.

To use this histogram feature, apply a DC voltage at the input. Figure 4 displays the results when the input of the EV kit are shorted to ground using jumpers JU1 and JU2. See Table 1 for placement of shunt positions.

MAX11905 EVALUATION KIT le Help		
Configuration Scope DMM	Histogram FFT	
Sampling Rate (SPS) 150000   Isolary Unit V Average Samples Remove DC Offset	Average -0.048 M Standard Deviation before Averaging 0.026 M Standard Deviation after Averaging 0.026 M	-0.154 Fundamental Frequency (Hz) 19409.1796875
	Capture	E)
9		

Figure 3. MAX11905 EV Kit Main Window (DMM Tab)

### Evaluates: MAX11905

### FFT Tab

The **FFT** tab sheet (Figure 6) is used to display the FFT of the data. Sampling rate and number of samples can also be set in this tab if they were not adjusted appropriately in other tabs. When coherent sampling is needed, this tab sheet allows the user to calculate the input frequency or the master clock coming into the board. Either adjust the input frequency applied to the signal generator or adjust the master clock applied to the DCLK\_IN SMA connector. See the *Sync Input and Sync Output* section before using this feature. Once the desired configuration is set, click on the **Capture** button. The right side of the tab sheet displays the performance based on the FFT, such as fundamental frequency, THD, SNR, SINAD, SFDR, ENOB, and noise floor. Figure 5 is the setup Maxim uses to capture data for coherent sampling.

The input signal from the signal generator must be exactly **10000.000000 Hz**. The low-jitter clock is synchronized with the signal generator. The master clock is initially set to **1000000000 Hz**. To achieve coherent sampling, the user must click on the **Calculate** button and use the **Adjusted(Hz)** frequency. **99523158.694 Hz** was entered into our low-jitter clock. The master clock is fed back to the ZedBoard and multiplied by 3/2, then generates a system clock that drives the Xilinx FPGA. All SPI timing and sampling rate are based off the system clock.

**Note:** If the results do not look similar to <u>Figure 6</u> and more similar to <u>Figure 7</u>, then check all connections in Figure 5 to make sure the setup is synchronizing properly.

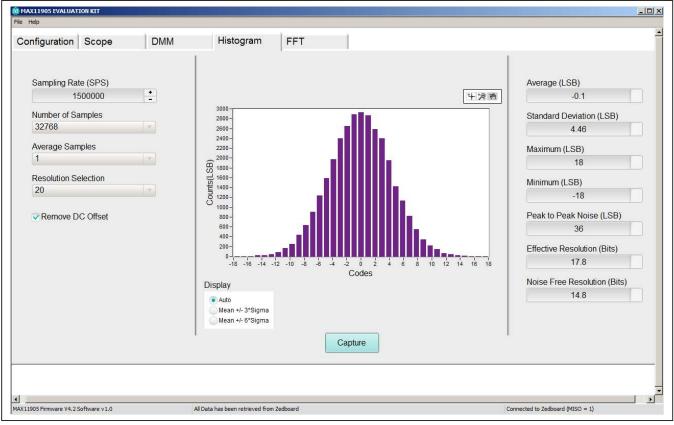


Figure 4. MAX11905 EV Kit Main Window (Histogram Tab)

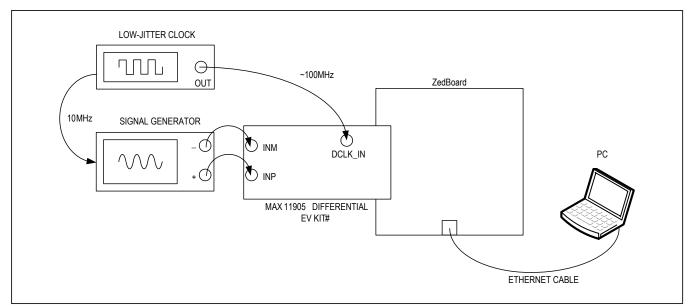


Figure 5. MAX11905 Differential EV Kit Coherent Sampling Setup

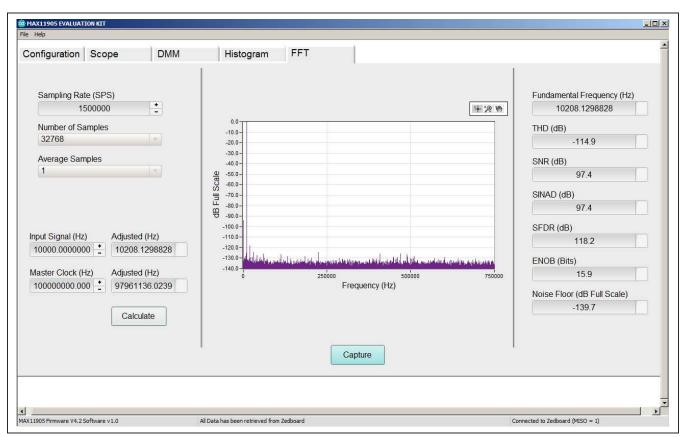


Figure 6. MAX11905 EV Kit Main Window, Coherent Sampling Results (FFT Tab)

1500000         •           Number of Samples         0.0           32768         •           Average Samples         •	Fundamental Frequency (Hz) 9979.24804687
g -co.o-	THD (dB) -49.9 SNR (dB) 14.3 SINAD (dB)
Input Signal (Hz)         Adjusted (Hz)         -100.0 -           10000.0000000 •         10208.1298828         -110.0 -           Master Clock (Hz)         Adjusted (Hz)         -120.0 -           -130.0 -         -140.0 -         -           0         250000         500000	14.3 SFDR (dB) 21.8 ENOB (Bits) 2.1
10000000.000         •         97961136.0239         Frequency (Hz)           Calculate         Capture	Noise Floor (dB Full Scale) -56.7

Figure 7. MAX11905 EV Kit Main Window, Noncoherent Sampling Results (FFT Tab)

### **General Description of Hardware**

The EV kit provides a proven layout to demonstrate the performance of the MAX11905 20-bit SAR ADC. Included in the EV kit are digital isolators, ultra-low-noise LDOs (MAX8510) to all supply pins of the IC, on-board reference (MAX6126), fully differential amplifier (MAX4205) for the analog inputs, and sync-in and sync-out signals for coherent sampling.

### Configuring the MAX44205

Jumpers are included to configure the MAX44205 appropriately. Jumper JU14 shut downs the MAX44205 by placing a shunt in the 2-3 position. Jumper JU11 is used to set the input common-mode voltage to REF/2. Jumper JU3 is used to set the output common-mode voltage to REF/2 by placing a shunt in the 1-2 position. Jumpers JU12 and JU13 are used to set the voltage clamps to protect the analog inputs of the MAX11905 ADC. The default position connects VCLPH to REFVDD and VCLPL to GND.

### **User-Supplied SPI**

To evaluate the EV kit with a user-supplied SPI bus, remove shunts from jumper JU9. Apply the user-supplied SPI signals to the SCLK, CNVST, DIN, and DOUT test points. Make sure the return ground is the same as the IC's ground.

### **User-Supplied REFVDD**

The REFVDD supply is powered through a +3.3V LDO by default. For user-supplied REFVDD, remove the shunt on jumper JU8 and apply +2.7V to +3.6V at JU8-1.

### **User-Supplied AVDD**

The AVDD supply is powered through a +1.8V LDO by default. For user-supplied AVDD, remove the shunt on jumper JU7 and apply +1.7V to +1.9V at JU7-2.

### **User-Supplied DVDD**

The DVDD supply is powered through a +1.8V LDO by default. For user-supplied DVDD, remove the shunt on jumper JU4 and apply +1.7V to +1.9V at JU4-2.

### **User-Supplied OVDD**

The OVDD supply is powered through a +3.3V LDO by default. For user-supplied OVDD, remove the shunt on jumper JU6 and apply +1.5V to +3.6V at JU6-2. Since

there is a supply limitation on the isolators (U3, U18), the OVDD supply should not be powered below +2.7V when the FMC connector or PMOD of the EV kit are being used.

### **User-Supplied REFIN**

The IC uses an on-board +3V reference (MAX6126) by default. For user-supplied REFIN, move the shunt on jumper JU5 to the 2-3 position. Make sure that REFIN is 300mV below REFVDD before applying the reference.

### **Analog Inputs**

Both analog inputs (AIN+ and AIN-) range from 0 to V<sub>REF</sub>. The differential input range is from -V<sub>REF</sub> to +V<sub>REF</sub> and the full-scale range is 2x the V<sub>REF</sub>. The desired input signals are applied at the INP and INM SMAs or test points.

### Sync Input and Sync Output

The DCLK\_IN SMA accepts an approximate 100MHz waveform signal to generate the system clock of the ZedBoard. For maximum performance, use a low-jitter clock that syncs to the user's analog function generator. The SYNC\_OUT SMA outputs a 10MHz square waveform that syncs to the user's analog function generator. Both options are used for coherent sampling of the IC. Only one option should be used at a time. The relationship between  $f_{IN}$ ,  $f_S$ ,  $N_{CYCLES}$ , and  $M_{SAMPLES}$  is given as follows:

$$\frac{f_{IN}}{f_{S}} = \frac{N_{CYCLES}}{M_{SAMPLES}}$$

where:

f<sub>IN</sub> = Input frequency

f<sub>S</sub> = Samping frequency

```
N<sub>CYCLES</sub> = Prime number of cycles in the sampled set
```

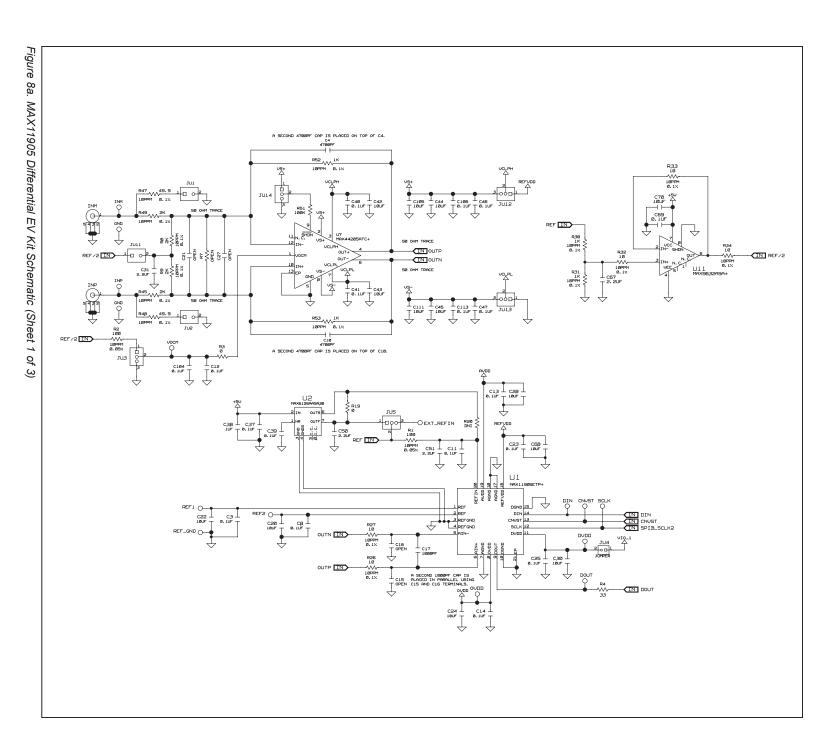
M<sub>SAMPLES</sub> = Total number of samples

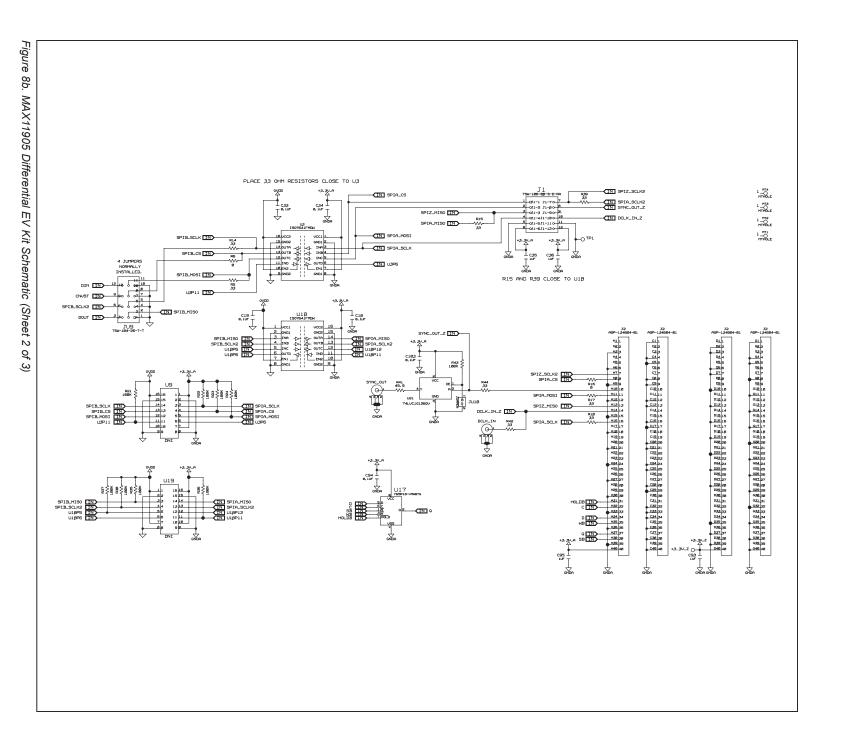
### Interface Connectors

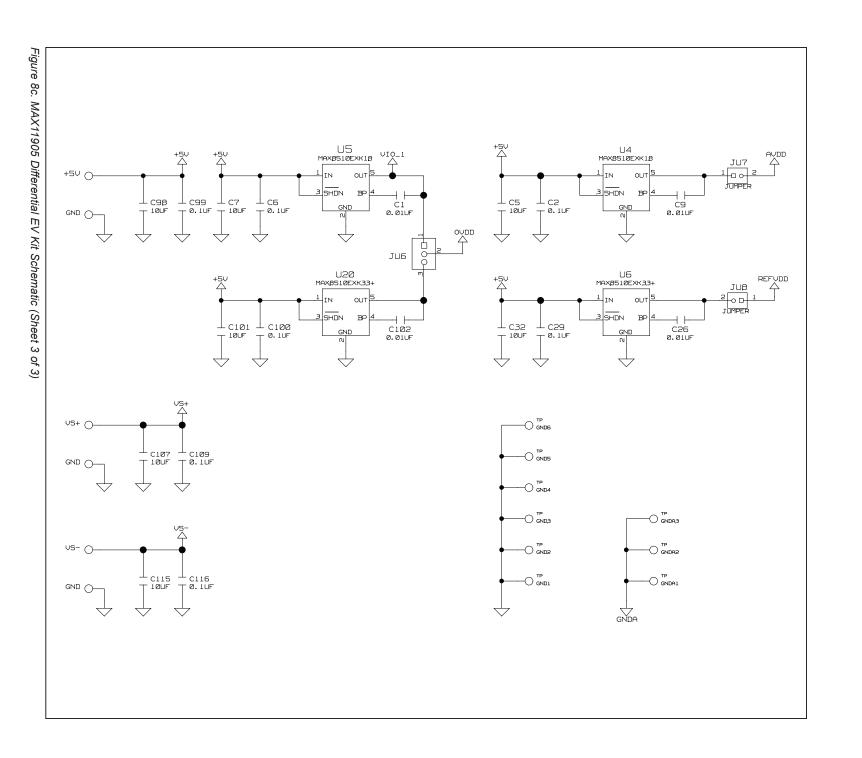
The EV kit and ZedBoard communicate in two ways, using the peripheral module connector (J1) or the FMC connector (J2) on the EV kit. The maximum SPI SCLK frequency is 37.5MHz for the peripheral module connector and 75MHz for the FMC connector.

### **Component List**

Refer to file "evkit\_bom\_max11905DIF\_evkit\_a.csv" attached to this PDF for component information.







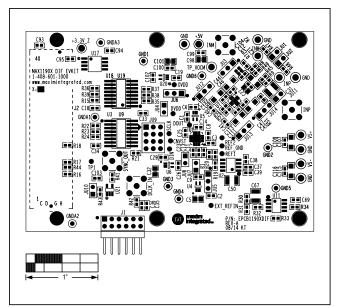


Figure 9. MAX11905 Differential EV Kit Component Placement Guide—Component Side

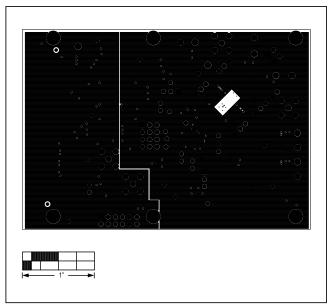


Figure 11. MAX11905 Differential EV Kit PCB Layout—Layer 2

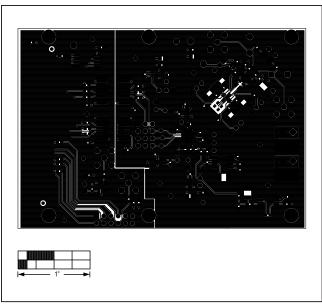


Figure 10. MAX11905 Differential EV Kit PCB Layout— Component Side

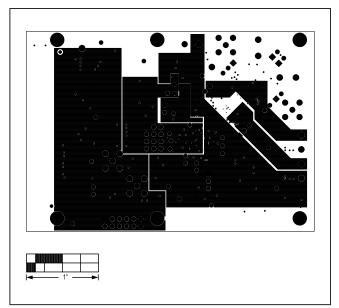


Figure 12. MAX11905 Differential EV Kit PCB Layout—Layer 3

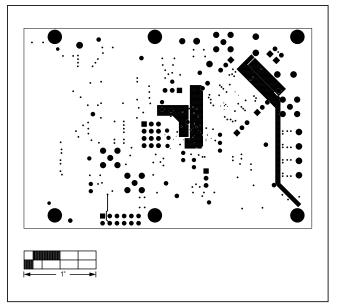


Figure 13. MAX11905 Differential EV Kit PCB Layout—Layer 4

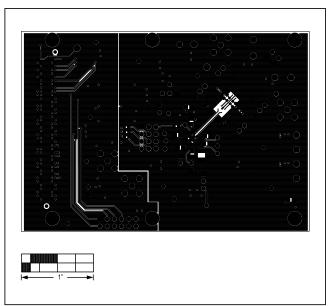


Figure 15. MAX11905 Differential EV Kit PCB Layout—Solder Side

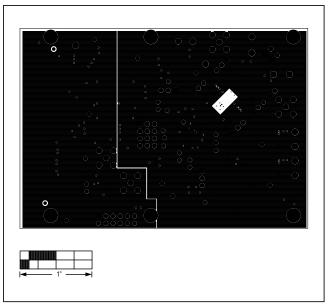


Figure 14. MAX11905 Differential EV Kit PCB Layout—Layer 5

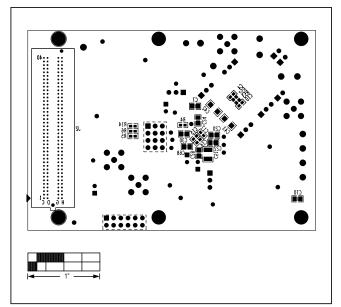


Figure 16. MAX11905 Differential EV Kit Component Placement Guide—Solder Side

### Evaluates: MAX11905

### **Ordering Information**

PART	TYPE
MAX11905DIFEVKIT#	EV Kit

#Denotes RoHS compliant.

### Evaluates: MAX11905

### **Revision History**

REVISION	REVISION	DESCRIPTION	PAGES
NUMBER	DATE		CHANGED
0	12/14	Initial release	—

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim Integrated's website at www.maximintegrated.com.

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