Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

MAX11905 Evaluation Kit

Evaluates: MAX11900, MAX11901, MAX11902, MAX11903, MAX11904, and MAX11905

General Description

The MAX11905 evaluation kit (EV kit) demonstrates the MAX11905, 20-bit, 1.6Msps, single-channel, fully differential SAR ADC with internal reference buffers. The EV kit includes a graphical user interface (GUI) that provides communication from the Avnet ZedBoard™ development board for the Xilinx® Zynq®-7000 SoC.

The ZedBoard communicates with the PC through an Ethernet cable using Windows XP®-, Windows Vista®-, Windows® 7-, or Windows 8/8.1-compatible software.

The EV kit comes with the MAX11905ETP+ installed.

Please contact the factory for the pin-compatible MAX11900ETP+ (16-bit, 1Msps), MAX11901ETP+ (16-bit, 1.6Msps), MAX11902ETP+ (18-bit, 1Msps), MAX11903ETP+ (18-bit, 1.6Msps), and MAX11904ETP+ (20-bit, 1Msps)

ZedBoard is a trademark of Avnet, Inc.

Xilinx and Zynq are registered trademarks and Xilinx is a registered service mark of Xilinx, Inc.

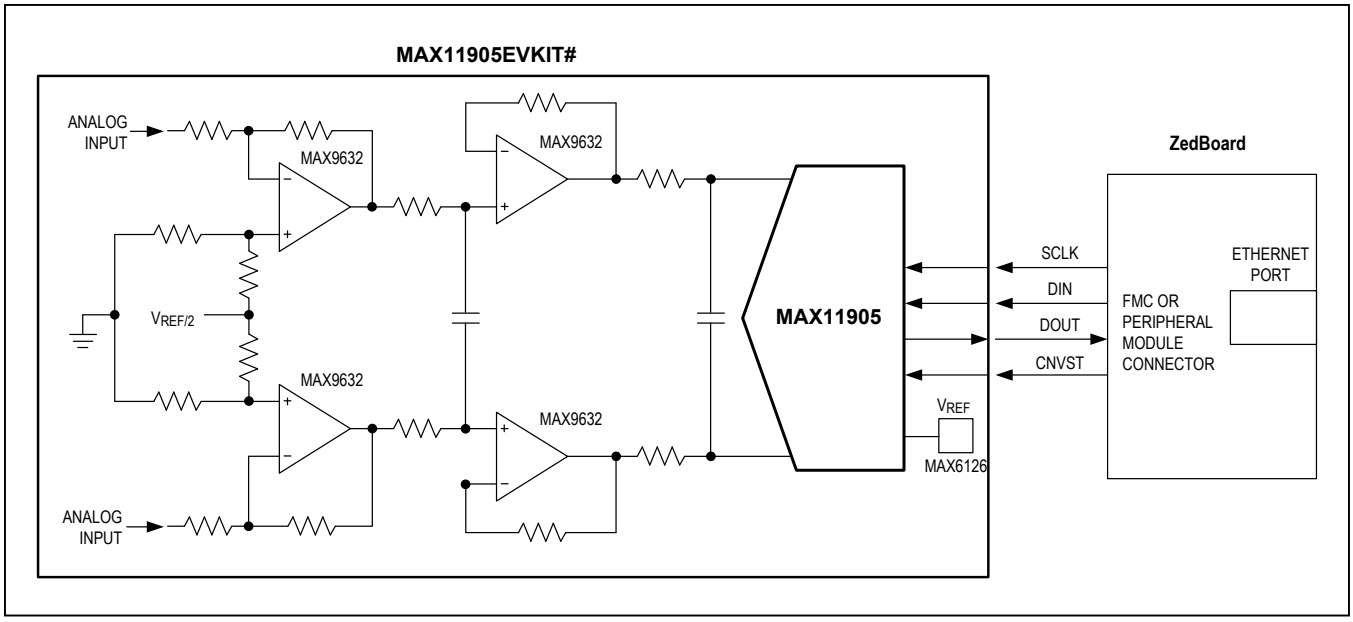
Windows, Windows XP, and Windows Vista are registered trademarks and registered service marks of Microsoft Corporation.

Features

- Peripheral Module and FMC Connector for Interface
- 75MHz SPI Clock Capability through FMC Connector
- 37.5MHz SPI Clock Capability through Peripheral Module Connector
- Sync In and Sync Out for Coherent Sampling
- On-Board Input Buffers (MAX9632)
- On-Board +3.0V Reference Voltage (MAX6126)
- Windows XP-, Windows Vista-, Windows 7-, and Windows 8/8.1-Compatible Software

***Ordering Information* appears at end of data sheet.**

System Block Diagram



maxim integrated™

Quick Start

Required Equipment

- MAX11905 EV kit
- ZedBoard development board (includes Micro A-to-B USB) with ISE Design Suite 14.4 or higher
- Windows PC
- Ethernet cable
- +5V DC power supply
- ±15V dual DC power supply
- Signal generator with differential outputs (e.g., Audio Precision 2700 series)
- Solderer, 2-pin 2.54 header

Note: In the following sections, software-related items are identified by bolding. Text in **bold** refers to items directly from the EV kit software. Text in **bold and underlined** refers to items from the Windows operating system.

Procedure

The EV kit is fully assembled and tested. Follow the steps below to verify board operation:

1) Download the LabView 2013 run-time engine from **www.ni.com/download/labview-run-time-engine-2013/4059/en**.
2) Visit **www.maximintegrated.com/evkitsoftware** to download the latest version of the EV kit firmware and software, 1190XFWVxx.ZIP and 1190XGUIVxx.ZIP. Save the EV kit firmware and software to a temporary folder and uncompress the ZIP file.
3) Solder the 2-pin header on J18-3V3 of the ZedBoard.
4) Connect the Ethernet cable from the PC to the ZedBoard and configure the **Internet Protocol Version 4 (TCP/IPv4)** properties in the local area connection to IP address **192.168.1.2** and subnet mask to **255.255.255.0**.
5) Connect the USB cable from PC to ZedBoard's USB programming connector (J17).
6) Verify that jumpers JP7–JP11 have shunts installed at the GND position.
7) Move the shunt on J18 of the ZedBoard to the 3V3 position from 1V8.
8) Turn on the power to the ZedBoard.
9) Start the Xilinx SDK under the ISE Design Suite.
10) From the menu bar, select Xilinx **Tools | Program Flash**. Select the image **file tcpTransfer.mcs** and ensure that **flash type** is set to **qspi_flash**. Click on the **Program** button and wait for the programming to complete.
11) Turn off the power to the ZedBoard.
12) Move the shunt on jumper JP10 to the 3V3 position on the ZedBoard to boot off the QSPI flash.
13) Verify that all jumpers on the EV kit are in their default positions, as shown in Table 1.
14) Connect the ZedBoard to J2 on the EV kit for FMC connection. If the peripheral module is used, the ZedBoard's JA1 connecter must be connected to J1 on the EV kit.
15) Connect the positive terminal of the +5V supply to the +5V test point and the negative terminal to the GND_+5 test point.
16) Connect the +15V supply to the +15V test point, -15V supply to the -15V test point, and the ground to the GND15 test point.
17) Make sure the GND_+5 and GND15 test points are connected at one point at the supplies.
18) Set the signal generator to $5.95V_{P-P}$ and 10kHz to the INV+ and INV- SMA connectors on the EV kit.
19) Turn on all power supplies.
20) Enable the function generator.
21) Open the EV kit GUI and click on the **run** arrow (➔) button at the top of the GUI screen (see Figure 1).
22) Verify that the IP address is **192.168.1.10**, the port is **6001**, and the status bar displays **TCP/IP Connection to Zedboard is successful** and **Connected to ZedBoard (MISO = 1)**.
23) Click on the **SET** button within the **SYSTEM** tab sheet.
24) Click on the **FFT** tab (Figure 6) and start capturing data.

Table 1. Jumper Descriptions

JUMPER	SHUNT POSITION	DESCRIPTION
JU1	Installed	Connects to GND.
	Not installed*	Apply the signal at the INV+ SMA connector when using inverting op-amp configuration.
JU2	Installed*	Connects to GND.
	Not installed	Apply the signal at the NONINV+ SMA connector when using noninverting op-amp configuration.
JU3	Installed	Connects signal to the NONINV+ SMA connector to the INV- SMA connector. Only use with single-ended signal source.
	Not installed*	Disconnects signal from the NONINV+ SMA connector to the INV- SMA connector.
JU4	Not installed	Apply the signal at the NONINV- SMA connector when using the noninverting op-amp configuration.
	1-2*	Connects to GND.
	2-3	Connects to 50Ω. Only use with single-ended signal source with 50Ω output impedance.
JU5	Installed	Connects to GND.
	Not installed*	Apply the signal at the INV- SMA connector when using the inverting op-amp configuration.
JU6	1-2*	Connects to REF/2 offset.
	2-3	Connects to GND.
JU7	1-2	Connects to REF. Only use with single-ended signal source.
	2-3*	Connects to JU6-2.
JU8	Not installed*	Enables the line driver.
	Installed	Disables the line driver.
JU9	2-3, 5-6, 8-9, 11-12*	Connects the SPI signals coming from the peripheral module or FMC connectors to the IC.
	Not installed	User-supplied SPI. Connect the SPI signals at the SCLK, CNVST, DIN, and DOUT test points.
JU11	Not installed	User-supplied OVDD. Apply +3.3V at the OVDD test point.
	1-2	Do not use.
	2-3*	OVDD supply connects to the on-board +3.3V LDO.
JU12	Installed*	AVDD supply connects to the on-board +1.8V LDO.
	Not installed	User-supplied AVDD. Apply +1.8V at the jumper JU12-2 pin.
JU13	Installed*	REFVDD supply connects to the on-board +3.3V LDO.
	Not installed	User-supplied REFVDD. Apply +3.3V at the JU13-2 pin.
JU14	1-2*	REFIN connects to the on-board +3.0V reference.
	2-3	User-supplied REFIN. Apply reference voltage at the EXT_REFIN test point.
JU15	Installed*	DVDD supply connects to the on-board +1.8V LDO.
	Not installed	User-supplied DVDD. Apply +1.8V at the DVDD test point.

**Default position.*
Note: *JU10 does not exist.*

General Description of Software

The main window of the MAX11905 EV kit software contains five tabs: **SYSTEM**, **SCOPE**, **DMM**, **HISTOGRAM**, and **FFT**. The **SYSTEM** tab provides control to communicate with the ZedBoard, SPI, and the IC registers. The other four tabs are used for evaluating the IC's high-speed ADC.

SYSTEM Tab

When all connections are made on the system and are fully powered, the **SYSTEM** tab sheet displays the correct IP address, port, and the lower status bar displays as shown Figure 1. These are all indicators that the system and GUI are ready for communication.

Before proceeding, the connector used on the ZedBoard should be connected to either the FMC or peripheral module connector on the EV kit. If the FMC connector is used, all SCLK frequencies are applicable. If the peripheral module connector is used, the maximum allowed frequency is 37.5MHz. For the **Clock Source** selection, the ZedBoard internal clock is always a valid option. If the external clock is selected, an external clock must be applied at the DCLK_IN SMA on the EV kit. The Sync-Out CLK selection is used to synchronize the signal generator with a 10MHz input. See the *Sync Input and Sync Output section* for more information. Once the above configurations are completed, adjust to the desired sampling rate, reference voltage, and number of samples, and then click on the **SET** button.

Also in this tab are the IC register controls. The Mode register is accessible using the controls on the **MAX11905 Mode Register Configuration** group box in the center, or the **Mode** control on the right. All other registers are read-only and are updated by clicking on the appropriate **Read** button. The first and second REF must be shorted on the board to use the REF controls. **1st REF BUF** and **2nd REF BUF** are internally set to the same value. The GUI forces these two controls to the same value, regardless of the user's choice.

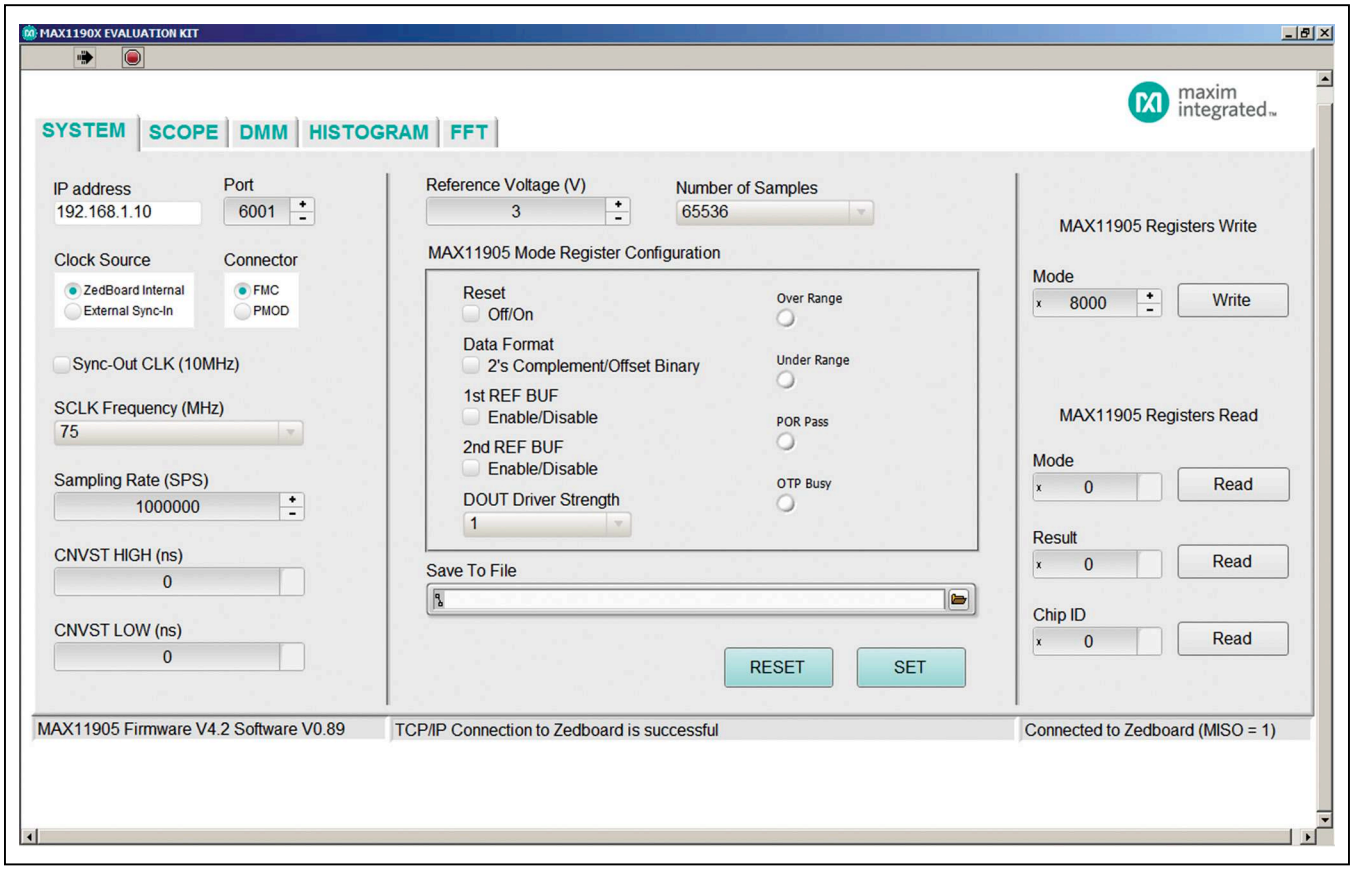


Figure 1. MAX1190X EV Kit Main Window (SYSTEM tab sheet)

The **RESET** button resets the firmware, as well as the device. It sends 0x8000 to the Mode register and causes the device to do a power-on reset. The **SET** button should be clicked to save the current screen settings.

SCOPE Tab

The **SCOPE** tab sheet is used to capture data and display it in the time domain. Sampling rate and number of samples can also be set in this tab if they were not appropriately adjusted in other tabs. The **Display Unit** drop-down list allows counts and voltages. Once the desired configuration is set, click on the **Capture** button. The right side of the tab sheet displays details of the waveform, such as average, standard deviation, maximum, minimum, and fundamental frequency.

Figure 2 displays the ADC data when differential sinusoidal are applied at the inputs on the EV kit.

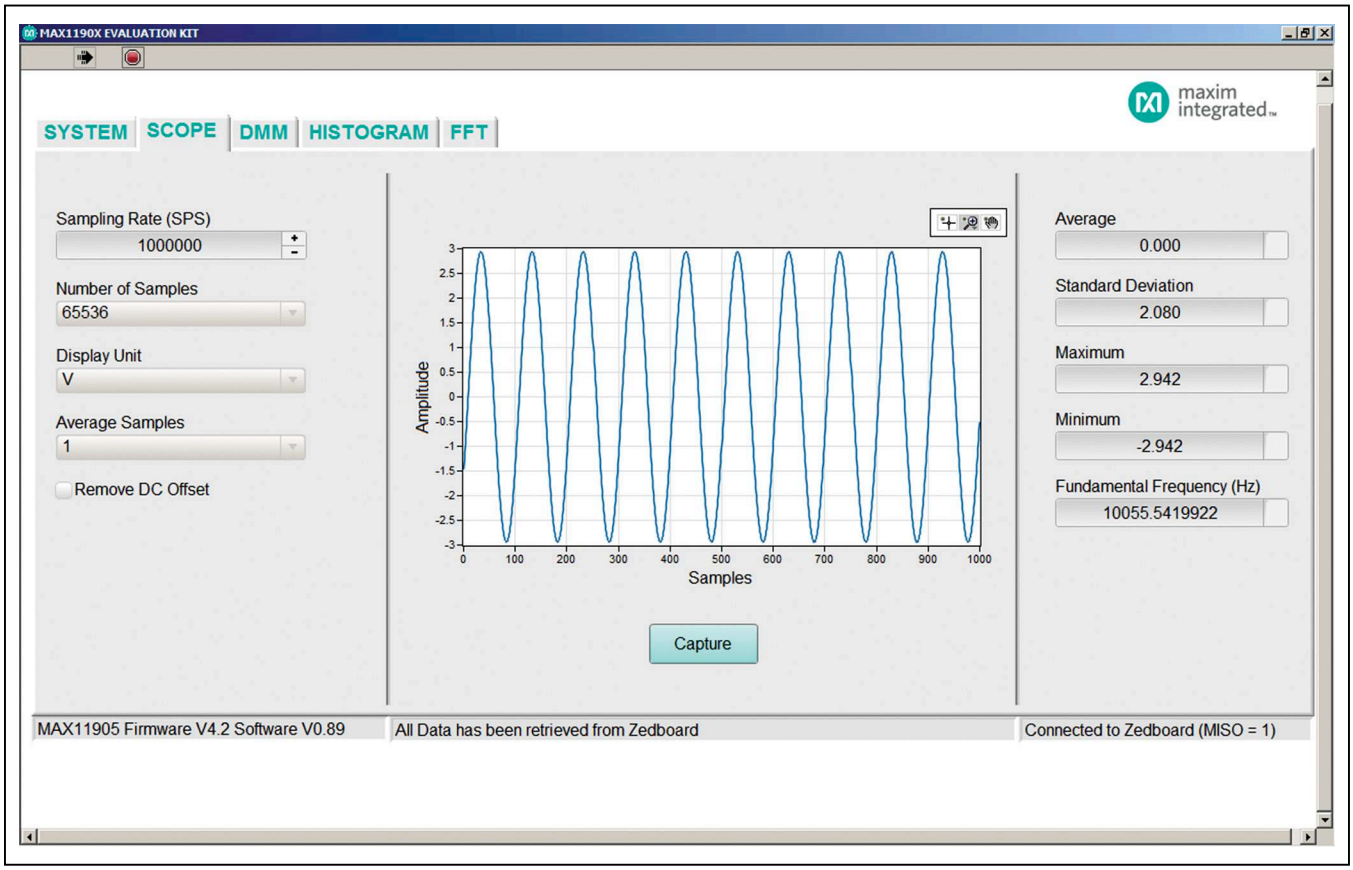


Figure 2. MAX1190X EV Kit Main Window (SCOPE Tab)

DMM Tab

The **DMM** tab sheet provides the typical information as a digital multimeter. Once the desired configuration is set, click on the **Capture** button.

Figure 3 displays the numerical value when the inputs on the EV kit are shorted to ground using the jumpers (JU1, JU2, JU4, and JU5). See Table 1 for shunt settings.

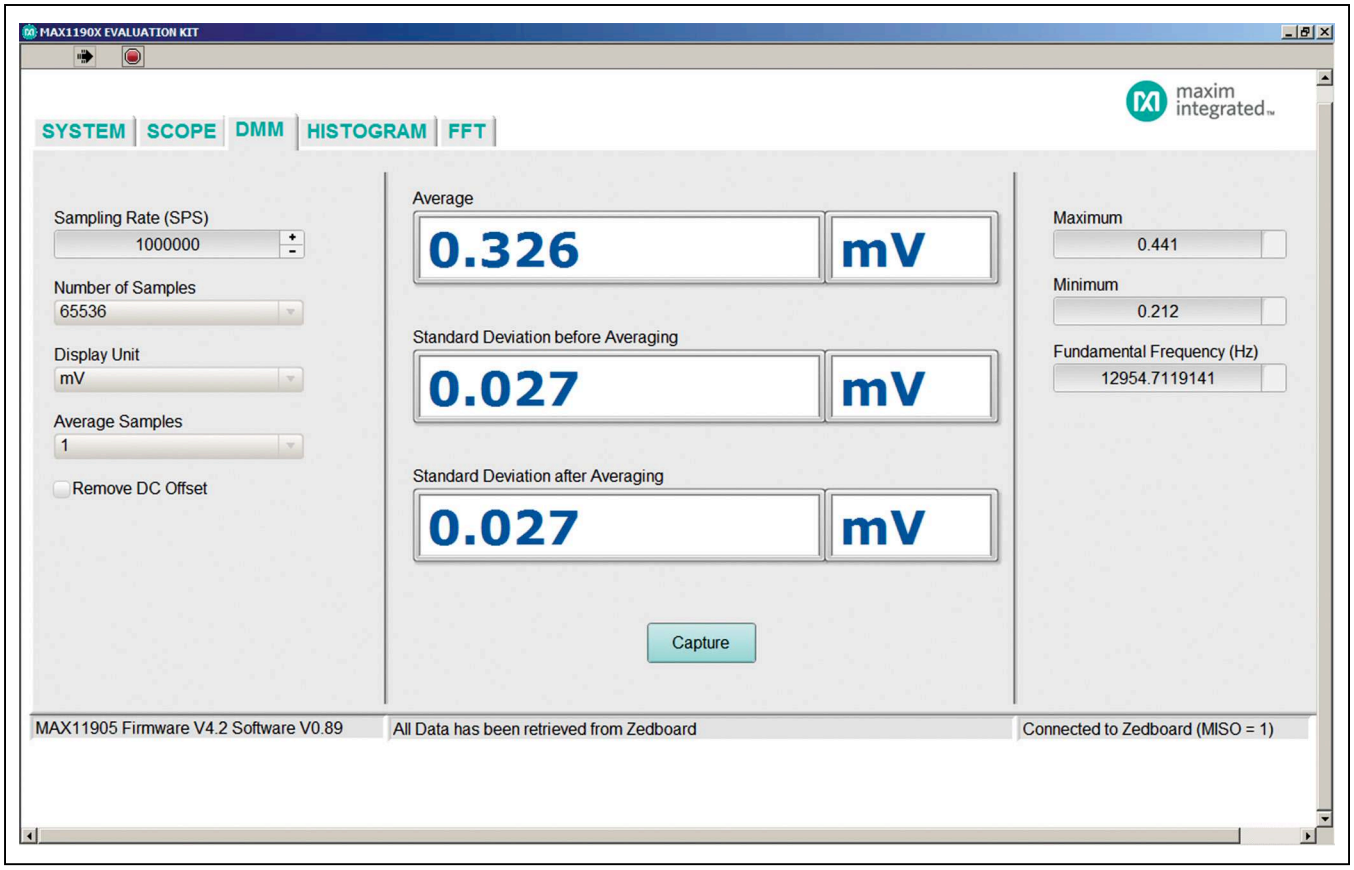


Figure 3. MAX1190X EV Kit Main Window (DMM Tab)

HISTOGRAM Tab

The **HISTOGRAM** tab sheet is used to capture the histogram of the data. Sampling rate and number of samples can also be set in this tab if they were not appropriately adjusted in other tabs. Make sure that the number of samples do not exceed 524,288. Otherwise, data capturing is longer than expected. Once the desired configuration is set, click on the **Capture** button. The right side of the tab sheet displays details of the histogram such as average, standard deviation, maximum, minimum, peak-to-peak noise, effective resolution, and noise-free resolution.

To use this histogram feature, apply a DC voltage at the input. Figure 4 displays the results when the inputs of the EV kit are shorted to ground using jumpers JU1, JU2, JU4, and JU5. See Table 1 for placement of shunt positions.

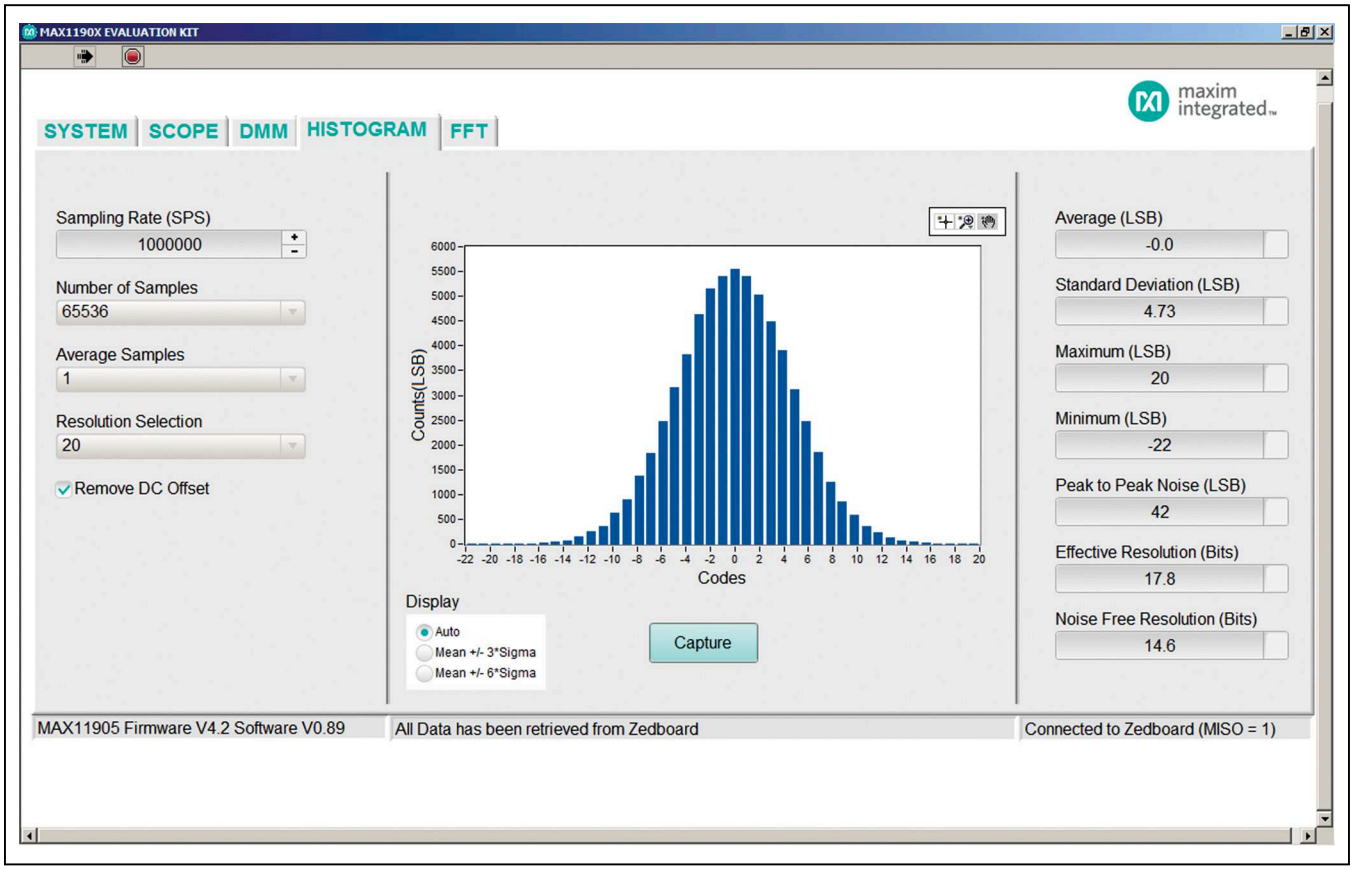


Figure 4. MAX1190X EV Kit Main Window (HISTOGRAM Tab)

FFT Tab

The **FFT** tab sheet is used to display the FFT of the data. Sampling rate and number of samples can also be set in this tab if they were not appropriately adjusted in other tabs. When coherent sampling is needed, this tab sheet allows the user to calculate the input frequency or the master clock coming into the board. Either adjust the input frequency applied to the signal generator or adjust the master applied to the DCLK_IN SMA connector. See the *Sync Input and Sync Output* section before using this feature. Once the desired configuration is set, click on the **Capture** button. The right side of the tab displays the performance based on the FFT, such as fundamental frequency, THD, SNR, SINAD, SFDR, ENOB, and noise floor.

Figure 5 shows the setup Maxim uses to capture data for coherent sampling.

To achieve the results similar to Figure 6, the daughter board was configured to inverting configuration. Use the jumper settings from Table 2 for proper configurations. The input signal from the signal generator must be exactly **10000.000000 Hz.** The low-jitter clock is synchronized with the signal generator. The master clock was initially set to **1000000000 Hz** but to achieve coherent sampling, the user must click on the **Calculate** button and use the **Adjusted(Hz)** frequency. **99523158.694 Hz** was entered into our low-jitter clock. The master clock is fed back to the ZedBoard and multiplied by 3/2, then generates a system clock that drives the Xilinx FPGA. Timing for all SPI timing and sampling rate are based off the system clock.

If the results do not look similar to Figure 6 and more similar to Figure 7, then check all connections in Figure 5 to make sure the setup is synchronizing properly.

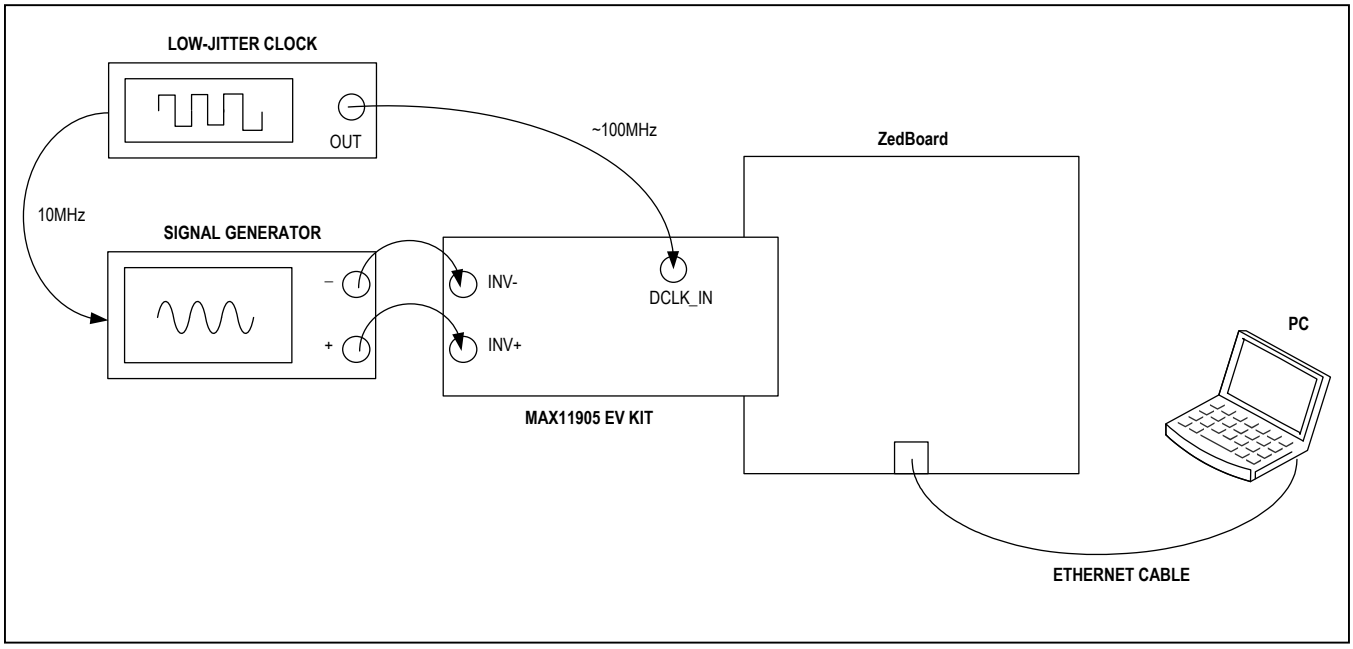


Figure 5. MAX11905 EV Kit Coherent Sampling Setup

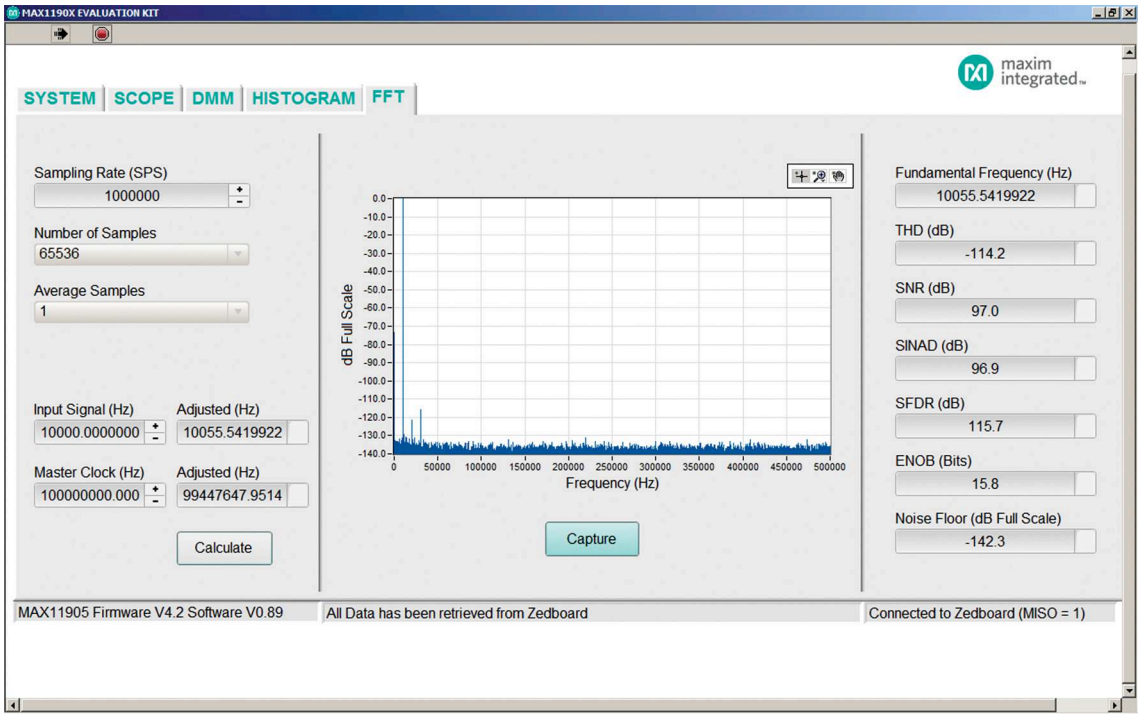


Figure 6. MAX1190X EV Kit Main Window, Results Using the Inverting Setup (FFT Tab)

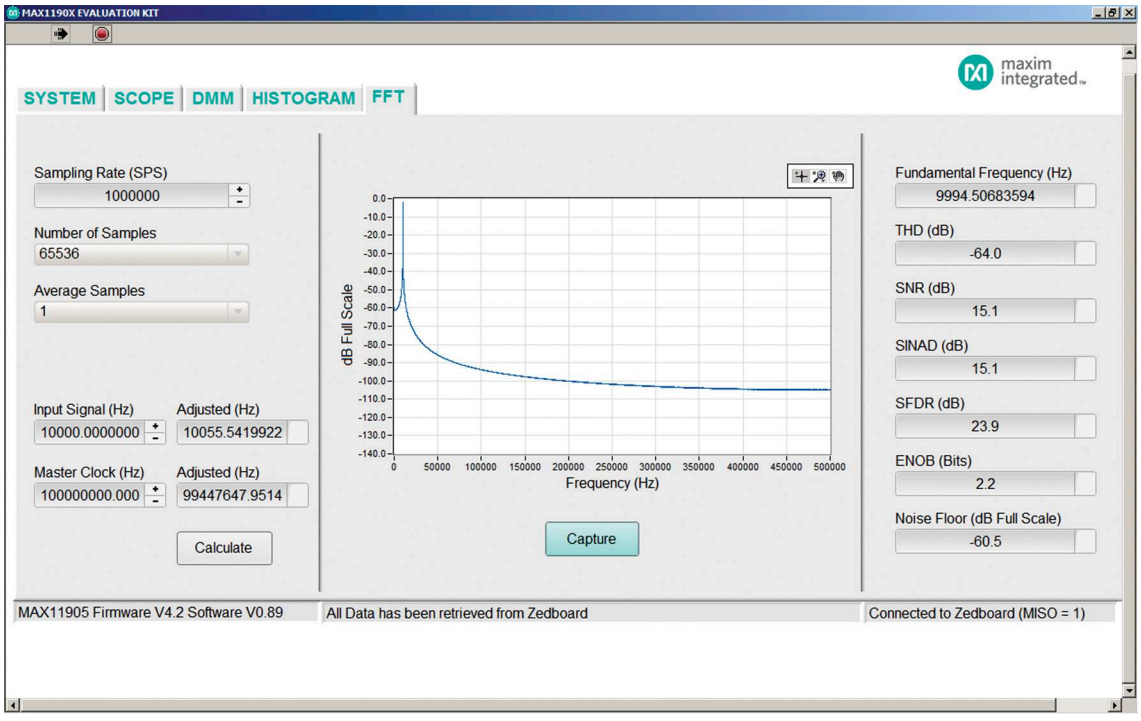


Figure 7. MAX1190X EV Kit Main Window, Results Using the Inverting Setup with Noncoherent Sampling (FFT Tab)

In Figure 8, the daughter board was configured to noninverting configuration. Use the jumper settings from Table 2 for proper configurations.

In Figure 9, the daughter board was configured to inverting, single-ended to differential configuration. Use the jumper settings from Table 2 for proper configurations.

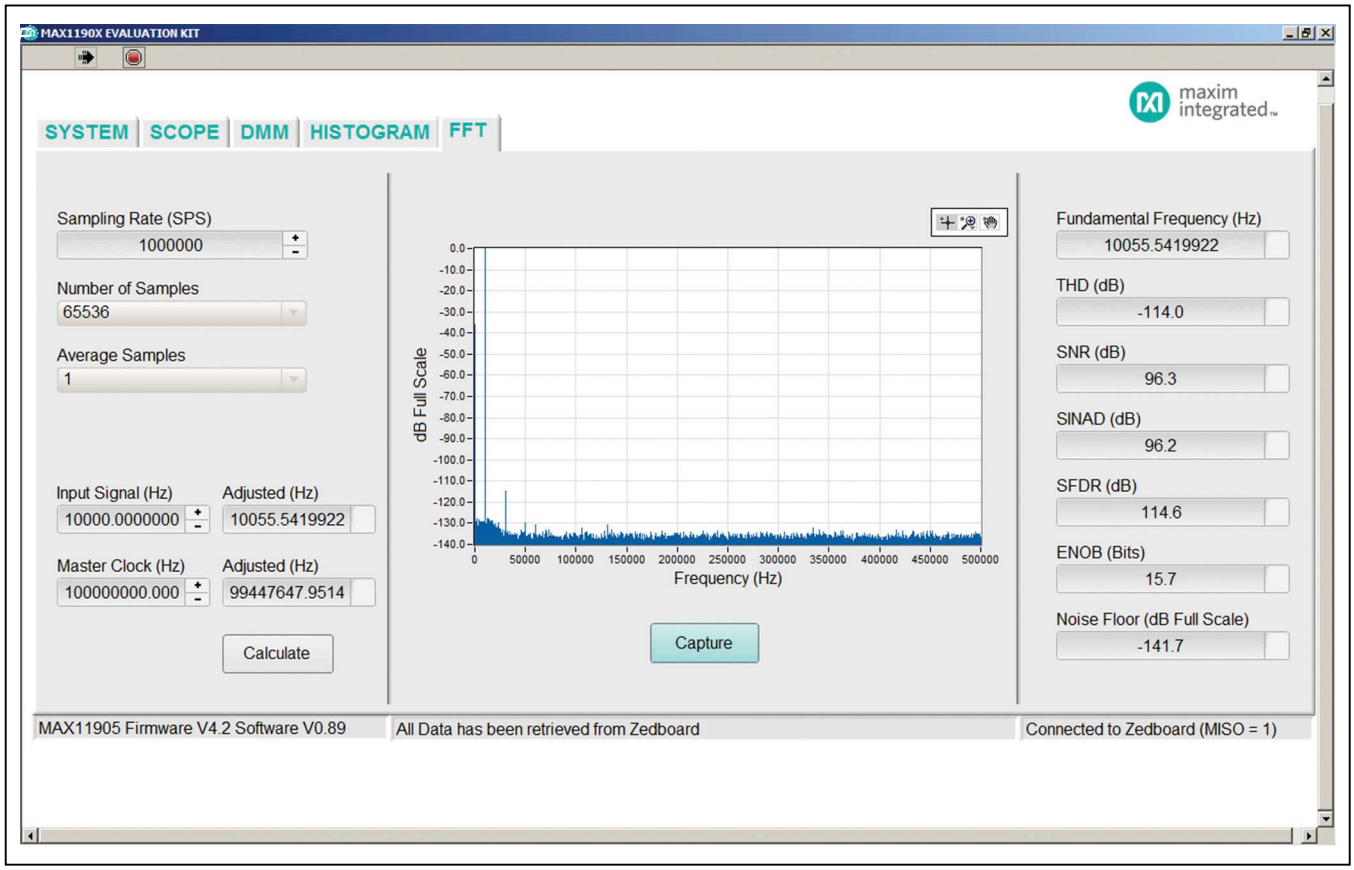


Figure 8. MAX1190X EV Kit Main Window, Results Using the Noninverting Setup (FFT Tab)

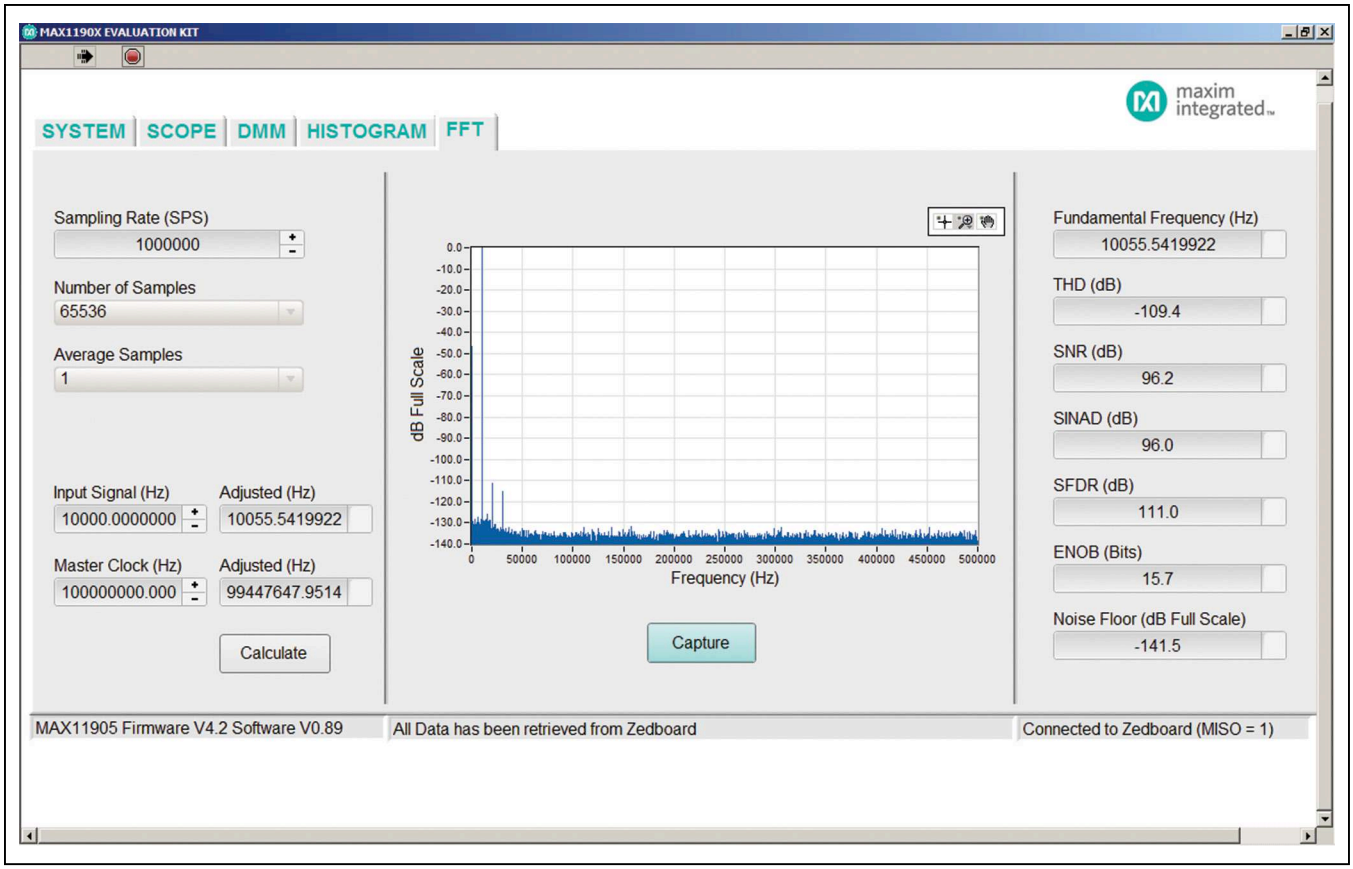


Figure 9. MAX1190X EV Kit Main Window, Results Using the Inverting Single to Differential Setup (FFT Tab)

General Description of Hardware

The MAX11905 EV kit provides a proven layout to demonstrate the performance of the MAX11905 20-bit SAR ADC. Included in the EV kit are digital isolators, ultra-low-noise LDOs (MAX8510) to all supply pins of the IC, on-board reference (MAX6126), precision amplifiers (MAX9632) for the analog inputs, and sync-in and sync-out signals for coherent sampling.

User-Supplied SPI

To evaluate the EV kit with a user-supplied SPI bus, remove shunts from jumper JU9. Apply the user-supplied SPI signals to the SCLK, CNVST, DIN, and DOUT test points. Make sure the return ground is the same as the IC's ground.

User-Supplied REFVDD

The REFVDD supply is powered through a +3.3V LDO by default. For user-supplied REFVDD, remove the shunt on jumper JU13 and apply +2.7V to +3.6V at jumper JU13-1.

User-Supplied AVDD

The AVDD supply is powered through a +1.8V LDO by default. For user-supplied AVDD, remove the shunt on jumper JU12 and apply +1.7V to +1.9V at jumper JU12-2.

User-Supplied DVDD

The DVDD supply is powered through a +1.8V LDO by default. For user-supplied DVDD, remove the shunt on jumper JU15 and apply +1.7V to +1.9V at the DVDD test point.

User-Supplied OVDD

The OVDD supply is powered through a +3.3V LDO by default. For user-supplied OVDD, remove the shunt on JU11 and apply +1.5V to +3.6V at jumper JU13-1. Since there is a supply limitation on the isolators (U3, U18), the OVDD supply should not be powered below +2.7V when the FMC connector or peripheral module of the EV kit are being used.

User-Supplied REFIN

The IC uses an on-board +3V reference (MAX6126) by default. For user-supplied REFIN, move the shunt on jumper JU14 to the 2-3 position. Make sure that REFIN is 300mV below REFVDD before applying the reference.

Analog Inputs

Both analog inputs (AIN+ and AIN-) range from 0 to V_{REF}. The differential input range is from $-V_{REF}$ to $+V_{REF}$ and the full-scale range is 2 times the V_{REF}. The desired input signals are applied at the INV+ and INV- SMAs for inverting configuration (see Figure 10), and NONINV+ and NONINV- SMAs for noninverting configuration (see Figure 11).

The EV kit is also configurable for single-ended input to differential (see Figure 12 and Figure 13). The desired signal should be applied at the INV+ SMA for inverting and at the NONINV+ SMA for noninverting. If the source is 50Ω output impedance, then jumper JU4 must be in the 2-3 position.

See Table 2 for all possible analog input configurations.

Table 2. Analog Input Configurations (JU1–JU7)

JUMPER	INVERTING AND DIFFERENTIAL	NONINVERTING AND DIFFERENTIAL	INVERTING, SINGLE-ENDED TO DIFFERENTIAL	NONINVERTING, SINGLE-ENDED TO DIFFERENTIAL
JU1	Not installed	Installed	Not installed	Installed
JU2	Installed	Not installed	Installed	Not installed
JU3	Not Installed	Not installed	Installed	Installed
JU4	1-2	Not installed	1-2	1-2
JU5	Not Installed	Installed	Not installed	Not installed
JU6	1-2	1-2	1-2	1-2
JU7	2-3	2-3	1-2	1-2

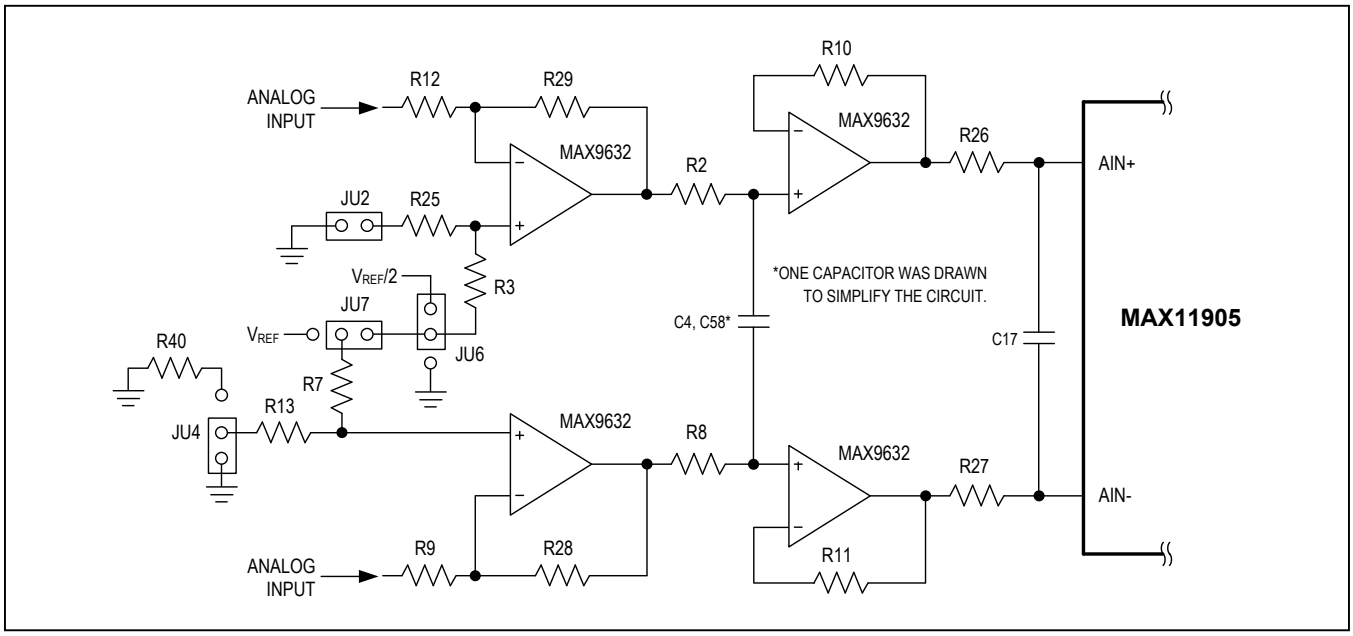


Figure 10. Inverting and Differential Configuration

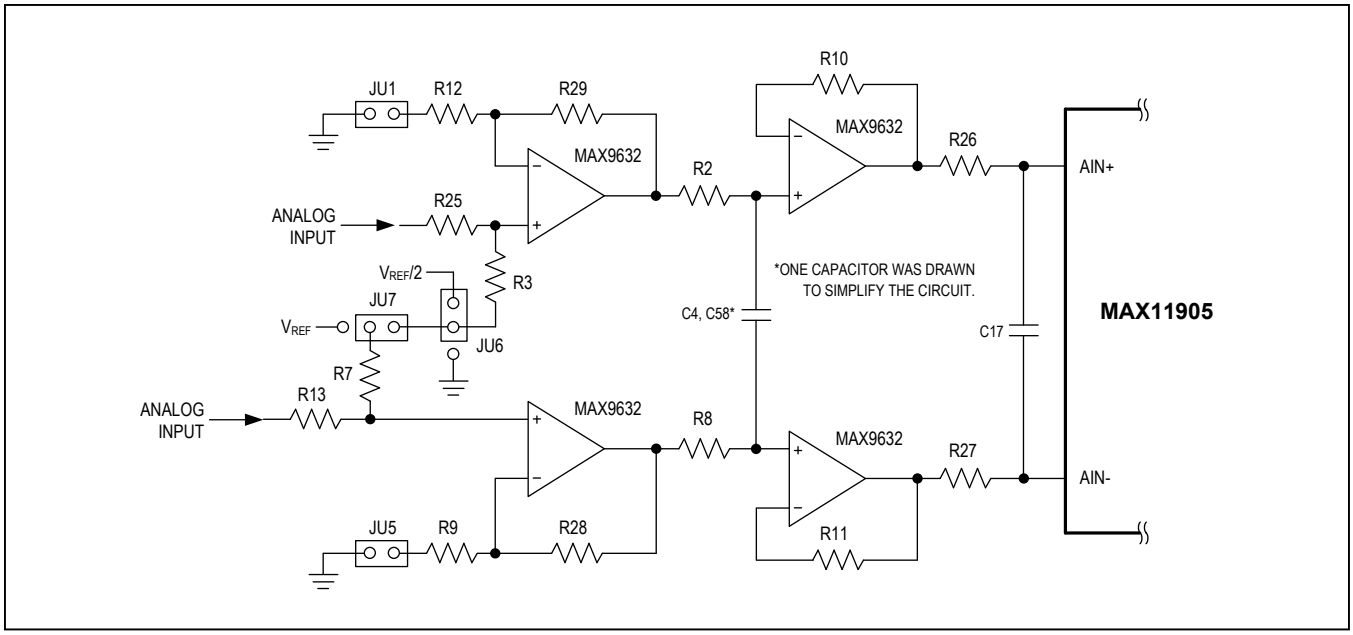


Figure 11. Noninverting and Differential Configuration

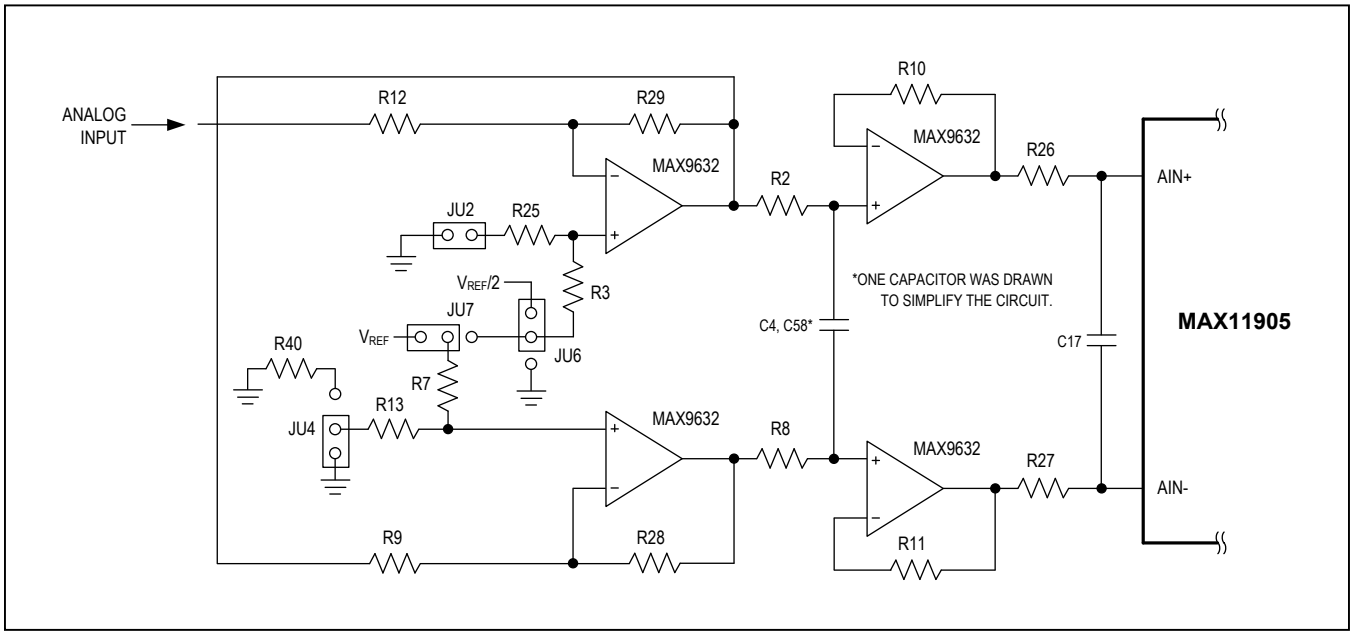


Figure 12. Inverting and Single-Ended to Differential Configuration

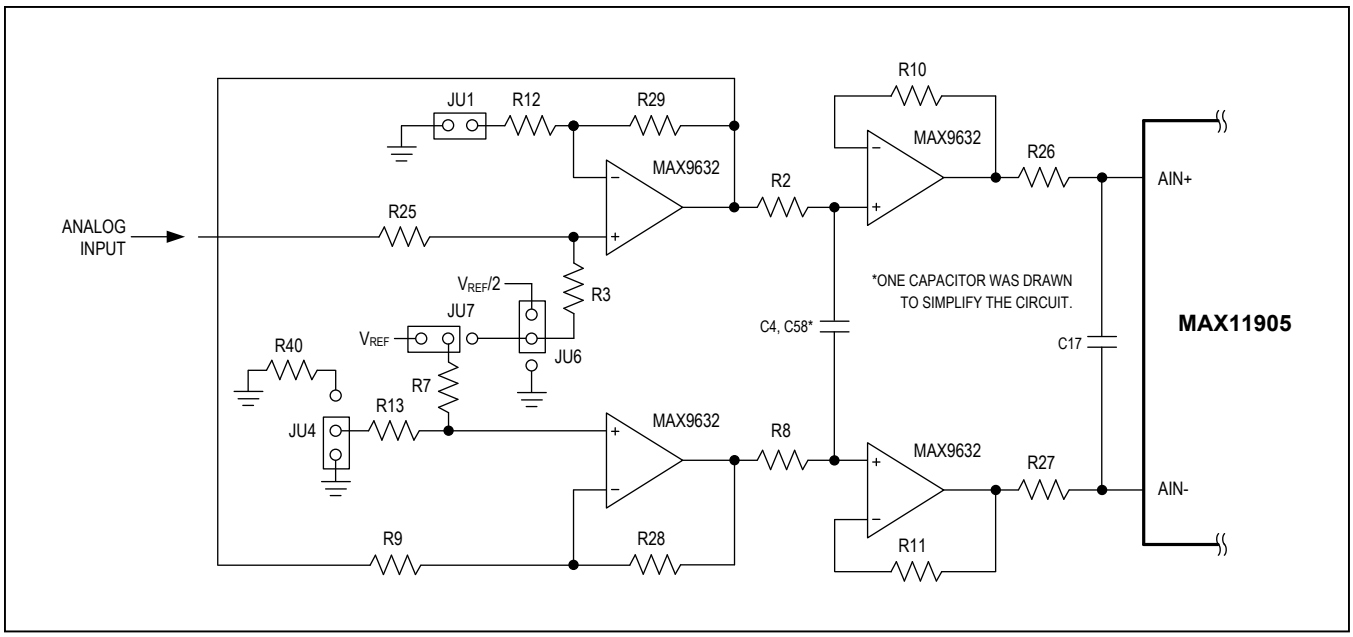


Figure 13. Noninverting and Single-Ended to Differential Configuration

Sync Input and Sync Output

The DCLK_IN SMA accepts an approximate 100MHz waveform signal to generate the system clock of the ZedBoard. For maximum performance, use a low-jitter clock that syncs to the user's analog function generator. The SYNC_OUT SMA outputs a 10MHz square waveform that syncs to the user's analog function generator. Both options are used for coherent sampling of the IC. Only one option should be used at a time. The relationship between f_{IN}, f_S, N_{CYCLES}, and $M_{SAMPLES}$ is given as follows:

$$\frac{f_{IN}}{f_S} = \frac{N_{CYCLES}}{M_{SAMPLES}}$$

where:

f_{IN} = Input frequency

f_S = Samping frequency

N_{CYCLES} = Prime number of cycles in the sampled set

$M_{SAMPLES}$ = Total number of samples

Interface Connectors

The EV kit and ZedBoard communicate in two ways, using the peripheral module connector (J1) or the FMC connector (J2) on the EV kit. The maximum SPI SCLK frequency is 37.5MHz for the peripheral module connector and 75MHz for the FMC connector.

Part Selection

Table 3 is the list of compatible parts that can be replaced at the U1 IC designator.

Table 3. Part Selection

PART	RESOLUTION (BITS)	SAMPLE RATE (Msps)
MAX11900ETP+	16	1.0
MAX11901ETP+	16	1.6
MAX11902ETP+	18	1.0
MAX11903ETP+	18	1.6
MAX11904ETP+	20	1.0
MAX11905ETP+*	20	1.6

**Default installed part*

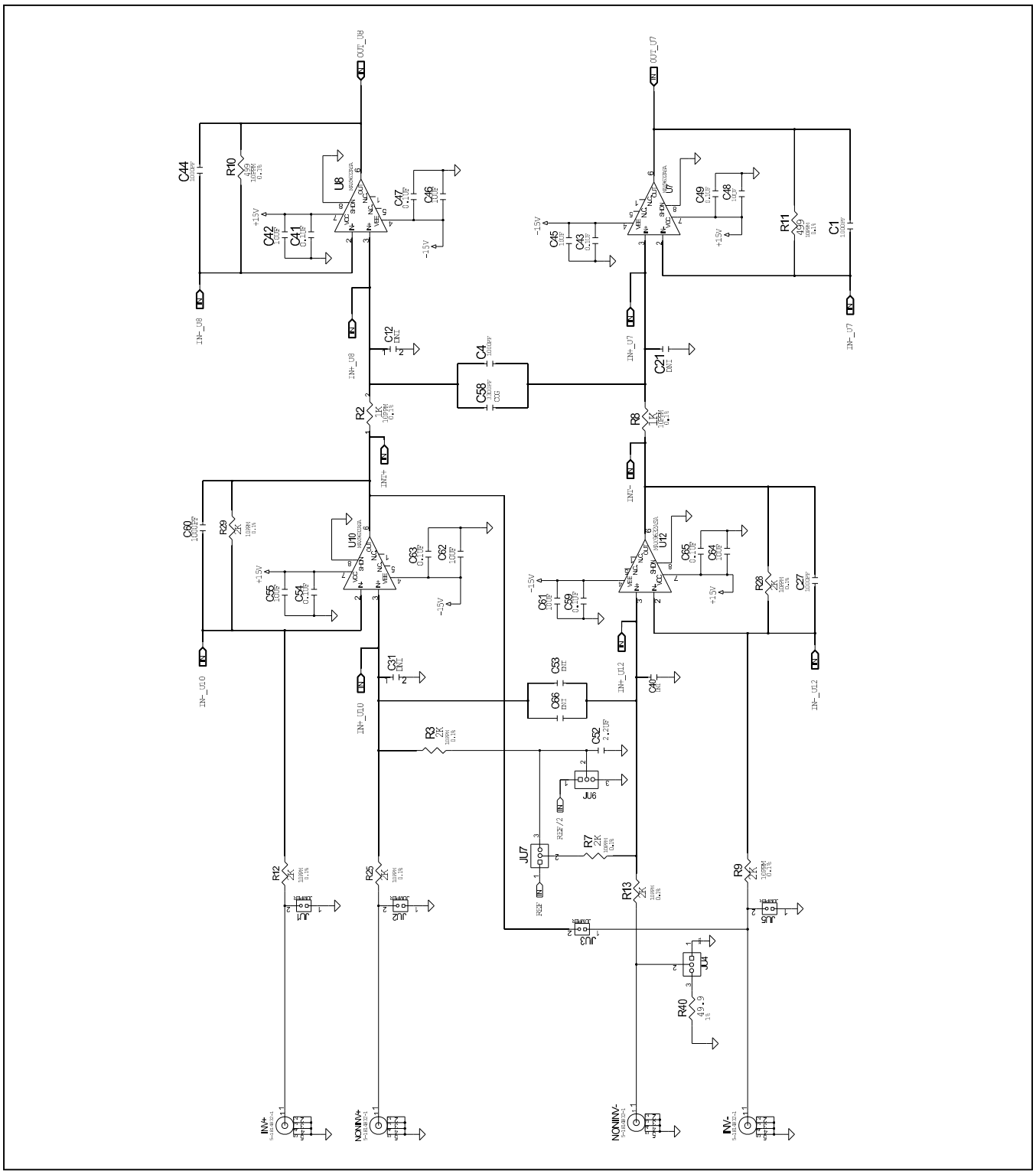


Figure 14a. MAX11905 EV Kit Schematic (Sheet 1 of 4)

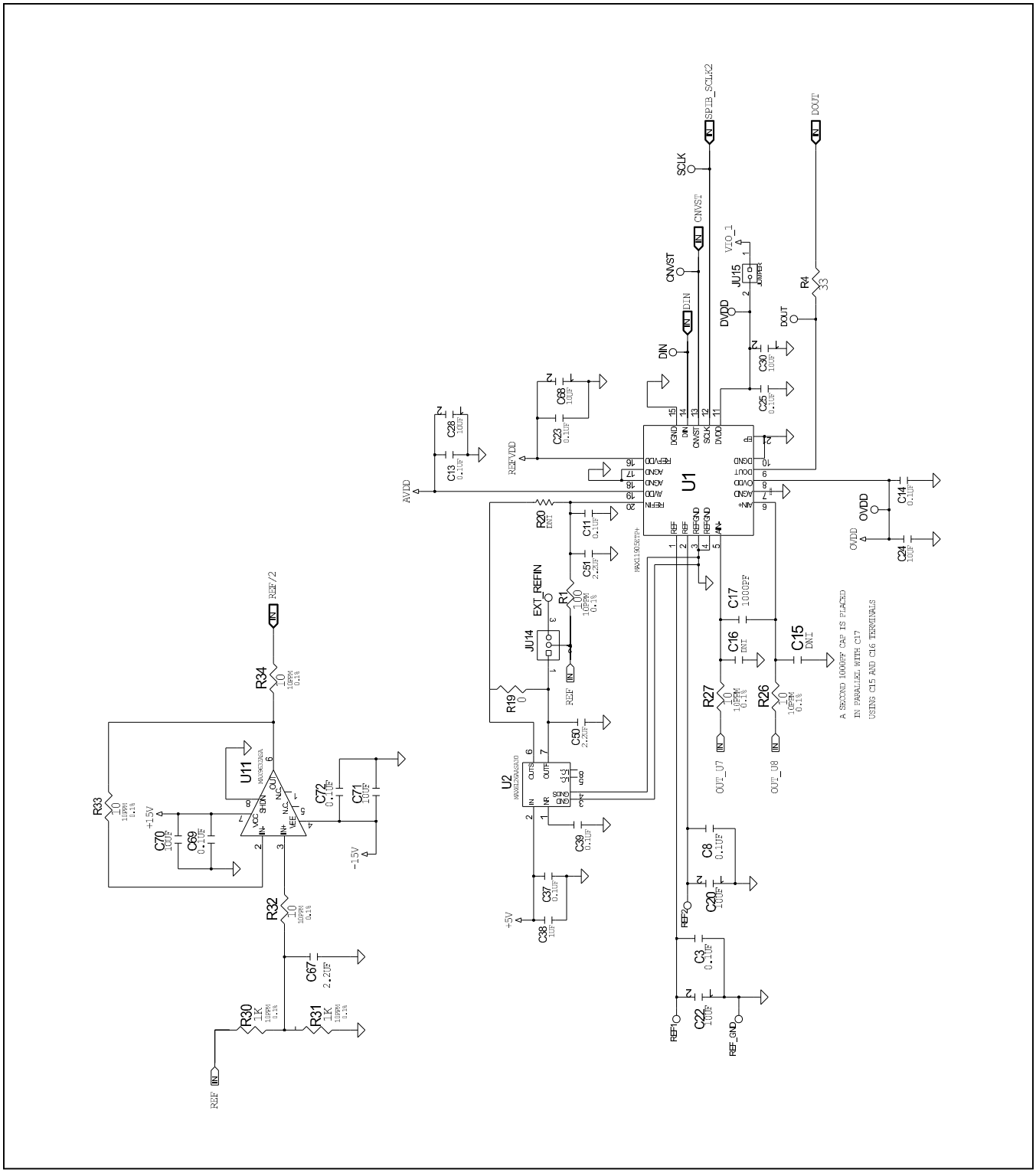


Figure 14b. MAX11905 EV Kit Schematic (Sheet 2 of 4)

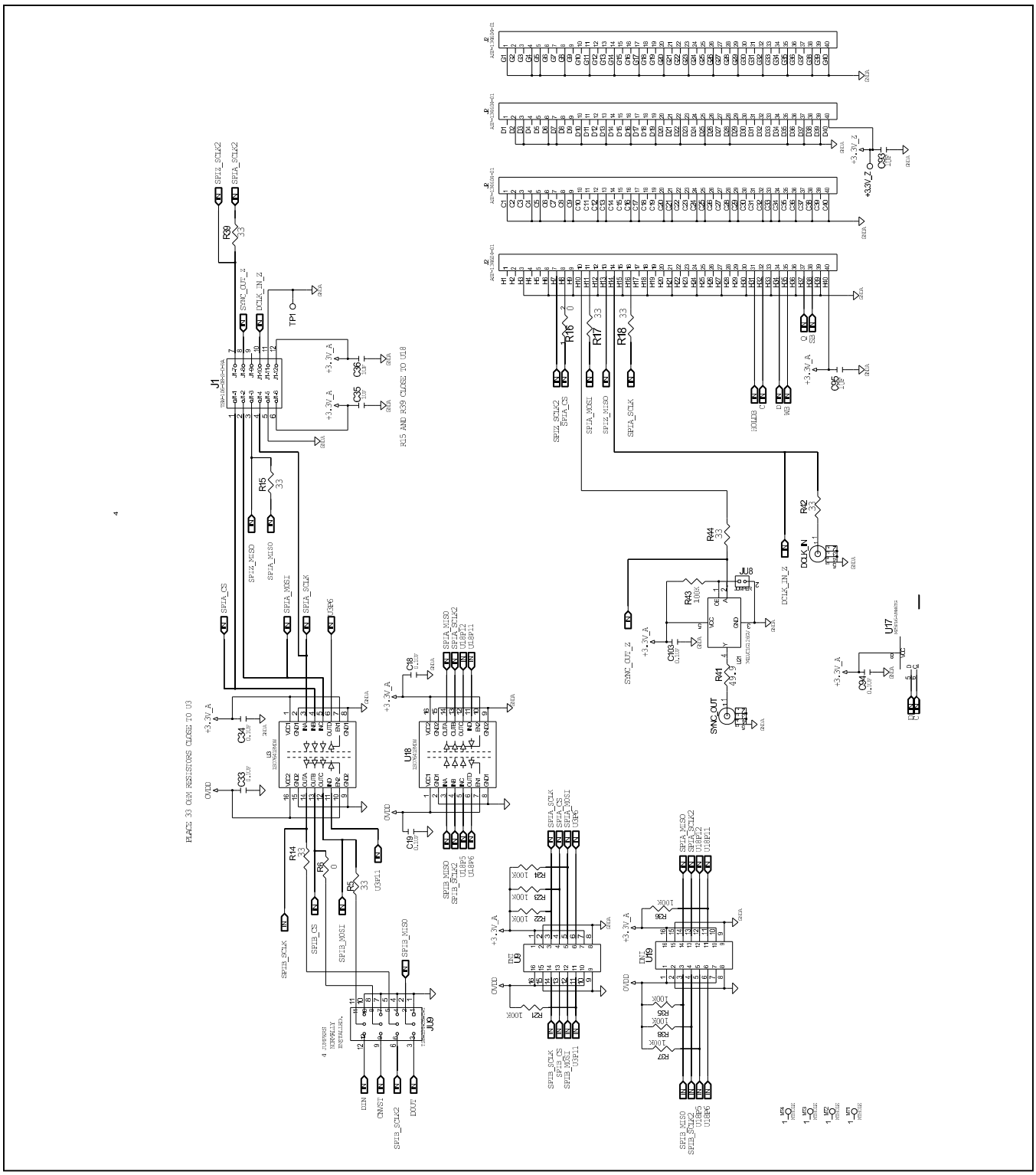


Figure 14c. MAX11905 EV Kit Schematic (Sheet 3 of 4)

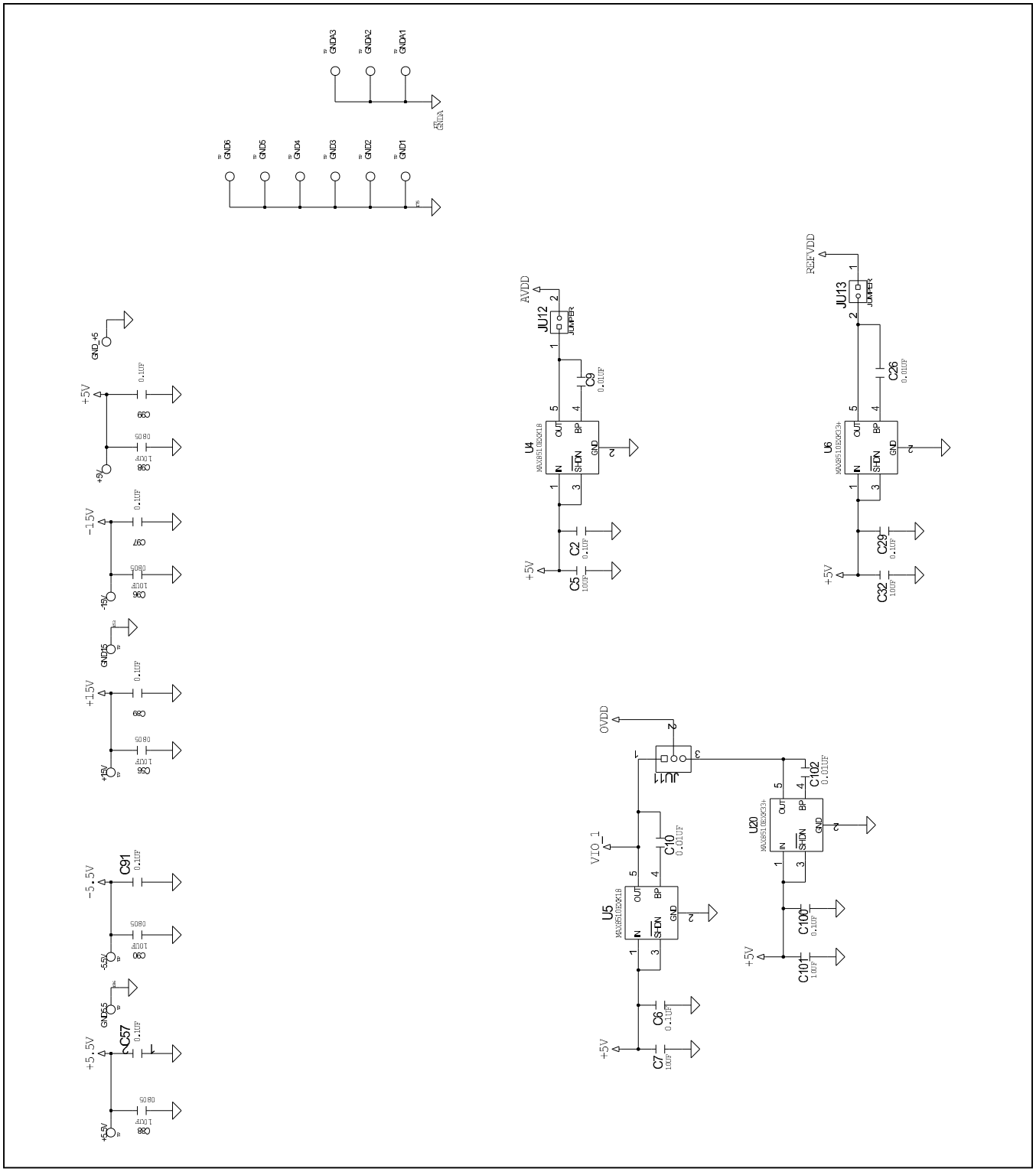


Figure 14d. MAX11905 EV Kit Schematic (Sheet 4 of 4)

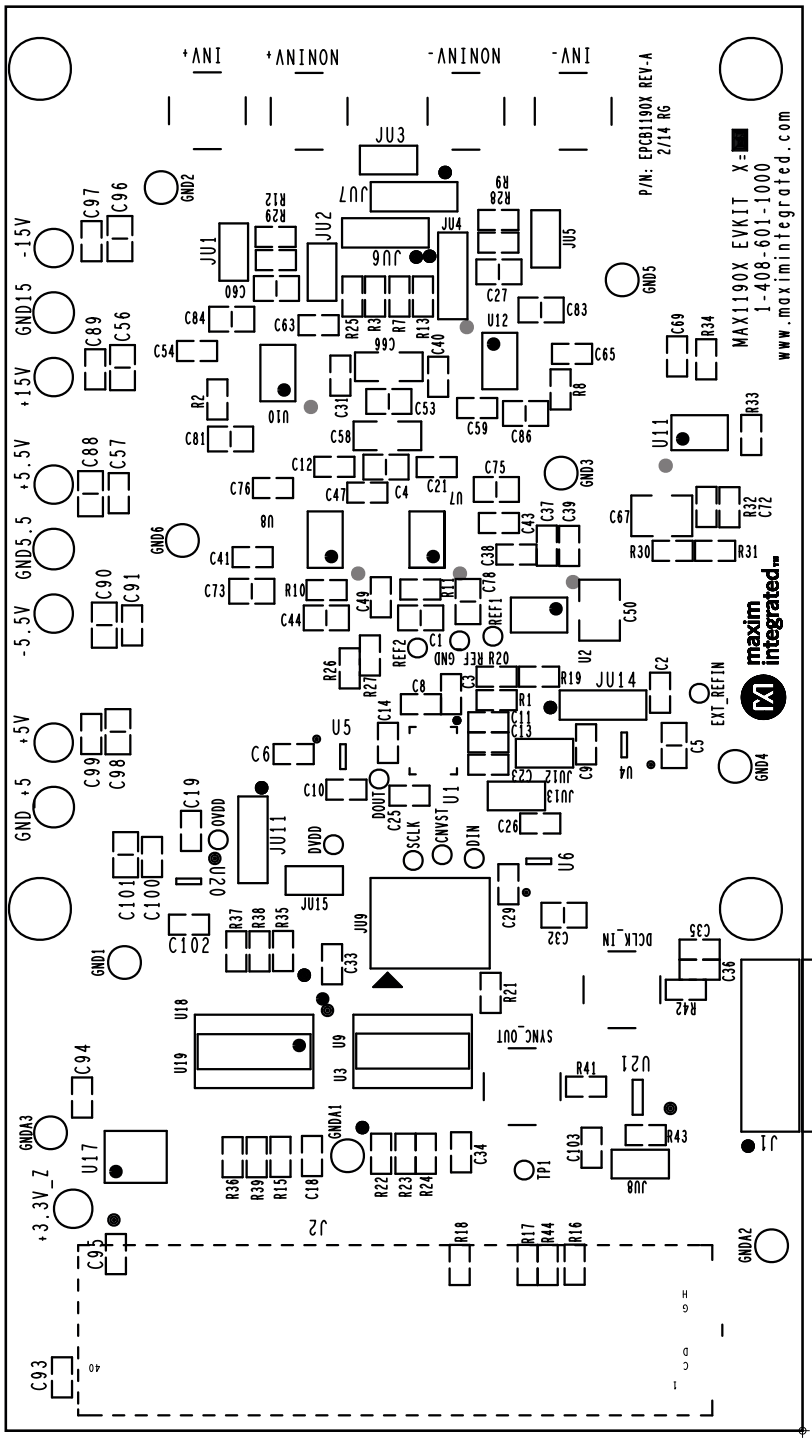


Figure 15. MAX11905 EV Kit Component Placement Guide—Component Side

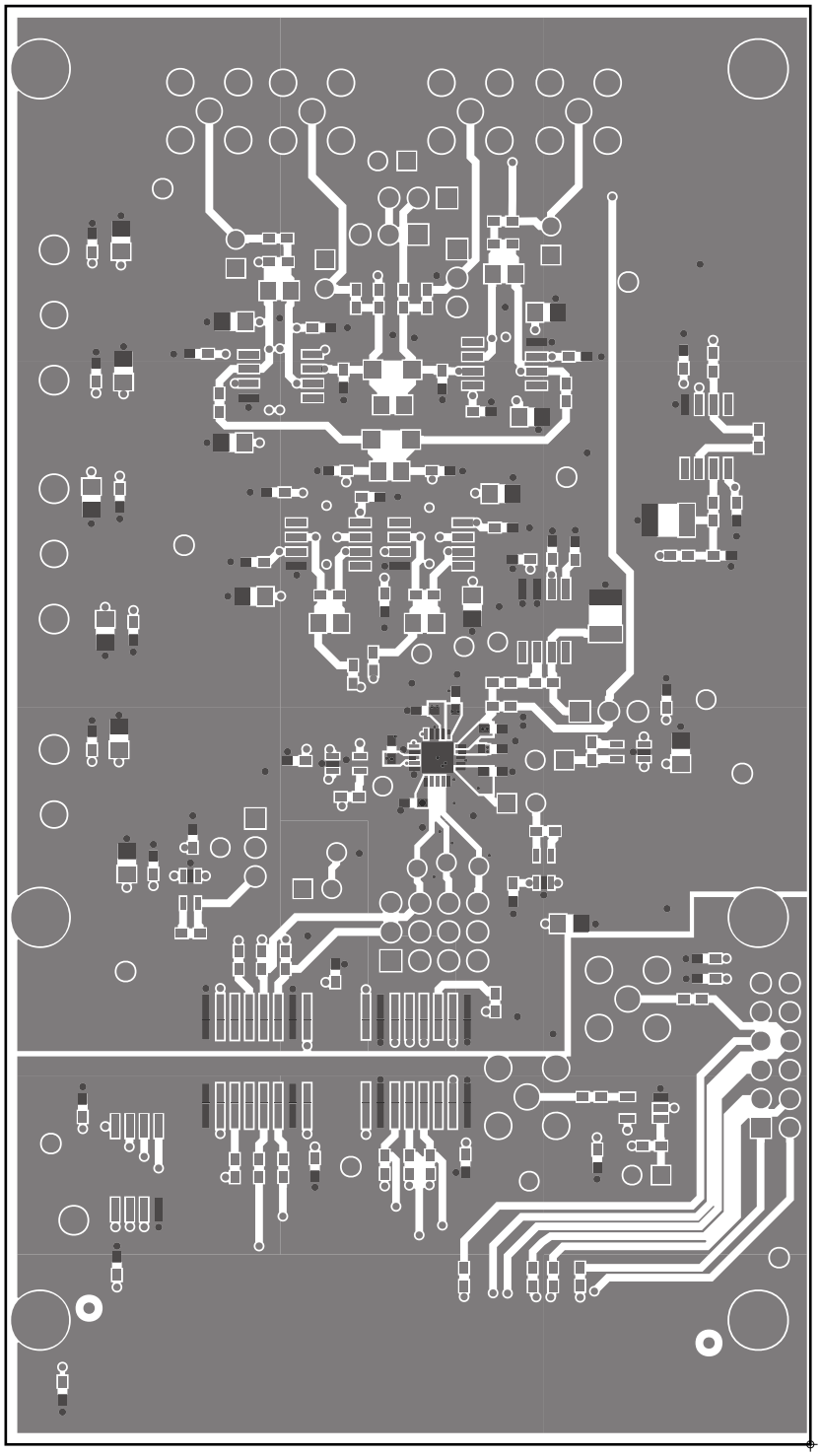


Figure 16. MAX11905 EV Kit PCB Layout—Component Side

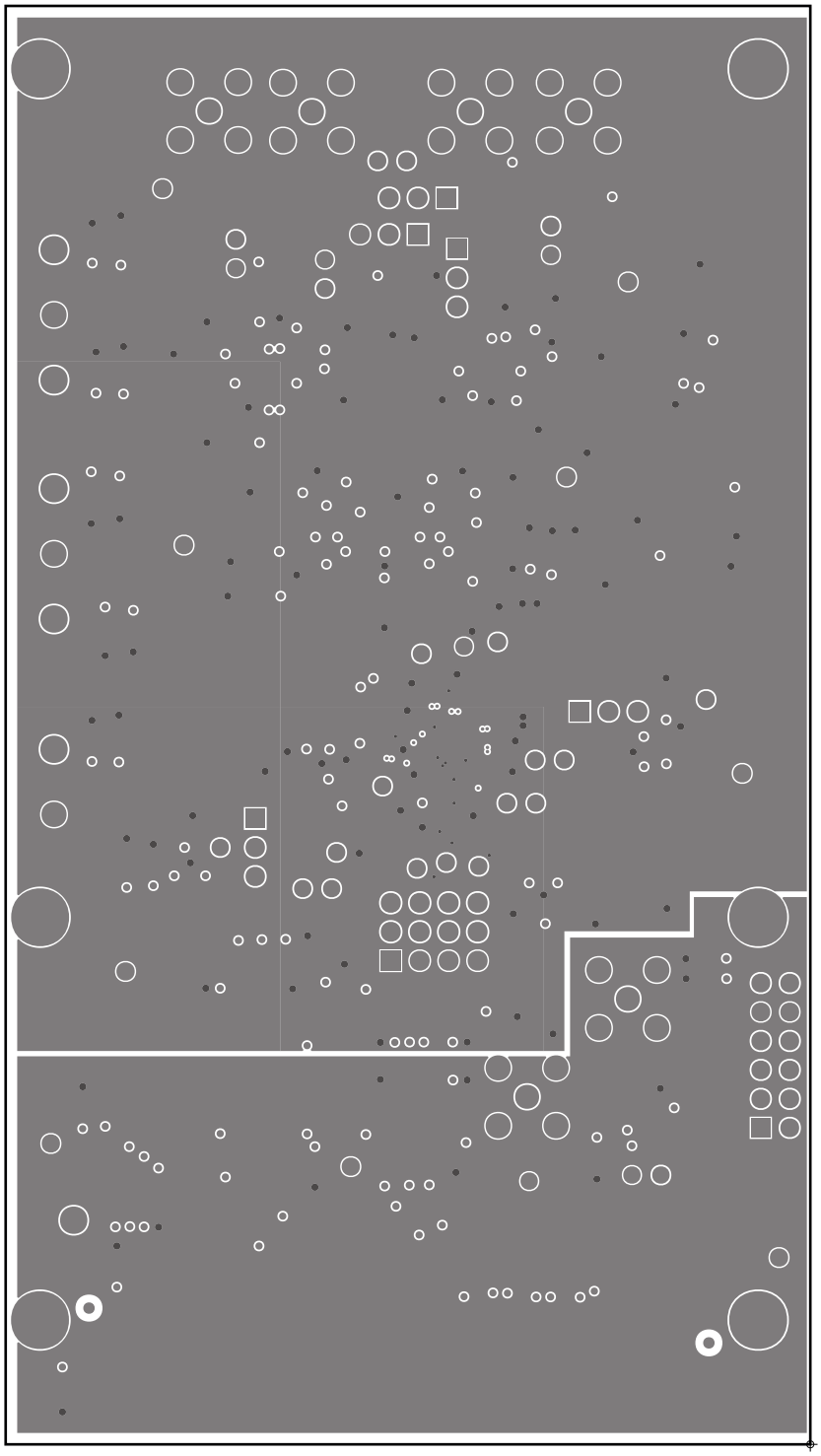


Figure 17. MAX11905 EV Kit PCB Layout—Layer 2

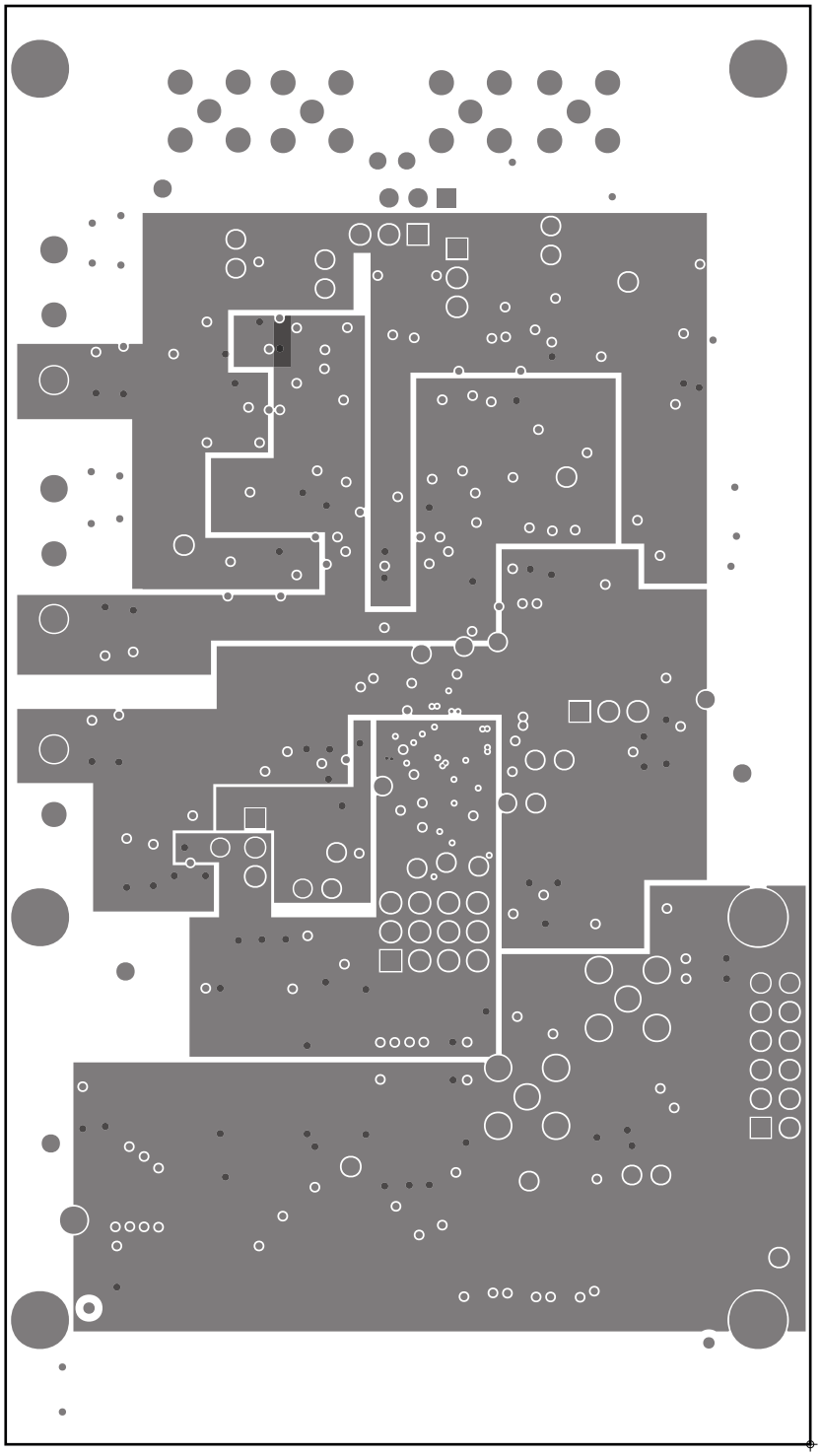


Figure 18. MAX11905 EV Kit PCB Layout—Layer 3

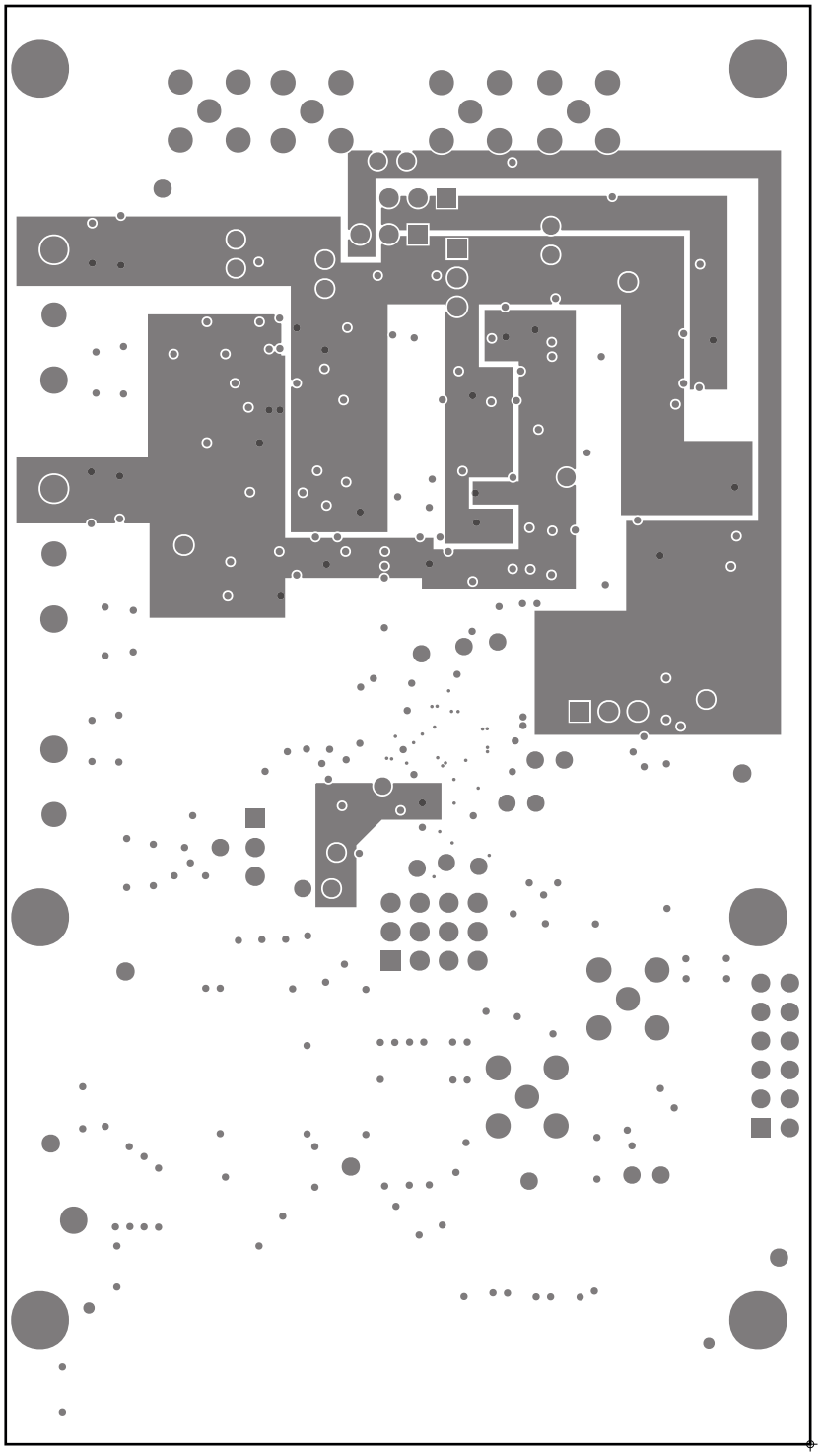


Figure 19. MAX11905 EV Kit PCB Layout—Layer 4

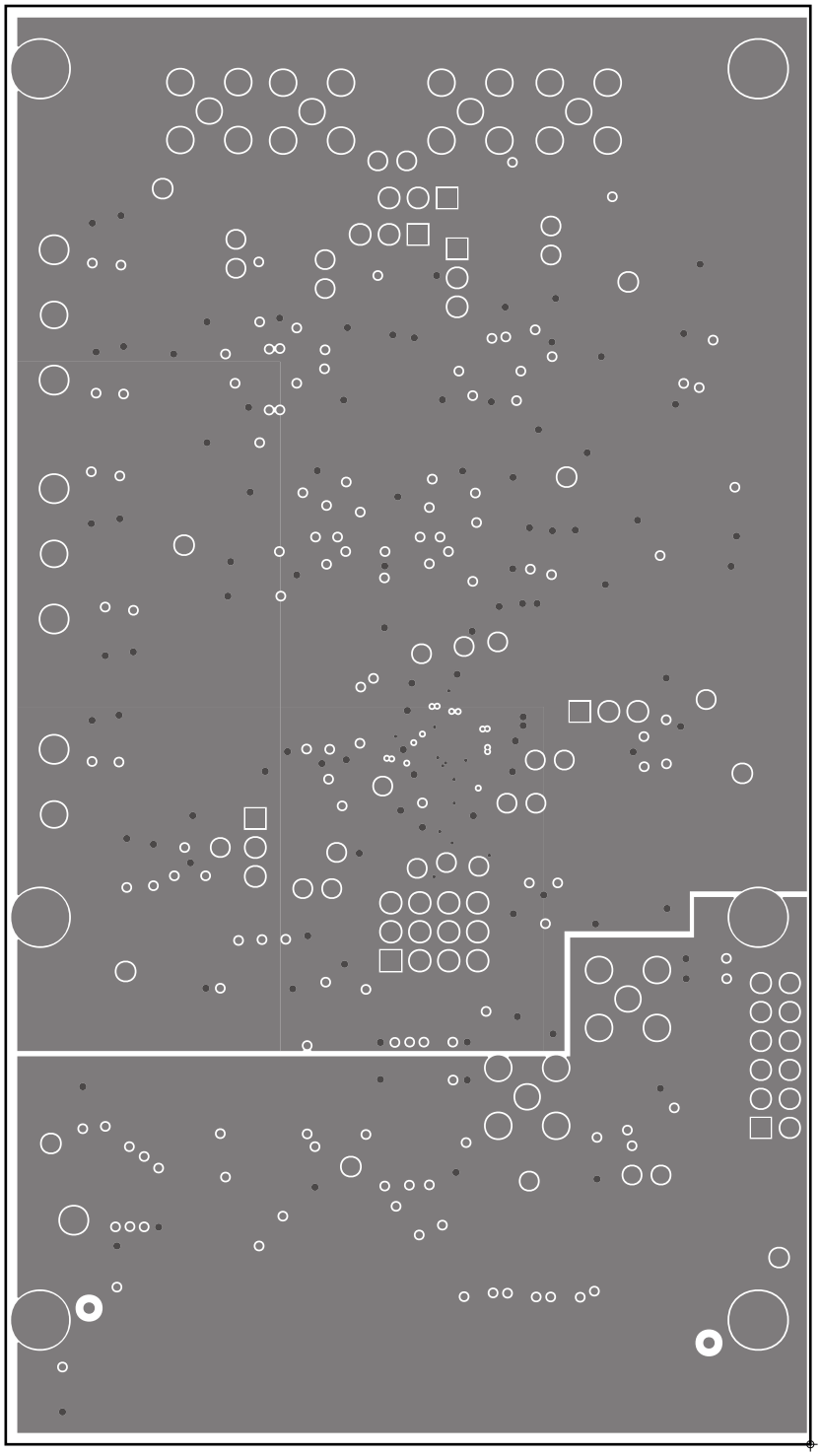


Figure 20. MAX11905 EV Kit PCB Layout—Layer 5

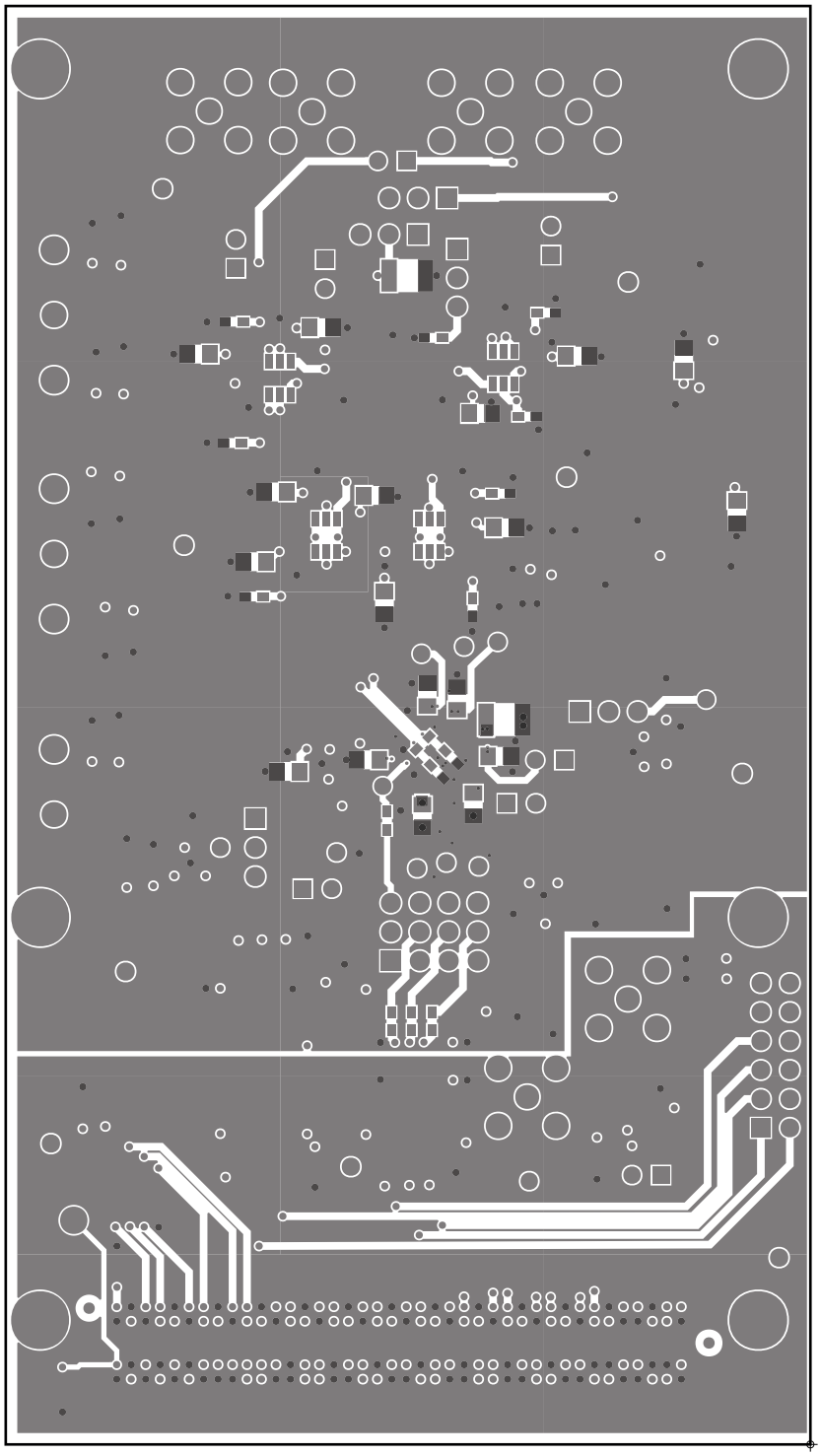


Figure 21. MAX11905 EV Kit PCB Layout—Solder Side