19-3295; Rev 7; 2/12

EVALUATION KIT AVAILABLE

12-Bit, Multichannel ADCs/DACs with FIFO, Temperature Sensing, and GPIO Ports

General Description

The MAX1220/MAX1257/MAX1258 integrate a 12-bit, multichannel, analog-to-digital converter (ADC), and a 12-bit, octal, digital-to-analog converter (DAC) in a single IC. These devices also include a temperature sensor and configurable general-purpose I/O ports (GPIOs) with a 25MHz SPI-/QSPI™-/MICROWIRE®-compatible serial interface. The ADC is available in 8 and 16 input-channel versions. The octal DAC outputs settle within 2.0µs and the ADC has a 225ksps conversion rate.

All devices include an internal reference (2.5V or 4.096V) for both the ADC and DAC. Programmable reference modes allow the use of an internal reference, an external reference, or a combination of both. Features such as an internal ±1°C accurate temperature sensor, FIFO, scan modes, programmable internal or external clock modes, data averaging, and AutoShutdown™ allow users to minimize power consumption and processor requirements. The low glitch energy (4nV•s) and low digital feedthrough (0.5nV•s) of the integrated octal DACs make these devices ideal for digital control of fast-response closed-loop systems.

The devices are guaranteed to operate with a supply voltage from +2.7V to +3.6V (MAX1257) and from +4.75V to +5.25V (MAX1220/MAX1258). These devices consume 2.5mA at 225ksps throughput, only 22µA at 1ksps throughput, and under 0.2µA in the shutdown mode. The MAX1257/MAX1258 feature 12 GPIOs, while the MAX1220 offers four GPIOs that can be configured as inputs or outputs.

The MAX1220 is available in a 36-pin TQFN package. The MAX1257/MAX1258 are available in 48-pin TQFN package. All devices are specified over the -40°C to +85°C temperature range.

Applications

Controls for Optical Components

Base-Station Control Loops

System Supervision and Control

Data-Acquisition Systems

Features

- **12-Bit, 225ksps ADC**
  - **Analog Multiplexer with True-Differential Track/Hold (T/H)**
  - **16 Single-Ended Channels or 8 Differential Channels (Unipolar or Bipolar) (MAX1257/MAX1258)**
  - **Eight Single-Ended Channels or Four Differential Channels (Unipolar or Bipolar) (MAX1220)**
  - **Excellent Accuracy: ±0.5 LSB INL, ±0.5 LSB DNL**
- **12-Bit, Octal, 2µs Settling DAC**
  - **Ultra-Low Glitch Energy (4nV•s)**
  - **Power-Up Options from Zero Scale or Full Scale**
  - **Excellent Accuracy: ±0.5 LSB INL**
- **Internal Reference or External Single-Ended/ Differential Reference**
  - **Internal Reference Voltage 2.5V or 4.096V**
- **Internal ±1°C Accurate Temperature Sensor**
- **On-Chip FIFO Capable of Storing 16 ADC Conversion Results and One Temperature Result**
- **On-Chip Channel-Scan Mode and Internal Data-Averaging Features**
- **Analog Single-Supply Operation**
  - **+2.7V to +3.6V or +4.75V to +5.25V**
- **Digital Supply: +2.7V to AVDD**
- **25MHz, SPI/QSPI/MICROWIRE Serial Interface**
- **AutoShutdown Between Conversions**
- **Low-Power ADC**
  - **2.5mA at 225ksps**
  - **22µA at 1ksps**
  - **0.2µA at Shutdown**
- **Low-Power DAC: 1.5mA**
- **Evaluation Kit Available (Order MAX1258EVKIT)**

Pin Configurations appear at end of data sheet.

Ordering Information/Selector Guide

PART	PIN-PACKAGE	REF VOLTAGE (V)	ANALOG SUPPLY VOLTAGE (V)	RESOLUTION BITS**	ADC CHANNELS	DAC CHANNELS	GPIOs
MAX1220BETX+	36 Thin QFN-EP*	4.096	4.75 to 5.25	12	8	8	4
MAX1257BETM+	48 Thin QFN-EP*	2.5	2.7 to 3.6	12	16	8	12
MAX1258BETM+	48 Thin QFN-EP*	4.096	4.75 to 5.25	12	16	8	12

Note: *All devices are specified over the -40°C to +85°C operating range.*
+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*
***Number of resolution bits refers to both DAC and ADC.*

ABSOLUTE MAXIMUM RATINGS

AVDD to AGND ....-0.3V to +6V
DGND to AGND...-0.3V to +0.3V
DVDD to AVDD...-3.0V to +0.3V
Digital Inputs to DGND..-0.3V to +6V
Digital Outputs to DGND........................-0.3V to (V_{DVDD} + 0.3V)
Analog Inputs, Analog Outputs and REF_
to AGND ....-0.3V to (V_{AVDD} + 0.3V)
Maximum Current into Any Pin (except AGND, DGND, AVDD, DVDD, and OUT_)...50mA
Maximum Current into OUT_..100mA
Continuous Power Dissipation (multilayer board, T_A = +70°C)
36-Pin TQFN (6mm x 6mm)
(derate 35.7mW/°C above +70°C)......................2857.1mW
48-Pin TQFN (7mm x 7mm)
(derate 40mW/°C above +70°C)...........................3200mW
Operating Temperature Range ....-40°C to +85°C
Storage Temperature Range ....-60°C to +150°C
Junction Temperature ....+150°C
Lead Temperature (soldering, 10s) ....+300°C
Soldering Temperature ....+260°C

Note: If the package power dissipation is not exceeded, one output at a time may be shorted to AVDD, DVDD, AGND, or DGND indefinitely.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{AVDD} = V_{DVDD} = 2.7V to 3.6V (MAX1257), external reference V_{REF} = 2.5V (MAX1257), V_{AVDD} = 4.75V to 5.25V, V_{DVDD} = 2.7V to V_{AVDD} (MAX1220/MAX1258), external reference V_{REF} = 4.096V (MAX1220/MAX1258), f_{CLK} = 3.6MHz (50% duty cycle), T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = 3V (MAX1257), V_{AVDD} = V_{DVDD} = 5V (MAX1220/MAX1258), T_A = +25°C. Outputs are unloaded, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ADC						
DC ACCURACY (Note 1)						
Resolution			12			Bits
Integral Nonlinearity	INL			±0.5	±1.0	LSB
Differential Nonlinearity	DNL			±0.5	±1.0	LSB
Offset Error				±1	±4.0	LSB
Gain Error		(Note 2)		±0.1	±4.0	LSB
Gain Temperature Coefficient				±0.8		ppm/°C
Channel-to-Channel Offset				±0.1		LSB
DYNAMIC SPECIFICATIONS (10kHz sine-wave input, V_{IN} = 2.5V_{P-P} (MAX1257), V_{IN} = 4.096V_{P-P} (MAX1220/MAX1258), 225ksps, f_{CLK} = 3.6MHz)						
Signal-to-Noise Plus Distortion	SINAD			70		dB
Total Harmonic Distortion (Up to the Fifth Harmonic)	THD			-76		dBc
Spurious-Free Dynamic Range	SFDR			72		dBc
Intermodulation Distortion	IMD	f_{IN1} = 9.9kHz, f_{IN2} = 10.2kHz		76		dBc
Full-Linear Bandwidth		SINAD > 70dB		100		kHz
Full-Power Bandwidth		-3dB point		1		MHz
CONVERSION RATE (Note 3)						
Power-Up Time	t_{PU}	External reference		0.8		µs
		Internal reference (Note 4)		218		Conversion clock cycles

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{DVDD} = 2.7V to 3.6V (MAX1257), external reference V_{REF} = 2.5V (MAX1257), V_{AVDD} = 4.75V to 5.25V, V_{DVDD} = 2.7V to V_{AVDD} (MAX1220/MAX1258), external reference V_{REF} = 4.096V (MAX1220/MAX1258), f_{CLK} = 3.6MHz (50% duty cycle), T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = 3V (MAX1257), V_{AVDD} = V_{DVDD} = 5V (MAX1220/MAX1258), T_A = +25°C. Outputs are unloaded, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Acquisition Time	t_{ACQ}	(Note 5)	0.6			µs
Conversion Time	t_{CONV}	Internally clocked		5.5		µs
		Externally clocked	3.6			
External Clock Frequency	f_{CLK}	Externally clocked conversion (Note 5)	0.1		3.6	MHz
Duty Cycle			40		60	%
Aperture Delay				30		ns
Aperture Jitter				< 50		ps
ANALOG INPUTS						
Input Voltage Range (Note 6)		Unipolar	0		V_{REF}	V
		Bipolar	$-V_{REF}/2$		$+V_{REF}/2$	
Input Leakage Current				±0.01	±1	µA
Input Capacitance				24		pF
INTERNAL TEMPERATURE SENSOR						
Measurement Error (Notes 5, 7)		T_A = +25°C		±0.7		°C
		T_A = T_{MIN} to T_{MAX}		±1.0	±3.0	
Temperature Resolution				1/8		°C/LSB
INTERNAL REFERENCE						
REF1 Output Voltage (Note 8)		MAX1257	2.482	2.50	2.518	V
		MAX1220/MAX1258	4.066	4.096	4.126	
REF1 Voltage Temperature Coefficient	TC_{REF}			±30		ppm/°C
REF1 Output Impedance				6.5		k
REF1 Short-Circuit Current		V_{REF} = 2.5V		0.39		mA
		V_{REF} = 4.096V		0.63		
EXTERNAL REFERENCE						
REF1 Input Voltage Range	V_{REF1}	REF mode 11 (Note 4)	1		V_{AVDD} + 0.05	V
REF2 Input Voltage Range (Note 4)	V_{REF2}	REF mode 01	1		V_{AVDD} + 0.05	V
		REF mode 11	0		1	

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{DVDD} = 2.7V to 3.6V (MAX1257), external reference V_{REF} = 2.5V (MAX1257), V_{AVDD} = 4.75V to 5.25V, V_{DVDD} = 2.7V to V_{AVDD} (MAX1220/MAX1258), external reference V_{REF} = 4.096V (MAX1220/MAX1258), f_{CLK} = 3.6MHz (50% duty cycle), T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = 3V (MAX1257), V_{AVDD} = V_{DVDD} = 5V (MAX1220/MAX1258), T_A = +25°C. Outputs are unloaded, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
REF1 Input Current (Note 9)	I_{REF1}	V_{REF} = 2.5V (MAX1257), f_{SAMPLE} =		25	80	µA
		V_{REF} = 4.096V (MAX1220/MAX1258), f_{SAMPLE} = 225ksps		40	80	
		Acquisition between conversions		±0.01	±1	
REF2 Input Current	I_{REF2}	V_{REF} = 2.5V (MAX1257), f_{SAMPLE} =		25	80	µA
		V_{REF} = 4.096V (MAX1220/MAX1258), f_{SAMPLE} = 225ksps		40	80	
		Acquisition between conversions		±0.01	±1	
DAC						
DC ACCURACY (Note 10)						
Resolution			12			Bits
Integral Nonlinearity	INL			±0.5	±4	LSB
Differential Nonlinearity	DNL	Guaranteed monotonic			±1.0	LSB
Offset Error	V_{OS}	(Note 8)		±3	±10	mV
Offset-Error Drift				±10		ppm of FS/°C
Gain Error	GE	(Note 8)		±5	±10	LSB
Gain Temperature Coefficient				±8		ppm of FS/°C
DAC OUTPUT						
Output-Voltage Range		No load	0.02		V_{AVDD} - 0.02	V
		10k load to either rail	0.1		V_{AVDD} - 0.1	
DC Output Impedance				0.5		
Capacitive Load		(Note 11)			1	nF
Resistive Load to AGND	R_L	V_{AVDD} = 2.7V, V_{REF} = 2.5V (MAX1257), gain error < 1%	2000			
		V_{AVDD} = 4.75V, V_{REF} = 4.096V (MAX1220/MAX1258), gain error < 2%	500			
Wake-Up Time (Note 12)		From power-down mode, V_{AVDD} = 5V		25		µs
		From power-down mode, V_{AVDD} = 2.7V		21		
1k Output Termination		Programmed in from power-down mode		1		k
100k Output Termination		At wake-up or programmed in power-down mode		100		k

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{DVDD} = 2.7V to 3.6V (MAX1257), external reference V_{REF} = 2.5V (MAX1257), V_{AVDD} = 4.75V to 5.25V, V_{DVDD} = 2.7V to V_{AVDD} (MAX1220/MAX1258), external reference V_{REF} = 4.096V (MAX1220/MAX1258), f_{CLK} = 3.6MHz (50% duty cycle), T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = 3V (MAX1257), V_{AVDD} = V_{DVDD} = 5V (MAX1220/MAX1258), T_A = +25°C. Outputs are unloaded, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DYNAMIC PERFORMANCE (Notes 5, 13)						
Output-Voltage Slew Rate	SR	Positive and negative	3			V/µs
Output-Voltage Settling Time	t_S	To 1 LSB, 400 - C00 hex (Note 7)		2	5	µs
Digital Feedthrough		Code 0, all digital inputs from 0 to V_{DVDD}		0.5		nV•s
Major Code Transition Glitch Impulse		Between codes 2047 and 2048		4		nV•s
Output Noise (0.1Hz to 50MHz)		From V_{REF}		660		$µV_{P-P}$
		Using internal reference		720		
Output Noise (0.1Hz to 500kHz)		From V_{REF}		260		$µV_{P-P}$
		Using internal reference		320		
DAC-to-DAC Transition Crosstalk				0.5		nV•s
INTERNAL REFERENCE						
REF1 Output Voltage (Note 8)		MAX1257	2.482	2.5	2.518	V
		MAX1220/MAX1258	4.066	4.096	4.126	
REF1 Temperature Coefficient	TC_{REF}			±30		ppm/°C
REF1 Short-Circuit Current		V_{REF} = 2.5V		0.39		mA
		V_{REF} = 4.096V		0.63		
EXTERNAL-REFERENCE INPUT						
REF1 Input Voltage Range	V_{REF1}	REF modes 01, 10, and 11 (Note 4)	0.7		V_{AVDD}	V
REF1 Input Impedance	R_{REF1}		70	100	130	kΩ
DIGITAL INTERFACE						
DIGITAL INPUTS (SCLK, DIN, $\overline{CS}$, $\overline{CNVST}$, $\overline{LDAC}$)						
Input-Voltage High	V_{IH}	V_{DVDD} = 2.7V to 5.25V	2.4			V
Input-Voltage Low	V_{IL}	V_{DVDD} = 3.6V to 5.25V			0.8	V
		V_{DVDD} = 2.7V to 3.6V			0.6	
Input Leakage Current	I_L			±0.01	±10	µA
Input Capacitance	C_{IN}			15		pF
DIGITAL OUTPUT (DOUT) (Note 14)						
Output-Voltage Low	V_{OL}	I_{SINK} = 2mA			0.4	V
Output-Voltage High	V_{OH}	I_{SOURCE} = 2mA	V_{DVDD} - 0.5			V
Three-State Leakage Current					±10	µA
Three-State Output Capacitance	C_{OUT}			15		pF

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{DVDD} = 2.7V to 3.6V (MAX1257), external reference V_{REF} = 2.5V (MAX1257), V_{AVDD} = 4.75V to 5.25V, V_{DVDD} = 2.7V to V_{AVDD} (MAX1220/MAX1258), external reference V_{REF} = 4.096V (MAX1220/MAX1258), f_{CLK} = 3.6MHz (50% duty cycle), T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = 3V (MAX1257), V_{AVDD} = V_{DVDD} = 5V (MAX1220/MAX1258), T_A = +25°C. Outputs are unloaded, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL OUTPUT ($\overline{EOC}$) (Note 14)						
Output-Voltage Low	V_{OL}	I_{SINK} = 2mA			0.4	V
Output-Voltage High	V_{OH}	I_{SOURCE} = 2mA	V_{DVDD} - 0.5			V
Three-State Leakage Current					±10	µA
Three-State Output Capacitance	C_{OUT}			15		pF
DIGITAL OUTPUTS (GPIO_) (Note 14)						
GPIOB_, GPIOC_ Output-Voltage Low		I_{SINK} = 2mA			0.4	V
		I_{SINK} = 4mA			0.8	
GPIOB_, GPIOC_ Output-Voltage High		I_{SOURCE} = 2mA	V_{DVDD} - 0.5			V
GPIOA_ Output-Voltage Low		I_{SINK} = 15mA			0.8	V
GPIOA_ Output-Voltage High		I_{SOURCE} = 15mA	V_{DVDD} - 0.8			V
Three-State Leakage Current					±10	µA
Three-State Output Capacitance	C_{OUT}			15		pF
POWER REQUIREMENTS (Note 15)						
Digital Positive-Supply Voltage	DV_{DD}		2.7		V_{AVDD}	V
Digital Positive-Supply Current	DI_{DD}	Idle, all blocks shut down		0.2	4	µA
		Only ADC on, external reference		1		mA
Analog Positive-Supply Voltage	AV_{DD}	MAX1257	2.7		3.6	V
		MAX1220/MAX1258	4.75		5.25	
Analog Positive-Supply Current	AI_{DD}	Idle, all blocks shut down		0.2	2	µA
		Only ADC on, external reference, f_{SAMPLE} = 225ksps		2.8	4.2	mA
		Only ADC on, external reference, f_{SAMPLE} = 100ksps		2.6		
		All DACs on, no load, internal reference		1.5	4	
REF1 Positive-Supply Rejection	PSRR	MAX1257, V_{AVDD} = 2.7V		-77		dB
		MAX1220/MAX1258, V_{AVDD} = 4.75V		-80		
DAC Positive-Supply Rejection	PSRD	Output code = FFFhex, MAX1257, V_{AVDD} = 2.7V to		±0.1	±0.5	mV
		Output code = FFFhex, MAX1220/MAX1258, V_{AVDD} = 4.75V to 5.25V		±0.1	±0.5	
ADC Positive-Supply Rejection	PSRA	Full-scale input, MAX1257, V_{AVDD} = 2.7V to		±0.06	±0.5	mV
		Full-scale input, MAX1220/MAX1258, V_{AVDD} = 4.75V to 5.25V		±0.06	±0.5	

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = V_{DVDD} = 2.7V to 3.6V (MAX1257), external reference V_{REF} = 2.5V (MAX1257), V_{AVDD} = 4.75V to 5.25V, V_{DVDD} = 2.7V to V_{AVDD} (MAX1220/MAX1258), external reference V_{REF} = 4.096V (MAX1220/MAX1258), f_{CLK} = 3.6MHz (50% duty cycle), T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = 3V (MAX1257), V_{AVDD} = V_{DVDD} = 5V (MAX1220/MAX1258), T_A = +25°C. Outputs are unloaded, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TIMING CHARACTERISTICS (Figures 6–13)						
SCLK Clock Period	t_{CP}		40			ns
SCLK Pulse-Width High	t_{CH}	40/60 duty cycle	16			ns
SCLK Pulse-Width Low	t_{CL}	60/40 duty cycle	16			ns
GPIO Output Rise/Fall After $\overline{CS}$ Rise	t_{GOD}	C_{LOAD} = 20pF			100	ns
GPIO Input Setup Before $\overline{CS}$ Fall	t_{GSU}		0			ns
$\overline{LDAC}$ Pulse Width	$t_{LDACPWL}$		20			ns
SCLK Fall to DOUT Transition (Note 16)	t_{DOT}	C_{LOAD} = 20pF, SLOW = 0	1.8		12.0	ns
		C_{LOAD} = 20pF, SLOW = 1	10		40	
SCLK Rise to DOUT Transition (Notes 16, 17)	t_{DOT}	C_{LOAD} = 20pF, SLOW = 0	1.8		12.0	ns
		C_{LOAD} = 20pF, SLOW = 1	10		40	
$\overline{CS}$ Fall to SCLK Fall Setup Time	t_{CSS}		10			ns
SCLK Fall to $\overline{CS}$ Rise Hold Time	t_{CSH}		0		2000	ns
DIN to SCLK Fall Setup Time	t_{DS}		10			ns
DIN to SCLK Fall Hold Time	t_{DH}		0			ns
$\overline{CS}$ Pulse-Width High	t_{CSPWH}		50			ns
$\overline{CS}$ Rise to DOUT Disable	t_{DOD}	C_{LOAD} = 20pF			25	ns
$\overline{CS}$ Fall to DOUT Enable	t_{DOE}	C_{LOAD} = 20pF	1.5		25.0	ns
$\overline{EOC}$ Fall to $\overline{CS}$ Fall	t_{RDS}		30			ns
$\overline{CS}$ or $\overline{CNVST}$ Rise to $\overline{EOC}$ Fall—Internally Clocked Conversion Time	t_{DOV}	CKSEL = 01 (temp sense) or CKSEL = 10 (temp sense), internal reference on (Note 18)			65	µs
		CKSEL = 01 (temp sense) or CKSEL = 10 (temp sense), internal reference initially off			140	
		CKSEL = 01 (voltage conversion)			9	
		CKSEL = 10 (voltage conversion), internal reference on (Note 18)			9	
		CKSEL = 10 (voltage conversion), internal reference initially off			80	
$\overline{CNVST}$ Pulse Width	t_{CSW}	CKSEL = 00, CKSEL = 01 (temp sense)	40			ns
		CKSEL = 01 (voltage conversion)	1.4			µs

12-Bit, Multichannel ADCs/DACs with FIFO, Temperature Sensing, and GPIO Ports

ELECTRICAL CHARACTERISTICS (continued)

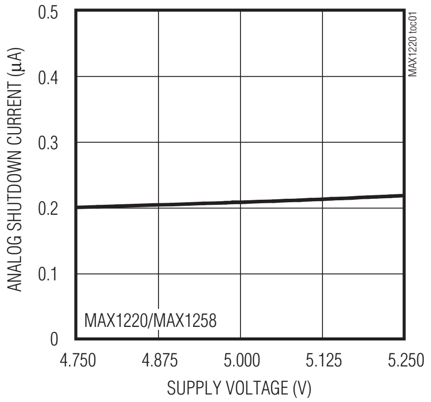
(V_{AVDD} = V_{DVDD} = 2.7V to 3.6V (MAX1257), external reference V_{REF} = 2.5V (MAX1257), V_{AVDD} = 4.75V to 5.25V, V_{DVDD} = 2.7V to V_{AVDD} (MAX1220/MAX1258), external reference V_{REF} = 4.096V (MAX1220/MAX1258), f_{CLK} = 3.6MHz (50% duty cycle), T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{AVDD} = V_{DVDD} = 3V (MAX1257), V_{AVDD} = V_{DVDD} = 5V (MAX1220/MAX1258), T_A = +25°C. Outputs are unloaded, unless otherwise noted.)

Note 1: Tested at V_{DVDD} = V_{AVDD} = +2.7V (MAX1257), V_{DVDD} = +2.7V, V_{AVDD} = +5.25V (MAX1220/MAX1258).
Note 2: Offset nulled.
Note 3: No bus activity during conversion. Conversion time is defined as the number of conversion clock cycles multiplied by the clock period.
Note 4: See Table 5 for reference-mode details.
Note 5: Not production tested. Guaranteed by design.
Note 6: See the *ADC/DAC References* section.
Note 7: Fast automated test, excludes self-heating effects.
Note 8: Specified over the -40°C to +85°C temperature range.
Note 9: REFSEL[1:0] = 00 and when DACs are not powered up.
Note 10: DAC linearity, gain, and offset measurements are made between codes 115 and 3981.
Note 11: The DAC buffers are guaranteed by design to be stable with a 1nF load.
Note 12: Time required by the DAC output to power up and settle within 1 LSB in the external reference mode.
Note 13: All DAC dynamic specifications are valid for a load of 100pF and 10kΩ.
Note 14: Only one digital output (either DOUT, $\overline{EOC}$, or the GPIOs) can be indefinitely shorted to either supply at one time.
Note 15: All digital inputs at either V_{DVDD} or DGND. V_{DVDD} should not exceed V_{AVDD}.
Note 16: See the *Reset Register* section and Table 9 for details on programming the SLOW bit.
Note 17: Clock mode 11 only.
Note 18: First conversion after reference power-up is always timed as if the internal reference was initially off to ensure the internal reference has settled. Subsequent conversions are timed as shown.

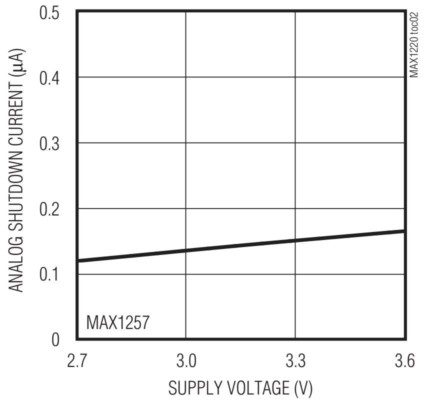
Typical Operating Characteristics

(V_{AVDD} = V_{DVDD} = 3V (MAX1257), external V_{REF} = 2.5V (MAX1257), V_{AVDD} = V_{DVDD} = 5V (MAX1220/MAX1258), external V_{REF} = 4.096V (MAX1220/MAX1258), f_{CLK} = 3.6MHz (50% duty cycle), f_{SAMPLE} = 225ksps, C_{LOAD} = 50pF, 0.1µF capacitor at REF, T_A = +25°C, unless otherwise noted.)

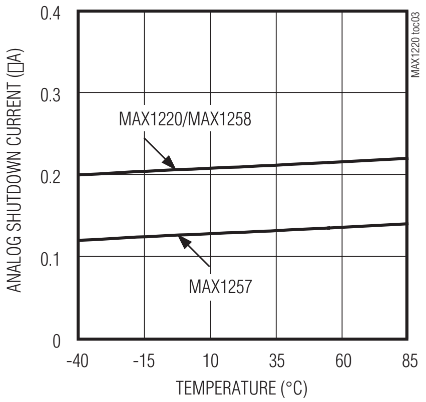
ANALOG SHUTDOWN CURRENT vs. ANALOG SUPPLY VOLTAGE



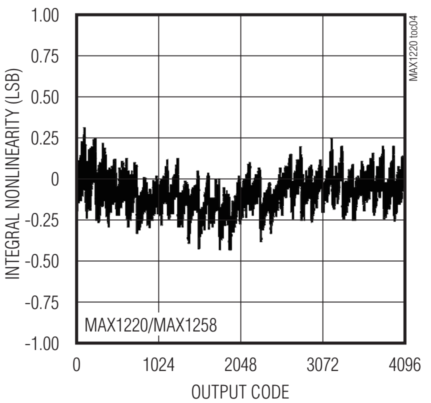
ANALOG SHUTDOWN CURRENT vs. ANALOG SUPPLY VOLTAGE



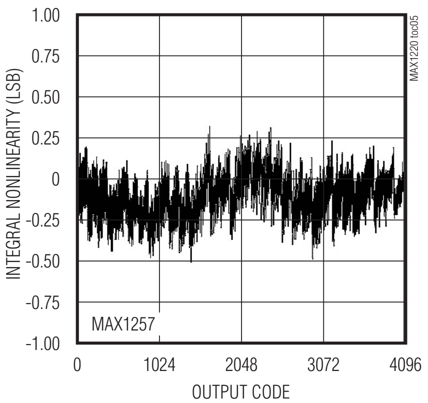
ANALOG SHUTDOWN CURRENT vs. TEMPERATURE



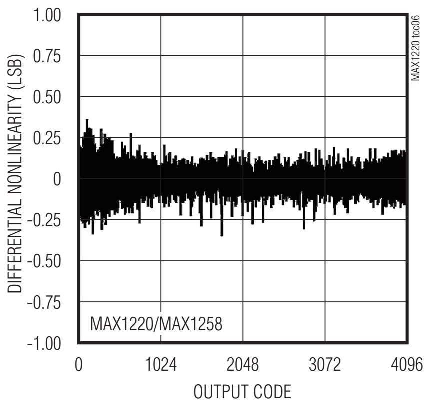
ADC INTEGRAL NONLINEARITY vs. OUTPUT CODE



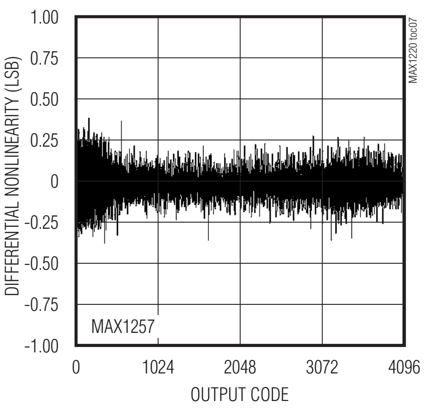
ADC INTEGRAL NONLINEARITY vs. OUTPUT CODE



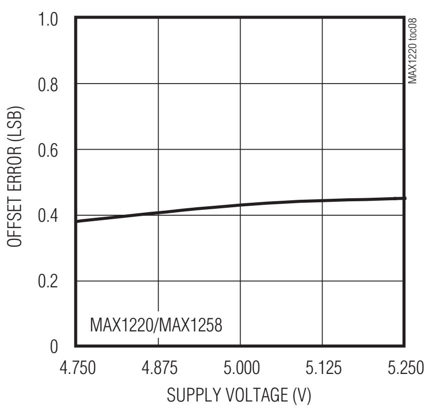
ADC DIFFERENTIAL NONLINEARITY vs. OUTPUT CODE



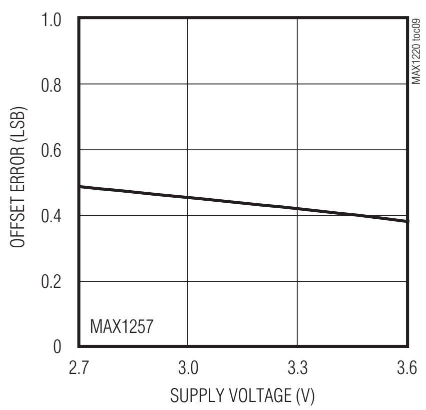
ADC DIFFERENTIAL NONLINEARITY vs. OUTPUT CODE



ADC OFFSET ERROR vs. ANALOG SUPPLY VOLTAGE



ADC OFFSET ERROR vs. ANALOG SUPPLY VOLATGE

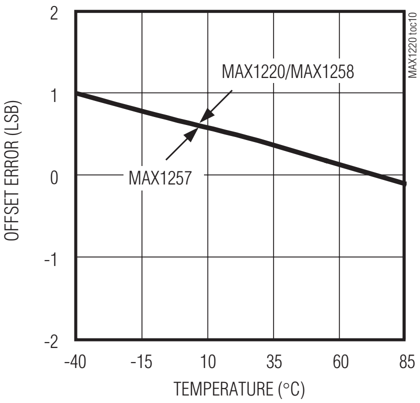


12-Bit, Multichannel ADCs/DACs with FIFO, Temperature Sensing, and GPIO Ports

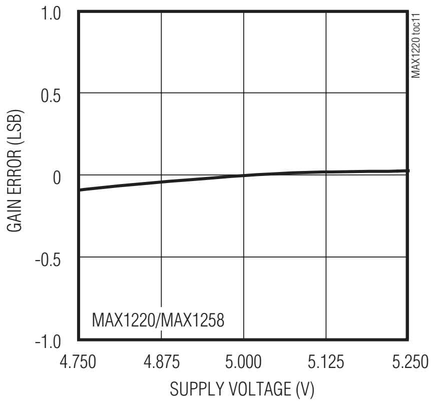
Typical Operating Characteristics (continued)

(V_{AVDD} = V_{DVDD} = 3V (MAX1257), external V_{REF} = 2.5V (MAX1257), V_{AVDD} = V_{DVDD} = 5V (MAX1220/MAX1258), external V_{REF} = 4.096V (MAX1220/MAX1258), f_{CLK} = 3.6MHz (50% duty cycle), f_{SAMPLE} = 225ksps, C_{LOAD} = 50pF, 0.1µF capacitor at REF, T_A = +25°C, unless otherwise noted.)

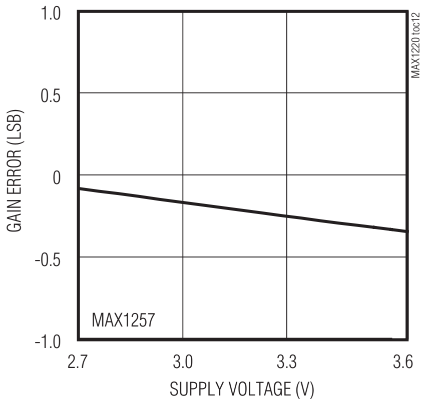
ADC OFFSET ERROR vs. TEMPERATURE



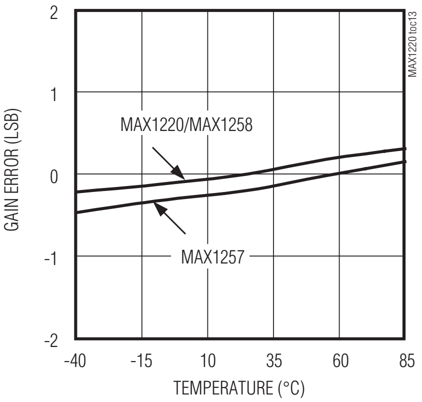
ADC GAIN ERROR vs. ANALOG SUPPLY VOLTAGE



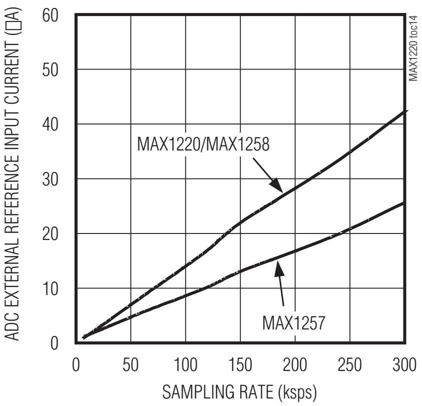
ADC GAIN ERROR vs. ANALOG SUPPLY VOLTAGE



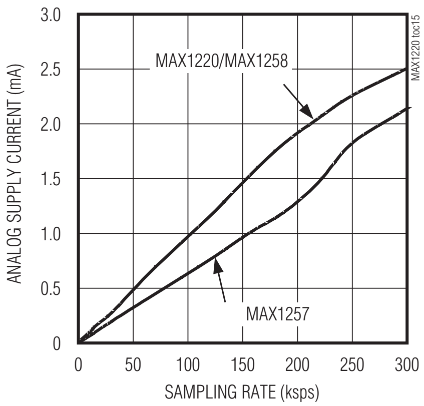
ADC GAIN ERROR vs. TEMPERATURE



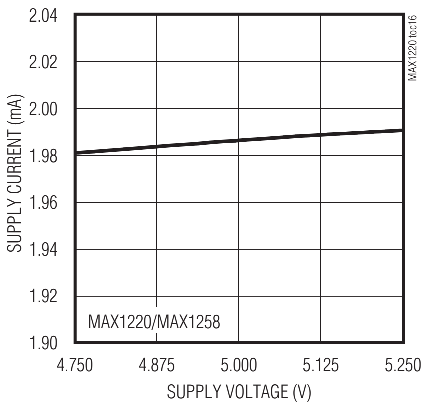
ADC EXTERNAL REFERENCE INPUT CURRENT vs. SAMPLING RATE



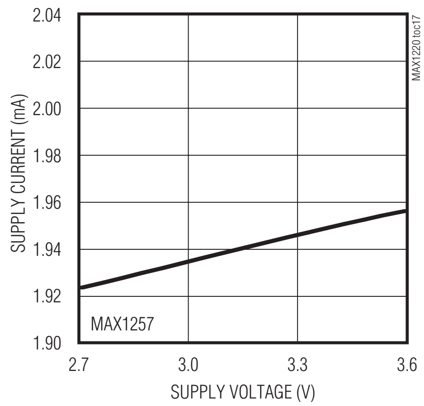
ANALOG SUPPLY CURRENT vs. SAMPLING RATE



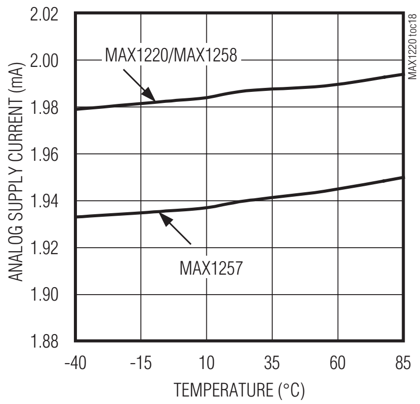
ANALOG SUPPLY CURRENT vs. ANALOG SUPPLY VOLTAGE



ANALOG SUPPLY CURRENT vs. ANALOG SUPPLY VOLTAGE



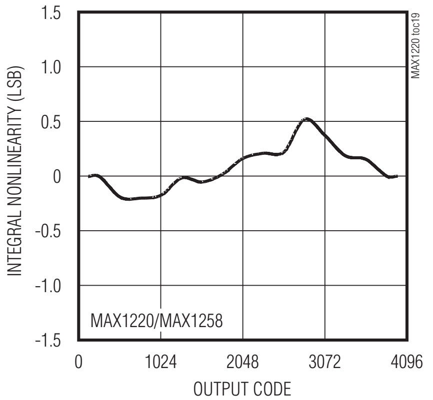
ANALOG SUPPLY CURRENT vs. TEMPERATURE



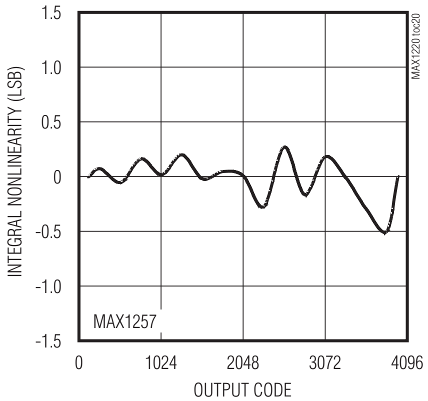
Typical Operating Characteristics (continued)

(V_{AVDD} = V_{DVDD} = 3V (MAX1257), external V_{REF} = 2.5V (MAX1257), V_{AVDD} = V_{DVDD} = 5V (MAX1220/MAX1258), external V_{REF} = 4.096V (MAX1220/MAX1258), f_{CLK} = 3.6MHz (50% duty cycle), f_{SAMPLE} = 225ksps, C_{LOAD} = 50pF, 0.1µF capacitor at REF, T_A = +25°C, unless otherwise noted.)

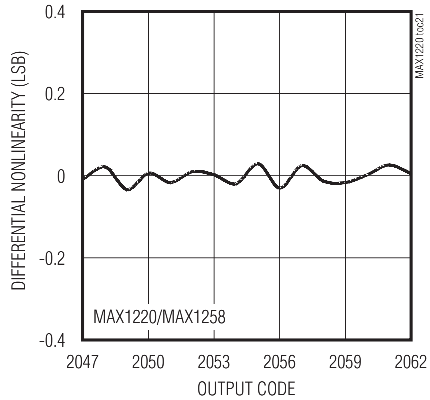
DAC INTEGRAL NONLINEARITY vs. OUTPUT CODE



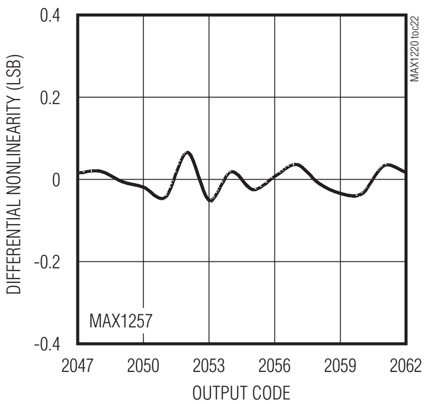
DAC INTEGRAL NONLINEARITY vs. OUTPUT CODE



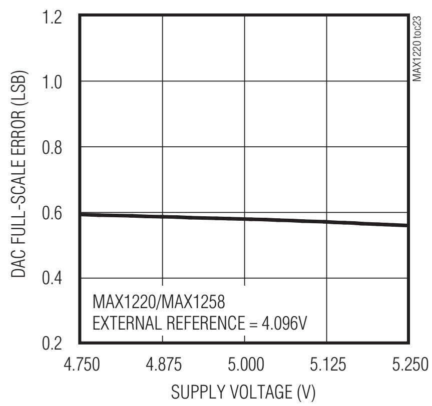
DAC DIFFERENTIAL NONLINEARITY vs. OUTPUT CODE



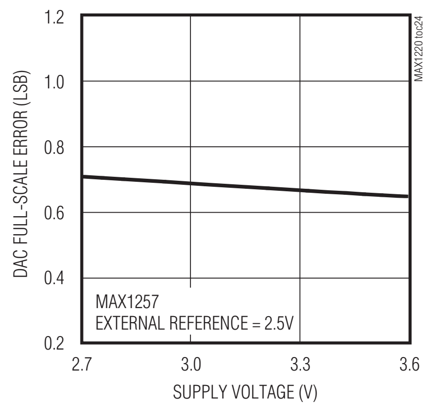
DAC DIFFERENTIAL NONLINEARITY vs. OUTPUT CODE



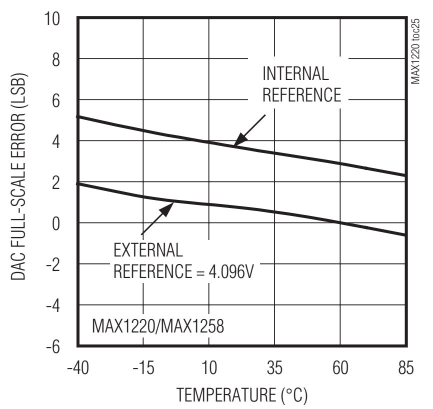
DAC FULL-SCALE ERROR vs. ANALOG SUPPLY VOLTAGE



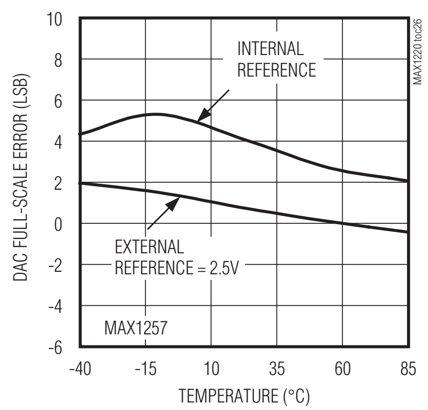
DAC FULL-SCALE ERROR vs. ANALOG SUPPLY VOLTAGE



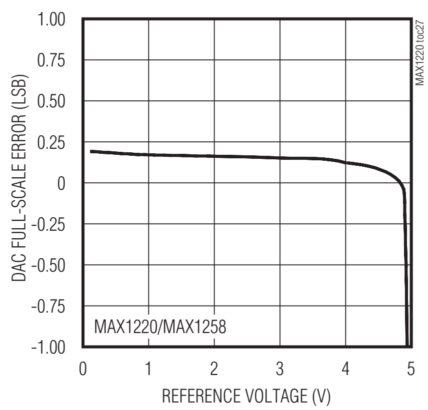
DAC FULL-SCALE ERROR vs. TEMPERATURE



DAC FULL-SCALE ERROR vs. TEMPERATURE



DAC FULL-SCALE ERROR vs. REFERENCE VOLTAGE

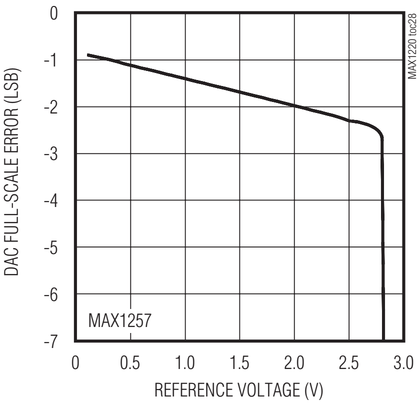


12-Bit, Multichannel ADCs/DACs with FIFO, Temperature Sensing, and GPIO Ports

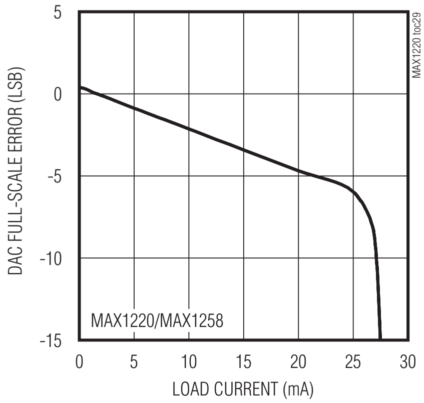
Typical Operating Characteristics (continued)

(V_{AVDD} = V_{DVDD} = 3V (MAX1257), external V_{REF} = 2.5V (MAX1257), V_{AVDD} = V_{DVDD} = 5V (MAX1220/MAX1258), external V_{REF} = 4.096V (MAX1220/MAX1258), f_{CLK} = 3.6MHz (50% duty cycle), f_{SAMPLE} = 225ksps, C_{LOAD} = 50pF, 0.1µF capacitor at REF, T_A = +25°C, unless otherwise noted.)

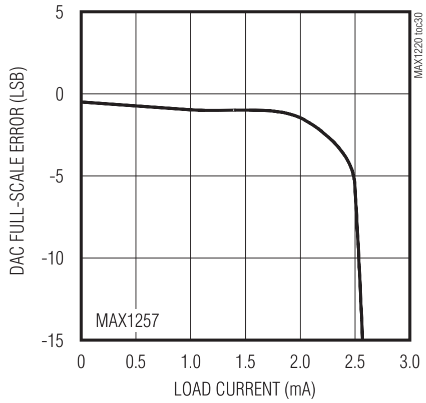
DAC FULL-SCALE ERROR vs. REFERENCE VOLTAGE



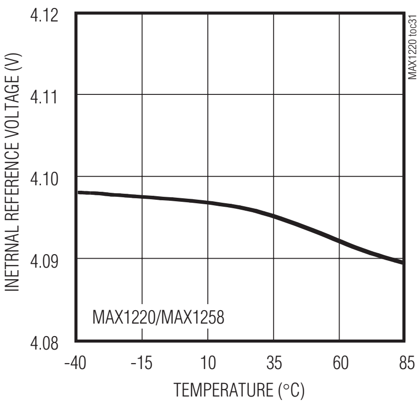
DAC FULL-SCALE ERROR vs. LOAD CURRENT



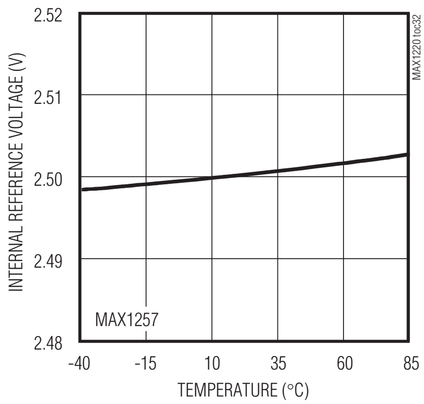
DAC FULL-SCALE ERROR vs. LOAD CURRENT



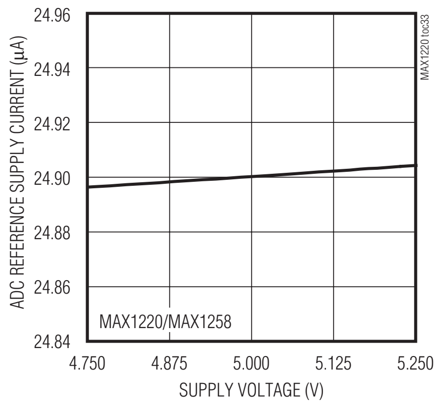
INTERNAL REFERENCE VOLTAGE vs. TEMPERATURE



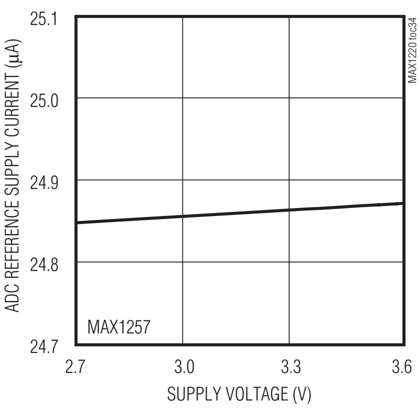
INTERNAL REFERENCE VOLTAGE vs. TEMPERATURE



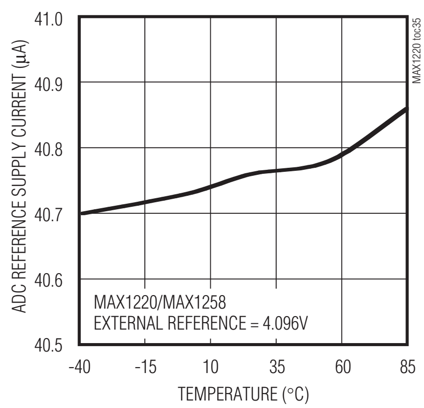
ADC REFERENCE SUPPLY CURRENT vs. ANALOG SUPPLY VOLTAGE



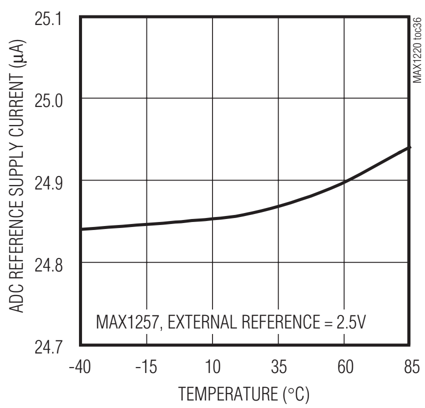
ADC REFERENCE SUPPLY CURRENT vs. ANALOG SUPPLY VOLATAGE



ADC REFERENCE SUPPLY CURRENT vs. TEMPERATURE



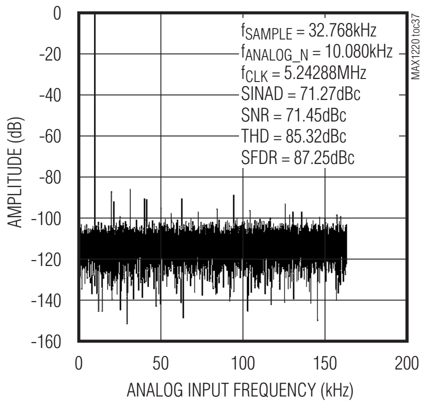
ADC REFERENCE SUPPLY CURRENT vs. TEMPERATURE



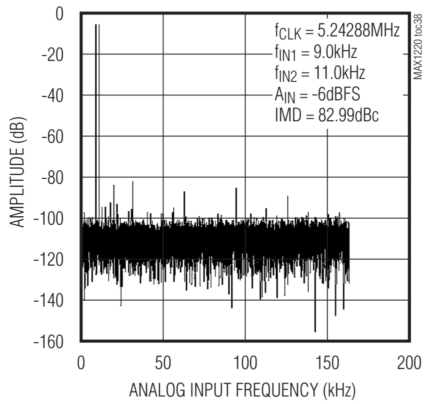
Typical Operating Characteristics (continued)

(V_{AVDD} = V_{DVDD} = 3V (MAX1257), external V_{REF} = 2.5V (MAX1257), V_{AVDD} = V_{DVDD} = 5V (MAX1220/MAX1258), external V_{REF} = 4.096V (MAX1220/MAX1258), f_{CLK} = 3.6MHz (50% duty cycle), f_{SAMPLE} = 225ksps, C_{LOAD} = 50pF, 0.1µF capacitor at REF, T_A = +25°C, unless otherwise noted.)

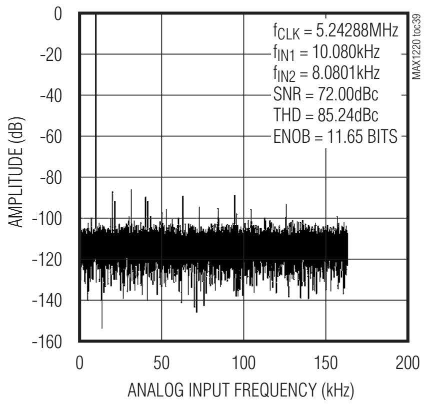
ADC FFT PLOT



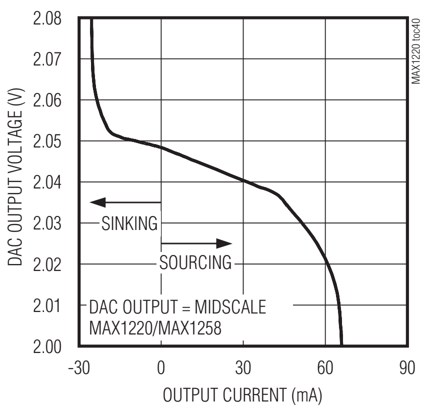
ADC IMD PLOT



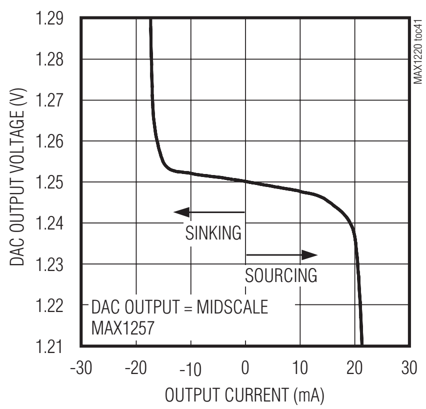
ADC CROSSTALK PLOT



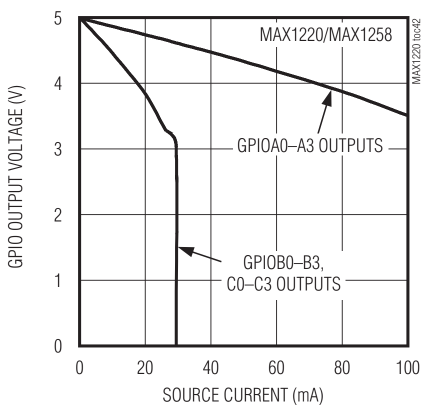
DAC OUTPUT LOAD REGULATION vs. OUTPUT CURRENT



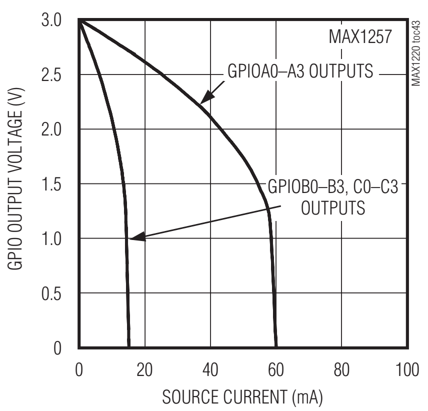
DAC OUTPUT LOAD REGULATION vs. OUTPUT CURRENT



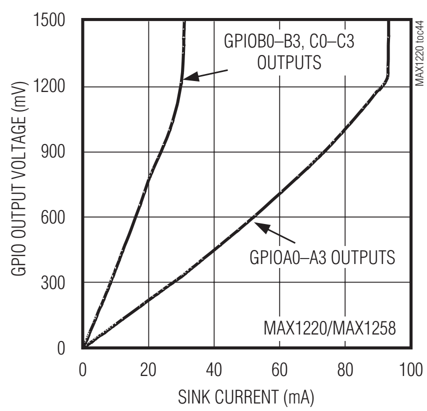
GPIO OUTPUT VOLTAGE vs. SOURCE CURRENT



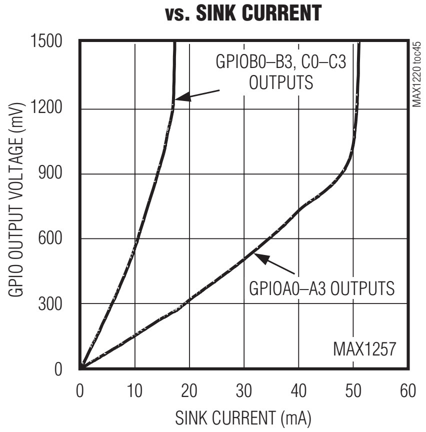
GPIO OUTPUT VOLTAGE vs. SOURCE CURRENT



GPIO OUTPUT VOLTAGE vs. SINK CURRENT



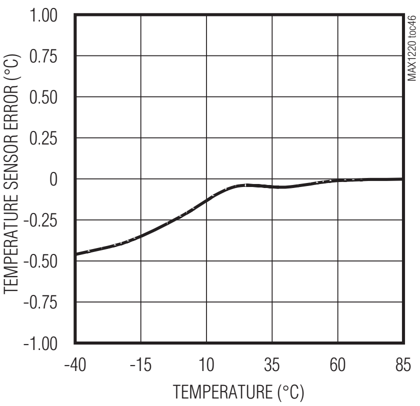
GPIO OUTPUT VOLTAGE vs. SINK CURRENT



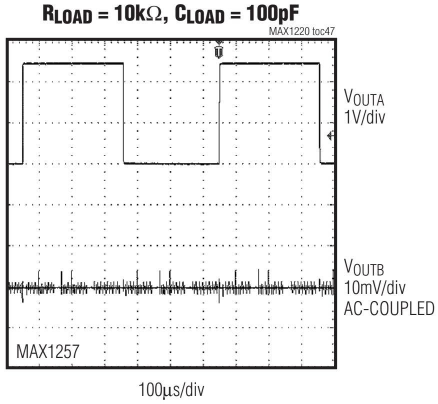
Typical Operating Characteristics (continued)

(V_{AVDD} = V_{DVDD} = 3V (MAX1257), external V_{REF} = 2.5V (MAX1257), V_{AVDD} = V_{DVDD} = 5V (MAX1220/MAX1258), external V_{REF} = 4.096V (MAX1220/MAX1258), f_{CLK} = 3.6MHz (50% duty cycle), f_{SAMPLE} = 225ksps, C_{LOAD} = 50pF, 0.1µF capacitor at REF, T_A = +25°C, unless otherwise noted.)

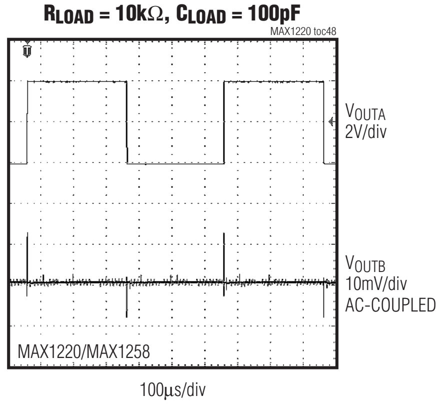
TEMPERATURE SENSOR ERROR vs. TEMPERATURE



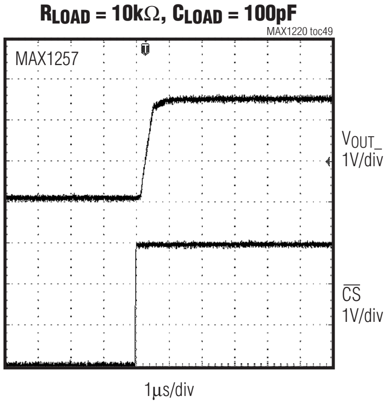
DAC-TO-DAC CROSSTALK R_{LOAD} = 10kΩ, C_{LOAD} = 100pF



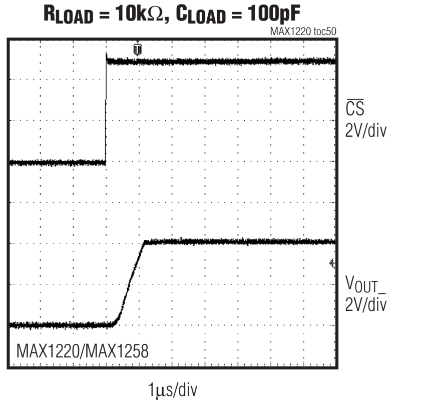
DAC-TO-DAC CROSSTALK R_{LOAD} = 10kΩ, C_{LOAD} = 100pF



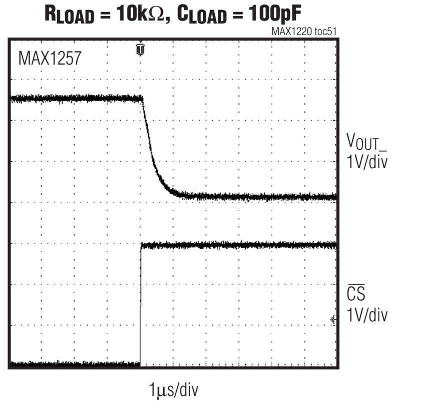
DYNAMIC RESPONSE RISE TIME R_{LOAD} = 10kΩ, C_{LOAD} = 100pF



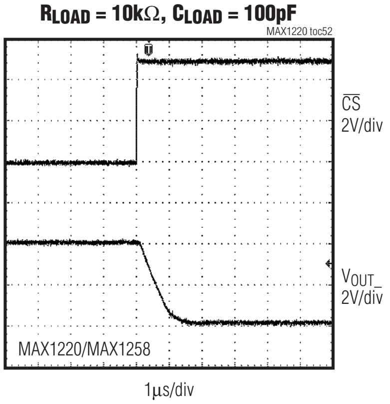
DYNAMIC RESPONSE RISE TIME R_{LOAD} = 10kΩ, C_{LOAD} = 100pF



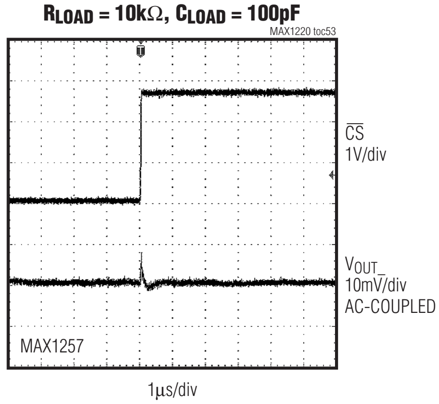
DYNAMIC RESPONSE FALL TIME R_{LOAD} = 10kΩ, C_{LOAD} = 100pF



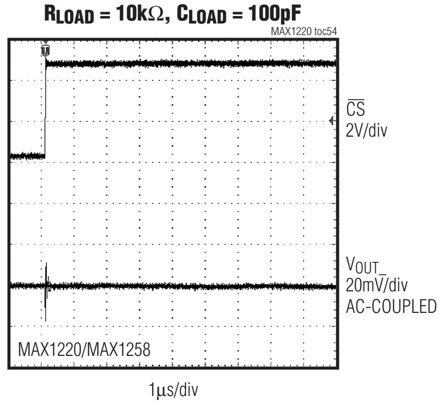
DYNAMIC RESPONSE FALL TIME R_{LOAD} = 10kΩ, C_{LOAD} = 100pF



MAJOR CARRY TRANSITION R_{LOAD} = 10kΩ, C_{LOAD} = 100pF



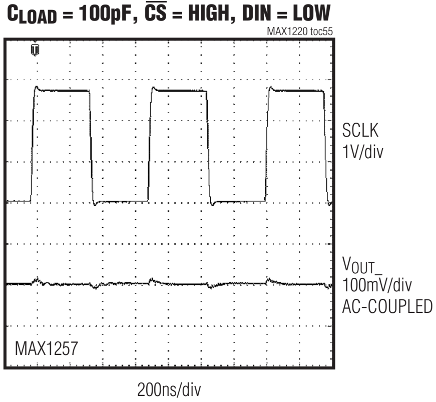
MAJOR CARRY TRANSITION R_{LOAD} = 10kΩ, C_{LOAD} = 100pF



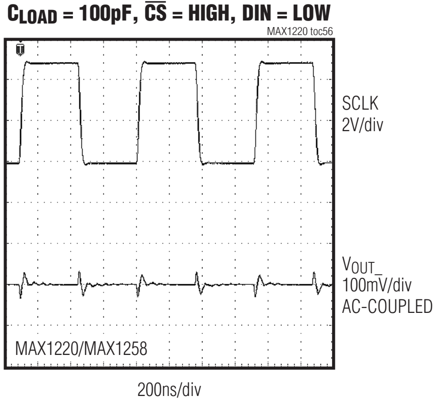
Typical Operating Characteristics (continued)

(V_{AVDD} = V_{DVDD} = 3V (MAX1257), external V_{REF} = 2.5V (MAX1257), V_{AVDD} = V_{DVDD} = 5V (MAX1220/MAX1258), external V_{REF} = 4.096V (MAX1220/MAX1258), f_{CLK} = 3.6MHz (50% duty cycle), f_{SAMPLE} = 225ksps, C_{LOAD} = 50pF, 0.1µF capacitor at REF, T_A = +25°C, unless otherwise noted.)

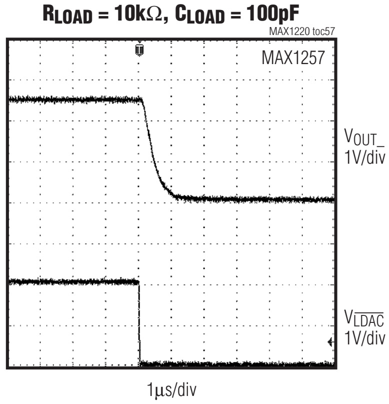
DAC DIGITAL FEEDTHROUGH R_{LOAD} = 10kΩ, C_{LOAD} = 100pF, $\overline{CS}$ = HIGH, DIN = LOW



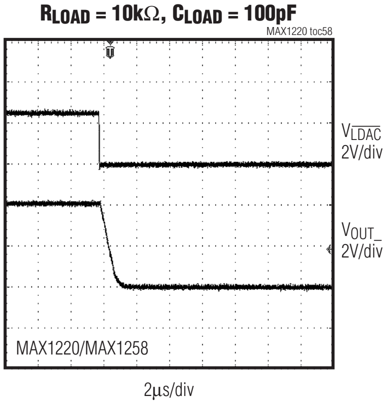
DAC DIGITAL FEEDTHROUGH R_{LOAD} = 10kΩ, C_{LOAD} = 100pF, $\overline{CS}$ = HIGH, DIN = LOW



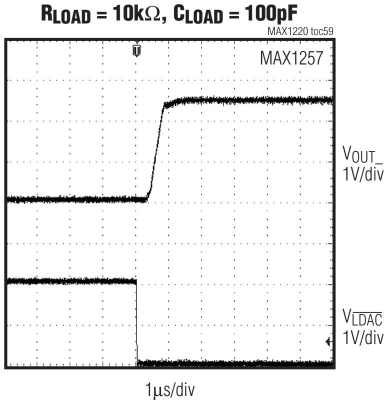
NEGATIVE FULL-SCALE SETTLING TIME R_{LOAD} = 10kΩ, C_{LOAD} = 100pF



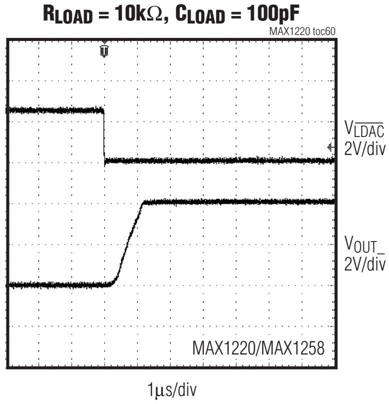
NEGATIVE FULL-SCALE SETTLING TIME R_{LOAD} = 10kΩ, C_{LOAD} = 100pF



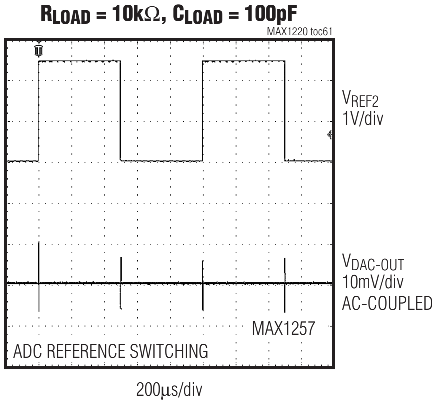
POSITIVE FULL-SCALE SETTLING TIME R_{LOAD} = 10kΩ, C_{LOAD} = 100pF



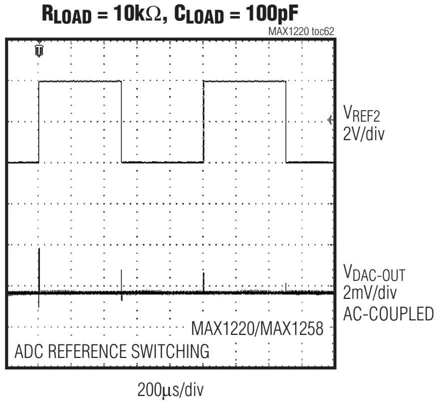
POSITIVE FULL-SCALE SETTLING TIME R_{LOAD} = 10kΩ, C_{LOAD} = 100pF



ADC REFERENCE FEEDTHROUGH R_{LOAD} = 10kΩ, C_{LOAD} = 100pF



ADC REFERENCE FEEDTHROUGH R_{LOAD} = 10kΩ, C_{LOAD} = 100pF



Pin Description

PIN		NAME	FUNCTION
MAX1220	MAX1257 MAX1258		
1, 2	—	GPIOA0, GPIOA1	General-Purpose I/O A0, A1. GPIOA0, A1 can sink and source 15mA.
3	4	$\overline{EOC}$	Active-Low End-of-Conversion Output. Data is valid after the falling edge of $\overline{EOC}$.
4	7	DVDD	Digital Positive-Power Input. Bypass DVDD to DGND with a 0.1µF capacitor.
5	8	DGND	Digital Ground. Connect DGND to AGND.
6	9	DOUT	Serial-Data Output. Data is clocked out on the falling edge of the SCLK clock in modes 00, 01, and 10. Data is clocked out on the rising edge of the SCLK clock in mode 11. It is high impedance when $\overline{CS}$ is high.
7	10	SCLK	Serial-Clock Input. Clocks data in and out of the serial interface. (Duty cycle must be 40% to 60%.) See Table 5 for details on programming the clock mode.
8	11	DIN	Serial-Data Input. DIN data is latched into the serial interface on the falling edge of SCLK.
9–12, 16–19	12–15, 22–25	OUT0–OUT7	DAC Outputs
13	18	AVDD	Positive Analog Power Input. Bypass AVDD to AGND with a 0.1µF capacitor.
14	19	AGND	Analog Ground
15, 23, 32, 33	—	N.C.	No Connection. Not internally connected.
20	26	$\overline{LDAC}$	Active-Low Load DAC. $\overline{LDAC}$ is an asynchronous active-low input that updates the DAC outputs. Drive $\overline{LDAC}$ low to make the DAC registers transparent.
21	27	$\overline{CS}$	Active-Low Chip-Select Input. When $\overline{CS}$ is low, the serial interface is enabled. When $\overline{CS}$ is high, DOUT is high impedance.
22	28	RES_SEL	Reset Select. Select DAC wake-up mode. Set RES_SEL low to wake up the DAC outputs with a 100kΩ resistor to AGND or set RES_SEL high to wake up the DAC outputs with a 100kΩ resistor to V_{REF}. Set RES_SEL high to power up the DAC input register to FFFh. Set RES_SEL low to power up the DAC input register to 000h.
24, 25	—	GPIOC0, GPIOC1	General-Purpose I/O C0, C1. GPIOC0, C1 can sink 4mA and source 2mA.

Pin Description (continued)

PIN		NAME	FUNCTION
MAX1220	MAX1257 MAX1258		
26	35	REF1	Reference 1 Input. Reference voltage; leave unconnected to use the internal reference (2.5V for the MAX1257 or 4.096V for the MAX1220/MAX1258). REF1 is the positive reference in ADC external differential reference mode. Bypass REF1 to AGND with a 0.1µF capacitor in external reference mode only. See the *ADC/DAC References* section.
27–31, 34	—	AIN0–AIN5	Analog Inputs
35	—	REF2/AIN6	Reference 2 Input/Analog Input 6. See Table 5 for details on programming the setup register. REF2 is the negative reference in the ADC external differential reference mode.
36	—	$\overline{\text{CNVST}}$/AIN7	Active-Low Conversion-Start Input/Analog Input 7. See Table 5 for details on programming the setup register.
—	1	$\overline{\text{CNVST}}$/AIN15	Active-Low Conversion-Start Input/Analog Input 15. See Table 5 for details on programming the setup register.
—	2, 3, 5, 6	GPIOA0–GPIOA3	General-Purpose I/O A0–A3. GPIOA0–GPIOA3 can sink and source 15mA.
—	16, 17, 20, 21	GPIOB0–GPIOB3	General-Purpose I/O B0–B3. GPIOB0–GPIOB3 can sink 4mA and source 2mA.
—	29–32	GPIOC0–GPIOC3	General-Purpose I/O C0–C3. GPIOC0–GPIOC3 can sink 4mA and source 2mA.
—	33, 34, 36–47	AIN0–AIN13	Analog Inputs
—	48	REF2/AIN14	Reference 2 Input/Analog Input 14. See Table 5 for details on programming the setup register. REF2 is the negative reference in the ADC external differential reference mode.
—	—	EP	Exposed Pad. Must be externally connected to AGND. Do not use as a ground connect.

Detailed Description

The MAX1220/MAX1257/MAX1258 integrate a 12-bit, multichannel, analog-to-digital converter (ADC), and a 12-bit, octal, digital-to-analog converter (DAC) in a single IC. These devices also include a temperature sensor and configurable GPIOs with a 25MHz SPI-/QSPI-/MICROWIRE-compatible serial interface. The ADC is available in 8 and 16 input-channel versions. The octal DAC outputs settle within 2.0µs, and the ADC has a 225ksps conversion rate.

All devices include an internal reference (2.5V or 4.096V) providing a well-regulated, low-noise reference for both the ADC and DAC. Programmable reference modes for the ADC and DAC allow the use of an internal reference, an external reference, or a combination of both. Features such as an internal ±1°C accurate temperature sensor, FIFO, scan modes, programmable internal or external clock modes, data averaging, and AutoShutdown allow users to minimize both power consumption and processor requirements. The low glitch energy (4nV•s) and low digital feedthrough (0.5nV•s) of the integrated octal DACs make these devices ideal for digital control of fast-response closed-loop systems.

These devices are guaranteed to operate with a supply voltage from +2.7V to +3.6V (MAX1257) and from +4.75V to +5.25V (MAX1220/MAX1258). These devices consume 2.5mA at 225ksps throughput, only 22µA at 1ksps throughput, and under 0.2µA in the shutdown mode. The MAX1257/MAX1258 feature 12 GPIOs while the MAX1220 offers four GPIOs that can be configured as inputs or outputs.

Figure 1 shows the MAX1257/MAX1258 functional diagram. The MAX1220 only includes the GPIOA0, GPIOA1 and GPIOC0, GPIOC1 block. The output-conditioning circuitry takes the internal parallel data bus and converts it to a serial data format at DOUT, with the appropriate wake-up timing. The arithmetic logic unit (ALU) performs the averaging function.

SPI-Compatible Serial Interface

The MAX1220/MAX1257/MAX1258 feature a serial interface that is compatible with SPI and MICROWIRE devices. For SPI, ensure the SPI bus master (typically a microcontroller (µC)) runs in master mode so that it generates the serial clock signal. Select the SCLK frequency of 25MHz or less, and set the clock polarity (CPOL) and phase (CPHA) in the µC control registers to the same value. The MAX1220/MAX1257/MAX1258 operate with SCLK idling high or low, and thus operate with CPOL = CPHA = 0 or CPOL = CPHA = 1. Set $\overline{CS}$ low to latch any input data at DIN on the falling edge of SCLK. Output data at DOUT is updated on the falling edge of SCLK in clock modes 00, 01, and 10. Output data at DOUT is updated on the rising edge of SCLK in clock mode 11. See Figures 6–11. Bipolar true-differential results and temperature-sensor results are available in two's complement format, while all other results are in binary.

A high-to-low transition on $\overline{CS}$ initiates the data-input operation. Serial communications to the ADC always begin with an 8-bit command byte (MSB first) loaded from DIN. The command byte and the subsequent data bytes are clocked from DIN into the serial interface on the falling edge of SCLK. The serial-interface and fast-interface circuitry is common to the ADC, DAC, and GPIO sections. The content of the command byte determines whether the SPI port should expect 8, 16, or 24 bits and whether the data is intended for the ADC, DAC, or GPIOs (if applicable). See Table 1. Driving $\overline{CS}$ high resets the serial interface.

The conversion register controls ADC channel selection, ADC scan mode, and temperature-measurement requests. See Table 4 for information on writing to the conversion register. The setup register controls the clock mode, reference, and unipolar/bipolar ADC configuration. Use a second byte, following the first, to write to the unipolar-mode or bipolar-mode registers. See Table 5 for details of the setup register and see Tables 6, 7, and 8 for setting the unipolar- and bipolar-mode registers. Hold $\overline{CS}$ low between the command byte and the second and third byte. The ADC averaging register is specific to the ADC. See Table 9 to address that register. Table 11 shows the details of the reset register.

Begin a write to the DAC by writing 0001XXXX as a command byte. The last 4 bits of this command byte are don't-care bits. Write another 2 bytes (holding $\overline{CS}$ low) to the DAC interface register following the command byte to select the appropriate DAC and the data to be written to it. See the *DAC Serial Interface* section and Tables 10, 20, and 21.

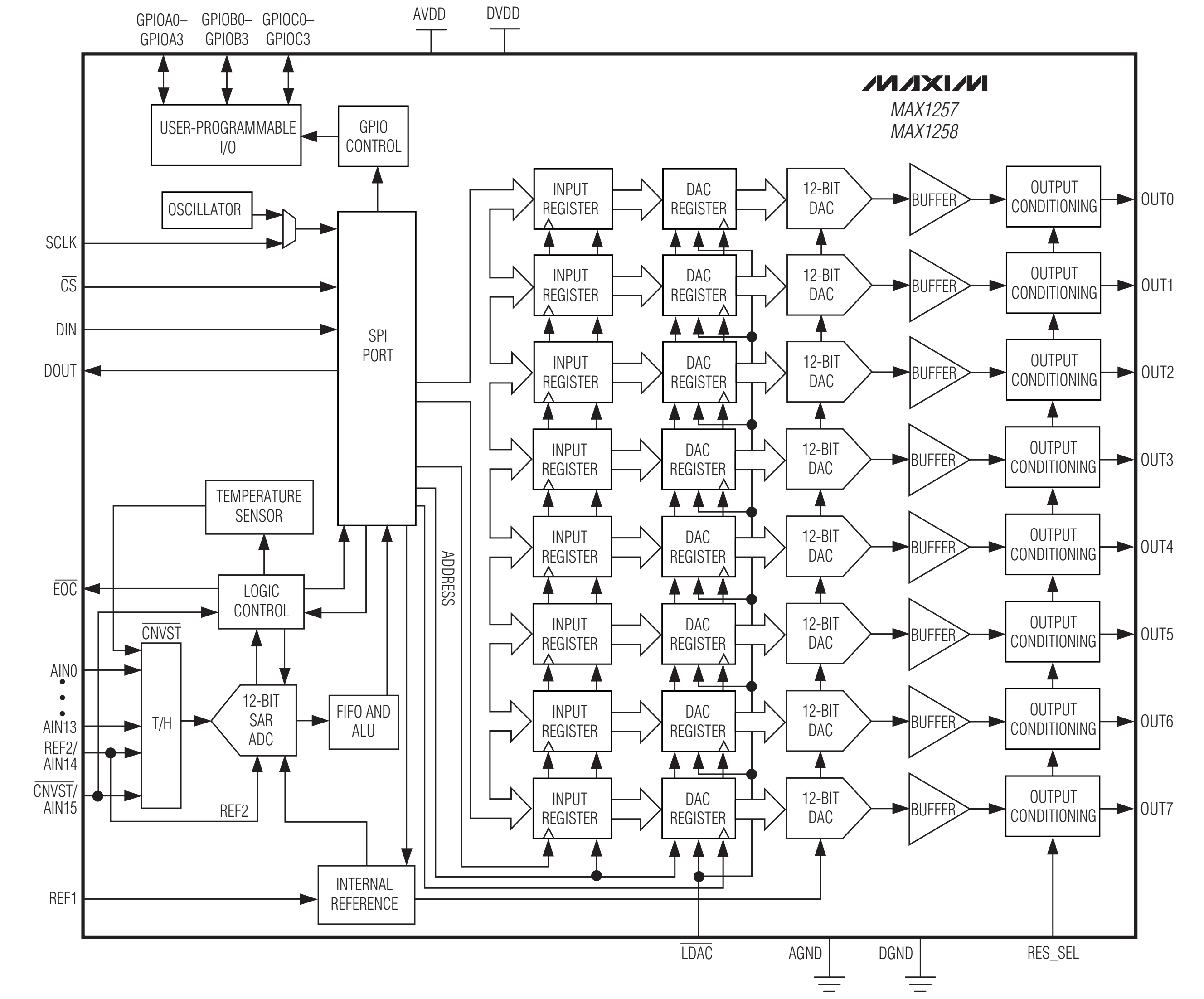


Figure 1. MAX1257/MAX1258 Functional Diagram

Table 1. Command Byte (MSB First)

REGISTER NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	ADDITIONAL NO. OF BYTES
Conversion	1	CHSEL3	CHSEL2	CHSEL1	CHSEL0	SCAN1	SCAN0	TEMP	0
Setup	0	1	CKSEL1	CKSEL0	REFSEL1	REFSEL0	DIFFSEL1	DIFFSEL0	1
ADC	0	0	1	AVGON	NAVG1	NAVG0	NSCAN1	NSCAN0	0
DAC Select	0	0	0	1	X	X	X	X	2
Reset	0	0	0	0	1	RESET	SLOW	FBGON	0
GPIO Configure	0	0	0	0	0	0	1	1	1 or 2
GPIO Write	0	0	0	0	0	0	1	0	1 or 2
GPIO Read	0	0	0	0	0	0	0	1	1 or 2
No Operation	0	0	0	0	0	0	0	0	0

X = Don't care.

Write to the GPIOs by issuing a command byte to the appropriate register. Writing to the MAX1220 GPIOs requires 1 additional byte following the command byte. Writing to the MAX1257/MAX1258 requires 2 additional bytes following the command byte. See Tables 12–19 for details on GPIO configuration, writes, and reads. See the *GPIO Command* section. Command bytes written to the GPIOs on devices without GPIOs are ignored.

Power-Up Default State

The MAX1220/MAX1257/MAX1258 power up with all blocks in shutdown (including the reference). All registers power up in state 00000000, except for the setup register and the DAC input register. The setup register powers up at 0010 1000 with CKSEL1 = 1 and REFSEL1 = 1. The DAC input register powers up to FFFh when RES_SEL is high and powers up to 000h when RES_SEL is low.

12-Bit ADC

The MAX1220/MAX1257/MAX1258 ADCs use a fully differential successive-approximation register (SAR) conversion technique and on-chip track-and-hold (T/H) circuitry to convert temperature and voltage signals into 12-bit digital results. The analog inputs accept both single-ended and differential input signals. Single-ended signals are converted using a unipolar transfer function, and differential signals are converted using a selectable bipolar or unipolar transfer function. See the *ADC Transfer Functions* section for more data.

ADC Clock Modes

When addressing the setup, register bits 5 and 4 of the command byte (CKSEL1 and CKSEL0, respectively) control the ADC clock modes. See Table 5. Choose between four different clock modes for various ways to start a conversion and determine whether the acquisitions are internally or externally timed. Select clock mode 00 to configure $\overline{\text{CNVST}}$/AIN_ to act as a conversion start and use it to request internally timed conversions, without tying up the serial bus. In clock mode 01, use $\overline{\text{CNVST}}$ to request conversions one channel at a time, thereby controlling the sampling speed without tying up the serial bus. Request and start internally timed conversions through the serial interface by writing to the conversion register in the default clock mode, 10. Use clock mode 11 with SCLK up to 3.6MHz for externally timed acquisitions to achieve sampling rates up to 225ksps. Clock mode 11 disables scanning and averaging. See Figures 6–9 for timing specifications on how to begin a conversion.

These devices feature an active-low, end-of-conversion output. $\overline{\text{EOC}}$ goes low when the ADC completes the last requested operation and is waiting for the next command byte. $\overline{\text{EOC}}$ goes high when $\overline{\text{CS}}$ or $\overline{\text{CNVST}}$ go low. $\overline{\text{EOC}}$ is always high in clock mode 11.

Single-Ended or Differential Conversions

The MAX1220/MAX1257/MAX1258 use a fully differential ADC for all conversions. When a pair of inputs are connected as a differential pair, each input is connected to the ADC. When configured in single-ended mode, the positive input is the single-ended channel and the negative input is referred to AGND. See Figure 2.

In differential mode, the T/H samples the difference between two analog inputs, eliminating common-mode DC offsets and noise. IN+ and IN- are selected from the following pairs: AIN0/AIN1, AIN2/AIN3, AIN4/AIN5, AIN6/AIN7, AIN8/AIN9, AIN10/AIN11, AIN12/AIN13, AIN14/AIN15. AIN0–AIN7 are available on all devices. AIN0–AIN15 are available on the MAX1257/MAX1258.

See Tables 5–8 for more details on configuring the inputs. For the inputs that are configurable as $\overline{CNVST}$, REF2, and an analog input, only one function can be used at a time.

Unipolar or Bipolar Conversions

Address the unipolar- and bipolar-mode registers through the setup register (bits 1 and 0). See Table 5 for the setup register. See Figures 3 and 4 for the transfer-function graphs. Program a pair of analog inputs for differential operation by writing a one to the appropriate bit of the bipolar- or unipolar-mode register. Unipolar mode sets the differential input range from 0 to V_{REF1}. A negative differential analog input in unipolar mode causes the digital output code to be zero. Selecting bipolar mode sets the differential input range to $\pm V_{REF1}$ / 2. The digital output code is binary in unipolar mode and two's complement in bipolar mode.

In single-ended mode, the MAX1220/MAX1257/MAX1258 always operate in unipolar mode. The analog inputs are internally referenced to AGND with a full-scale input range from 0 to the selected reference voltage.

Analog Input (T/H)

The equivalent circuit of Figure 2 shows the ADC input architecture of the MAX1220/MAX1257/MAX1258. In track mode, a positive input capacitor is connected to AIN0–AIN15 in single-ended mode and AIN0, AIN2, and AIN4–AIN14 (only positive inputs) in differential mode. A negative input capacitor is connected to AGND in single-ended mode or AIN1, AIN3, and AIN5–AIN15 (only negative inputs) in differential mode. For external T/H timing, use clock mode 01. After the T/H enters hold mode, the difference between the sampled positive and negative input voltages is converted. The input capacitance charging rate determines the time required for the T/H to acquire an input signal. If the input signal's source impedance is high, the required acquisition time lengthens.

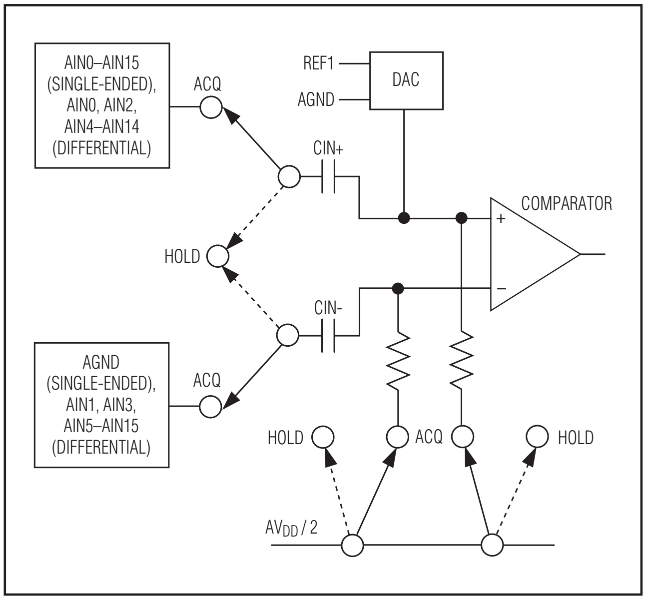


Figure 2. Equivalent Input Circuit

Any source impedance below 300Ω does not significantly affect the ADC's AC performance. A high-impedance source can be accommodated either by lengthening t_{ACQ} (only in clock mode 01) or by placing a 1µF capacitor between the positive and negative analog inputs. The combination of the analog-input source impedance and the capacitance at the analog input creates an RC filter that limits the analog input bandwidth.

Input Bandwidth

The ADC's input-tracking circuitry has a 1MHz small-signal bandwidth, making it possible to digitize high-speed transient events and measure periodic signals with bandwidths exceeding the ADC's sampling rate by using undersampling techniques. Anti-alias prefiltering of the input signals is necessary to avoid high-frequency signals aliasing into the frequency band of interest.

Analog Input Protection

Internal electrostatic-discharge (ESD) protection diodes clamp all analog inputs to AVDD and AGND, allowing the inputs to swing from (AGND - 0.3V) to (AVDD + 0.3V) without damage. However, for accurate conversions near full scale, the inputs must not exceed AVDD by more than 50mV or be lower than AGND by 50mV. If an analog input voltage exceeds the supplies, limit the input current to 2mA.

Internal FIFO

The MAX1220/MAX1257/MAX1258 contain a first-in/first-out (FIFO) buffer that holds up to 16 ADC results plus one temperature result. The internal FIFO allows the ADC to process and store multiple internally clocked conversions and a temperature measurement without being serviced by the serial bus.

If the FIFO is filled and further conversions are requested without reading from the FIFO, the oldest ADC results are overwritten by the new ADC results. Each result contains 2 bytes, with the MSB preceded by four leading zeros. After each falling edge of $\overline{CS}$, the oldest available pair of bytes of data is available at DOUT, MSB first. When the FIFO is empty, DOUT is zero.

12-Bit, Multichannel ADCs/DACs with FIFO, Temperature Sensing, and GPIO Ports

The first 2 bytes of data read out after a temperature measurement always contain the 12-bit temperature result, preceded by four leading zeros, MSB first. If another temperature measurement is performed before the first temperature result is read out, the old measurement is overwritten by the new result. Temperature results are in degrees Celsius (two's complement), at a resolution of 8 LSB per degree. See the *Temperature Measurements* section for details on converting the digital code to a temperature.

12-Bit DAC

In addition to the 12-bit ADC, the MAX1220/MAX1257/MAX1258 also include eight voltage-output, 12-bit, monotonic DACs with less than 4 LSB integral nonlinearity error and less than 1 LSB differential nonlinearity error. Each DAC has a 2µs settling time and ultra-low glitch energy (4nV•s). The 12-bit DAC code is unipolar binary with 1 LSB = V_{REF}/4096.

DAC Digital Interface

Figure 1 shows the functional diagram of the MAX1257/MAX1258. The shift register converts a serial 16-bit word to parallel data for each input register operating with a clock rate up to 25MHz. The SPI-compatible digital interface to the shift register consists of $\overline{CS}$, SCLK, DIN, and DOUT. Serial data at DIN is loaded on the falling edge of SCLK. Pull $\overline{CS}$ low to begin a write sequence. Begin a write to the DAC by writing 0001XXXX as a command byte. The last 4 bits of the DAC select register are don't-care bits. See Table 10. Write another 2 bytes to the DAC interface register following the command byte to select the appropriate DAC and the data to be written to it. See Tables 20 and 21.

The eight double-buffered DACs include an input and a DAC register. The input registers are directly connected to the shift register and hold the result of the most recent write operation. The eight 12-bit DAC registers hold the current output code for the respective DAC. Data can be transferred from the input registers to the DAC registers by pulling $\overline{LDAC}$ low or by writing the appropriate DAC command sequence at DIN. See Table 20. The outputs of the DACs are buffered through eight rail-to-rail op amps.

The MAX1220/MAX1257/MAX1258 DAC output voltage range is based on the internal reference or an external reference. Write to the setup register (see Table 5) to program the reference. If using an external voltage reference, bypass REF1 with a 0.1µF capacitor to AGND. The MAX1257 internal reference is 2.5V. The MAX1220/MAX1258 internal reference is 4.096V. When using an external reference on any of these devices, the voltage range is 0.7V to V_{AVDD}.

DAC Transfer Function

See Table 2 for various analog outputs from the DAC.

DAC Power-On Wake-Up Modes

The state of the RES_SEL input determines the wake-up state of the DAC outputs. Connect RES_SEL to AVDD or AGND upon power-up to be sure the DAC outputs wake up to a known state. Connect RES_SEL to AGND to wake up all DAC outputs at 000h. While RES_SEL is low, the 100kΩ internal resistor pulls the DAC outputs to AGND and the output buffers are powered down. Connect RES_SEL to AVDD to wake up all DAC outputs at FFFh. While RES_SEL is high, the 100kΩ pullup resistor pulls the DAC outputs to V_{REF1} and the output buffers are powered down.

DAC Power-Up Modes

See Table 21 for a description of the DAC power-up and power-down modes.

GPIOs

In addition to the internal ADC and DAC, the MAX1257/MAX1258 also provide 12 general-purpose input/output channels, GPIOA0–GPIOA3, GPIOB0–

Table 2. DAC Output Code Table

DAC CONTENTS			ANALOG OUTPUT
MSB		LSB	
1111	1111	1111	$+V_{REF}\left(\frac{4095}{4096}\right)$
1000	0000	0001	$+V_{REF}\left(\frac{2049}{4096}\right)$
1000	0000	0000	$+V_{REF}\left(\frac{2048}{4096}\right)=\left(\frac{+V_{REF}}{2}\right)$
0111	0111	0111	$+V_{REF}\left(\frac{2047}{4096}\right)$
0000	0000	0001	$+V_{REF}\left(\frac{1}{4096}\right)$
0000	0000	0000	0

GPIOB3, and GPIOC0–GPIOC3. The MAX1220 includes four GPIO channels (GPIOA0, GPIOA1, GPIOC0, GPIOC1). Read and write to the GPIOs as detailed in Table 1 and Tables 12–19. Also, see the *GPIO Command* section. See Figures 11 and 12 for GPIO timing.

Write to the GPIOs by writing a command byte to the GPIO command register. Write a single data byte to the MAX1220 following the command byte. Write 2 bytes to the MAX1257/MAX1258 following the command byte.

The GPIOs can sink and source current. The MAX1257/MAX1258 GPIOA0–GPIOA3 can sink and source up to 15mA. GPIOB0–GPIOB3 and GPIOC0–GPIOC3 can sink 4mA and source 2mA. The MAX1220 GPIOA0 and GPIOA1 can sink and source up to 15mA. The MAX1220 GPIOC0 and GPIOC1 can sink 4mA and source 2mA. See Table 3.

Clock Modes

Internal Clock

The MAX1220/MAX1257/MAX1258 can operate from an internal oscillator. The internal oscillator is active in clock modes 00, 01, and 10. Figures 6, 7, and 8 show how to start an ADC conversion in the three internally timed conversion modes.

Read out the data at clock speeds up to 25MHz through the SPI interface.

External Clock

Set CKSEL1 and CKSEL0 in the setup register to 11 to set up the interface for external clock mode 11. See Table 5. Pulse SCLK at speeds from 0.1MHz to 3.6MHz. Write to SCLK with a 40% to 60% duty cycle. The SCLK frequency controls the conversion timing. See Figures 9a and 9b for clock mode 11 timing. See the *ADC Conversions in Clock Mode 11* section.

ADC/DAC References

Address the reference through the setup register, bits 3 and 2. See Table 5. Following a wake-up delay, set REFSEL[1:0] = 00 to program both the ADC and DAC for internal reference use. Set REFSEL[1:0] = 10 to program the ADC for internal reference. Set REFSEL[1:0] = 10 to program the DAC for external reference, REF1. When using REF1 or REF2/AIN_ in external-reference mode, connect a 0.1µF capacitor to AGND. Set REFSEL[1:0] = 01 to program the ADC and DAC for external-reference mode. The DAC uses REF1 as its external reference, while the ADC uses REF2 as its external reference. Set REFSEL[1:0] = 11 to program the ADC for external differential reference mode. REF1 is the positive reference and REF2 is the negative reference in the ADC external differential mode.

When REFSEL[1:0] = 00 or 10, REF2/AIN_ functions as an analog input channel. When REFSEL[1:0] = 01 or 11, REF2/AIN_ functions as the device's negative reference.

Temperature Measurements

Issue a command byte setting bit 0 of the conversion register to one to take a temperature measurement. See Table 4. The MAX1220/MAX1257/MAX1258 perform temperature measurements with an internal diode-connected transistor. The diode bias current changes from 68µA to 4µA to produce a temperature-dependent bias voltage difference. The second conversion result at 4µA is subtracted from the first at 68µA to calculate a digital value that is proportional to absolute temperature. The output data appearing at DOUT is the digital code above, minus an offset to adjust from Kelvin to Celsius.

The reference voltage used for the temperature measurements is always derived from the internal reference source to ensure that 1 LSB corresponds to 1/8 of a degree Celsius. On every scan where a temperature measurement is requested, the temperature conversion is carried out first. The first 2 bytes of data read from the FIFO contain the result of the temperature measurement. If another temperature measurement is performed before the first temperature result is read out, the old measurement is overwritten by the new result. Temperature results are in degrees Celsius (two's complement). See the *Applications Information* section for information on how to perform temperature measurements in each clock mode.

Register Descriptions

The MAX1220/MAX1257/MAX1258 communicate between the internal registers and the external circuitry through the SPI-compatible serial interface. Table 1 details the command byte, the registers, and the bit

Table 3. GPIO Maximum Sink/Source Current

CURRENT	MAX1257/MAX1258 (mA)			MAX1220 (mA)	
	GPIOA0–GPIOA3	GPIOB0–GPIOB3	GPIOC0–GPIOC3	GPIOA0, GPIOA1	GPIOC0, GPIOC1
Sink	15	4	4	15	4
Source	15	2	2	15	2

names. Tables 4–12 show the various functions within the conversion register, setup register, unipolar-mode register, bipolar-mode register, ADC averaging register, DAC select register, reset register, and GPIO command register, respectively.

Conversion Register

Select active analog input channels, scan modes, and a single temperature measurement per scan by issuing a command byte to the conversion register. Table 4 details channel selection, the four scan modes, and how to request a temperature measurement. Start a scan by writing to the conversion register when in clock mode 10 or 11, or by applying a low pulse to the $\overline{CNVST}$ pin when in clock mode 00 or 01. See Figures 6 and 7 for timing specifications for starting a scan with $\overline{CNVST}$.

A conversion is not performed if it is requested on a channel or one of the channel pairs that has been configured as $\overline{CNVST}$ or REF2. For channels configured as differential pairs, the CHSEL0 bit is ignored and the two pins are treated as a single differential channel.

Select scan mode 00 or 01 to return one result per single-ended channel and one result per differential pair within the selected scanning range (set by bits 2 and 1, SCAN1 and SCAN0), plus one temperature result, if selected. Select scan mode 10 to scan a single input channel numerous times, depending on NSCAN1 and NSCAN0 in the ADC averaging register (Table 9). Select scan mode 11 to return only one result from a single channel.

Setup Register

Issue a command byte to the setup register to configure the clock, reference, power-down modes, and ADC single-ended/differential modes. Table 5 details the bits in the setup-register command byte. Bits 5 and 4 (CKSEL1 and CKSEL0) control the clock mode, acquisition and sampling, and the conversion start. Bits 3 and 2 (REFSEL1 and REFSEL0) set the device for either internal or external reference. Bits 1 and 0 (DIFFSEL1 and DIFFSEL0) address the ADC unipolar-mode and bipolar-mode registers and configure the analog input channels for differential operation.

Table 4. Conversion Register*

BIT NAME	BIT	FUNCTION
—	7 (MSB)	Set to one to select conversion register.
CHSEL3	6	Analog-input channel select.
CHSEL2	5	Analog-input channel select.
CHSEL1	4	Analog-input channel select.
CHSEL0	3	Analog-input channel select.
SCAN1	2	Scan-mode select.
SCAN0	1	Scan-mode select.
TEMP	0 (LSB)	Set to one to take a single temperature measurement. The first conversion result of a scan contains temperature information.

**See below for bit details.*

CHSEL3	CHSEL2	CHSEL1	CHSEL0	SELECTED CHANNEL (N)
0	0	0	0	AIN0
0	0	0	1	AIN1
0	0	1	0	AIN2
0	0	1	1	AIN3
0	1	0	0	AIN4
0	1	0	1	AIN5
0	1	1	0	AIN6
0	1	1	1	AIN7
1	0	0	0	AIN8
1	0	0	1	AIN9
1	0	1	0	AIN10
1	0	1	1	AIN11
1	1	0	0	AIN12
1	1	0	1	AIN13
1	1	1	0	AIN14
1	1	1	1	AIN15

SCAN1	SCAN0	SCAN MODE (CHANNEL N IS SELECTED BY BITS CHSEL3–CHSEL0)
0	0	Scans channels 0 through N.
0	1	Scans channels N through the highest numbered channel.
1	0	Scans channel N repeatedly. The ADC averaging register sets the number of results.
1	1	No scan. Converts channel N once only.

Table 5. Setup Register*

BIT NAME	BIT	FUNCTION
—	7 (MSB)	Set to zero to select setup register.
—	6	Set to one to select setup register.
CKSEL1	5	Clock mode and $\overline{\text{CNVST}}$ configuration; resets to one at power-up.
CKSEL0	4	Clock mode and $\overline{\text{CNVST}}$ configuration.
REFSEL1	3	Reference-mode configuration.
REFSEL0	2	Reference-mode configuration.
DIFFSEL1	1	Unipolar-/bipolar-mode register configuration for differential mode.
DIFFSEL0	0 (LSB)	Unipolar-/bipolar-mode register configuration for differential mode.

See below for bit details.

Table 5a. Clock Modes*

CKSEL1	CKSEL0	CONVERSION CLOCK	ACQUISITION/SAMPLING	$\overline{\text{CNVST}}$ CONFIGURATION
0	0	Internal	Internally timed.	$\overline{\text{CNVST}}$
0	1	Internal	Externally timed by $\overline{\text{CNVST}}$.	$\overline{\text{CNVST}}$
1	0	Internal	Internally timed.	AIN15/AIN7
1	1	External (3.6MHz max)	Externally timed by SCLK.	AIN15/AIN7

See the Clock Modes section.

Table 5b. Clock Modes 00, 01, and 10

REFSEL1	REFSEL0	VOLTAGE REFERENCE	OVERRIDE CONDITIONS	AUTOSHUTDOWN	REF2 CONFIGURATION
0	0	Internal (DAC and ADC)	AIN	Internal reference turns off after scan is complete. If internal reference is turned off, there is a programmed delay of 218 internal-conversion clock cycles.	AIN14/AIN6
			Temperature	Internal reference required. There is a programmed delay of 244 internal-conversion clock cycles for the internal reference to settle after wake-up.	
0	1	External single-ended (REF1 for DAC and REF2 for ADC)	AIN	Internal reference not used.	REF2
			Temperature	Internal reference required. There is a programmed delay of 244 internal-conversion clock cycles for the internal reference to settle after wake-up.	
1	0	Internal (ADC) and external REF1 (DAC)	AIN	Default reference mode. Internal reference turns off after scan is complete. If internal reference is turned off, there is a programmed delay of 218 internal-conversion clock cycles.	AIN14/AIN6
			Temperature	Internal reference required. There is a programmed delay of 244 internal-conversion clock cycles for the internal reference to settle after wake-up.	
1	1	External differential (ADC), external REF1 (DAC)	AIN	Internal reference not used.	REF2
			Temperature	Internal reference required. There is a programmed delay of 244 internal-conversion clock cycles for the internal reference to settle after wake-up.	