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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
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19-3052; Rev 5; 3/11

EVALUATION KIT AVAILABLE

8-/4-/2-Channel, 12-Bit, Simultaneous-Sampling ADCs with ±10V, ±5V, and 0 to +5V Analog Input Ranges

General Description

The MAX1304–MAX1306/MAX1308–MAX1310/MAX1312–MAX1314 12-bit, analog-to-digital converters (ADCs) offer eight, four, or two independent input channels. Independent track-and-hold (T/H) circuitry provides simultaneous sampling for each channel. The MAX1304/MAX1305/MAX1306 provide a 0 to +5V input range with ±6V fault-tolerant inputs. The MAX1308/MAX1309/MAX1310 provide a ±5V input range with ±16.5V fault-tolerant inputs. The MAX1312/MAX1313/MAX1314 have a ±10V input range with ±16.5V fault-tolerant inputs. These ADCs convert two channels in 0.9µs, and up to eight channels in 1.98µs, with an 8-channel throughput of 456ksps per channel. Other features include a 20MHz T/H input bandwidth, internal clock, internal (+2.5V) or external (+2.0V to +3.0V) reference, and power-saving modes.

A 20MHz, 12-bit, bidirectional parallel data bus provides the conversion results and accepts digital inputs that activate each channel individually.

All devices operate from a +4.75V to +5.25V analog supply and a +2.7V to +5.25V digital supply and consume 57mA total supply current when fully operational.

Each device is available in a 48-pin 7mm x 7mm LQFP package and operates over the extended -40°C to +85°C temperature range.

Applications

SIN/COS Position Encoder

Multiphase Motor Control

Multiphase Power Monitoring

Power-Grid Synchronization

Power-Factor Monitoring

Vibration and Waveform Analysis

Selector Guide

PART	INPUT RANGE (V)	CHANNEL COUNT
MAX1304ECM	0 to +5	8
MAX1305ECM	0 to +5	4
MAX1306ECM	0 to +5	2
MAX1308ECM	±5	8
MAX1309ECM	±5	4
MAX1310ECM	±5	2
MAX1312ECM	±10	8
MAX1313ECM	±10	4
MAX1314ECM	±10	2

Pin Configurations appear at end of data sheet.

Features

- **Up to Eight Channels of Simultaneous Sampling**
  - **8ns Aperture Delay**
  - **100ps Channel-to-Channel T/H Match**
- **Extended Input Ranges**
  - **0 to +5V (MAX1304/MAX1305/MAX1306)**
  - **-5V to +5V (MAX1308/MAX1309/MAX1310)**
  - **-10V to +10V (MAX1312/MAX1313/MAX1314)**
- **Fast Conversion Time**
  - **One Channel in 0.72µs**
  - **Two Channels in 0.9µs**
  - **Four Channels in 1.26µs**
  - **Eight Channels in 1.98µs**
- **High Throughput**
  - **1075ksps/Channel for One Channel**
  - **901ksps/Channel for Two Channels**
  - **680ksps/Channel for Four Channels**
  - **456ksps/Channel for Eight Channels**
- **±1 LSB INL, ±0.9 LSB DNL (max)**
- **84dBc SFDR, -86dBc THD, 71dB SINAD, f_{IN} = 500kHz at 0.4dBFS**
- **12-Bit, 20MHz, Parallel Interface**
- **Internal or External Clock**
- **+2.5V Internal Reference or +2.0V to +3.0V External Reference**
- **+5V Analog Supply, +3V to +5V Digital Supply**
  - **55mA Analog Supply Current**
  - **1.3mA Digital Supply Current**
  - **Shutdown and Power-Saving Modes**
- **48-Pin LQFP Package (7mm x 7mm Footprint)**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX1304ECM+	-40°C to +85°C	48 LQFP
MAX1304ECM/V+	-40°C to +85°C	48 LQFP
MAX1305ECM+	-40°C to +85°C	48 LQFP
MAX1306ECM+	-40°C to +85°C	48 LQFP
MAX1308ECM+	-40°C to +85°C	48 LQFP
MAX1308ECM/V+	-40°C to +85°C	48 LQFP
MAX1309ECM+	-40°C to +85°C	48 LQFP
MAX1309ECM/V+	-40°C to +85°C	48 LQFP
MAX1310ECM+	-40°C to +85°C	48 LQFP
MAX1312ECM+	-40°C to +85°C	48 LQFP
MAX1313ECM+	-40°C to +85°C	48 LQFP
MAX1314ECM+	-40°C to +85°C	48 LQFP

+Denotes a lead(Pb)-free/RoHS-compliant package.
/V denotes an automotive qualified part.

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

8-/4-/2-Channel, 12-Bit, Simultaneous-Sampling ADCs with ±10V, ±5V, and 0 to +5V Analog Input Ranges

ABSOLUTE MAXIMUM RATINGS

AVDD to AGND .....-0.3V to +6V
DVDD to DGND .....-0.3V to +6V
AGND to DGND .....-0.3V to +0.3V
CH0–CH7, I.C. to AGND (MAX1304/MAX1305/MAX1306) ....±6V
CH0–CH7, I.C. to AGND (MAX1308/MAX1309/MAX1310) ..±16.5V
CH0–CH7, I.C. to AGND (MAX1312/MAX1313/MAX1314) ..±16.5V
$\overline{D0}$–$\overline{D11}$ to DGND .....-0.3V to (V_{DVDD} + 0.3V)
$\overline{EOC}$, $\overline{EOLC}$, $\overline{RD}$, $\overline{WR}$, $\overline{CS}$ to DGND .....-0.3V to (V_{DVDD} + 0.3V)
CONVST, CLK, $\overline{SHDN}$, $\overline{CHSHDN}$ to DGND -0.3V to (V_{DVDD} + 0.3V)
INTCLK/$\overline{EXTCLK}$ to AGND .....-0.3V to (V_{AVDD} + 0.3V)
REF_{MS}, REF, MSV to AGND .....-0.3V to (V_{AVDD} + 0.3V)
REF+, COM, REF- to AGND .....-0.3V to (V_{AVDD} + 0.3V)
Maximum Current into Any Pin Except AVDD, DVDD, AGND, DGND .....±50mA
Continuous Power Dissipation (T_A = +70°C)
LQFP (derate 22.7mW/°C above +70°C).....1818.2mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{AVDD} = +5V, V_{DVDD} = +3V, V_{AGND} = V_{DGND} = 0V, V_{REF} = V_{REFMS} = +2.5V (external reference), C_{REF} = C_{REFMS} = 0.1µF, C_{REF+} = C_{REF-} = 0.1µF, $C_{REF+-to-REF-}$ = 2.2µF ll 0.1µF, C_{COM} = 2.2µF ll 0.1µF, C_{MSV} = 2.2µF ll 0.1µF (unipolar devices), MSV = AGND (bipolar devices), f_{CLK} = 16.67MHz 50% duty cycle, INTCLK/$\overline{EXTCLK}$ = AGND (external clock), $\overline{SHDN}$ = DGND, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C. See Figures 3 and 4.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC PERFORMANCE (Note 1)						
Resolution	N		12			Bits
Integral Nonlinearity	INL	(Note 2)		±0.5	±1.0	LSB
Differential Nonlinearity	DNL	No missing codes (Note 2)		±0.3	±0.9	LSB
Offset Error		Unipolar, 0x000 to 0x001		±3	±16	LSB
		Bipolar, 0xFFF to 0x000		±3	±16	
Offset-Error Matching		Unipolar, between all channels		±9	±20	LSB
		Bipolar, between all channels		±9	±20	
Offset-Error Temperature Drift		Unipolar, 0x000 to 0x001		7		ppm/°C
		Bipolar, 0xFFF to 0x000		7		
Gain Error				±2	±16	LSB
Gain-Error Matching		Between all channels		±3	±14	LSB
Gain-Error Temperature Drift				4		ppm/°C
DYNAMIC PERFORMANCE at f_{IN} = 500kHz, A_{IN} = -0.4dBFS (Note 2)						
Signal-to-Noise Ratio	SNR		68	71		dB
Signal-to-Noise Plus Distortion	SINAD		68	71		dB
Total Harmonic Distortion	THD			-86	-80	dBc
Spurious-Free Dynamic Range	SFDR			84		dBc
Channel-to-Channel Isolation			80	86		dB
ANALOG INPUTS (CH0 through CH7)						
Input Voltage	V_{CH}	MAX1304/MAX1305/MAX1306	0		+5	V
		MAX1308/MAX1309/MAX1310	-5		+5	
		MAX1312/MAX1313/MAX1314	-10		+10	

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = +5V, V_{DVDD} = +3V, V_{AGND} = V_{DGND} = 0V, V_{REF} = V_{REFMS} = +2.5V (external reference), C_{REF} = C_{REFMS} = 0.1µF, C_{REF+} = C_{REF-} = 0.1µF, $C_{REF+\text{-to-}REF-}$ = 2.2µF ll 0.1µF, C_{COM} = 2.2µF ll 0.1µF, C_{MSV} = 2.2µF ll 0.1µF (unipolar devices), MSV = AGND (bipolar devices), f_{CLK} = 16.67MHz 50% duty cycle, INTCLK/$\overline{EXTCLK}$ = AGND (external clock), SHDN = DGND, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C. See Figures 3 and 4.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Resistance (Note 3)	R_{CH}	MAX1304/MAX1305/MAX1306			7.58		kΩ
		MAX1308/MAX1309MAX1310			8.66		
		MAX1312/MAX1313/MAX1314			14.26		
Input Current (Note 3)	I_{CH}	MAX1304/MAX1305/MAX1306	V_{CH} = +5V		0.54	0.72	mA
			V_{CH} = 0V	-0.157	-0.12		
		MAX1308/MAX1309/MAX1310	V_{CH} = +5V		0.29	0.39	
			V_{CH} = -5V	-1.16	-0.87		
		MAX1312/MAX1313/MAX1314	V_{CH} = +10V		0.56	0.74	
			V_{CH} = -10V	-1.13	-0.85		
Input Capacitance	C_{CH}				15		pF
TRACK/HOLD							
External-Clock Throughput Rate (Note 4)	f_{TH}	One channel selected for conversion			1075		ksps
		Two channels selected for conversion			901		
		Four channels selected for conversion			680		
		Eight channels selected for conversion			456		
Internal-Clock Throughput Rate (Note 4, Table 1)	f_{TH}	One channel selected for conversion			983		ksps
		Two channels selected for conversion			821		
		Four channels selected for conversion			618		
		Eight channels selected for conversion			413		
Small-Signal Bandwidth					20		MHz
Full-Power Bandwidth					20		MHz
Aperture Delay	t_{AD}				8		ns
Aperture-Delay Matching					100		ps
Aperture Jitter	t_{AJ}				50		ps_{RMS}
INTERNAL REFERENCE							
REF Output Voltage	V_{REF}			2.475	2.500	2.525	V
Reference Output-Voltage Temperature Drift					30		ppm/°C
REF_{MS} Output Voltage	V_{REFMS}			2.475	2.500	2.525	V
REF+ Output Voltage	V_{REF+}				3.850		V
COM Output Voltage	V_{COM}				2.600		V
REF- Output Voltage	V_{REF-}				1.350		V
Differential Reference Voltage	V_{REF+} - V_{REF-}				2.500		V

8-/4-/2-Channel, 12-Bit, Simultaneous-Sampling ADCs with ±10V, ±5V, and 0 to +5V Analog Input Ranges

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = +5V, V_{DVDD} = +3V, V_{AGND} = V_{DGND} = 0V, V_{REF} = V_{REFMS} = +2.5V (external reference), C_{REF} = C_{REFMS} = 0.1µF, C_{REF+} = C_{REF-} = 0.1µF, $C_{REF+-to-REF-}$ = 2.2µF ll 0.1µF, C_{COM} = 2.2µF ll 0.1µF, C_{MSV} = 2.2µF ll 0.1µF (unipolar devices), MSV = AGND (bipolar devices), f_{CLK} = 16.67MHz 50% duty cycle, INTCLK/$\overline{EXTCLK}$ = AGND (external clock), SHDN = DGND, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C. See Figures 3 and 4.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
EXTERNAL REFERENCE (REF and REF_{MS} are externally driven)						
REF Input Voltage Range	V_{REF}		2.0	2.5	3.0	V
REF Input Resistance	R_{REF}	(Note 5)		5		kΩ
REF Input Capacitance				15		pF
REF_{MS} Input Voltage Range	V_{REFMS}		2.0	2.5	3.0	V
REF_{MS} Input Resistance	R_{REFMS}	(Note 6)		5		kΩ
REF_{MS} Input Capacitance				15		pF
REF+ Output Voltage	V_{REF+}	V_{REF} = +2.5V		3.850		V
COM Output Voltage	V_{COM}	V_{REF} = +2.5V		2.600		V
REF- Output Voltage	V_{REF-}	V_{REF} = +2.5V		1.350		V
Differential Reference Voltage	V_{REF+} - V_{REF-}	V_{REF} = +2.5V		2.500		V
DIGITAL INPUTS (D0–D7, $\overline{RD}$, $\overline{WR}$, $\overline{CS}$, CLK, SHDN, $\overline{CHSHDN}$, CONVST)						
Input-Voltage High	V_{IH}		0.7 x V_{DVDD}			V
Input-Voltage Low	V_{IL}				0.3 x V_{DVDD}	V
Input Hysteresis				20		mV
Input Capacitance	C_{IN}			15		pF
Input Current	I_{IN}	V_{IN} = 0V or V_{DVDD}		0.02	±1	µA
CLOCK-SELECT INPUT (INTCLK/$\overline{EXTCLK}$)						
Input-Voltage High	V_{IH}		0.7 x V_{AVDD}			V
Input-Voltage Low	V_{IL}				0.3 x V_{AVDD}	V
DIGITAL OUTPUTS (D0–D11, $\overline{EOC}$, $\overline{EOLC}$)						
Output-Voltage High	V_{OH}	I_{SOURCE} = 0.8mA, Figure 1	V_{DVDD} - 0.6			V
Output-Voltage Low	V_{OL}	I_{SINK} = 1.6mA, Figure 1			0.4	V
D0–D11 Tri-State Leakage Current		$\overline{RD}$ = high or $\overline{CS}$ = high		0.06	1	µA
D0–D11 Tri-State Output Capacitance		$\overline{RD}$ = high or $\overline{CS}$ = high		15		pF
POWER SUPPLIES						
Analog Supply Voltage	AVDD		4.75		5.25	V
Digital Supply Voltage	DVDD		2.70		5.25	V
Analog Supply Current	I_{AVDD}	MAX1304/MAX1305/MAX1306, all channels selected		55	60	mA
		MAX1308/MAX1309/MAX1310, all channels selected		54	60	
		MAX1312/MAX1313/MAX1314, all channels selected		54	60	

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = +5V, V_{DVDD} = +3V, V_{AGND} = V_{DGND} = 0V, V_{REF} = V_{REFMS} = +2.5V (external reference), C_{REF} = C_{REFMS} = 0.1µF, C_{REF+} = C_{REF-} = 0.1µF, $C_{REF+\text{-to-}REF-}$ = 2.2µF ll 0.1µF, C_{COM} = 2.2µF ll 0.1µF, C_{MSV} = 2.2µF ll 0.1µF (unipolar devices), MSV = AGND (bipolar devices), f_{CLK} = 16.67MHz 50% duty cycle, INTCLK/$\overline{EXTCLK}$ = AGND (external clock), SHDN = DGND, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C. See Figures 3 and 4.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Digital Supply Current (C_{LOAD} = 100pF) (Note 7)	I_{DVDD}	MAX1304/MAX1305/MAX1306, all channels selected		1.3	2.6	mA
		MAX1308/MAX1309/MAX1310, all channels selected		1.3	2.6	
		MAX1312/MAX1313/MAX1314, all channels selected		1.3	2.6	
Shutdown Current (Note 8)	I_{AVDD}	SHDN = DVDD, V_{CH} = open		0.6	10	µA
	I_{DVDD}	SHDN = DVDD, $\overline{RD}$ = $\overline{WR}$ = high		0.02	1	
Power-Supply Rejection Ratio	PSRR	V_{AVDD} = +4.75V to +5.25V		50		dB
TIMING CHARACTERISTICS (Figure 1)						
Time to First Conversion Result	t_{CONV}	Internal clock, Figure 7		800	900	ns
		External clock, Figure 8		12		CLK Cycles
Time to Subsequent Conversions	t_{NEXT}	Internal clock, Figure 7		200	225	ns
		External clock, Figure 8		3		CLK Cycles
CONVST Pulse-Width Low (Acquisition Time)	t_{ACQ}	(Note 9) Figures 6–10	0.1		1000.0	µs
$\overline{CS}$ Pulse Width	t_{CS}	Figure 6	30			ns
$\overline{RD}$ Pulse-Width Low	t_{RDL}	Figures 7, 8, 9	30			ns
$\overline{RD}$ Pulse-Width High	t_{RDH}	Figures 7, 8, 9	30			ns
$\overline{WR}$ Pulse-Width Low	t_{WRL}	Figure 6	30			ns
$\overline{CS}$ to $\overline{WR}$	t_{CTW}	Figure 6		(Note 10)		ns
$\overline{WR}$ to $\overline{CS}$	t_{WTC}	Figure 6		(Note 10)		ns
$\overline{CS}$ to $\overline{RD}$	t_{CTR}	Figures 7, 8, 9		(Note 10)		ns
$\overline{RD}$ to $\overline{CS}$	t_{RTC}	Figures 7, 8, 9		(Note 10)		ns
Data Access Time ($\overline{RD}$ Low to Valid Data)	t_{ACC}	Figures 7, 8, 9			30	ns
Bus Relinquish Time ($\overline{RD}$ High)	t_{REQ}	Figures 7, 8, 9	5		30	ns
CLK Rise to $\overline{EOC}$ Delay	t_{EOCD}	Figure 8		20		ns
CLK Rise to $\overline{EOLC}$ Fall Delay	t_{EOLCD}	Figure 8		20		ns
CONVST Fall to $\overline{EOLC}$ Rise Delay	$t_{CVEOLCD}$	Figures 7, 8, 9		20		ns
$\overline{EOC}$ Pulse Width	t_{EOC}	Internal clock, Figure 7	50			ns
		External clock, Figure 8		1		CLK Cycle

8-/4-/2-Channel, 12-Bit, Simultaneous-Sampling ADCs with ±10V, ±5V, and 0 to +5V Analog Input Ranges

ELECTRICAL CHARACTERISTICS (continued)

(V_{AVDD} = +5V, V_{DVDD} = +3V, V_{AGND} = V_{DGND} = 0V, V_{REF} = V_{REFMS} = +2.5V (external reference), C_{REF} = C_{REFMS} = 0.1µF, C_{REF+} = C_{REF-} = 0.1µF, $C_{REF+-to-REF-}$ = 2.2µF ll 0.1µF, C_{COM} = 2.2µF ll 0.1µF, C_{MSV} = 2.2µF ll 0.1µF (unipolar devices), MSV = AGND (bipolar devices), f_{CLK} = 16.67MHz 50% duty cycle, INTCLK/$\overline{EXTCLK}$ = AGND (external clock), SHDN = DGND, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C. See Figures 3 and 4.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input-Data Setup Time	t_{DTW}	Figure 6	10			ns
Input-Data Hold Time	t_{WTD}	Figure 6	10			ns
External CLK Period	t_{CLK}	Figures 8, 9	0.05		10.00	µs
External CLK High Period	t_{CLKH}	Logic sensitive to rising edges, Figures 8, 9	20			ns
External CLK Low Period	t_{CLKL}	Logic sensitive to rising edges, Figures 8, 9	20			ns
External Clock Frequency	f_{CLK}	(Note 11)	0.1		20	MHz
Internal Clock Frequency	f_{INT}			15		MHz
CONVST High to CLK Edge	t_{CNTC}	Figures 8, 9	20			ns

Note 1: For the MAX1304/MAX1305/MAX1306, V_{IN} = 0 to +5V. For the MAX1308/MAX1309/MAX1310, V_{IN} = -5V to +5V. For the MAX1312/MAX1313/MAX1314, V_{IN} = -10V to +10V.

Note 2: All channel performance is guaranteed by correlation to a single channel test.

Note 3: The analog input resistance is terminated to an internal bias point (Figure 5). Calculate the analog input current using:

$$I_{CH_} = \frac{V_{CH_} - V_{BIAS}}{R_{CH_}}$$

for $V_{CH_}$ within the input voltage range.

Note 4: Throughput rate is given per channel. Throughput rate is a function of clock frequency (f_{CLK}). The external clock throughput rate is specified with f_{CLK} = 16.67MHz and the internal clock throughput rate is specified with f_{CLK} = 15MHz. See the *Data Throughput* section for more information.

Note 5: The REF input resistance is terminated to an internal +2.5V bias point (Figure 2). Calculate the REF input current using:

$$I_{REF} = \frac{V_{REF} - 2.5V}{R_{REF}}$$

for V_{REF} within the input voltage range.

Note 6: The REF_{MS} input resistance is terminated to an internal +2.5V bias point (Figure 2). Calculate the REF_{MS} input current using:

$$I_{REFMS} = \frac{V_{REFMS} - 2.5V}{R_{REFMS}}$$

for V_{REFMS} within the input voltage range.

Note 7: All analog inputs are driven with a -0.4dBFS 500kHz sine wave.

Note 8: Shutdown current is measured with the analog input unconnected. The large amplitude of the maximum shutdown current specification is due to automated test equipment limitations.

Note 9: CONVST must remain low for at least the acquisition period. The maximum acquisition time is limited by internal capacitor droop.

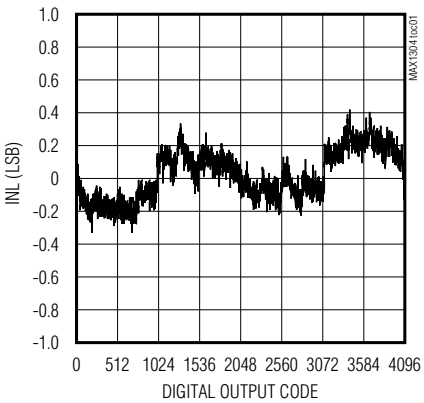
Note 10: $\overline{CS}$ to $\overline{WR}$ and $\overline{CS}$ to $\overline{RD}$ are internally AND together. Setup and hold times do not apply.

Note 11: Minimum CLK frequency is limited only by the internal T/H droop rate. Limit the time between the rising edge of CONVST and the falling edge of $\overline{EOLC}$ to a maximum of 1ms.

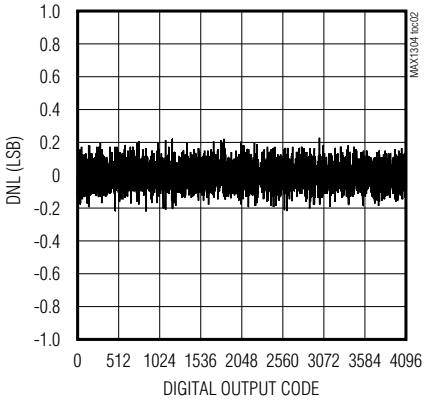
Typical Operating Characteristics

(V_{AVDD} = +5V, V_{DVDD} = +3V, V_{AGND} = V_{DGND} = 0V, V_{REF} = V_{REFMS} = +2.5V (external reference), C_{REF} = C_{REFMS} = 0.1µF, C_{REF+} = C_{REF-} = 0.1µF, $C_{REF+-to-REF-}$ = 2.2µF ll 0.1µF, C_{COM} = 2.2µF ll 0.1µF, C_{MSV} = 2.2µF ll 0.1µF (unipolar devices), MSV = AGND (bipolar devices), f_{CLK} = 16.67MHz 50% duty cycle, INTCLK/$\overline{EXTCLK}$ = AGND (external clock), f_{IN} = 500kHz, A_{IN} = -0.4dBFS. T_A = +25°C, unless otherwise noted.) (Figures 3 and 4)

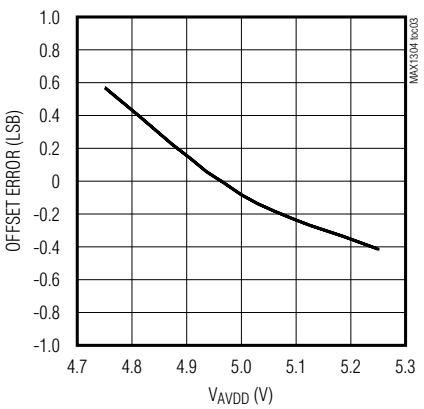
INTEGRAL NONLINEARITY vs. DIGITAL OUTPUT CODE



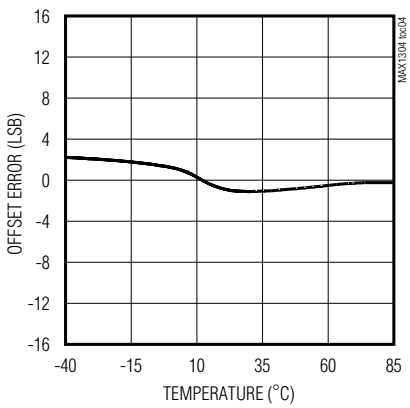
DIFFERENTIAL NONLINEARITY vs. DIGITAL OUTPUT CODE



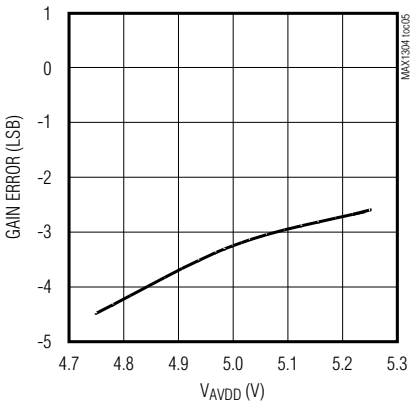
OFFSET ERROR vs. ANALOG SUPPLY VOLTAGE



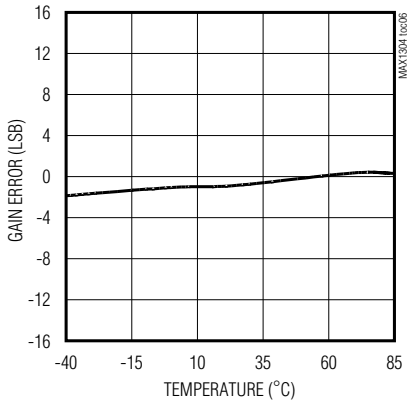
OFFSET ERROR vs. TEMPERATURE



GAIN ERROR vs. ANALOG SUPPLY VOLTAGE



GAIN ERROR vs. TEMPERATURE

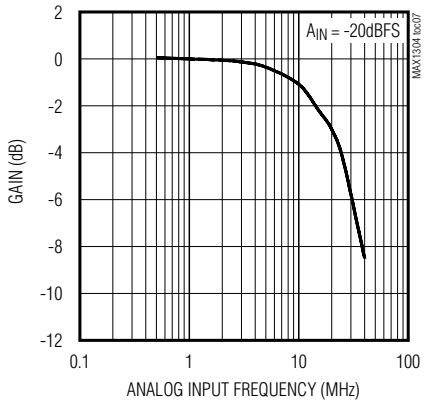


8-/4-/2-Channel, 12-Bit, Simultaneous-Sampling ADCs with ±10V, ±5V, and 0 to +5V Analog Input Ranges

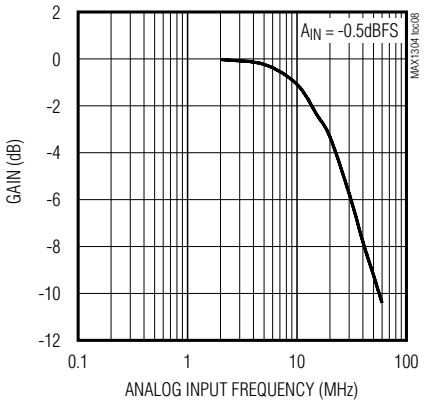
Typical Operating Characteristics (continued)

(V_{AVDD} = +5V, V_{DVDD} = +3V, V_{AGND} = V_{DGND} = 0V, V_{REF} = V_{REFMS} = +2.5V (external reference), C_{REF} = C_{REFMS} = 0.1µF, C_{REF+} = C_{REF-} = 0.1µF, $C_{REF+-to-REF-}$ = 2.2µF ll 0.1µF, C_{COM} = 2.2µF ll 0.1µF, C_{MSV} = 2.2µF ll 0.1µF (unipolar devices), MSV = AGND (bipolar devices), f_{CLK} = 16.67MHz 50% duty cycle, INTCLK/$\overline{EXTCLK}$ = AGND (external clock), f_{IN} = 500kHz, A_{IN} = -0.4dBFS. T_A = +25°C, unless otherwise noted.) (Figures 3 and 4)

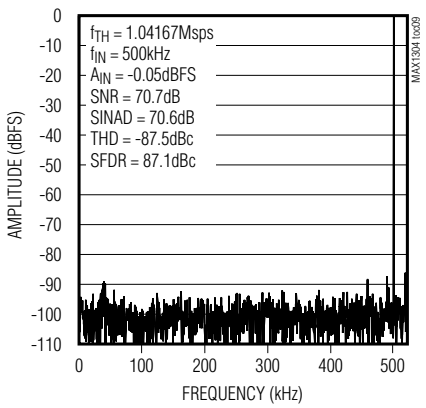
SMALL-SIGNAL BANDWIDTH vs. ANALOG INPUT FREQUENCY



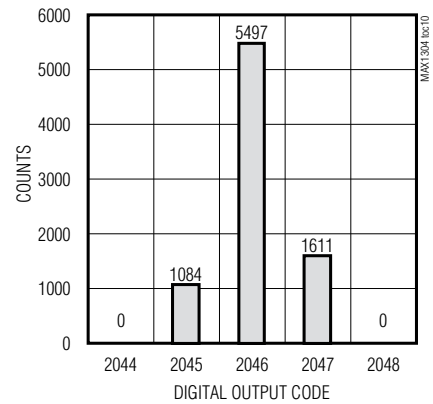
LARGE-SIGNAL BANDWIDTH vs. ANALOG INPUT FREQUENCY



FFT PLOT (2048-POINT DATA RECORD)



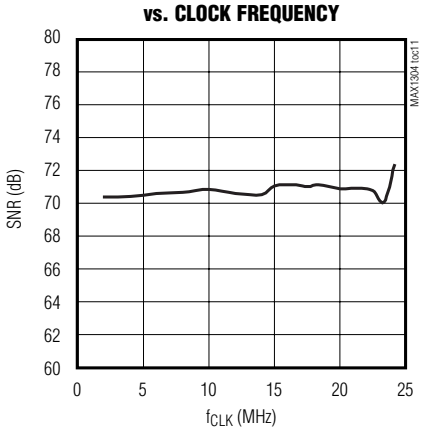
OUTPUT HISTOGRAM (DC INPUT)



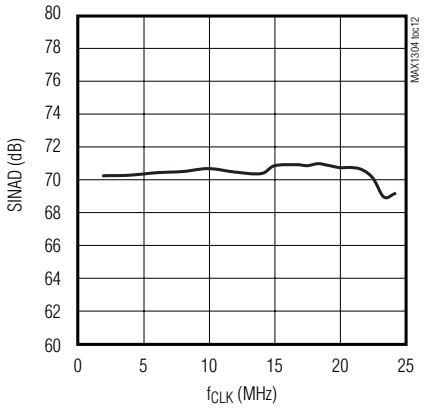
Typical Operating Characteristics (continued)

(V_{AVDD} = +5V, V_{DVDD} = +3V, V_{AGND} = V_{DGND} = 0V, V_{REF} = V_{REFMS} = +2.5V (external reference), C_{REF} = C_{REFMS} = 0.1µF, C_{REF+} = C_{REF-} = 0.1µF, $C_{REF+\text{-to-}REF-}$ = 2.2µF ll 0.1µF, C_{COM} = 2.2µF ll 0.1µF, C_{MSV} = 2.2µF ll 0.1µF (unipolar devices), MSV = AGND (bipolar devices), f_{CLK} = 16.67MHz 50% duty cycle, INTCLK/$\overline{EXTCLK}$ = AGND (external clock), f_{IN} = 500kHz, A_{IN} = -0.4dBFS. T_A = +25°C, unless otherwise noted.) (Figures 3 and 4)

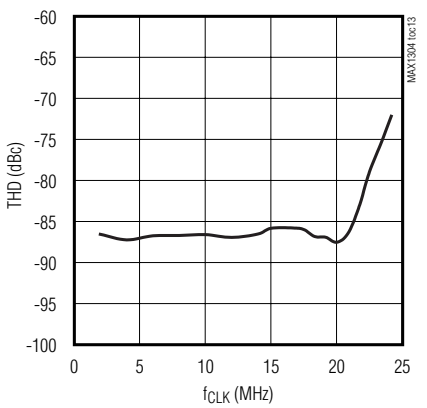
SIGNAL-TO-NOISE RATIO vs. CLOCK FREQUENCY



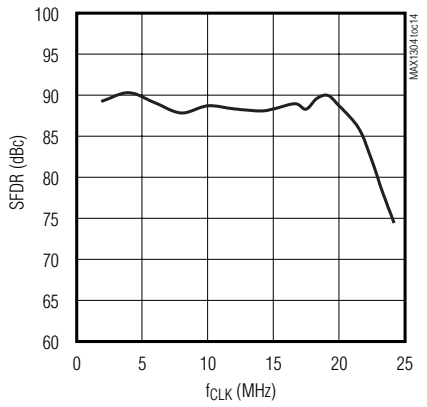
SIGNAL-TO-NOISE PLUS DISTORTION vs. CLOCK FREQUENCY



TOTAL HARMONIC DISTORTION vs. CLOCK FREQUENCY



SPURIOUS-FREE DYNAMIC RANGE vs. CLOCK FREQUENCY

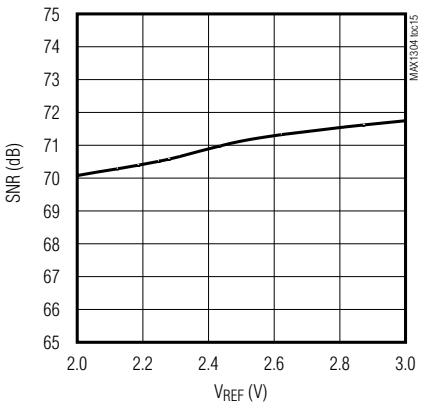


8-/4-/2-Channel, 12-Bit, Simultaneous-Sampling ADCs with ±10V, ±5V, and 0 to +5V Analog Input Ranges

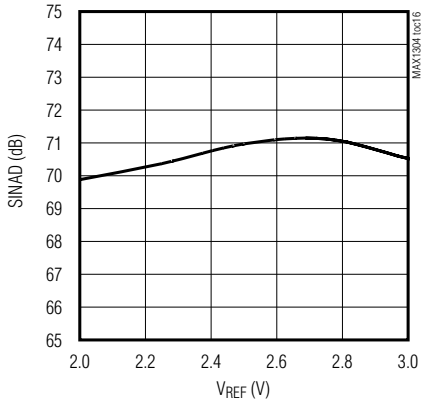
Typical Operating Characteristics (continued)

(V_{AVDD} = +5V, V_{DVDD} = +3V, V_{AGND} = V_{DGND} = 0V, V_{REF} = V_{REFMS} = +2.5V (external reference), C_{REF} = C_{REFMS} = 0.1µF, C_{REF+} = C_{REF-} = 0.1µF, $C_{REF+-to-REF-}$ = 2.2µF ll 0.1µF, C_{COM} = 2.2µF ll 0.1µF, C_{MSV} = 2.2µF ll 0.1µF (unipolar devices), MSV = AGND (bipolar devices), f_{CLK} = 16.67MHz 50% duty cycle, INTCLK/$\overline{EXTCLK}$ = AGND (external clock), f_{IN} = 500kHz, A_{IN} = -0.4dBFS. T_A = +25°C, unless otherwise noted.) (Figures 3 and 4)

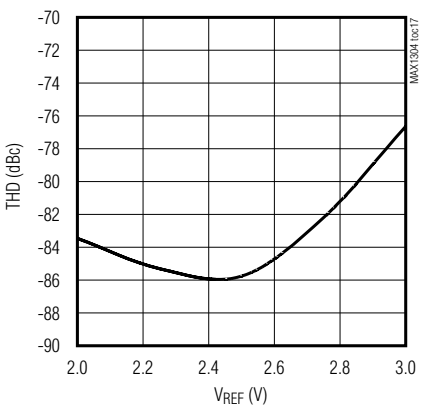
SIGNAL-TO-NOISE RATIO vs. REFERENCE VOLTAGE



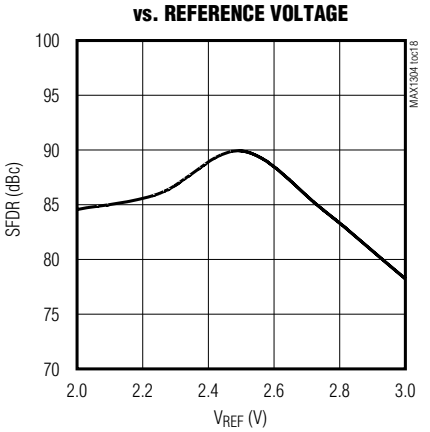
SIGNAL-TO-NOISE PLUS DISTORTION vs. REFERENCE VOLTAGE



TOTAL HARMONIC DISTORTION vs. REFERENCE VOLTAGE



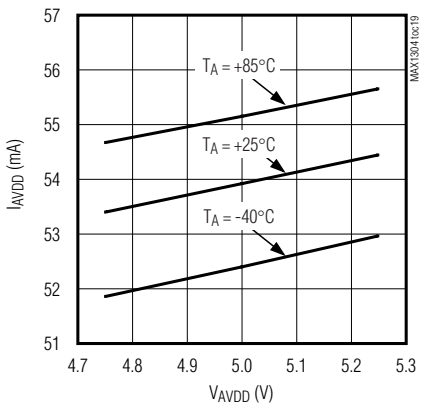
SPURIOUS-FREE DYNAMIC RANGE vs. REFERENCE VOLTAGE



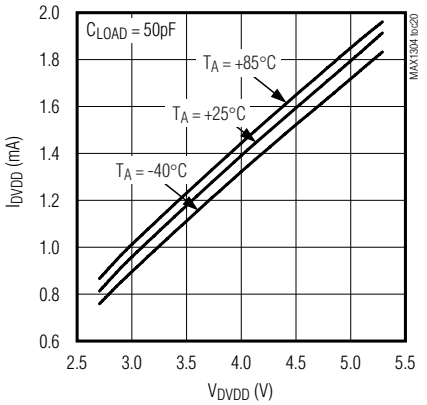
Typical Operating Characteristics (continued)

(V_{AVDD} = +5V, V_{DVDD} = +3V, V_{AGND} = V_{DGND} = 0V, V_{REF} = V_{REFMS} = +2.5V (external reference), C_{REF} = C_{REFMS} = 0.1µF, C_{REF+} = C_{REF-} = 0.1µF, $C_{REF+-to-REF-}$ = 2.2µF ll 0.1µF, C_{COM} = 2.2µF ll 0.1µF, C_{MSV} = 2.2µF ll 0.1µF (unipolar devices), MSV = AGND (bipolar devices), f_{CLK} = 16.67MHz 50% duty cycle, INTCLK/$\overline{EXTCLK}$ = AGND (external clock), f_{IN} = 500kHz, A_{IN} = -0.4dBFS. T_A = +25°C, unless otherwise noted.) (Figures 3 and 4)

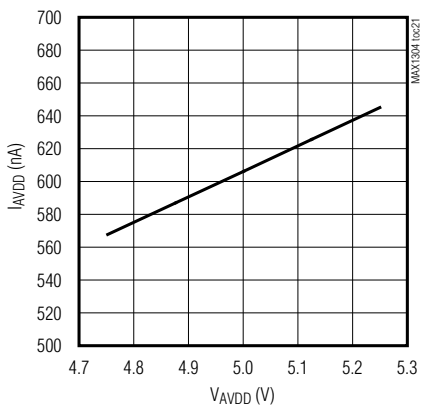
ANALOG SUPPLY CURRENT vs. ANALOG SUPPLY VOLTAGE



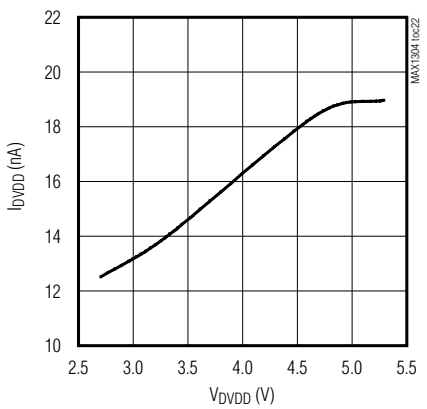
DIGITAL SUPPLY CURRENT vs. DIGITAL SUPPLY VOLTAGE



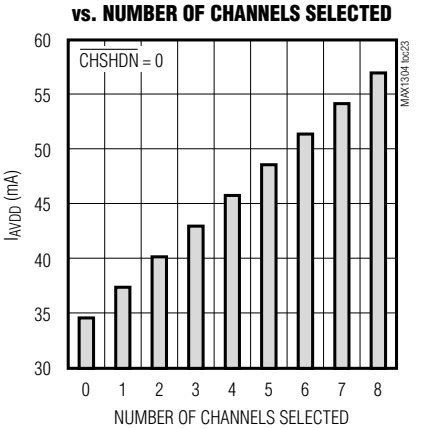
ANALOG SHUTDOWN CURRENT vs. ANALOG SUPPLY VOLTAGE



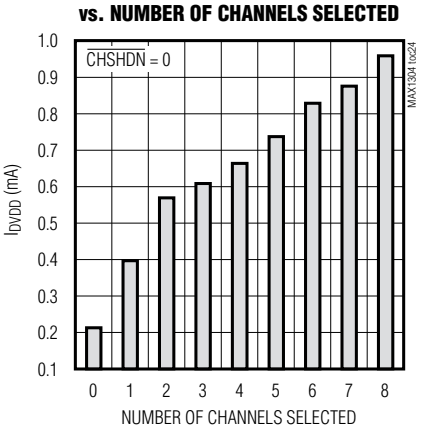
DIGITAL SHUTDOWN CURRENT vs. DIGITAL SUPPLY VOLTAGE



ANALOG SUPPLY CURRENT vs. NUMBER OF CHANNELS SELECTED



DIGITAL SUPPLY CURRENT vs. NUMBER OF CHANNELS SELECTED

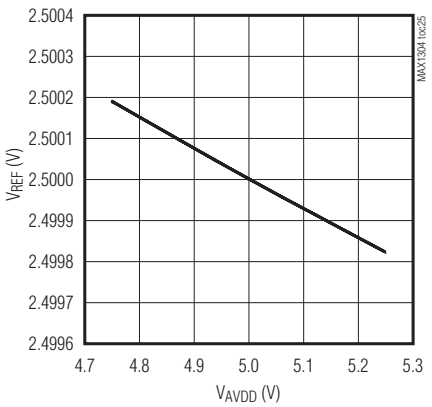


8-/4-/2-Channel, 12-Bit, Simultaneous-Sampling ADCs with ±10V, ±5V, and 0 to +5V Analog Input Ranges

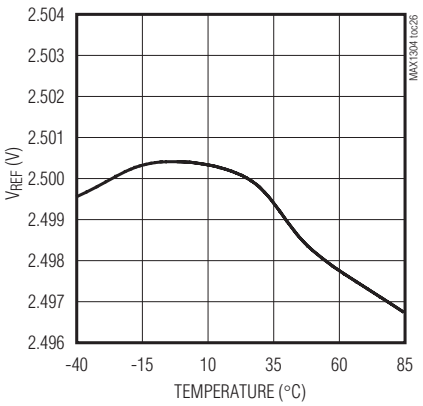
Typical Operating Characteristics (continued)

(V_{AVDD} = +5V, V_{DVDD} = +3V, V_{AGND} = V_{DGND} = 0V, V_{REF} = V_{REFMS} = +2.5V (external reference), C_{REF} = C_{REFMS} = 0.1µF, C_{REF+} = C_{REF-} = 0.1µF, $C_{REF+-to-REF-}$ = 2.2µF ll 0.1µF, C_{COM} = 2.2µF ll 0.1µF, C_{MSV} = 2.2µF ll 0.1µF (unipolar devices), MSV = AGND (bipolar devices), f_{CLK} = 16.67MHz 50% duty cycle, INTCLK/$\overline{EXTCLK}$ = AGND (external clock), f_{IN} = 500kHz, A_{IN} = -0.4dBFS. T_A = +25°C, unless otherwise noted.) (Figures 3 and 4)

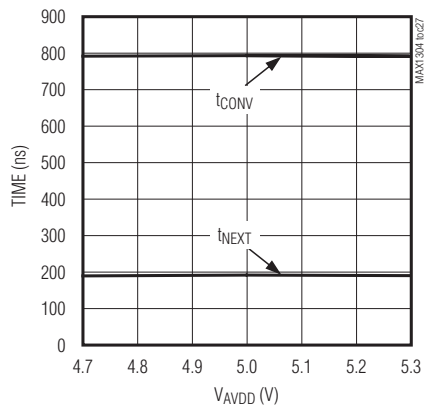
INTERNAL REFERENCE VOLTAGE vs. ANALOG SUPPLY VOLTAGE



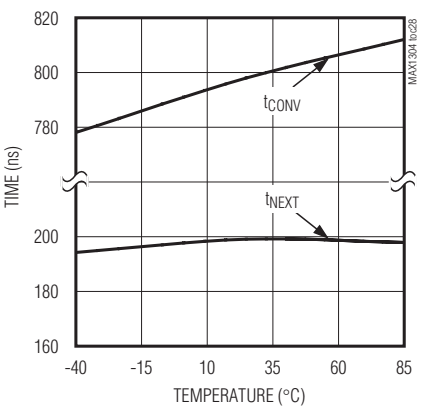
INTERNAL REFERENCE VOLTAGE vs. TEMPERATURE



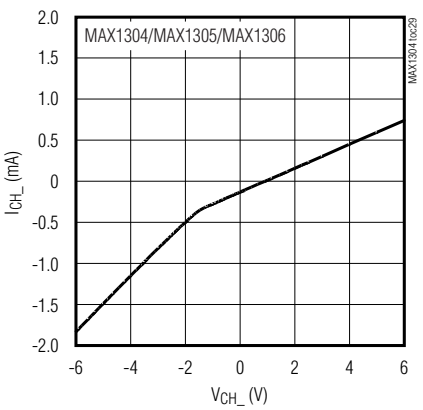
INTERNAL CLOCK CONVERSION TIME vs. ANALOG SUPPLY VOLTAGE



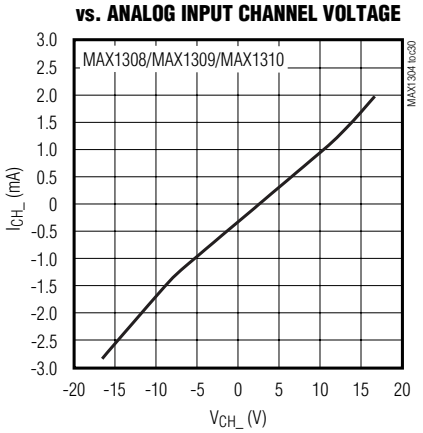
INTERNAL CLOCK CONVERSION TIME vs. TEMPERATURE



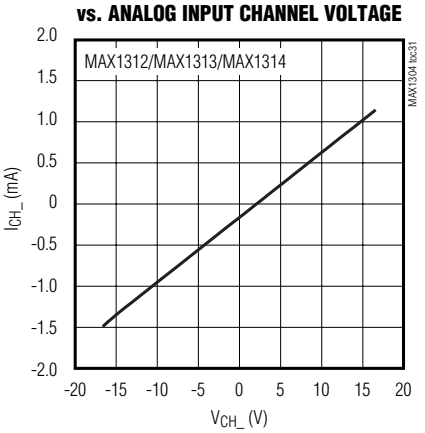
ANALOG INPUT CHANNEL CURRENT vs. ANALOG INPUT CHANNEL VOLTAGE



ANALOG INPUT CHANNEL CURRENT vs. ANALOG INPUT CHANNEL VOLTAGE



ANALOG INPUT CHANNEL CURRENT vs. ANALOG INPUT CHANNEL VOLTAGE



Pin Description

PIN			NAME	FUNCTION
MAX1304 MAX1308 MAX1312	MAX1305 MAX1309 MAX1313	MAX1306 MAX1310 MAX1314		
1, 15, 17	1, 15, 17	1, 15, 17	AVDD	Analog Power Input. AVDD is the power input for the analog section of the converter. Apply +5V to AVDD. Connect all AVDD pins together. See the *Layout, Grounding, and Bypassing* section for additional information.
2, 3, 14, 16, 23	2, 3, 14, 16, 23	2, 3, 14, 16, 23	AGND	Analog Ground. AGND is the power return for AVDD. Connect all AGND pins together.
4	4	4	CH0	Channel 0 Analog Input
5	5	5	CH1	Channel 1 Analog Input
6	6	6	MSV	Midscale Voltage Bypass. For the unipolar MAX1304/MAX1305/MAX1306, connect a 2.2µF and a 0.1µF capacitor from MSV to AGND. For the bipolar MAX1308/MAX1309/MAX1310/MAX1312/MAX1313/MAX1314, connect MSV to AGND.
7	7	—	CH2	Channel 2 Analog Input
8	8	—	CH3	Channel 3 Analog Input
9	—	—	CH4	Channel 4 Analog Input
10	—	—	CH5	Channel 5 Analog Input
11	—	—	CH6	Channel 6 Analog Input
12	—	—	CH7	Channel 7 Analog Input
13	13	13	INTCLK/$\overline{\text{EXTCLK}}$	Clock-Mode Select Input. Connect INTCLK/$\overline{\text{EXTCLK}}$ to AVDD to select the internal clock. Connect INTCLK/$\overline{\text{EXTCLK}}$ to AGND to use an external clock connected to CLK.
18	18	18	REF_{MS}	Midscale Reference Bypass or Input. REF_{MS} connects through a 5k_ resistor to the internal +2.5V bandgap reference buffer. For the MAX1304/MAX1305/MAX1306 unipolar devices, V_{REFMS} is the input to the unity-gain buffer that drives MSV. MSV sets the midpoint of the input voltage range. For internal reference operation, bypass REF_{MS} with a ≥ 0.01µF capacitor to AGND. For external reference operation, drive REF_{MS} with an external voltage from +2V to +3V. For the MAX1308/MAX1309/MAX1310/MAX1312/MAX1313/MAX1314 bipolar devices, connect REF_{MS} to REF. For internal reference operation, bypass the REF_{MS}/REF node with a ≥ 0.01µF capacitor to AGND. For external reference operation, drive the REF_{MS}/REF node with an external voltage from +2V to +3V.
19	19	19	REF	ADC Reference Bypass or Input. REF connects through a 5k_ resistor to the internal +2.5V bandgap reference buffer. For internal reference operation, bypass REF with a ≥ 0.01µF capacitor. For external reference operation with the MAX1304/MAX1305/MAX1306 unipolar devices, drive REF with an external voltage from +2V to +3V. For external reference operation with the MAX1308/MAX1309/MAX1310/ MAX1312/MAX1313/MAX1314 bipolar devices, connect REF_{MS} to REF and drive the REF_{MS}/REF node with an external voltage from +2V to +3V.

8-/4-/2-Channel, 12-Bit, Simultaneous-Sampling ADCs with ±10V, ±5V, and 0 to +5V Analog Input Ranges

Pin Description (continued)

PIN			NAME	FUNCTION
MAX1304 MAX1308 MAX1312	MAX1305 MAX1309 MAX1313	MAX1306 MAX1310 MAX1314		
20	20	20	REF+	Positive Reference Bypass. Bypass REF+ with a 0.1µF capacitor to AGND. Also bypass REF+ to REF- with a 2.2µF and a 0.1µF capacitor. $V_{REF+} = V_{COM} + V_{REF}/2$.
21	21	21	COM	Reference Common Bypass. Bypass COM to AGND with a 2.2µF and a 0.1µF capacitor. V_{COM} = 13/25 x AVDD.
22	22	22	REF-	Negative Reference Bypass. Bypass REF- with a 0.1µF capacitor to AGND. Also bypass REF- to REF+ with a 2.2µF and a 0.1µF capacitor. $V_{REF-} = V_{COM} - V_{REF}/2$.
24, 39	24, 39	24, 39	DGND	Digital Ground. DGND is the power return for DVDD. Connect all DGND pins together.
25, 38	25, 38	25, 38	DVDD	Digital Power Input. DVDD powers the digital section of the converter, including the parallel interface. Apply +2.7V to +5.25V to DVDD. Bypass DVDD to DGND with a 0.1µF capacitor. Connect all DVDD pins together.
26	26	26	D0	Digital I/O 0 of 12-Bit Parallel Data Bus. High impedance when $\overline{RD}$ = 1 or $\overline{CS}$ = 1.
27	27	27	D1	Digital I/O 1 of 12-Bit Parallel Data Bus. High impedance when $\overline{RD}$ = 1 or $\overline{CS}$ = 1.
28	28	28	D2	Digital I/O 2 of 12-Bit Parallel Data Bus. High impedance when $\overline{RD}$ = 1 or $\overline{CS}$ = 1.
29	29	29	D3	Digital I/O 3 of 12-Bit Parallel Data Bus. High impedance when $\overline{RD}$ = 1 or $\overline{CS}$ = 1.
30	30	30	D4	Digital I/O 4 of 12-Bit Parallel Data Bus. High impedance when $\overline{RD}$ = 1 or $\overline{CS}$ = 1.
31	31	31	D5	Digital I/O 5 of 12-Bit Parallel Data Bus. High impedance when $\overline{RD}$ = 1 or $\overline{CS}$ = 1.
32	32	32	D6	Digital I/O 6 of 12-Bit Parallel Data Bus. High impedance when $\overline{RD}$ = 1 or $\overline{CS}$ = 1.
33	33	33	D7	Digital I/O 7 of 12-Bit Parallel Data Bus. High impedance when $\overline{RD}$ = 1 or $\overline{CS}$ = 1.
34	34	34	D8	Digital Output 8 of 12-Bit Parallel Data Bus. High impedance when $\overline{RD}$ = 1 or $\overline{CS}$ = 1.
35	35	35	D9	Digital Output 9 of 12-Bit Parallel Data Bus. High impedance when $\overline{RD}$ = 1 or $\overline{CS}$ = 1.
36	36	36	D10	Digital Output 10 of 12-Bit Parallel Data Bus. High impedance when $\overline{RD}$ = 1 or $\overline{CS}$ = 1.
37	37	37	D11	Digital Output 11 of 12-Bit Parallel Data Bus. High impedance when $\overline{RD}$ = 1 or $\overline{CS}$ = 1.
40	40	40	$\overline{EOC}$	End-of-Conversion Output. $\overline{EOC}$ goes low to indicate the end of a conversion. It returns high on the next rising CLK edge or the falling CONVST edge.
41	41	41	$\overline{EOLC}$	End-of-Last-Conversion Output. $\overline{EOLC}$ goes low to indicate the end of the last conversion. It returns high when CONVST goes low for the next conversion sequence.
42	42	42	$\overline{RD}$	Read Input. Pulling $\overline{RD}$ low initiates a read command of the parallel data bus.
43	43	43	$\overline{WR}$	Write Input. Pulling $\overline{WR}$ low initiates a write command for configuring the device with D0–D7.

Pin Description (continued)

PIN			NAME	FUNCTION
MAX1304 MAX1308 MAX1312	MAX1305 MAX1309 MAX1313	MAX1306 MAX1310 MAX1314		
44	44	44	$\overline{CS}$	Chip-Select Input. Pulling $\overline{CS}$ low activates the digital interface. Forcing $\overline{CS}$ high places D0–D11 in high-impedance mode.
45	45	45	CONVST	Conversion Start Input. Driving CONVST high initiates the conversion process. The analog inputs are sampled on the rising edge of CONVST.
46	46	46	CLK	External Clock Input. For external clock operation, connect INTCLK/$\overline{EXTCLK}$ to AGND and drive CLK with an external clock signal from 100kHz to 20MHz. For internal clock operation, connect INTCLK/$\overline{EXTCLK}$ to AVDD and connect CLK to DGND.
47	47	47	SHDN	Shutdown Input. Driving SHDN high initiates device shutdown. Connect SHDN to DGND for normal operation.
48	48	48	$\overline{CHSHDN}$	Active-Low Analog-Input Channel-Shutdown Input. Drive $\overline{CHSHDN}$ low to power down analog inputs that are not selected for conversion in the configuration register. Drive $\overline{CHSHDN}$ high to power up all analog input channels regardless of whether they are selected for conversion in the configuration register. See the *Channel Shutdown ($\overline{CHSHDN}$)* section for more information.
—	9, 10, 11, 12	7, 8, 9, 10, 11, 12	I.C.	Internally connected. Connect I.C. to AGND.

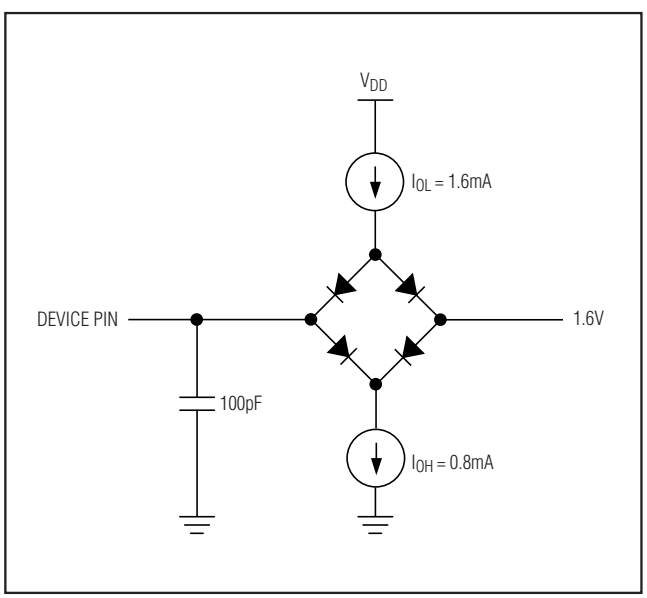


Figure 1. Digital Load Test Circuit

Detailed Description

The MAX1304–MAX1306/MAX1308–MAX1310/MAX1312–MAX1314 are 12-bit ADCs. The devices offer 8, 4, or 2 independently selectable input channels, each with dedicated T/H circuitry. Simultaneous sampling of all active channels preserves relative phase information making these devices ideal for motor control and power monitoring. Three input ranges are available, 0 to +5V, ±5V and ±10V. The 0 to +5V devices provide ±6V fault-tolerant inputs. The ±5V and ±10V devices provide ±16.5V fault-tolerant inputs. Two-channel conversion results are available in 0.9µs. Conversion results from all eight channels are available in 1.98µs. The 8-channel throughput is 456ksps per channel. Internal or external reference and clock capability offer great flexibility, and ease of use. A write-only configuration register can mask out unused channels and a shutdown feature reduces power. A 20MHz, 12-bit, parallel data bus outputs the conversion results. Figure 2 shows the functional diagram of these ADCs.

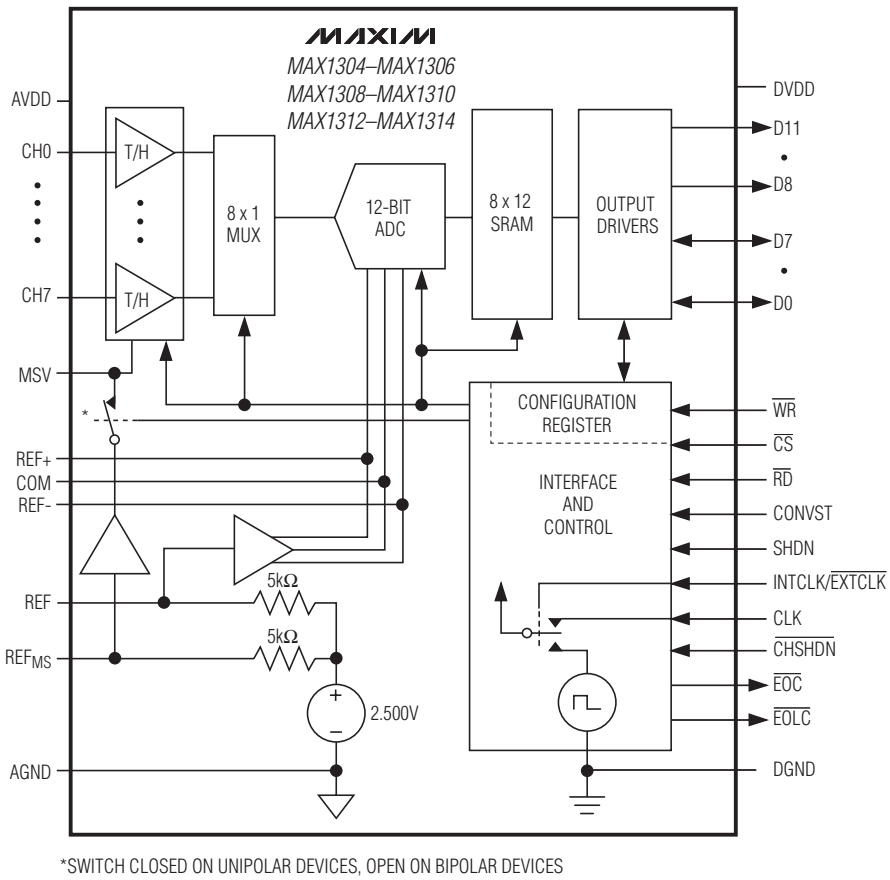


Figure 2. Functional Diagram

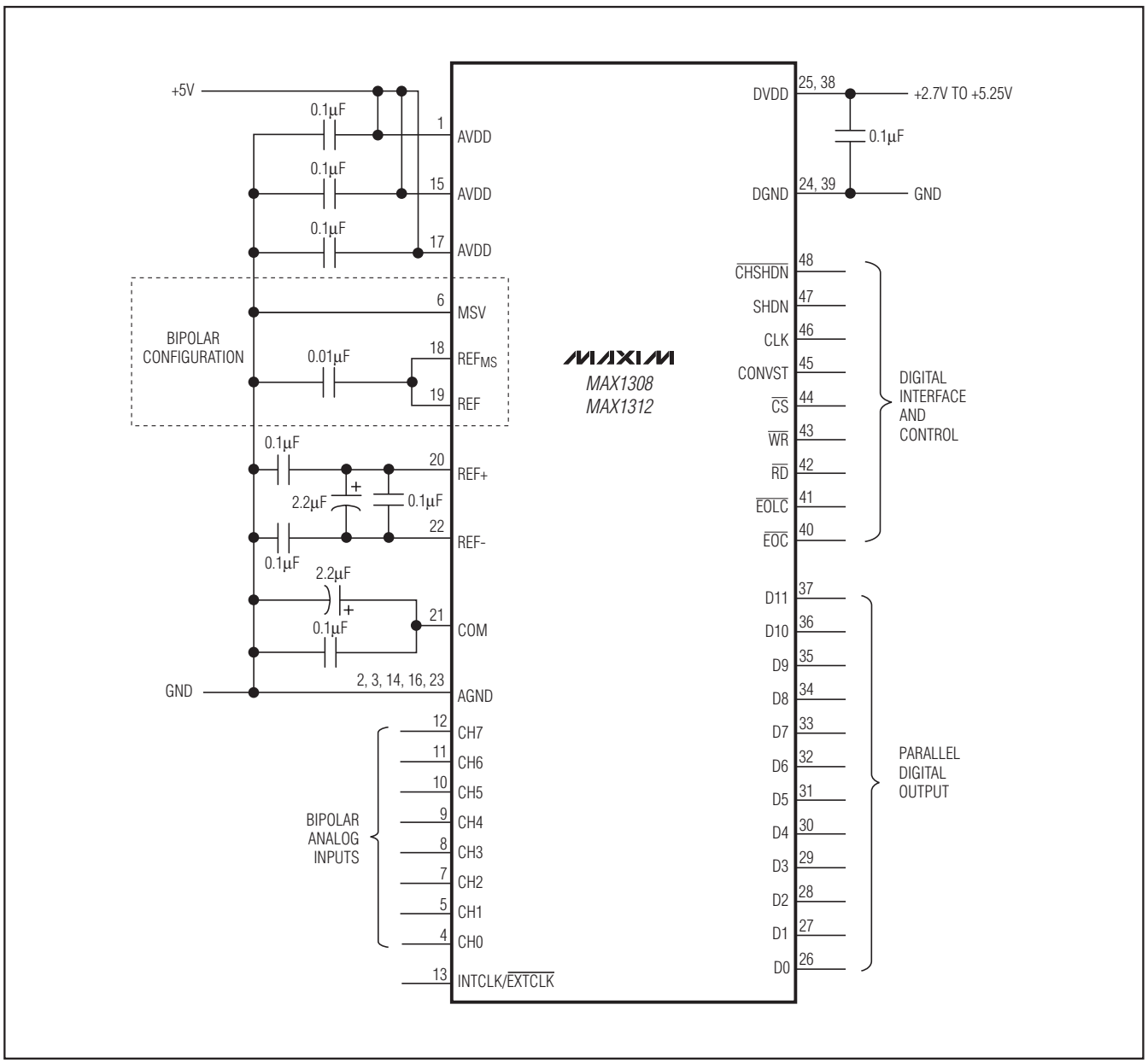


Figure 3. Typical Bipolar Operating Circuit

8-/4-/2-Channel, 12-Bit, Simultaneous-Sampling ADCs with ±10V, ±5V, and 0 to +5V Analog Input Ranges

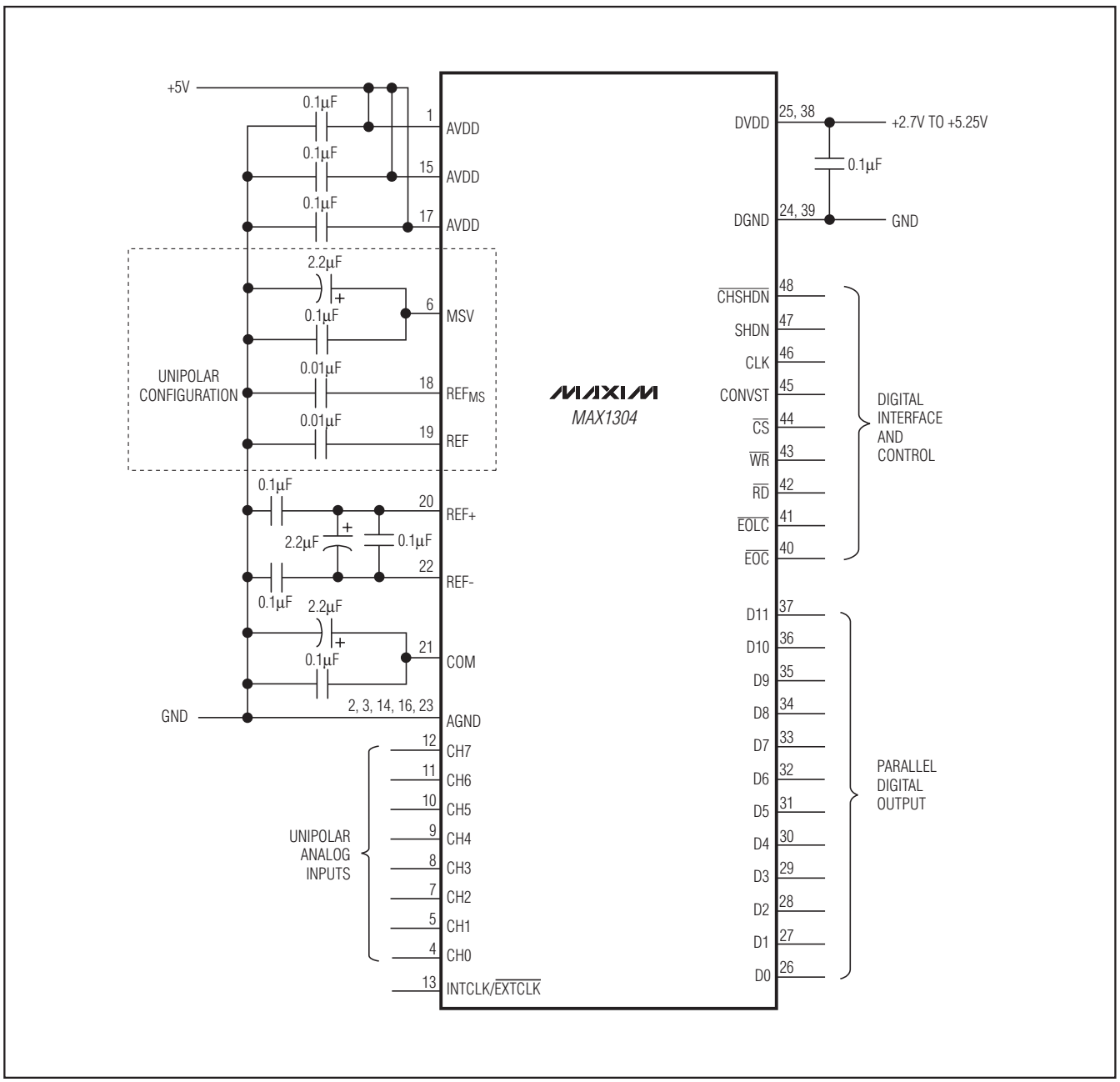
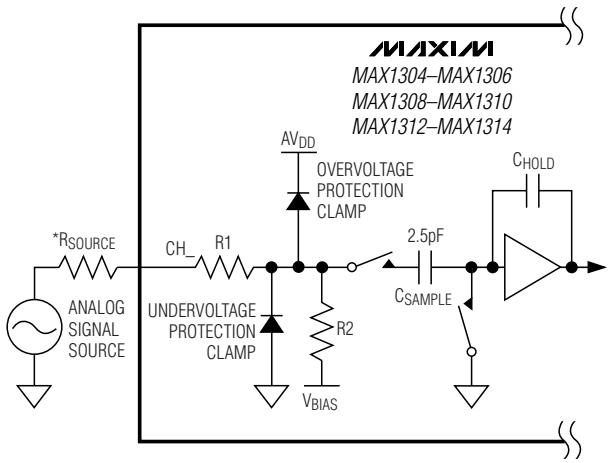


Figure 4. Typical Unipolar Operating Circuit



*MINIMIZE R_{SOURCE} TO AVOID GAIN ERROR AND DISTORTION.

PART	INPUT RANGE (V)	R1 (kΩ)	R2 (kΩ)	V_{BIAS} (V)
MAX1304 MAX1305 MAX1306	0 TO +5	3.33	5.00	0.90
MAX1308 MAX1309 MAX1310	±5	6.67	2.86	2.50
MAX1312 MAX1313 MAX1314	±10	13.33	2.35	2.06

R1 | | R2 = 2kΩ

Figure 5. Single-Channel, Equivalent Analog Input T/H Circuit

Analog Inputs

Track and Hold (T/H)

To preserve phase information across the multichannel MAX1304–MAX1306/MAX1308–MAX1310/MAX1312–MAX1314, all input channels have dedicated T/H amplifiers. Figure 5 shows the equivalent analog input T/H circuit for one channel.

The input T/H circuit is controlled by the CONVST input. When CONVST is low, the T/H circuit tracks the analog input. When CONVST is high the T/H circuit holds the analog input. The rising edge of CONVST is the analog input sampling instant. There is an aperture delay (t_{AD}) of 8ns and a $50ps_{RMS}$ aperture jitter (t_{AJ}). The aperture delay of each dedicated T/H input is matched within 100ps of each other.

To settle the charge on C_{SAMPLE} to 12-bit accuracy, use a minimum acquisition time (t_{ACQ}) of 100ns. Therefore, CONVST must be low for at least 100ns. Although longer acquisition times allow the analog input to settle to its final value more accurately, the maximum acquisition time must be limited to 1ms. Accuracy with conversion times longer than 1ms cannot be guaranteed due to capacitor droop in the input circuitry.

Due to the analog input resistive divider formed by R1 and R2 in Figure 5, any significant analog input source resistance (R_{SOURCE}) results in gain error. Furthermore, R_{SOURCE} causes distortion due to nonlinear analog input currents. Limit R_{SOURCE} to a maximum of 100Ω.

Selecting an Input Buffer

To improve the input signal bandwidth under AC conditions, drive the input with a wideband buffer (>50MHz) that can drive the ADC's input capacitance (15pF) and settle quickly. For example, the MAX4431 or the MAX4265 can be used for the 0 to +5V unipolar devices, or the MAX4350 can be used for ±5V bipolar inputs.

Most applications require an input buffer to achieve 12-bit accuracy. Although slew rate and bandwidth are important, the most critical input buffer specification is settling time. The simultaneous sampling of multiple channels requires an acquisition time of 100ns. At the beginning of the acquisition, the ADC internal sampling capacitor array connects to the analog inputs, causing some disturbance. Ensure the amplifier is capable of settling to at least 12-bit accuracy during this interval. Use a low-noise, low-distortion, wideband amplifier that settles quickly and is stable with the ADC's 15pF input capacitance.

See the Maxim website at **www.maxim-ic.com** for application notes on how to choose the optimum buffer amplifier for your ADC application.

Input Bandwidth

The input-tracking circuitry has a 20MHz small-signal bandwidth, making it possible to digitize high-speed transient events and measure periodic signals with bandwidths exceeding the ADC's sampling rate by using undersampling techniques. To avoid high-frequency signals being aliased into the frequency band of interest, anti-alias filtering is recommended.

Input Range and Protection

The MAX1304/MAX1305/MAX1306 provide a 0 to +5V input voltage range with fault protection of ±6V. The MAX1308/MAX1309/MAX1310 provide a ±5V input voltage range with fault protection of ±16.5V. The MAX1312/MAX1313/MAX1314 provide a ±10V input voltage range with fault protection of ±16.5V. Figure 5 shows the single-channel equivalent input circuit.

Data Throughput

The data throughput (f_{TH}) of the MAX1304–MAX1306/MAX1308–MAX1310/MAX1312–MAX1314 is a function of the clock speed (f_{CLK}). In internal clock mode, f_{CLK} = 15MHz (typ). In external clock mode, 100kHz ≤ f_{CLK} ≤ 20MHz. When reading during conversion (Figures 7 and 8), calculate f_{TH} as follows:

$$f_{TH} = \frac{1}{t_{ACQ} + t_{QUIET} + \frac{12 + 3\ x\ (N-1) + 1}{f_{CLK}}}$$

where N is the number of active channels and t_{QUIET} is the period of bus inactivity before the rising edge of CONVST. See the *Starting a Conversion* section for more information.

Table 1 uses the above equation and shows the total throughput as a function of the number of channels selected for conversion.

Clock Modes

The MAX1304–MAX1306/MAX1308–MAX1310/MAX1312–MAX1314 provide a 15MHz internal conversion clock. Alternatively, an external clock can be used.

Internal Clock

Internal clock mode frees the microprocessor from the burden of running the ADC conversion clock. For internal clock operation, connect INTCLK/$\overline{\text{EXTCLK}}$ to AVDD and connect CLK to DGND. Note that INTCLK/$\overline{\text{EXTCLK}}$ is referenced to AV_{DD}, not DV_{DD}.

External Clock

For external clock operation, connect INTCLK/$\overline{\text{EXTCLK}}$ to AGND and connect an external clock source to CLK. Note that INTCLK/$\overline{\text{EXTCLK}}$ is referenced to AVDD, not DVDD. The external clock frequency can be up to 20MHz. Linearity is not guaranteed with clock frequencies below 100kHz due to droop in the T/H circuits.

Table 1. Throughput vs. Channels Sampled: f_{CLK} = 15MHz, t_{ACQ} = 100ns, t_{QUIET} = 50ns

CHANNELS SAMPLED (N)	CLOCK CYCLES UNTIL LAST RESULT	CLOCK CYCLE FOR READING LAST CONVERSION	TOTAL CONVERSION TIME (ns)	TOTAL THROUGHPUT (ksps)	THROUGHPUT PER CHANNEL (f_{TH})
1	12	1	800	983	983
2	15	1	1000	1643	821
3	18	1	1200	2117	705
4	21	1	1400	2474	618
5	24	1	1600	2752	550
6	27	1	1800	2975	495
7	30	1	2000	3157	451
8	33	1	2200	3310	413

Applications Information

Digital Interface

The bidirectional parallel digital interface allows for setting the 8-bit configuration register (see the *Configuration Register* section) and reading the 12-bit conversion result. The interface includes the following control signals: chip select ($\overline{CS}$), read ($\overline{RD}$), write ($\overline{WR}$), end of conversion ($\overline{EOC}$), end of last conversion ($\overline{EOLC}$), conversion start (CONVST), shutdown (SHDN), channel shutdown ($\overline{CHSHDN}$), internal clock select (INTCLK/$\overline{EXTCLK}$), and external clock input (CLK). Figures 6, 7, 8, 9, Table 2, and the *Timing Characteristics* show the operation of the interface. D0–D7 are bidirectional, and D8–D11 are output only. D0–D11 go high impedance when $\overline{RD}$ = 1 or $\overline{CS}$ = 1.

Configuration Register

Enable channels as active by writing to the configuration register through I/O lines D0–D7 (Table 2). The bits in the configuration register map directly to the channels, with D0 controlling channel zero, and D7 controlling channel seven. Setting any bit high activates the corresponding input channel, while resetting any bit low deactivates the corresponding channel. On the devices with less than eight channels, some of the bits have no function (Table 2).

To write to the configuration register, pull $\overline{CS}$ and $\overline{WR}$ low, load bits D0 through D7 onto the parallel bus, and force $\overline{WR}$ high. The data are latched on the rising edge of $\overline{WR}$ (Figure 6). Write to the configuration register at any point during the conversion sequence. At power-up, write to the configuration register to select the active channels before beginning a conversion.

However, the new configuration does not take effect until the next CONVST falling edge. At power-up all channels default active. Shutdown does not change the configuration register. The configuration register may be written to in shutdown. See the *Channel Shutdown ($\overline{CHSHDN}$)* section for information about using the configuration register for power saving.

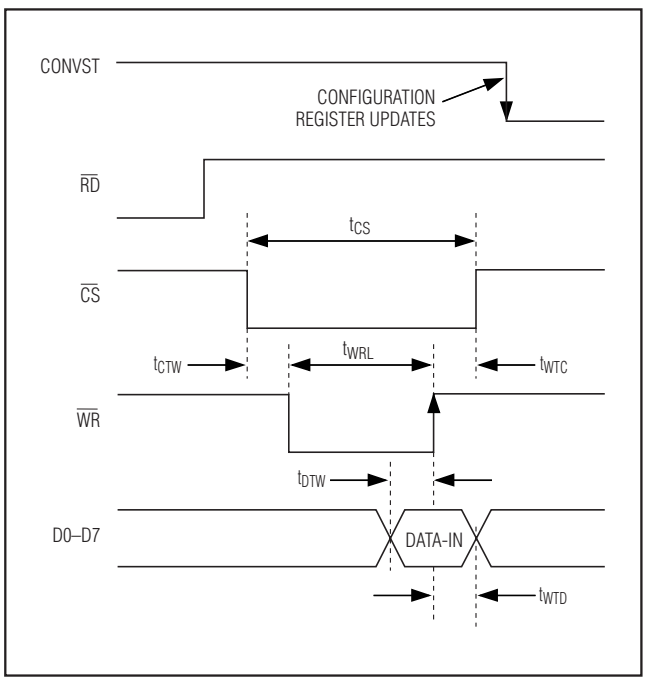


Figure 6. Write Timing

Table 2. Configuration Register

PART NUMBER	STATE	BIT/CHANNEL							
		D0/CH0	D1/CH1	D2/CH2	D3/CH3	D4/CH4	D5/CH5	D6/CH6	D7/CH7
MAX1304 MAX1308 MAX1312	ON	1	1	1	1	1	1	1	1
	OFF	0	0	0	0	0	0	0	0
MAX1305 MAX1309 MAX1313	ON	1	1	1	1	X	X	X	X
	OFF	0	0	0	0	X	X	X	X
MAX1306 MAX1310 MAX1314	ON	1	1	X	X	X	X	X	X
	OFF	0	0	X	X	X	X	X	X

X = Don't care (must be 1 or 0).

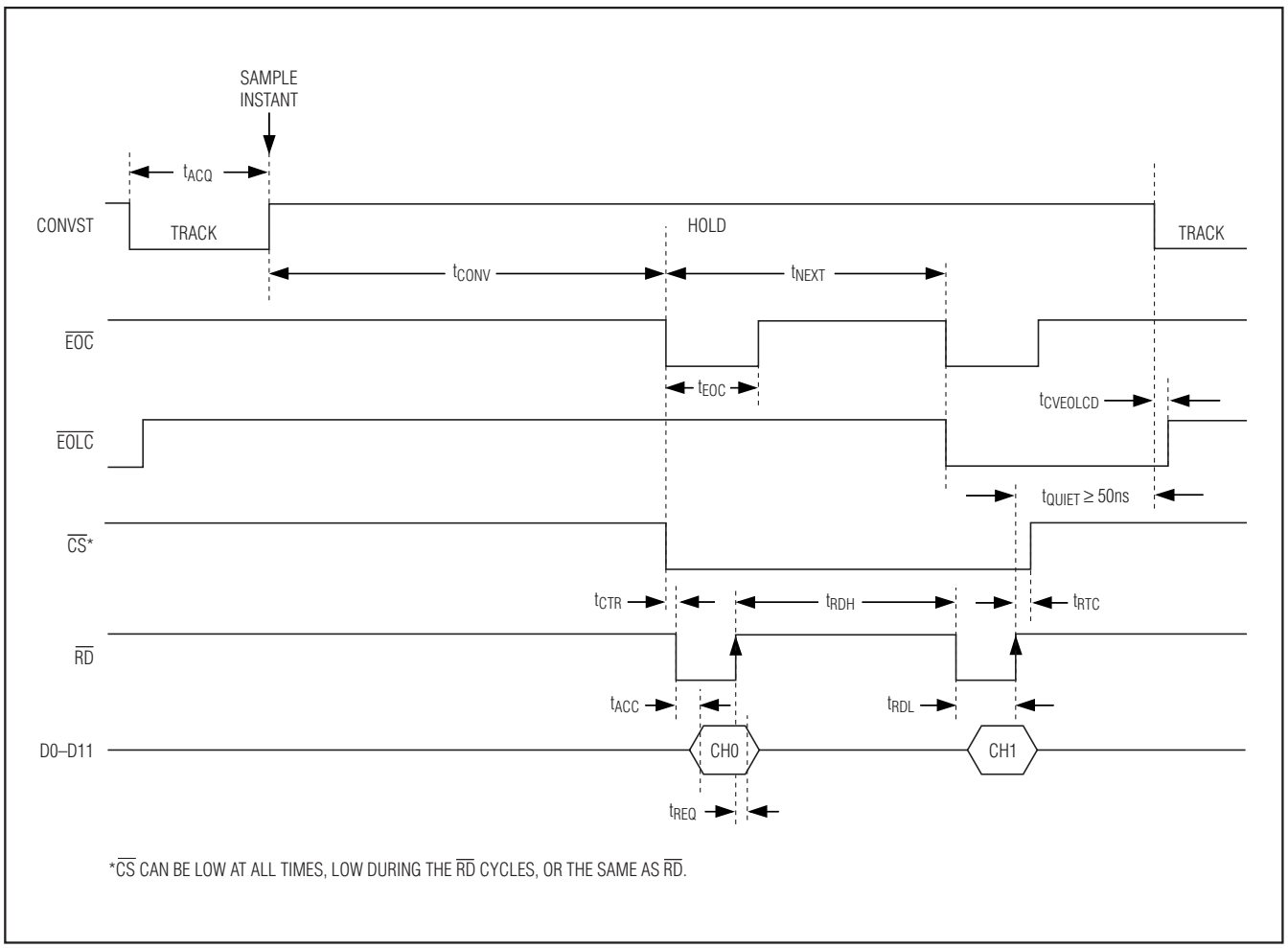


Figure 7. Read During Conversion—Channel 0 and Channel 1 Selected, Internal Clock

Starting a Conversion

To start a conversion using internal clock mode, pull CONVST low for the acquisition time (t_{ACQ}). The T/H acquires the signal while CONVST is low, and conversion begins on the rising edge of CONVST. The end-of-conversion signal ($\overline{EOC}$) pulses low whenever a conversion result becomes available for read. The end-of-last-conversion signal ($\overline{EOLC}$) goes low when the last conversion result is available (Figure 7).

To start a conversion using external clock mode, pull CONVST low for the acquisition time (t_{ACQ}). The T/H acquires the signal while CONVST is low. The rising edge of CONVST is the sampling instant. Apply an external clock to CLK to start the conversion. To avoid T/H droop degrading the sampled analog input signals, the first CLK pulse must occur within 10µs from the rising edge of CONVST. Additionally, the external clock frequency must be greater than 100kHz to avoid T/H droop-degrading accuracy. The first conversion result is available for read when $\overline{EOC}$ goes low on the rising edge of the 13th clock cycle. Subsequent conversion results are available after every third clock cycle thereafter (Figures 8 and 9).

In both internal and external clock modes, hold CONVST high until the last conversion result is read. If CONVST goes low in the middle of a conversion, the current conversion is aborted and a new conversion is initiated. Furthermore, there must be a period of bus inactivity (t_{QUIET}) for 50ns or longer before the falling edge of CONVST for the specified ADC performance.

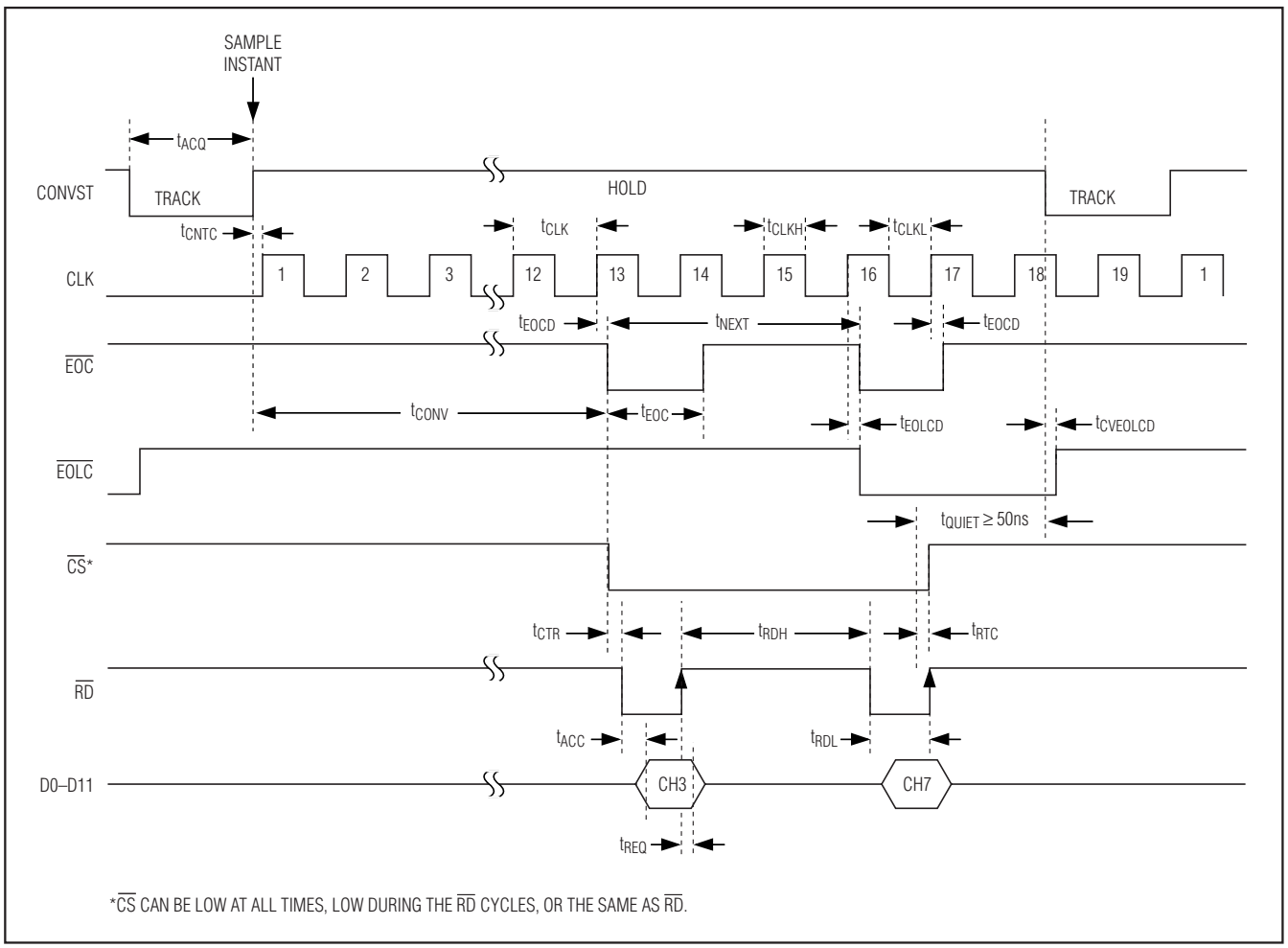


Figure 8. Read During Conversion—Channel 3 and Channel 7 Selected, External Clock

Reading a Conversion Result

Reading During a Conversion

Figures 7 and 8 show the interface signals to initiate a read operation during a conversion cycle. These figures show two channels selected for conversion. If more channels are selected, the results are available successively at every $\overline{EOC}$ falling edge. $\overline{CS}$ can be low at all times, low during the $\overline{RD}$ cycles, or the same as $\overline{RD}$.

After initiating a conversion by bringing CONVST high, wait for $\overline{EOC}$ to go low. In internal clock mode, $\overline{EOC}$ goes low within 900ns. In external clock mode, $\overline{EOC}$ goes low on the rising edge of the 13th CLK cycle. To read the conversion result, drive $\overline{CS}$ and $\overline{RD}$ low to latch data to the parallel digital output bus. Bring $\overline{RD}$ high to release the digital bus. In internal clock mode, the next $\overline{EOC}$ falling edge occurs within 225ns. In external clock mode, the next $\overline{EOC}$ falling edge occurs in three CLK cycles. When the last result is available $\overline{EOLC}$ goes low.

Reading After Conversion

Figure 9 shows the interface signals for a read operation after a conversion with all eight channels enabled. At the falling of $\overline{EOLC}$, driving $\overline{CS}$ and $\overline{RD}$ low places the first conversion result onto the parallel bus. Successive low pulses of $\overline{RD}$ place the successive conversion results onto the bus. When the last conversion results in the sequence are read, additional read pulses wrap the pointer back to the first converted result.

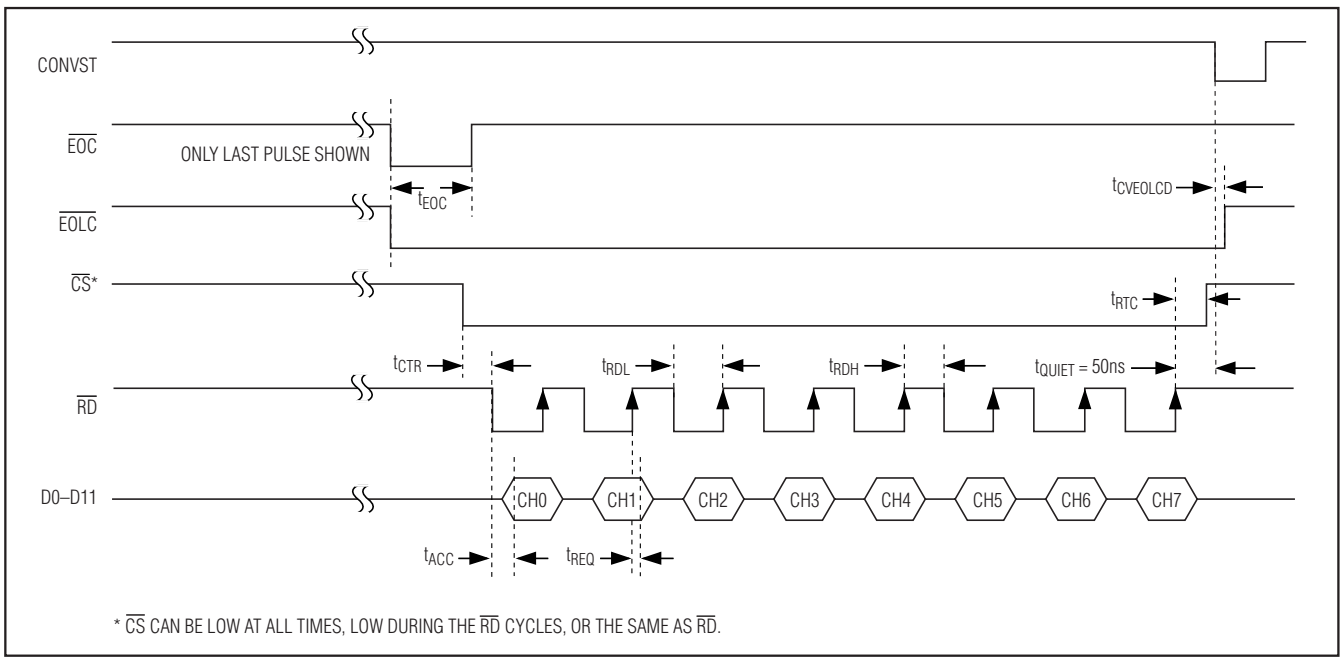


Figure 9. Read After Conversion—Eight Channels Selected, External Clock

Power-Up Reset

At power-up, all channels are selected for conversion (see the *Configuration Register* section). After applying power, allow the 1ms wake-up time to elapse and then initiate a dummy conversion and discard the results. After the dummy conversion is complete, accurate conversions can be obtained.

Power-Saving Modes

Shutdown Mode

During shutdown the internal reference and analog circuits in the device shutdown and the analog supply current drops to 0.6µA (typ). Select shutdown mode using the SHDN input. Set SHDN high to enter shutdown mode. SHDN takes precedence over CHSHDN.

Entering and exiting shutdown mode does not change the configuration byte. However, a new configuration byte can be written while in shutdown mode by following the standard write procedure shown in Figure 6.

EOC and EOLC are high when the MAX1304–MAX1306/MAX1308–MAX1310/MAX1312–MAX1314 are shut down.

The state of the digital outputs D0–D11 is independent of the state of SHDN. If CS and RD are low, the digital outputs D0–D11 are active regardless of SHDN. The digital outputs only go high impedance when CS or RD is high. When the digital outputs are powered down, the digital supply current drops to 20nA.

Exiting shutdown (falling edge of SHDN) starts a conversion in the same way as the rising edge of CONVST. After coming out of shutdown, initiate a dummy conversion and discard the results. After the dummy conversion, allow the 1ms wake-up time to expire before initiating the first accurate conversion.

Channel Shutdown (CHSHDN)

The channel-shutdown feature allows analog input channels to be powered down when they are not selected for conversion. Powering down channels that are not selected for conversion reduces the analog supply current by 2.9mA per channel. To power down channels that are not selected for conversion, pull CHSHDN low. See the *Configuration Register* section for information on selecting and deselecting channels for conversion.

The drawback of powering down analog inputs that are not selected for conversion is that it takes time to power them up. Figure 10 shows how a dummy conversion is used to power up an analog input in external clock mode. After selecting a new channel in the configuration register, initiate a dummy conversion and discard the results. After the dummy conversion, allow the 1ms wake-up time (t_{WAKE}) to expire before initiating the first accurate conversion.

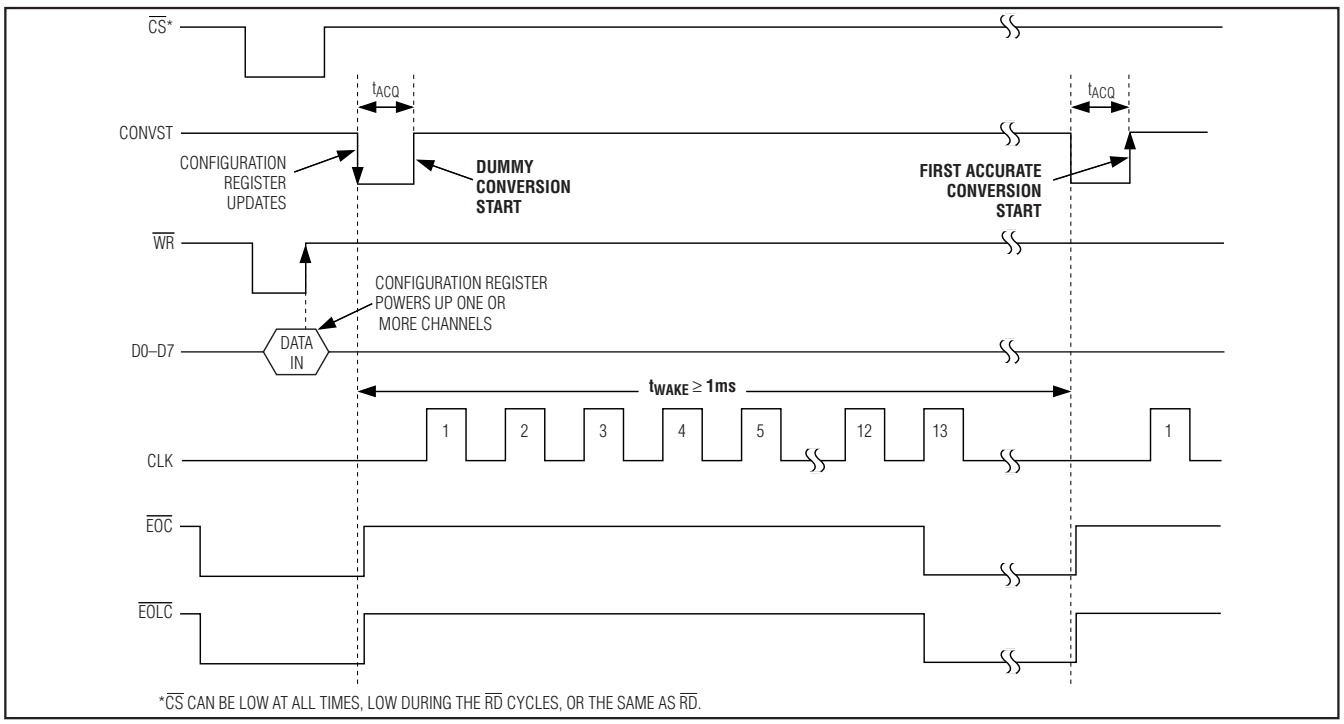


Figure 10. Powering Up an Analog Input Channel with a Dummy Conversion and Wake-Up Time (CHSHDN = 0, External-Clock Mode, One Channel Selected)

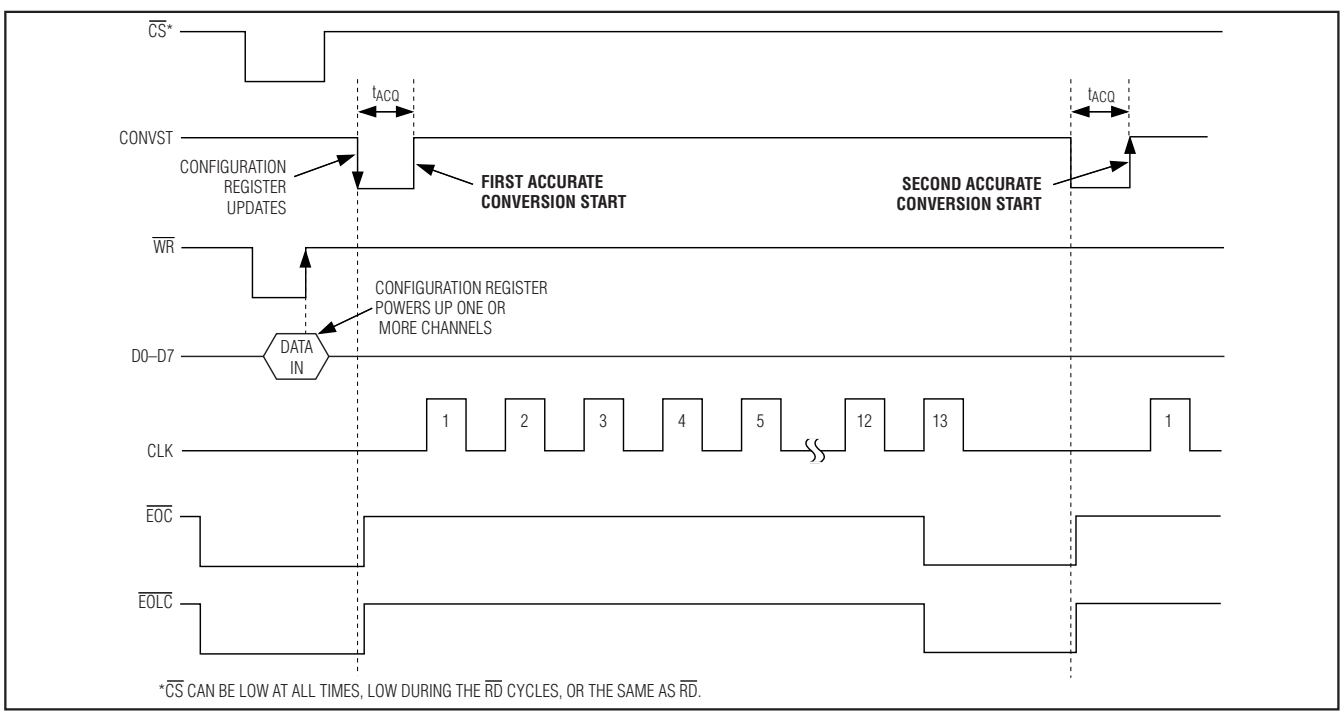


Figure 11. Powering Up an Analog Input Channel Directly (CHSHDN = 1, External-Clock Mode, One Channel Selected)