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Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

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MAXIM

12-/16-Bit DASs with ADC, DACs, DPIOs, APIOs, Reference, Voltage Monitors, and Temp Sensor

General Description

The MAX1329/MAX1330 are smart data acquisition systems (DASs) based on a successive approximation register (SAR) analog-to-digital converter (ADC). These devices are highly integrated, offering an ADC, digital-to-analog converters (DACs), operational amplifiers (op amps), voltage reference, temperature sensors, and analog switches in the same device.

The MAX1329/MAX1330 offer a single ADC with a reference buffer. The ADC is capable of operating in one of two user-programmable modes. In normal mode, the ADC provides up to 12 bits of resolution at 312ksps. In DSP mode, the ADC provides up to 16 bits of resolution at 1000sps. The ADC accepts one external differential input or two external single-ended inputs as well as inputs from other circuitry on-board. An on-chip programmable gain amplifier (PGA) follows the analog inputs, reducing external circuitry requirements. The PGA gain is adjustable from 1V/V to 8V/V.

The MAX1329/MAX1330 operate from a 1.8V to 3.6V digital power supply. Shutdown and sleep modes are available for power-saving applications. Under normal operation, an internal charge pump boosts the supply voltage for the analog circuitry when the supply is < 2.7V.

The MAX1329/MAX1330 offer four analog programmable I/Os (APIOs) and four digital programmable I/Os (DPIOs). The APIOs can be configured as general-purpose logic inputs and outputs, as a wake-up function, or as a buffer and level shifter for the serial interface to communicate with slave devices powered by the analog supply, AV_{DD}. The DPIOs can be configured as general-purpose logic inputs and outputs as well as inputs to directly control the ADC conversion rate, the analog switches, the loading of the DACs, wake-up, sleep, and shutdown modes, and as an interrupt for when the analog-to-digital conversion is complete.

The MAX1329 includes dual 12-bit force-sense DACs with a programmable reference buffer and one op amp. The MAX1330 provides one 12-bit force-sense DAC with a programmable reference buffer and two op amps. For the MAX1329/MAX1330, a 16-word DAC FIFO can be used with the DACA for direct digital synthesis (DDS) of waveforms.

The 4-wire serial interface is compatible with SPI™, QSPI™, and MICROWIRE™.

Applications

Battery-Powered and Portable Devices
Electrochemical and Optical Sensors
Medical Instruments
Industrial Control
Data Acquisition Systems
Low-Cost CODECs

SPI/QSPI are trademarks of Motorola, Inc.
MICROWIRE is a trademark of National Semiconductor Corp.

Features

- **1.8V to 3.6V Single Digital Supply Operation**
- **Internal Charge Pump for Analog Circuits (2.7V to 5.5V)**
- **12-Bit SAR ADC**
  - **12 Bits, 312ksps, No Missing Codes**
  - **16 Bits, 1000sps, DSP Mode**
  - **16-Word FIFO and 20-Bit Accumulator**
  - **PGA with Gains of 1, 2, 4, and 8**
  - **Unipolar and Bipolar Modes**
  - **16-Input Differential Multiplexer**
- **Dual 12-Bit Force-Sense DACs**
  - **16-Word FIFO (DACA Only)**
- **Independent Voltage References for ADC and DACs**
  - **Internal 2.5V Reference**
  - **Adjustable Reference Buffers Provide 1.25V, 2.048V, or 2.5V**
- **System Support**
  - **ADC Alarm Register**
  - **Uncommitted Op Amps**
  - **Dual SPDT Analog Switches**
  - **Internal/External Temperature Sensor**
  - **Internal Oscillator with Clock I/O**
  - **Digital Programmable I/O**
  - **Analog Programmable I/O**
  - **Programmable Interrupts**
  - **Accurate Supply Voltage Measurement**
  - **Programmable Dual Voltage Monitors**
- **SPI-/QSPI-/MICROWIRE-Compatible, 4-Wire Serial Interface**
- **Space-Saving, 6mm x 6mm, 40-Pin Thin QFN Package**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX1329BETL+	-40°C to +85°C	40 Thin QFN-EP**
MAX1330BETL+*	-40°C to +85°C	40 Thin QFN-EP**

**Future product—contact factory for availability.*
***EP = Exposed pad.*
+Denotes a lead-free/RoHS-compliant package.

Pin Configurations appear at end of data sheet.

12-/16-Bit DASs with ADC, DACs, DPIOs, APIOs, Reference, Voltage Monitors, and Temp Sensor

ABSOLUTE MAXIMUM RATINGS

AV_{DD} to AGND .....-0.3V to +6V
DV_{DD} to DGND.....-0.3V to +6V
Analog Inputs to AGND.....-0.3V to the lower of (AV_{DD} + 0.3V) or +6V
Digital Inputs to DGND.....-0.3V to the lower of (DV_{DD} + 0.3V) or +6V
Analog Outputs to AGND.....-0.3V to the lower of (AV_{DD} + 0.3V) or +6V
Digital Outputs to DGND.....-0.3V to the lower of (DV_{DD} + 0.3V) or 6V
AGND to DGND..... -0.3V to +0.3V
Continuous Current into Any Pin.....±50mA
Continuous Power Dissipation (T_A = +70°C)
40-Pin Thin QFN (derate 37mW/°C above +70°C) 2963mW
Operation Temperature Range.....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Junction Temperature.....+150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(DV_{DD} = 1.8V to 3.6V, AV_{DD} = 2.7V to 5.5V, V_{REFDAC} = V_{REFADC} = 2.5V, external reference; 10µF capacitor at REFADC and REFDAC; 0.01µF capacitor at REFADJ; T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ADC						
Resolution		No missing codes	12			Bits
DSP-Mode Resolution		256 oversampling, dither enabled	16			Bits
Integral Nonlinearity	INL	Normal mode (Note 1)			±1	LSB_{12}
Differential Nonlinearity	DNL	Normal mode (Note 1)			±1	LSB_{12}
Offset Error		(Note 1)			±4	mV
Offset Drift				±1.5		µV/°C
Gain Error (Excluding Reference) (Note 1)		Gain = 1			±0.1	% FS
		Gain = 2, 4			±1.5	
		Gain = 8			±2.5	
Gain Temperature Coefficient		Excluding reference		±0.8		ppm/°C
Voltage Range		Unipolar mode, gain = 1, 2, 4, 8	0		$+V_{REFADC}$/ Gain	V
		Bipolar mode, gain = 1, 2, 4, 8	$-V_{REFADC}$/ (2 x Gain)		$+V_{REFADC}$/ (2 x Gain)	
Absolute Input Voltage Range			AGND		AV_{DD}	V
Input Leakage Current into Analog Inputs		(Note 2)		±0.5	±1	nA
Input Capacitance		Gain = 1, 2		24		pF
		Gain = 4, 8		48		
Acquisition Time	t_{ACQ}	Gain = 1, 2	0.6			µs
		Gain = 4, 8	1.2			
Conversion Time	t_{CONV}	12 clocks	2.4			µs
Conversion Clock Frequency			0.1		5.0	MHz
ADC Supply Current (Note 3)		Normal operation mode, ADC converting at 234ksps		325		µA
		Fast power-down mode, ADC converting at 234ksps		210		
Aperture Delay	t_{AD}			30		ns

ELECTRICAL CHARACTERISTICS (continued)

(DV_{DD} = 1.8V to 3.6V, AV_{DD} = 2.7V to 5.5V, V_{REFDAC} = V_{REFADC} = 2.5V, external reference; 10µF capacitor at REFADC and REFDAC; 0.01µF capacitor at REFADJ; T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Aperture Jitter	t_{AJ}			50		ps
Sample Rate		Gain = 1, 2; DV_{DD} ≥ 2.7V, AV_{DD} ≥ 5.0V			312	ksps
		Gain = 4, 8; DV_{DD} ≥ 2.7V, AV_{DD} ≥ 5.0V			263	
		Gain = 1, 2			234	
		Gain = 4, 8			200	
Power-Supply Rejection	PSR	AV_{DD} = 2.7V to 5.5V, full-scale input		±0.06	±0.5	mV/V
Turn-On Time		Supply and reference have settled		1		µs
ADC DYNAMIC ACCURACY (10kHz sine wave, V_{IN} = 2.5V_{P-P}, f_{SAMPLE} = 234ksps, gain = 1)						
Signal-to-Noise Plus Distortion	SINAD			71		dB
Total Harmonic Distortion	THD	Up to the 5th harmonic		82		dB
Spurious-Free Dynamic Range	SFDR			84		dB
Channel-to-Channel Crosstalk				100		dB
Full-Power Bandwidth	FPBW	-3dB point		4		MHz
DAC (R_L = 5kΩ, C_L = 200pF, tested in unity gain, unless otherwise noted)						
Resolution			12			Bits
Differential Nonlinearity	DNL	Guaranteed monotonic (Note 4)			±1.0	LSB
Integral Nonlinearity	INL	(Note 4)		±1	±8	LSB
Offset Error		Code = 0x000 (tested at 0x032)		±2.5	±30	mV
Offset-Error Temperature Coefficient		Due to amplifier		±7		µV/°C
Gain Error		Code = 0xFFF		0	±5	% FS
Gain-Error Temperature Coefficient		Excluding reference drift		±7		ppm/°C
Output Voltage Range		No load	AGND		AV_{DD}	V
Output Slew Rate		C_L = 200pF		0.5		V/µs
Output Settling Time		Code = 0x400 to 0xC00 (Note 2)		4	10	µs
FB_ Input Bias Current		(Note 2)		±0.1	1	nA
FB_ Switch Resistance					200	Ω
FB_ Switch Turn-On/-Off Time				40		ns
FB_ Switch Off Isolation		f = 10kHz		100		dB
FB_ Switch Charge Injection				1		pC
DAC-to-DAC Crosstalk				0.5		nV-s
Short-Circuit Current		Sink		13		mA
		Source		50		
DC Output Impedance		Code = 0x800		0.8		Ω
Power-Up Time		0.5 LSB settling to 0x800		5		µs
Power-Supply Rejection	PSR	AV_{DD} = 2.7V to 5.5V		±1		mV/V
Charge-Pump Output Feedthrough		Code = 0x800, buffer on, R_L = 5kΩ, C_L = 200pF		100		$µV_{RMS}$

ELECTRICAL CHARACTERISTICS (continued)

(DV_{DD} = 1.8V to 3.6V, AV_{DD} = 2.7V to 5.5V, V_{REFDAC} = V_{REFADC} = 2.5V, external reference; 10µF capacitor at REFADC and REFDAC; 0.01µF capacitor at REFADJ; T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power-Down Output Leakage Current					±100	nA
Supply Current per DAC		No load (Note 3)		70		µA
INTERNAL REFERENCE (10µF capacitor at REFADC and REFDAC, 0.01µF capacitor at REFADJ)						
Output Voltage at REFADC and REFDAC		T_A = +25°C, AREF<1:0> = DREF<1:0> = 01	1.225	1.250	1.275	V
		T_A = +25°C, AREF<1:0> = DREF<1:0> = 10	2.007	2.048	2.089	
		T_A = +25°C, AREF<1:0> = DREF<1:0> = 11	2.450	2.500	2.550	
Output-Voltage Temperature		(Note 2)		±10	±75	ppm/°C
REFADC and REFDAC Output Short-Circuit Current		Source		40		mA
		Sink		13		
REFADC and REFDAC Line Regulation				±100	±600	µV/V
Load Regulation		I_{SOURCE} = 0µA to 500µA, T_A = +25°C			10	µV/µA
		I_{SINK} = 0µA to 80µA, T_A = +25°C			10	
Long-Term Stability		T_A = +25°C		±100		ppm/ 1000hrs
Turn-On Time		At REFADJ		2		ms
Turn-Off Time				100		ns
Reference Supply Current (Note 3)		Internal reference		445		µA
		REFADC buffer		270		
		REFDAC buffer		270		
EXTERNAL REFERENCE AT REFADJ						
External Reference Input Voltage Range		AREF<1:0> = DREF<1:0> = 11	1.225V		AV_{DD} - 0.1V	V
		AREF<1:0> = DREF<1:0> = 10	1.496V to AV_{DD} - 0.1V			
		AREF<1:0> = DREF<1:0> = 01	2.450V to AV_{DD} - 0.1V			
Input Resistance			50	75		kΩ
REFADC Buffer Gain		AREF<1:0> = 01		1		V/V
		AREF<1:0> = 10		0.8192		
		AREF<1:0> = 11		0.5		
REFDAC Buffer Gain		DREF<1:0> = 01		1		V/V
		DREF<1:0> = 10		0.8192		
		DREF<1:0> = 11		0.5		
Minimum Capacitive Bypass		REFADJ to AGND		10		nF

ELECTRICAL CHARACTERISTICS (continued)

(DV_{DD} = 1.8V to 3.6V, AV_{DD} = 2.7V to 5.5V, V_{REFDAC} = V_{REFADC} = 2.5V, external reference; 10µF capacitor at REFADC and REFDAC; 0.01µF capacitor at REFADJ; T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
EXTERNAL REFERENCE AT REFADC						
External Reference Input Voltage Range			AGND		AV_{DD}	V
REFADC Input Resistance			50	75		kΩ
REFADC Input Current		V_{REFADC} = 2.5V, 300ksps		30	40	µA
Turn-On Time		REFADC buffer, C_{REFADC} = 1µF		75		µs
Shutdown REFADC Input Current				0.01	1.0	µA
Minimum Capacitive Bypass		REFADC to AGND	10			µF
EXTERNAL REFERENCE AT REFDAC						
REFDAC Input Voltage Range			AGND		AV_{DD}	V
REFDAC Input Resistance		MAX1329	64	90	180	kΩ
		MAX1330	128	180	360	
REFDAC Input Current		MAX1329, V_{REFDAC} = 2.5V		28	86	µA
		MAX1330, V_{REFDAC} = 2.5V		14	43	
Turn-On Time		REFDAC buffer		75		µs
Shutdown REFDAC Input Current				0.1	1	µA
Minimum Capacitive Bypass		REFDAC to AGND	10			µF
MULTIPLEXER						
Absolute Input Voltage Range			AGND		AV_{DD}	V
Absolute Input Leakage Current		(AGND + 100mV) < $V_{AIN\_}$ < (AV_{DD} - 100mV) (Note 2)		±0.01	±1	nA
Input Capacitance		ADC gain = 1, 2		24		pF
		ADC gain = 4, 8		48		
On Resistance				340		Ω
INTERNAL TEMPERATURE SENSOR						
Internal Sensor Measurement Error (Note 5)		T_A = +25°C		±0.25		°C
		T_A = -40°C to +85°C			±3	
External Sensor Measurement Error (Note 5)		T_A = +25°C		±0.4		°C
		T_A = 0°C to +70°C		±2		
		T_A = -40°C to +85°C		±3		

ELECTRICAL CHARACTERISTICS (continued)

(DV_{DD} = 1.8V to 3.6V, AV_{DD} = 2.7V to 5.5V, V_{REFDAC} = V_{REFADC} = 2.5V, external reference; 10µF capacitor at REFADC and REFDAC; 0.01µF capacitor at REFADJ; T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Temperature Resolution		V_{REFADC} = 2.5V		1/8		°C/LSB
External-Diode Drive Ratio		$I_{DRIVEMIN}$ = 4µA, $I_{DRIVEMAX}$ = 68µA		17:1		
Temperature-Sensor Supply Current		Not including ADC current (Note 3)		100		µA
Temperature-Sensor Conversion Time		307 clocks per measurement, master clock = 5.00MHz		65		µs
CHARGE PUMP						
Input Voltage	DV_{DD}		1.8		3.6	V
No-Load Output Voltage	AV_{DD}	DV_{DD} = 1.8V to 3.0V, VM2CP<2:0> = 001	2.85	3.0	3.20	V
		DV_{DD} = 2.2V to 3.6V, VM2CP<2:0> = 010	3.75	4.0	4.30	
		DV_{DD} = 2.7V to 3.6V, VM2CP<2:0> = 011	4.80	5.0	5.40	
Output Current		Including internal current (Table 32)	25			mA
No-Load Supply Current		DV_{DD} = 2.7V, AV_{DD} = 4V, 39kHz clock		250		µA
Switching Frequency			39		78	kHz
Switch Turn-On/-Off Time		Between DV_{DD} to AV_{DD}, charge pump off		40		ns
Switch Impedance		Shorts DV_{DD} to AV_{DD}, charge pump off		25	50	Ω
Efficiency		25mA load, DV_{DD} = 1.8V, AV_{DD} = 3.0V, 39kHz clock		80		%
DV_{DD} VOLTAGE MONITOR (VM1)						
Supply Voltage Range			1.0		3.6	V
Trip Threshold (DV_{DD} Falling)	V_{DTH}	VM1<1:0> = 0x, $\overline{RST1}$ input	1.80	1.865	1.93	V
		VM1<1:0> = x0, $\overline{RST2}$ input	2.65	2.750	2.90	
Hysteresis	V_{DHYS}	VM1<1:0> = 0x, $\overline{RST1}$ input		15		mV
		VM1<1:0> = x0, $\overline{RST2}$ input		22.5		
Reset Timeout Period		V_{DVDD} = V_{DTH} + V_{DHYS}		170		ms
Turn-On Time		DV_{DD} = 1.8V, enabled by VM1 <1:0>		2		ms
AV_{DD} VOLTAGE MONITOR (VM2)						
Supply Voltage Range			1.0		5.5	V
Trip Threshold (AV_{DD} Falling) (Note 6)	V_{ATH}	VM2CP<1:0> = 01	2.53	2.775	2.975	V
		VM2CP<1:0> = 10	3.4	3.700	3.925	
		VM2CP<1:0> = 11	4.25	4.625	4.925	
Hysteresis	V_{AHYS}	VM2CP<1:0> = 01		22.5		mV
		VM2CP<1:0> = 10		30		
		VM2CP<1:0> = 11		37.5		

ELECTRICAL CHARACTERISTICS (continued)

(DV_{DD} = 1.8V to 3.6V, AV_{DD} = 2.7V to 5.5V, V_{REFDAC} = V_{REFADC} = 2.5V, external reference; 10µF capacitor at REFADC and REFDAC; 0.01µF capacitor at REFADJ; T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Turn-On Time		AV_{DD} = 2.7V, enabled by VM2CP<1:0>		2		ms
INTERNAL OSCILLATOR						
Clock Frequency		T_A = T_{MIN} to T_{MAX}	3.5758	3.6864	3.7970	MHz
Turn-Off Delay		Using clock at CLKIO pin, ODLY = 1		1024		Clocks
Turn-On Time				200		ns
Supply Current		(Note 7)		120		µA
SWITCHES (SPDT)						
On Resistance		AV_{DD} = 2.7V to 5.5V		140	200	Ω
		AV_{DD} = 4.5V to 5.5V		90	120	
On-Resistance Match				15		Ω
On-Resistance Flatness		Over analog voltage range		12		Ω
Analog Voltage Range			AGND		AV_{DD}	V
Turn-On/-Off Time		Break-before-make for SPDT configuration		50		ns
Leakage Current		AGND + 100mV < $V_{SN\_}$ < AV_{DD} - 100mV (Note 2)		0.08	±1	nA
Off Isolation		f = 10kHz		100		dB
Charge Injection				1		pC
Input Capacitance				2		pF
OPERATIONAL AMPLIFIER (R_L = 10kΩ, C_L = 200pF)						
Input Bias Current		(Note 2)		0.3	±1	nA
Input Offset Voltage	V_{OS}			2	±20	mV
Input Offset Drift	ΔV_{OS}			±10		µV/°C
Common-Mode Rejection Ratio	CMRR	AGND + 100mV < V_{CM} < AV_{DD} - 100mV		75		dB
Phase Margin				60		degrees
Charge-Pump Output Feedthrough				100		μV_{P-P}
Common-Mode Input Voltage Range			AGND		AV_{DD}	V
Output Voltage Range		No load	AGND		AV_{DD}	V
		10kΩ load	0.1		AV_{DD} - 0.1	
		100kΩ load	0.1		AV_{DD} - 0.1	
Gain Bandwidth Product				1		MHz
Slew Rate				0.5		V/µs
OSW_ Switch Resistance		AV_{DD} = 2.7V to 5.5V		140	200	Ω
		AV_{DD} = 4.5V to 5.5V		90	120	
OSW_ Switch Turn-On/-Off Time				50		ns

ELECTRICAL CHARACTERISTICS (continued)

(DV_{DD} = 1.8V to 3.6V, AV_{DD} = 2.7V to 5.5V, V_{REFDAC} = V_{REFADC} = 2.5V, external reference; 10µF capacitor at REFADC and REFDAC; 0.01µF capacitor at REFADJ; T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OSW_ Switch Charge Injection				1		pC
Input Noise Voltage Density		$f_{IN\_}$ = 1kHz		330		nV/√Hz
Input Noise Voltage		$f_{IN\_}$ = 0.1Hz to 10Hz		9		μV_{RMS}
Power-Down Output Leakage					±10	nA
Power-Supply Rejection Ratio		AV_{DD} = 2.7V to 5.5V	65	100		dB
Supply Current per Amplifier		(Note 3)		70		µA
Turn-On Time				5		µs
Short-Circuit Current		Source		50		mA
		Sink		13		
DC Output Impedance		A_V = 1V/V		0.2		Ω
DIGITAL INPUTS (DIN, SCLK, $\overline{CS}$)						
Input High Voltage	V_{IH}		0.7 x DV_{DD}			V
Input Low Voltage	V_{IL}				0.3 x DV_{DD}	V
Input Hysteresis		DV_{DD} = 3V		200		mV
Input Leakage Current		V_{IN} = 0 or DV_{DD}		±0.01	±10	µA
DIGITAL OUTPUTS (DOUT, $\overline{RST1}$, $\overline{RST2}$)						
Output Low Voltage	V_{OL}	I_{SINK} = 1mA, DV_{DD} = 2.7V to 3.6V			0.4	V
		I_{SINK} = 200µA, DV_{DD} = 1.8V to 3.6V			0.4	
Output High Voltage	V_{OH}	I_{SOURCE} = 0.2mA, DV_{DD} = 2.7V to 3.6V	0.8 x DV_{DD}			V
		I_{SOURCE} = 100µA, DV_{DD} = 1.8V to 3.6V	0.8 x DV_{DD}			
DOUT Three-State Leakage				±0.01	±10	µA
DOUT Three-State Capacitance		(Note 2)			15	pF
$\overline{RST1}$, $\overline{RST2}$ Open-Drain Output Low Voltage		I_{SINK} = 1mA, DV_{DD} = 2.7V to 3.6V			0.4	V
		I_{SINK} = 200µA, DV_{DD} = 1.8V to 3.6V			0.4	
$\overline{RST1}$, $\overline{RST2}$ Open-Drain Output Leakage Current		(Note 2)		0.13	100	nA
DIGITAL I/O (DPIO1–DPIO4, CLKIO)						
Output Low Voltage		I_{SINK} = 2mA, DV_{DD} = 2.7V to 3.6V			0.4	V
		I_{SINK} = 1mA, DV_{DD} = 1.8V to 3.6V			0.4	
Output High Voltage		I_{SOURCE} = 2mA, DV_{DD} = 2.7V to 3.6V	0.8 x DV_{DD}			V
		I_{SOURCE} = 1mA, DV_{DD} = 1.8V to 3.6V	0.8 x DV_{DD}			

ELECTRICAL CHARACTERISTICS (continued)

(DV_{DD} = 1.8V to 3.6V, AV_{DD} = 2.7V to 5.5V, V_{REFDAC} = V_{REFADC} = 2.5V, external reference; 10µF capacitor at REFADC and REFDAC; 0.01µF capacitor at REFADJ; T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage			0.7 x DV_{DD}			V
Input Low Voltage		DPIO1–DPIO4			0.3 x DV_{DD}	V
		CLKIO			0.25 x DV_{DD}	
Input Hysteresis		DV_{DD} = 3V		110		mV
Three-State Leakage				±0.01	±1	µA
Three-State Capacitance		(Note 2)			15	pF
DPIO_ Pullup Resistance				0.5		MΩ
ANALOG I/O (APIO1–APIO4)						
Output Low Voltage		I_{SINK} = 2mA, AV_{DD} = 2.7V to 5.5V			0.4	V
		I_{SINK} = 1mA, AV_{DD} = 1.8V to 5.5V			0.4	
Output High Voltage		I_{SOURCE} = 2mA, AV_{DD} = 2.7V to 5.5V	0.8 x AV_{DD}			V
		I_{SOURCE} = 1mA, AV_{DD} = 1.8V to 5.5V	0.8 x AV_{DD}			
Input High Voltage		AV_{DD} = 2.7V to 5.5V	0.7 x AV_{DD}			V
		AV_{DD} = DV_{DD} = 1.8V to 3.6V	0.7 x AV_{DD}			
Input Low Voltage		AV_{DD} = 2.7V to 5.5V			0.3 x AV_{DD}	V
		AV_{DD} = DV_{DD} = 1.8V to 3.6V			0.3 x AV_{DD}	
Input Hysteresis		AV_{DD} = 3V		120		mV
		AV_{DD} = 5V		160		
Three-State Leakage				±0.01	±10	µA
Three-State Capacitance		(Note 2)			15	pF
Pullup Resistance				0.5		MΩ
POWER REQUIREMENTS						
DV_{DD} Supply Voltage Range			1.8		3.6	V
AV_{DD} Supply Voltage Range			2.7		5.5	V
Supply Current (Note 8)		Run (all on, except charge pump)		3.75	7.5	mA
		Sleep (1.8V or 2.7V monitor on)		1	2.5	µA
Shutdown Current		All off		0.5	1	µA

12-/16-Bit DASs with ADC, DACs, DPIOs, APIOs, Reference, Voltage Monitors, and Temp Sensor

TIMING CHARACTERISTICS

(DV_{DD} = 1.8V to 3.6V, AV_{DD} = 2.7V to 5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SERIAL-INTERFACE TIMING PARAMETERS (DV_{DD} = 2.7V to 3.6V) (Figures 1 and 2)						
SCLK Operating Frequency	f_{OP}		0		20	MHz
SCLK Cycle Time	t_{CYC}		50			ns
DIN to SCLK Setup	t_{DS}		15			ns
DIN to SCLK Hold	t_{DH}		0			ns
SCLK Fall to Output Data Valid	t_{DO}				20	ns
$\overline{CS}$ Fall to Output Enable	t_{DV}				24	ns
$\overline{CS}$ Rise to Output Disable	t_{TR}				24	ns
$\overline{CS}$ to SCLK Rise Setup	t_{CSS}		15			ns
$\overline{CS}$ to SCLK Rise Hold	t_{CSH}		0			ns
SCLK Pulse-Width High	t_{CH}		20			ns
SCLK Pulse-Width Low	t_{CL}		20			ns
SERIAL-INTERFACE TIMING PARAMETERS (DV_{DD} = 1.8V to 3.6V) (Figures 1 and 2)						
SCLK Operating Frequency	f_{OP}		0		10	MHz
SCLK Cycle Time	t_{CYC}		100			ns
DIN to SCLK Setup	t_{DS}		30			ns
DIN to SCLK Hold	t_{DH}		0			ns
SCLK Fall to Output Data Valid	t_{DO}				40	ns
$\overline{CS}$ Fall to Output Enable	t_{DV}				48	ns
$\overline{CS}$ Rise to Output Disable	t_{TR}				48	ns
$\overline{CS}$ to SCLK Rise Setup	t_{CSS}		30			ns
$\overline{CS}$ to SCLK Rise Hold	t_{CSH}		0			ns
SCLK Pulse-Width High	t_{CH}		40			ns
SCLK Pulse-Width Low	t_{CL}		40			ns
DIGITAL PROGRAMMABLE I/O TIMING PARAMETERS (DPIO1–DPIO4, DV_{DD} = 2.7V to 3.6V, C_L = 20pF)						
SPI Write to DPIO Output Valid	t_{SD}	From last SCLK rising edge			50	ns
DPIO Rise/Fall Input to Interrupt Asserted Delay	t_{DI}	Interrupt programmed on $\overline{RST1}$ and/or $\overline{RST2}$, corresponding status bits unmasked			55	ns
DPIO Input to Analog Block Delay	t_{DA}	When controlling ADC, DACs, or switches		40		ns
DIGITAL PROGRAMMABLE I/O TIMING PARAMETERS (DPIO1–DPIO4, DV_{DD} = 1.8V to 3.6V, C_L = 20pF)						
SPI Write to DPIO Output Valid	t_{SD}	From last SCLK rising edge			100	ns
DPIO Rise/Fall Input to Interrupt Asserted Delay	t_{DI}	Interrupt programmed on $\overline{RST1}$ and/or $\overline{RST2}$, corresponding status bits unmasked			150	ns
DPIO Input to Analog Block Delay	t_{DA}	When controlling ADC, DACs, or switches		50		ns
ANALOG PROGRAMMABLE I/O TIMING PARAMETERS (APIO1–APIO4, DV_{DD} = 2.7V to 3.6V, AV_{DD} = 2.7V to 5.5V, C_L = 20pF)						
SPI Write to APIO Output Valid	t_{SD}	From last SCLK rising edge			50	ns
APIO Rise/Fall Input to Interrupt Asserted Delay	t_{DI}	Interrupt programmed on $\overline{RST1}$ and/or $\overline{RST2}$, corresponding status bits unmasked			50	ns
$\overline{CS}$ to APIO4 Propagation Delay	t_{DCA}	AP4MD<1:0> = 11			35	ns

TIMING CHARACTERISTICS (continued)

(DV_{DD} = 1.8V to 3.6V, AV_{DD} = 2.7V to 5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLK to APIO3 Propagation Delay	t_{DSA}	AP3MD<1:0> = 11, $\overline{CS}$ is high			30	ns
DIN to APIO2 Propagation Delay	t_{DDA}	AP2MD<1:0> = 11, $\overline{CS}$ is high			25	ns
APIO1 to DOUT Propagation Delay	t_{DAD}	AP1MD<1:0> = 11, $\overline{CS}$ is high			20	ns
SPI-Mode Propagation Delay Matching	t_{DM}	Among APIO4, APIO3, APIO2, and APIO1			±10	ns
ANALOG PROGRAMMABLE I/O TIMING PARAMETERS (APIO1–APIO4, DV_{DD} = 1.8V to 3.6V, AV_{DD} = 2.7V to 5.5V, C_L = 20pF)						
SPI Write to APIO Output Valid	t_{SD}	From last SCLK rising edge			100	ns
APIO Rise/Fall Input to Interrupt Asserted Delay	t_{DI}	Interrupt programmed on $\overline{RST1}$ and/or $\overline{RST2}$, corresponding status bits unmasked			175	ns
$\overline{CS}$ to APIO4 Propagation Delay	t_{DCA}	AP4MD<1:0> = 11			60	ns
SCLK to APIO3 Propagation Delay	t_{DSA}	AP3MD<1:0> = 11, $\overline{CS}$ is high			50	ns
DIN to APIO2 Propagation Delay	t_{DDA}	AP2MD<1:0> = 11, $\overline{CS}$ is high			50	ns
APIO1 to DOUT Propagation Delay	t_{DAD}	AP1MD<1:0> = 11, $\overline{CS}$ is high			80	ns
SPI-Mode Propagation Delay Matching	t_{DM}	Among APIO4, APIO3, APIO2, and APIO1			±30	ns

Note 1: ADC INL and DNL, offset, and gain are tested at DV_{DD} = 1.8V, AV_{DD} = 2.7V, f_{SAMPLE} = 234ksps to guarantee performance at f_{SAMPLE} = 312ksps, $DV_{DD} \geq$ 2.7V and $AV_{DD} \geq$ 5.0V.

Note 2: Guaranteed by design. Not production tested.

Note 3: AV_{DD} supply current contribution for this module.

Note 4: DNL and INL are measured between code 115 and 4095.

Note 5: Temperature sensor accuracy is tested using a 2.5084V reference applied to REFADJ.

Note 6: The maximum trip levels for the AV_{DD} monitor are 5% below the typical charge-pump output value. The charge-pump output voltage and the trip thresholds track to prevent tripping at -5% below the typical charge-pump output value.

Note 7: DV_{DD} supply current contribution for this module.

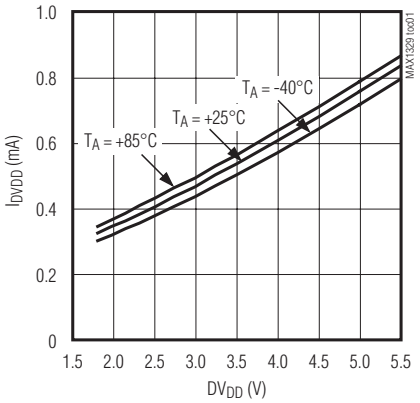
Note 8: The normal operation and sleep mode supply currents are measured with no load on DOUT, SCLK idle, and all digital inputs at DGND or DV_{DD}. CLKIO runs in normal mode operation and idle in sleep mode.

12-/16-Bit DASs with ADC, DACs, DPIOs, APIOs, Reference, Voltage Monitors, and Temp Sensor

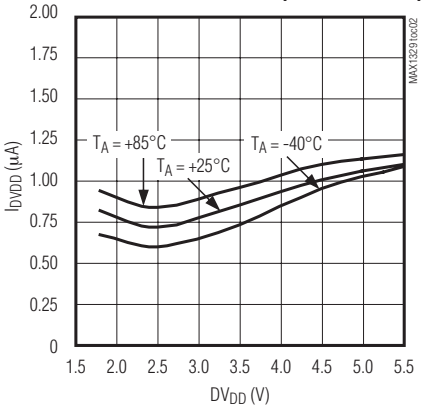
Typical Operating Characteristics

(AV_{DD} = 5.0V, V_{REFADC} = V_{REFDAC} = 2.5V for DV_{DD} = 3.0V; T_A = +25°C, unless otherwise noted.)

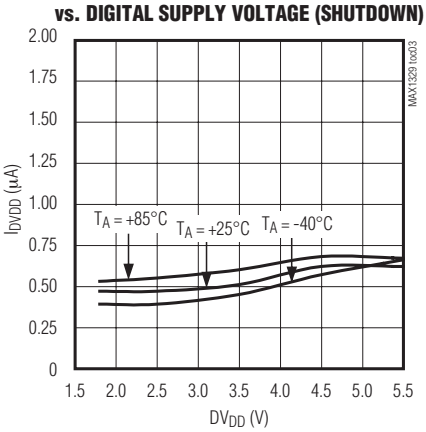
STATIC DIGITAL SUPPLY CURRENT vs. DIGITAL SUPLY VOLTAGE (EVERYTHING ON)



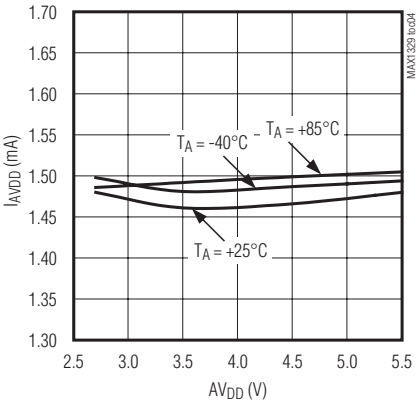
STATIC DIGITAL SUPPLY CURRENT vs. DIGITAL SUPPLY VOLTAGE (ONLY VM1A ON)



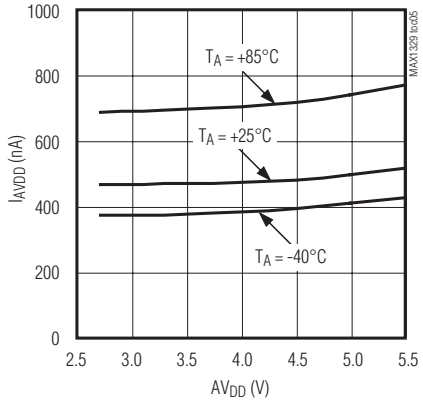
STATIC DIGITAL SUPPLY CURRENT vs. DIGITAL SUPPLY VOLTAGE (SHUTDOWN)



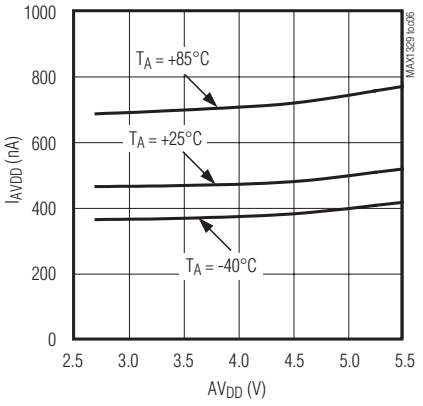
STATIC ANALOG SUPPLY CURRENT vs. ANALOG SUPPLY VOLTAGE (EVERYTHING ON)



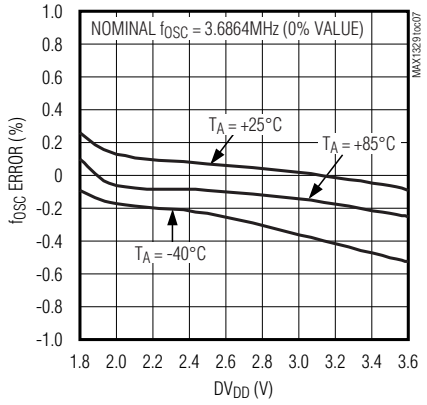
STATIC ANALOG SUPPLY CURRENT vs. ANALOG SUPPLY VOLTAGE (ONLY VM1A AND VM1B ON)



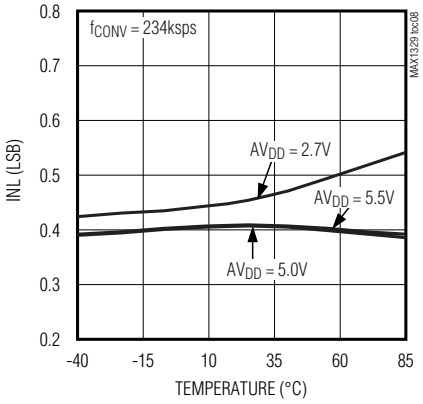
STATIC ANALOG SUPPLY CURRENT vs. ANALOG SUPPLY VOLTAGE (SHUTDOWN)



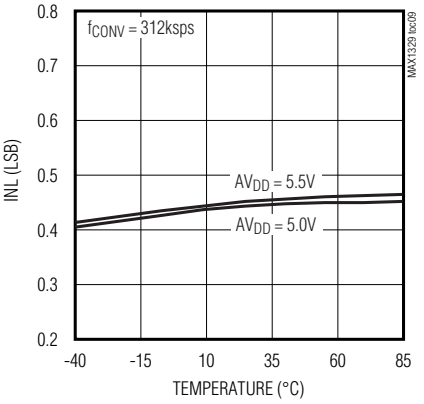
f_{OSC} ERROR vs. DIGITAL SUPPLY VOLTAGE



ADC INTEGRAL NONLINEARITY vs. TEMPERATURE



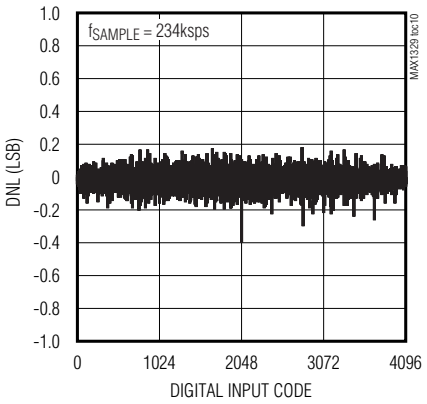
ADC INTEGRAL NONLINEARITY vs. TEMPERATURE



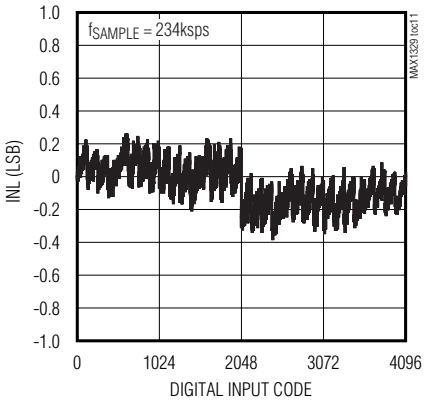
Typical Operating Characteristics (continued)

(AV_{DD} = 5.0V, V_{REFADC} = V_{REFDAC} = 2.5V for DV_{DD} = 3.0V; T_A = +25°C, unless otherwise noted.)

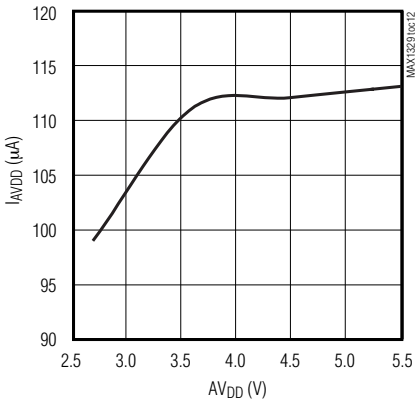
ADC DIFFERENTIAL NONLINEARITY vs. DIGITAL INPUT CODE (AV_{DD} = 3.0V)



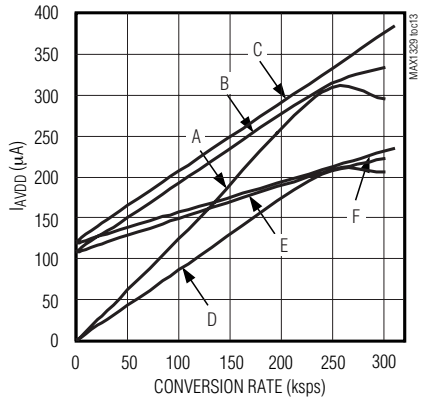
ADC INTEGRAL NONLINEARITY vs. DIGITAL INPUT CODE (AV_{DD} = 3.0V)



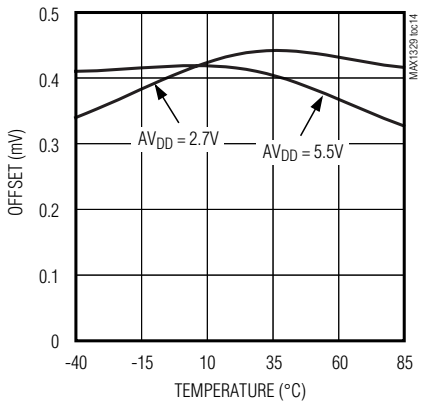
ADC SUPPLY CURRENT vs. ANALOG SUPPLY VOLTAGE



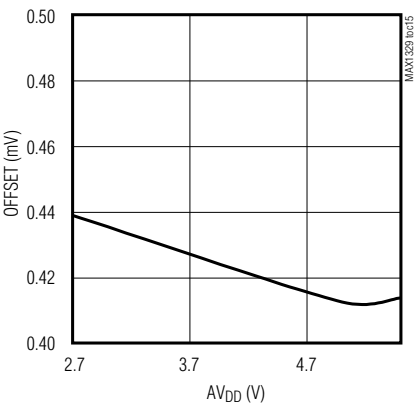
ADC SUPPLY CURRENT vs. CONVERSION RATE



ADC OFFSET VOLTAGE vs. TEMPERATURE



ADC OFFSET ERROR vs. SUPPLY VOLTAGE



A = FAST POWER-DOWN
AV_{DD} = 5V, V_{REFDAC} = 2.5V

B = NORMAL MODE
AV_{DD} = 5V, V_{REFDAC} = 2.5V

C = BURST MODE
AV_{DD} = 5V, V_{REFDAC} = 2.5V

D = FAST POWER-DOWN
AV_{DD} = 3V, V_{REFADC} = 1.25V

E = NORMAL MODE
AV_{DD} = 3V, V_{REFADC} = 1.25V

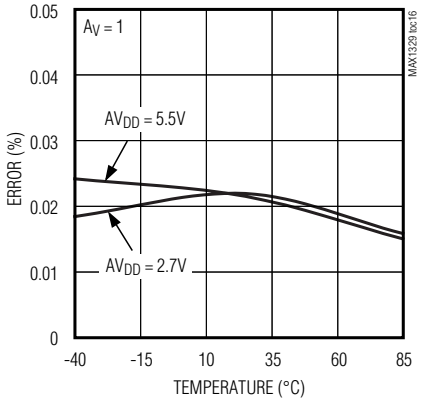
F = BURST MODE
AV_{DD} = 3V, V_{REFADC} = 1.25V

12-/16-Bit DASs with ADC, DACs, DPIOs, APIOs, Reference, Voltage Monitors, and Temp Sensor

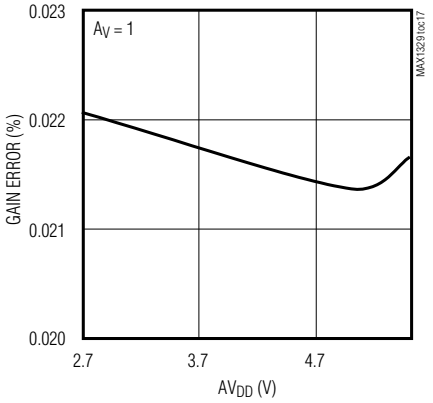
Typical Operating Characteristics (continued)

(AV_{DD} = 5.0V, V_{REFADC} = V_{REFDAC} = 2.5V for DV_{DD} = 3.0V; T_A = +25°C, unless otherwise noted.)

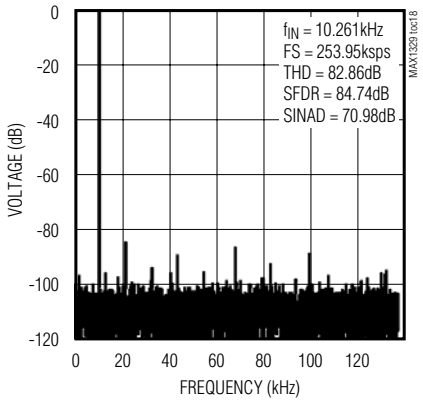
ADC GAIN ERROR vs. TEMPERATURE



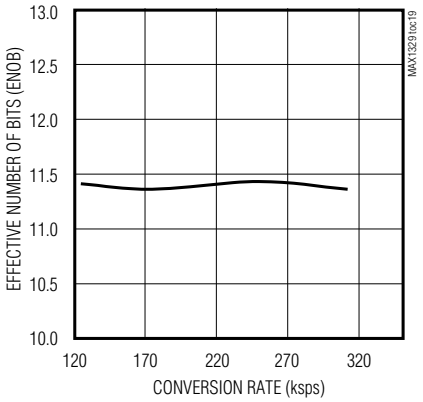
ADC GAIN ERROR vs. SUPPLY VOLTAGE



ADC 4096-POINT FFT PLOT



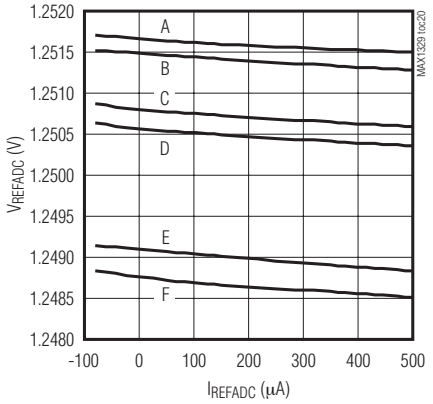
ADC ENOB vs. FREQUENCY



Typical Operating Characteristics (continued)

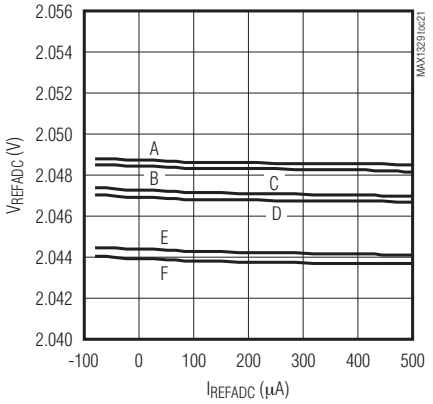
(AV_{DD} = 5.0V, V_{REFADC} = V_{REFDAC} = 2.5V for DV_{DD} = 3.0V; T_A = +25°C, unless otherwise noted.)

ADC REFERENCE VOLTAGE (1.25V) vs. LOAD CURRENT



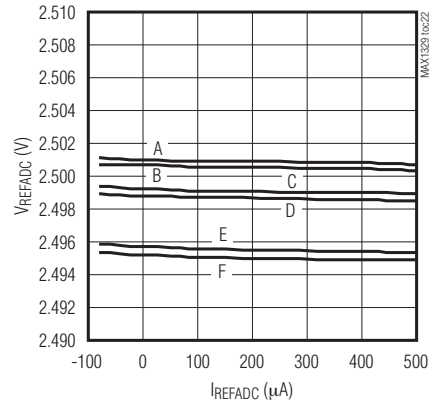
A: T_A = -40°C, AV_{DD} = 5V, DV_{DD} = 3V
B: T_A = -40°C, AV_{DD} = 3V, DV_{DD} = 2V
C: T_A = +25°C, AV_{DD} = 5V, DV_{DD} = 3V
D: T_A = +25°C, AV_{DD} = 3V, DV_{DD} = 2V
E: T_A = +85°C, AV_{DD} = 5V, DV_{DD} = 3V
F: T_A = +85°C, AV_{DD} = 3V, DV_{DD} = 2V

ADC REFERENCE VOLTAGE (2.048V) vs. LOAD CURRENT



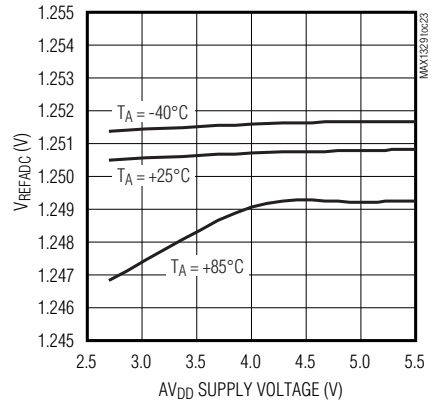
A: T_A = -40°C, AV_{DD} = 5V, DV_{DD} = 3V
B: T_A = -40°C, AV_{DD} = 3V, DV_{DD} = 2V
C: T_A = +25°C, AV_{DD} = 5V, DV_{DD} = 3V
D: T_A = +25°C, AV_{DD} = 3V, DV_{DD} = 2V
E: T_A = +85°C, AV_{DD} = 5V, DV_{DD} = 3V
F: T_A = +85°C, AV_{DD} = 3V, DV_{DD} = 2V

ADC REFERENCE VOLTAGE (2.5V) vs. LOAD CURRENT



A: T_A = -40°C, AV_{DD} = 5V, DV_{DD} = 3V
B: T_A = -40°C, AV_{DD} = 3V, DV_{DD} = 2V
C: T_A = +25°C, AV_{DD} = 5V, DV_{DD} = 3V
D: T_A = +25°C, AV_{DD} = 3V, DV_{DD} = 2V
E: T_A = +85°C, AV_{DD} = 5V, DV_{DD} = 3V
F: T_A = +85°C, AV_{DD} = 3V, DV_{DD} = 2V

ADC REFERENCE VOLTAGE (1.25V) vs. ANALOG SUPPLY VOLTAGE

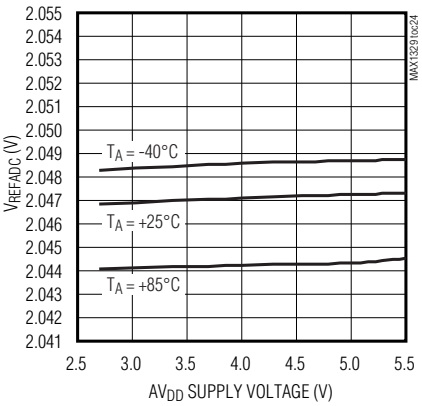


12-/16-Bit DASs with ADC, DACs, DPIOs, APIOs, Reference, Voltage Monitors, and Temp Sensor

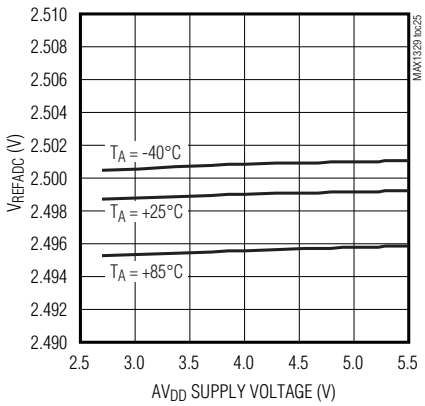
Typical Operating Characteristics (continued)

(AV_{DD} = 5.0V, V_{REFADC} = V_{REFDAC} = 2.5V for DV_{DD} = 3.0V; T_A = +25°C, unless otherwise noted.)

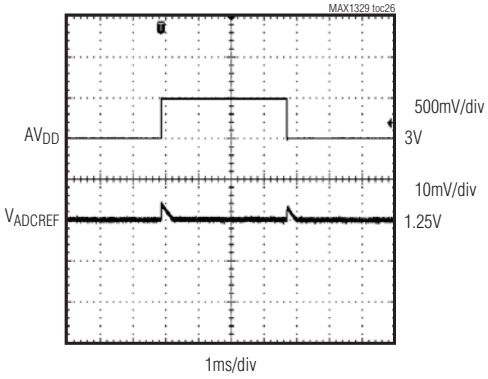
ADC REFERENCE VOLTAGE (2.048V) vs. ANALOG SUPPLY VOLTAGE



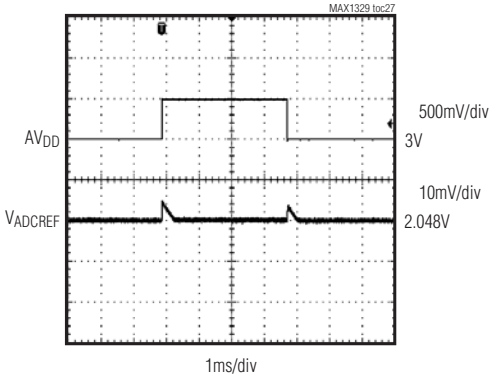
ADC REFERENCE VOLTAGE (2.5V) vs. ANALOG SUPPLY VOLTAGE



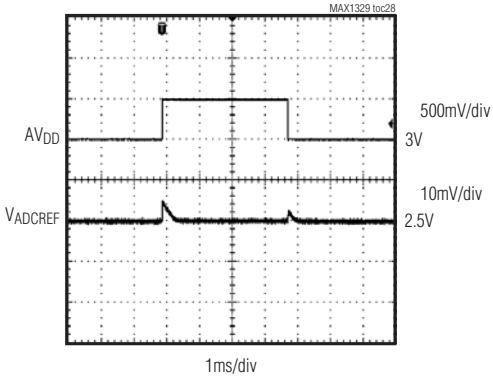
ADC REFERENCE LINE TRANSIENT (V_{ADCREF} = +1.25V)



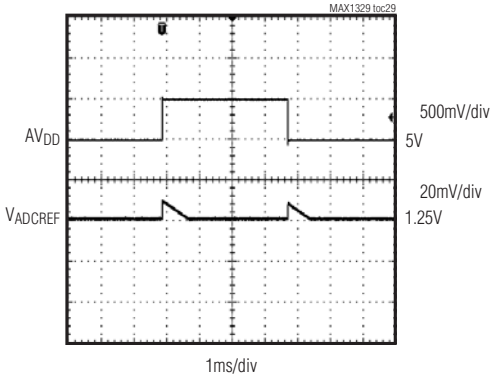
ADC REFERENCE LINE TRANSIENT (V_{ADCREF} = +2.048V)



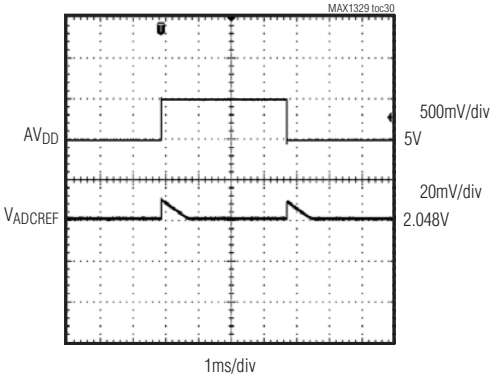
ADC REFERENCE LINE TRANSIENT (V_{ADCREF} = +2.5V)



ADC REFERENCE LINE TRANSIENT (V_{ADCREF} = +1.25V)



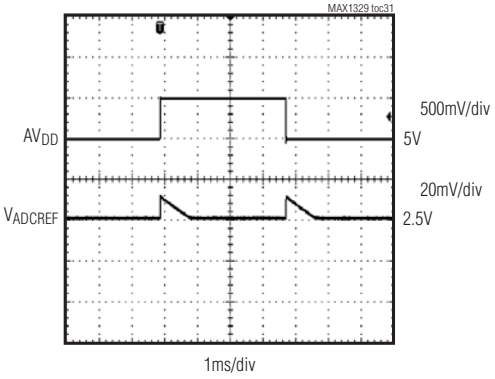
ADC REFERENCE LINE TRANSIENT (V_{ADCREF} = +2.048V)



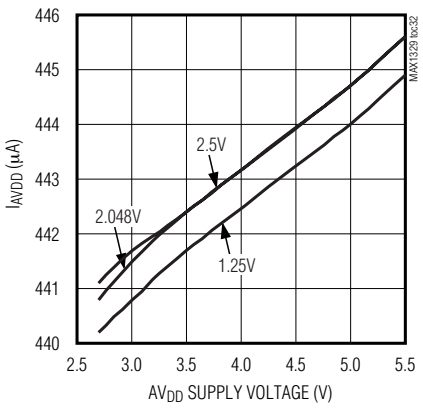
Typical Operating Characteristics (continued)

(AV_{DD} = 5.0V, V_{REFADC} = V_{REFDAC} = 2.5V for DV_{DD} = 3.0V; T_A = +25°C, unless otherwise noted.)

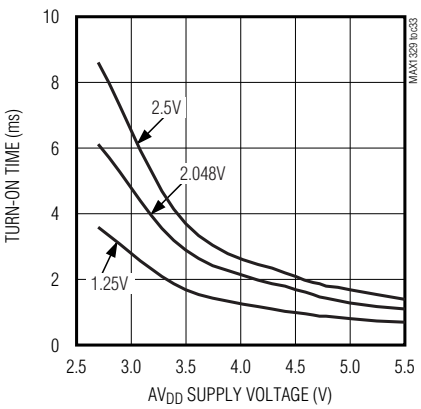
ADC REFERENCE LINE TRANSIENT (V_{ADCREF} = +2.5V)



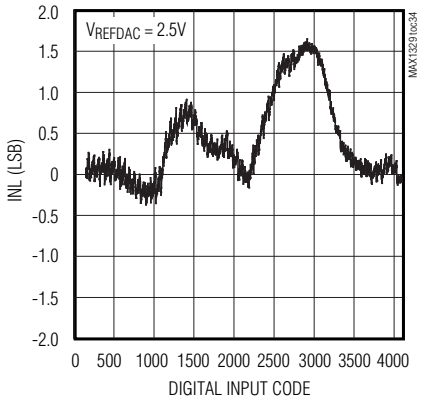
ADC REFERENCE SUPPLY CURRENT vs. ANALOG SUPPLY VOLTAGE



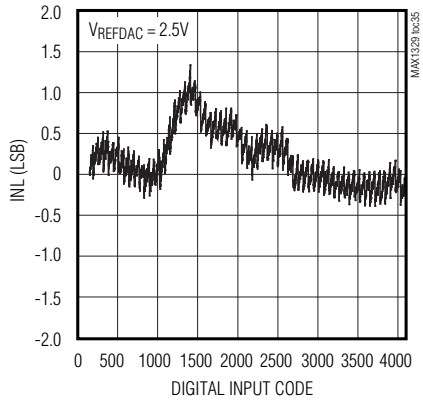
ADC REFERENCE TURN-ON TIME vs. ANALOG SUPPLY VOLTAGE



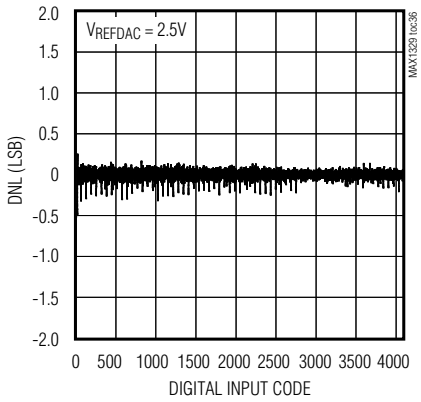
DAC INTEGRAL NONLINEARITY vs. DIGITAL INPUT CODE (AV_{DD} = 3V)



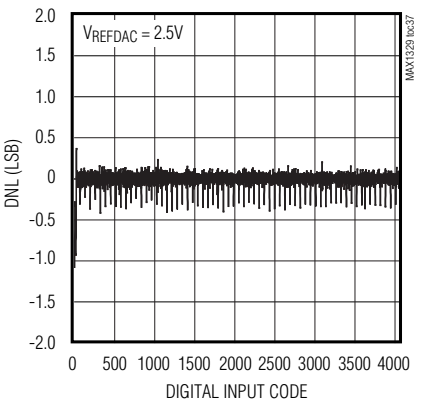
DAC INTEGRAL NONLINEARITY vs. DIGITAL INPUT CODE (AV_{DD} = 5V)



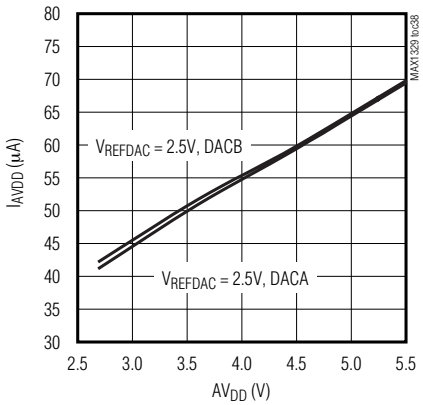
DAC DIFFERENTIAL NONLINEARITY vs. DIGITAL INPUT CODE (AV_{DD} = 3V)



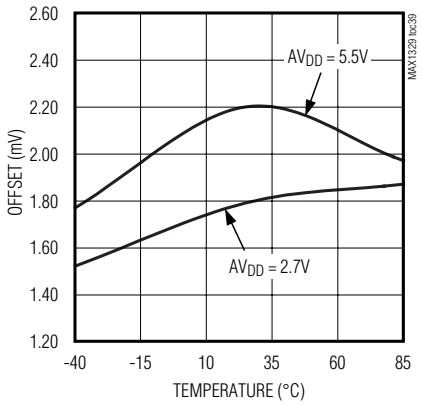
DAC DIFFERENTIAL NONLINEARITY vs. DIGITAL INPUT CODE (AV_{DD} = 5V)



DAC SUPPLY CURRENT vs. ANALOG SUPPLY VOLTAGE



DAC OFFSET VOLTAGE vs. TEMPERATURE

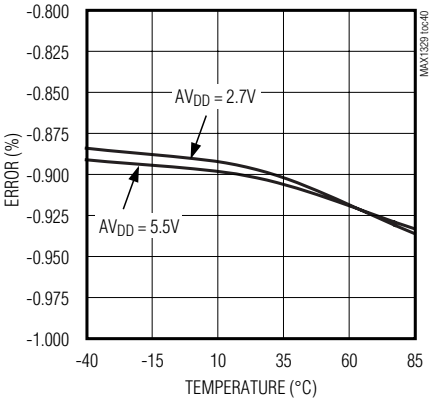


12-/16-Bit DASs with ADC, DACs, DPIOs, APIOs, Reference, Voltage Monitors, and Temp Sensor

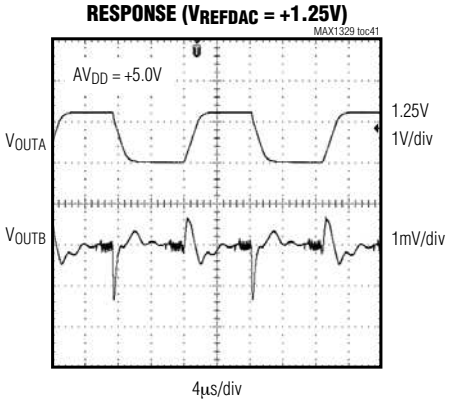
Typical Operating Characteristics (continued)

(AV_{DD} = 5.0V, V_{REFADC} = V_{REFDAC} = 2.5V for DV_{DD} = 3.0V; T_A = +25°C, unless otherwise noted.)

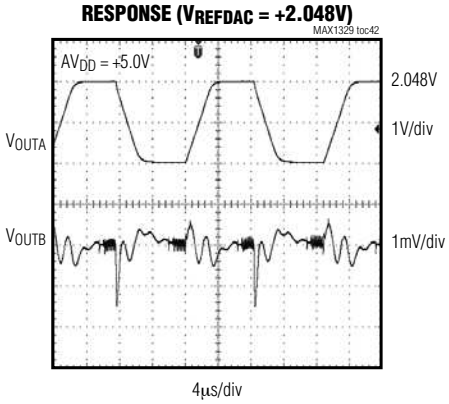
DAC GAIN ERROR vs. TEMPERATURE



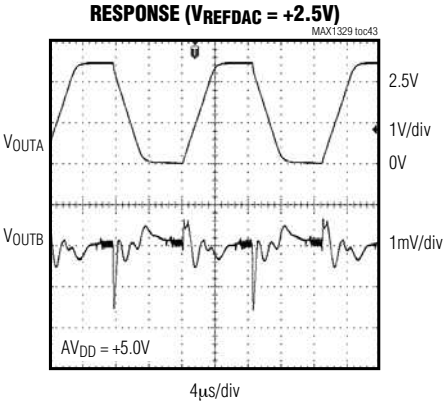
DAC SLEW RATE/CROSSTALK TRANSIENT RESPONSE (V_{REFDAC} = +1.25V)



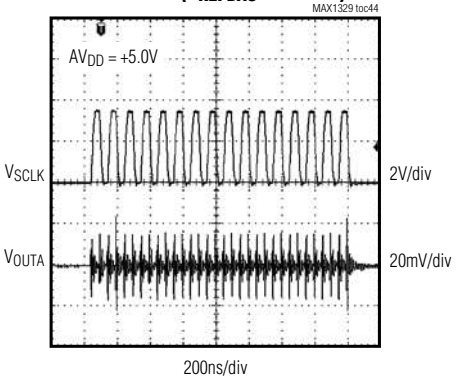
DAC SLEW RATE/CROSSTALK TRANSIENT RESPONSE (V_{REFDAC} = +2.048V)



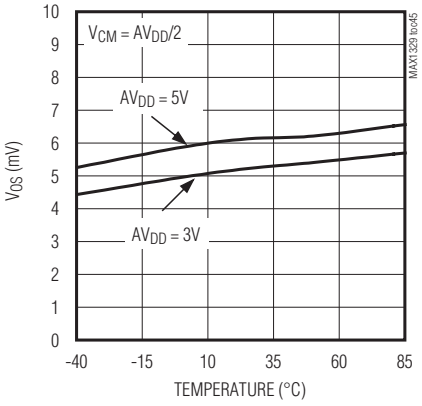
DAC SLEW RATE/CROSSTALK TRANSIENT RESPONSE (V_{REFDAC} = +2.5V)



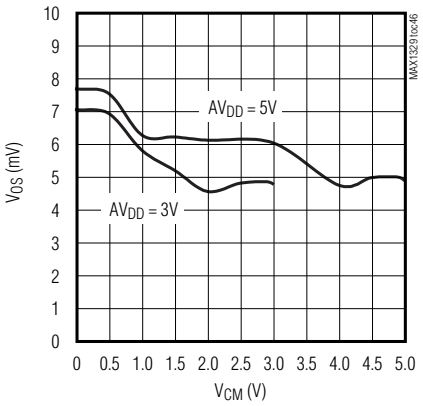
DAC DIGITAL FEEDTHROUGH TRANSIENT RESPONSE (V_{REFDAC} = +2.50V)



OP-AMP INPUT OFFSET VOLTAGE vs. TEMPERATURE



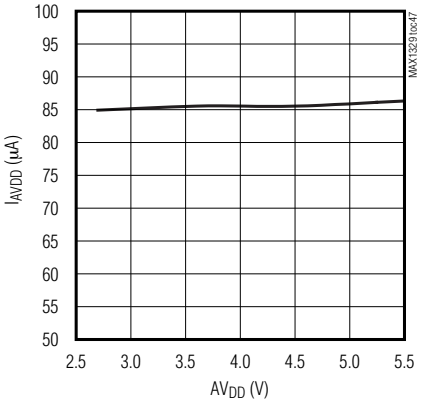
OP-AMP INPUT OFFSET VOLTAGE vs. COMMON-MODE VOLTAGE



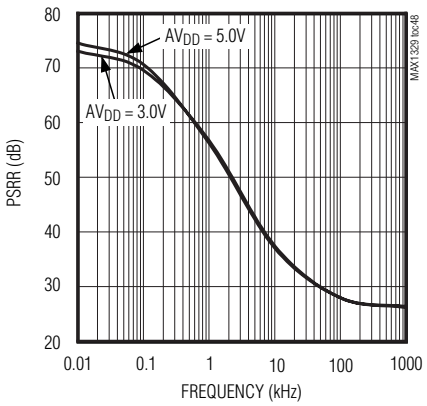
Typical Operating Characteristics (continued)

(AV_{DD} = 5.0V, V_{REFADC} = V_{REFDAC} = 2.5V for DV_{DD} = 3.0V; T_A = +25°C, unless otherwise noted.)

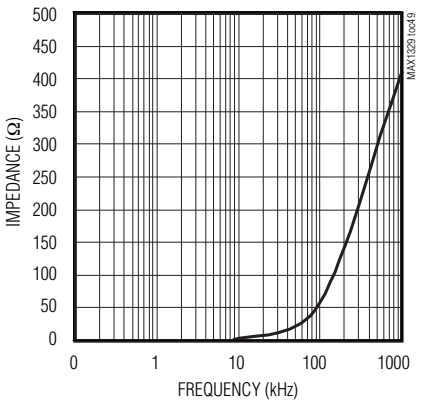
OP-AMP SUPPLY CURRENT vs. ANALOG SUPPLY VOLTAGE



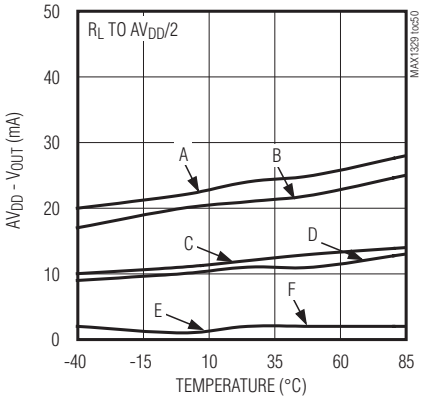
OP-AMP PSRR vs. FREQUENCY



OP-AMP OUTPUT IMPEDANCE vs. FREQUENCY

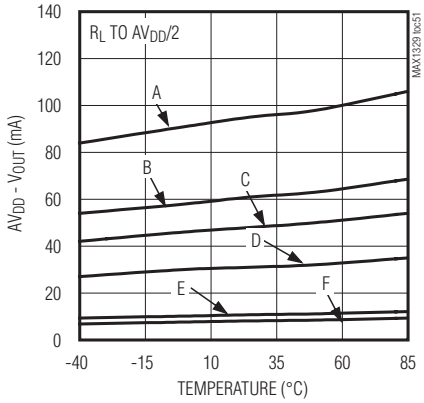


OP-AMP MAXIMUM OUTPUT VOLTAGE vs. TEMPERATURE



A: = R_L = 5kΩ, AV_{DD} = 5V, DV_{DD} = 3V B: = R_L = 5kΩ, AV_{DD} = 3V, DV_{DD} = 2V
C: = R_L = 10kΩ, AV_{DD} = 5V, DV_{DD} = 3V D: = R_L = 10kΩ, AV_{DD} = 3V, DV_{DD} = 2V
E: = R_L = 100kΩ, AV_{DD} = 5V, DV_{DD} = 3V F: = R_L = 100kΩ, AV_{DD} = 3V, DV_{DD} = 2V

OP-AMP MAXIMUM OUTPUT VOLTAGE vs. TEMPERATURE



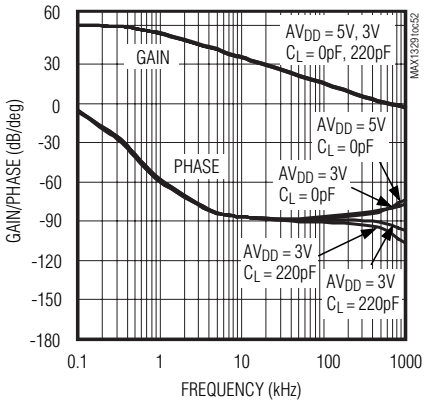
A: = R_L = 5kΩ, AV_{DD} = 5V, DV_{DD} = 3V B: = R_L = 5kΩ, AV_{DD} = 3V, DV_{DD} = 2V
C: = R_L = 10kΩ, AV_{DD} = 5V, DV_{DD} = 3V D: = R_L = 10kΩ, AV_{DD} = 3V, DV_{DD} = 2V
E: = R_L = 100kΩ, AV_{DD} = 5V, DV_{DD} = 3V F: = R_L = 100kΩ, AV_{DD} = 3V, DV_{DD} = 2V

12-/16-Bit DASs with ADC, DACs, DPIOs, APIOs, Reference, Voltage Monitors, and Temp Sensor

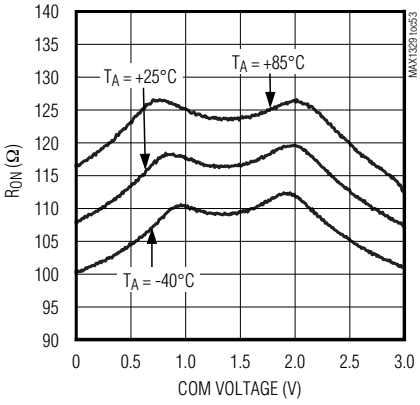
Typical Operating Characteristics (continued)

(AV_{DD} = 5.0V, V_{REFADC} = V_{REFDAC} = 2.5V for DV_{DD} = 3.0V; T_A = +25°C, unless otherwise noted.)

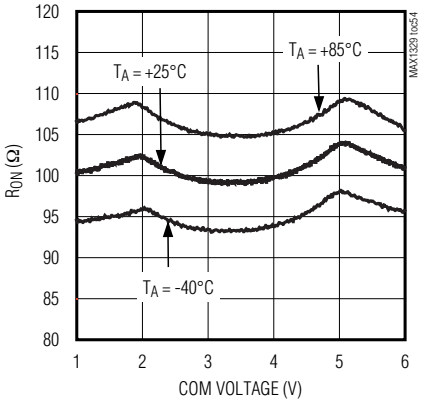
OP-AMP GAIN AND PHASE vs. FREQUENCY



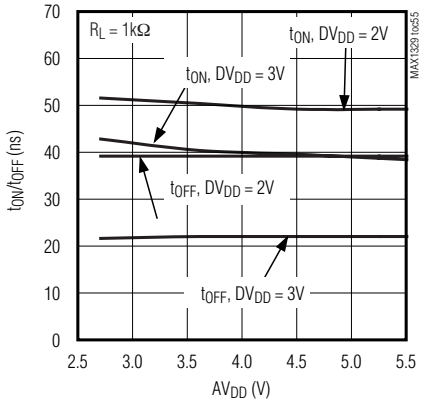
ANALOG SWITCH ON-RESISTANCE vs. COM VOLTAGE (AV_{DD} = 3V)



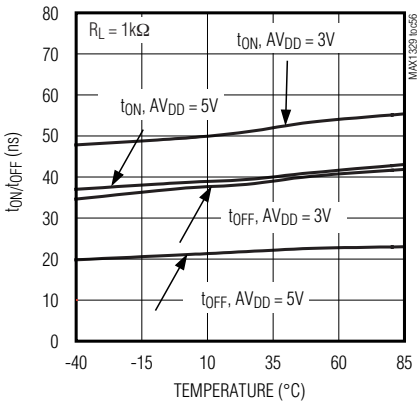
ANALOG SWITCH ON-RESISTANCE vs. COM VOLTAGE (AV_{DD} = 5V)



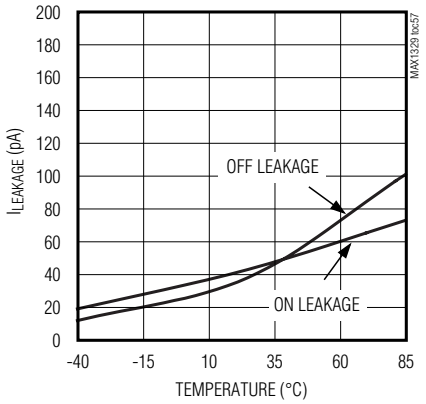
ANALOG SWITCH TURN-ON/-OFF TIME vs. ANALOG SUPPLY VOLTAGE



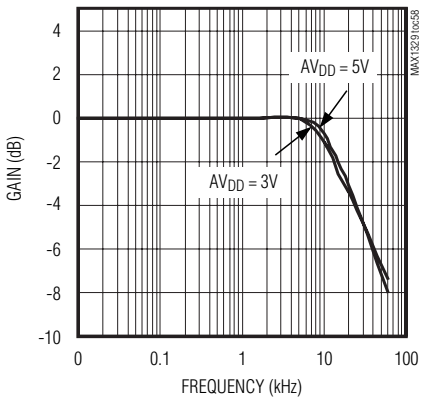
ANALOG SWITCH TURN-ON/-OFF TIME vs. TEMPERATURE



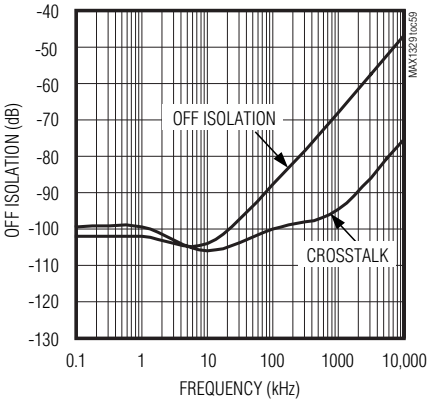
ANALOG SWITCH LEAKAGE CURRENT vs. TEMPERATURE



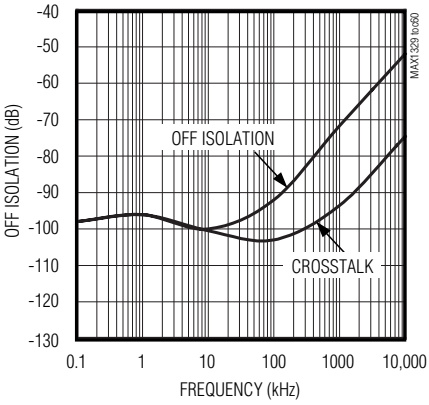
ANALOG SWITCH ON-RESPONSE vs. FREQUENCY



ANALOG SWITCH CROSSTALK AND OFF ISOLATION vs. FREQUENCY (AV_{DD} = 3V)



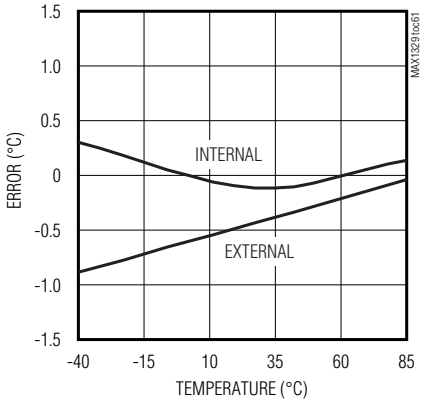
ANALOG SWITCH CROSSTALK AND OFF ISOLATION vs. FREQUENCY (AV_{DD} = 5V)



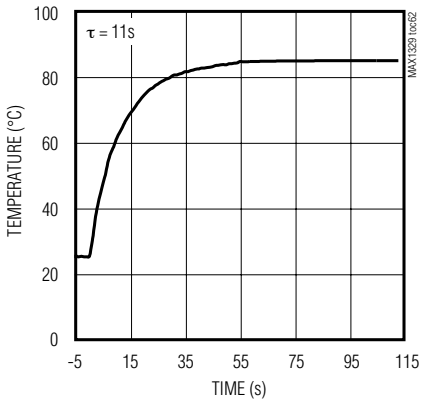
Typical Operating Characteristics (continued)

(AV_{DD} = 5.0V, V_{REFADC} = V_{REFDAC} = 2.5V for DV_{DD} = 3.0V; T_A = +25°C, unless otherwise noted.)

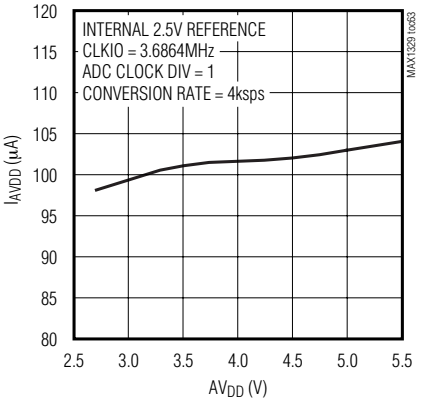
TEMPERATURE-SENSOR ACCURACY vs. TEMPERATURE



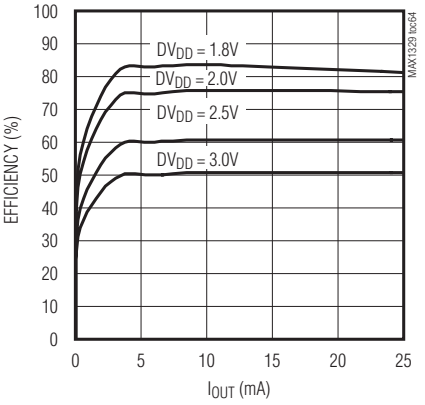
TEMPERATURE-SENSOR THERMAL STEP RESPONSE (+25°C TO +85°C)



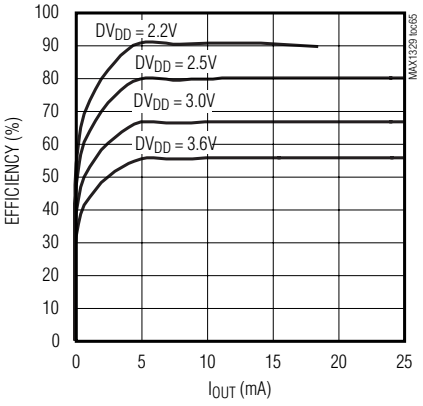
INTERNAL TEMPERATURE-SENSOR SUPPLY CURRENT vs. SUPPLY VOLTAGE



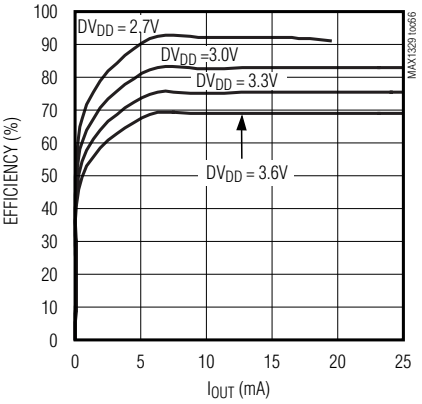
CHARGE-PUMP EFFICIENCY vs. OUTPUT CURRENT (AV_{DD} = 3V)



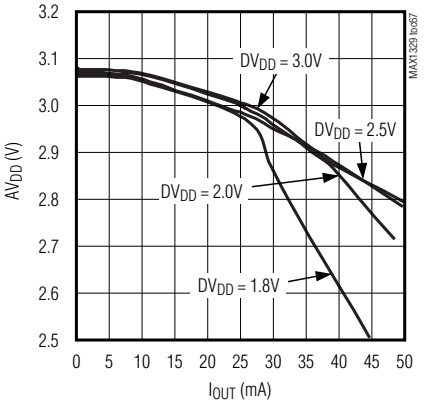
CHARGE-PUMP EFFICIENCY vs. OUTPUT CURRENT (AV_{DD} = 4V)



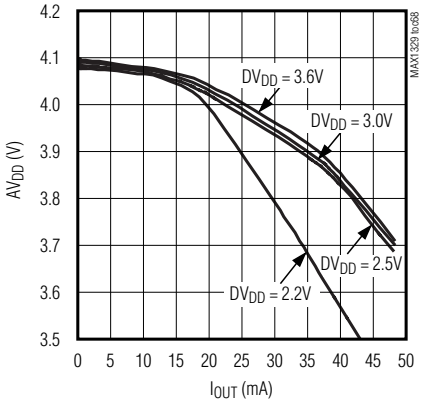
CHARGE-PUMP EFFICIENCY vs. OUTPUT CURRENT (AV_{DD} = 5V)



CHARGE-PUMP OUTPUT VOLTAGE vs. OUTPUT CURRENT (AV_{DD} = 3V)



CHARGE-PUMP OUTPUT VOLTAGE vs. OUTPUT CURRENT (AV_{DD} = 4V)

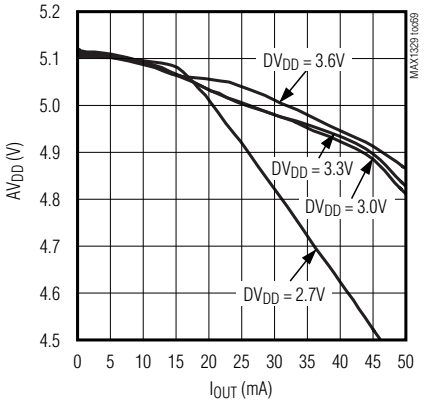


12-/16-Bit DASs with ADC, DACs, DPIOs, APIOs, Reference, Voltage Monitors, and Temp Sensor

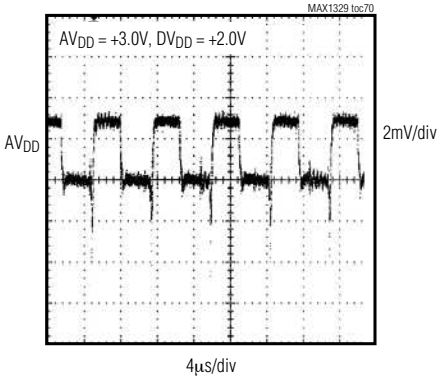
Typical Operating Characteristics (continued)

(AV_{DD} = 5.0V, V_{REFADC} = V_{REFDAC} = 2.5V for DV_{DD} = 3.0V; T_A = +25°C, unless otherwise noted.)

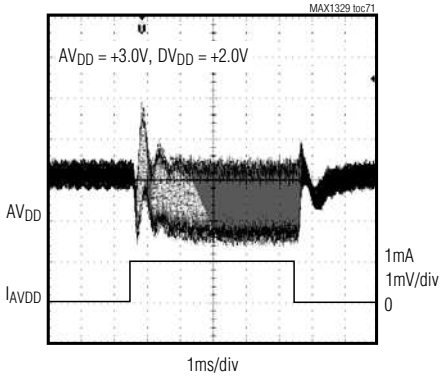
CHARGE-PUMP OUTPUT VOLTAGE vs. OUTPUT CURRENT (AV_{DD} = 5V)



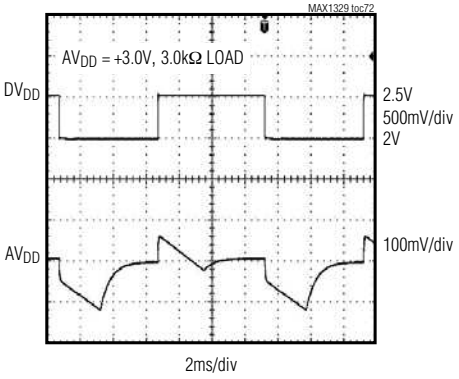
CHARGE-PUMP RIPPLE (I_{OUT} = 5mA, DV_{DD} = 2V, CHARGE-PUMP CLOCK = 78kHz)



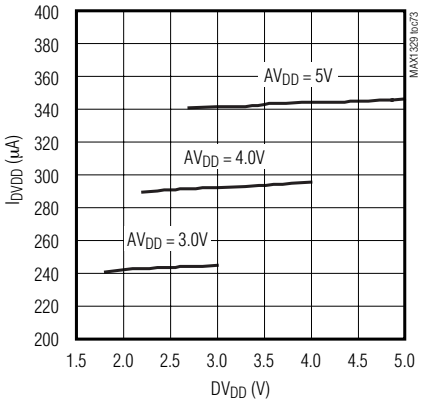
CHARGE-PUMP LOAD TRANSIENT RESPONSE FOR 0.1mA TO 1.0mA LOAD



CHARGE-PUMP LINE TRANSIENT RESPONSE FOR +2.0V TO +2.5V STEP INPUT



CHARGE-PUMP SUPPLY CURRENT vs. SUPPLY VOLTAGE



Pin Description

PIN		NAME	FUNCTION
MAX1329	MAX1330		
1	1	DPIO1	Digital Programmable Input/Output 1
2	2	DPIO2	Digital Programmable Input/Output 2
3	3	DPIO3	Digital Programmable Input/Output 3
4	4	DPIO4	Digital Programmable Input/Output 4
5	5	DOUT	Serial-Data Output. DOUT outputs serial data from the data register. DOUT changes on the falling edge of SCLK and is valid on the rising edge of SCLK. When $\overline{CS}$ is high, DOUT is high impedance, unless APIO1 is programmed for SPI mode.
6	6	SCLK	Serial-Clock Input. Apply an external serial clock to transfer data to and from the device. When $\overline{CS}$ is high, SCLK is inactive unless APIO3 is configured for SPI mode. Then the input on SCLK is level-shifted and output at APIO3.
7	7	DIN	Serial-Data Input. Data on DIN is clocked in on the rising edge of SCLK when $\overline{CS}$ is low. When $\overline{CS}$ is high, DIN is inactive unless APIO2 is configured for SPI mode. Then the input on DIN is level-shifted and output at APIO2.
8	8	$\overline{CS}$	Active-Low Chip-Select Input. Drive $\overline{CS}$ low to transfer data to and from the device. When $\overline{CS}$ is high and APIO4 is configured for SPI mode, APIO4 is low.
9	9	$\overline{RST1}$	Open-Drain Reset Output 1. $\overline{RST1}$ remains low while DV_{DD} is below 1.8V. $\overline{RST1}$ can be reprogrammed as a push-pull, active-high, or active-low Status register interrupt output.
10	10	$\overline{RST2}$	Open-Drain Reset Output 2. $\overline{RST2}$ remains low while DV_{DD} is below 2.7V. $\overline{RST2}$ can be reprogrammed as a push-pull, active-high, or active-low Status register interrupt output.
11	11	APIO1	Analog Programmable Input/Output 1
12	12	APIO2	Analog Programmable Input/Output 2
13	13	APIO3	Analog Programmable Input/Output 3
14	14	APIO4	Analog Programmable Input/Output 4
15	15	SNO1	Analog Switch 1 Normally-Open Terminal
16	16	SCM1	Analog Switch 1 Common Terminal
17	17	SNC1	Analog Switch 1 Normally-Closed Terminal
18	18	IN1+	Operational Amplifier 1 Noninverting Input
19	19	IN1-	Operational Amplifier 1 Inverting Input. Also internally connected to ADC mux.
20	20	OUT1	Operational Amplifier 1 Output. Also internally connected to ADC mux.
21	—	N.C.	No Connection. Not internally connected.
22	—	FBB	DACB Force-Sense Feedback Input. Also internally connected to ADC mux.
23	—	OUTB	DACB Force-Sense Output. Also internally connected to ADC mux.
—	21	IN2+	Operational Amplifier 2 Noninverting Input
—	22	IN2-	Operational Amplifier 2 Inverting Input. Also internally connected to ADC mux.
—	23	OUT2	Operational Amplifier 2 Output. Also internally connected to ADC mux.

12-/16-Bit DASs with ADC, DACs, DPIOs, APIOs, Reference, Voltage Monitors, and Temp Sensor

Pin Description (continued)

PIN		NAME	FUNCTION
MAX1329	MAX1330		
24	24	OUTA	DACA Force-Sense Output. Also internally connected to ADC mux.
25	25	FBA	DACA Force-Sense Feedback Input. Also internally connected to ADC mux.
26	26	REFDAC	DAC Internal Reference Buffer Output/DAC External Reference Input. In internal reference mode, REFDAC provides a 1.25V, 2.048V, or 2.5V internal reference buffer output. In external DAC reference buffer mode, disable internal reference buffer. Bypass REFDAC to AGND with a 1µF capacitor.
27	27	SNC2	Analog Switch 2 Normally-Closed Terminal
28	28	SCM2	Analog Switch 2 Common Terminal
29	29	SNO2	Analog Switch 2 Normally-Open Terminal
30	30	AIN2	Analog Input 2. Also internally connected to ADC mux.
31	31	AIN1	Analog Input 1. Also internally connected to ADC mux.
32	32	REFADC	ADC Internal Reference Buffer Output/ADC External Reference Input. In internal reference mode, REFADC provides a 1.25V, 2.048V, or 2.5V internal reference buffer output. In external ADC reference buffer mode, disable internal reference buffer. Bypass REFADC to AGND with a 1µF capacitor.
33	33	REFADJ	Internal Reference Output/Reference Buffer Amplifiers Input. In internal reference mode, bypass REFADJ to AGND with a 0.01µF capacitor. In external reference mode, disable internal reference.
34	34	AGND	Analog Ground
35	35	AV_{DD}	Analog Supply Input. Bypass AV_{DD} to AGND with at least a 0.01µF capacitor. With the charge pump enabled, see Table 32 for required capacitor values.
36	36	C1B	Charge-Pump Capacitor Input B. Connect C_{FLY} across C1A and C1B. See Table 32 for required capacitor values.
37	37	C1A	Charge-Pump Capacitor Input A. Connect C_{FLY} across C1A and C1B. See Table 32 for required capacitor values.
38	38	DV_{DD}	Digital Supply Input. Bypass DV_{DD} to DGND with at least a 0.01µF capacitor. When using charge pump, see Table 32 for required capacitor values.
39	39	DGND	Digital Ground
40	40	CLKIO	Clock Input/Output. In internal clock mode, enable CLKIO output for external use. In external clock mode, apply a clock signal at CLKIO for the ADC and charge pump.
—	—	EP	Exposed Pad. The exposed pad is located on the package bottom and is internally connected to AGND. Connect EP to the analog ground plane. Do not route any PCB traces under the package.

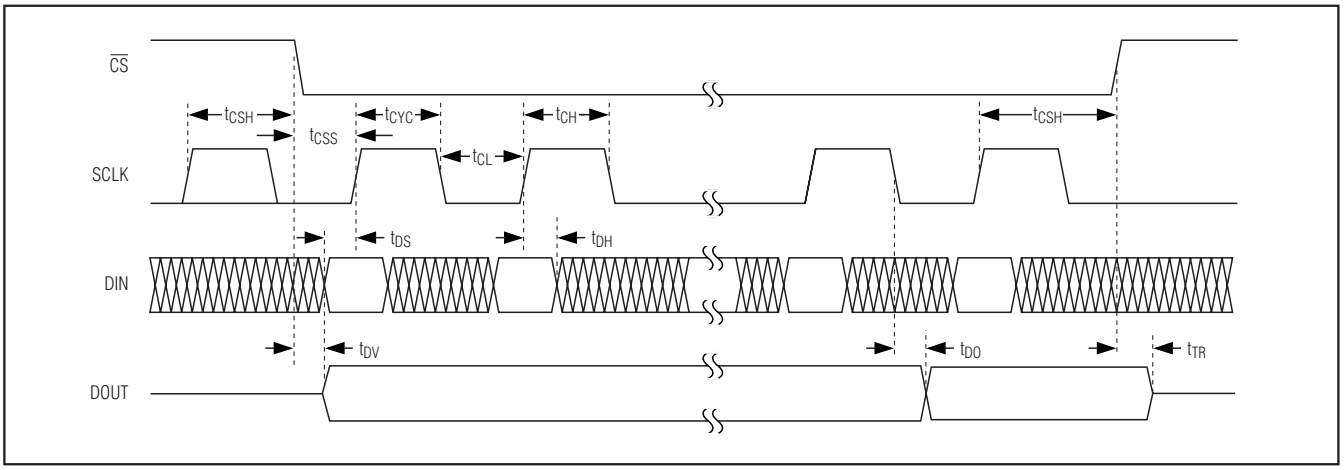


Figure 1. Detailed Serial-Interface Timing Diagram

Detailed Description

The MAX1329/MAX1330 smart DASs are based on a 312ksps, 12-bit SAR ADC with a 1ksps, 16-bit DSP mode. The ADC includes a differential multiplexer, a programmable gain amplifier (PGA) with gains of 1, 2, 4, and 8, a 20-bit accumulator, internal dither, a 16-word FIFO, and an alarm register. The MAX1329/MAX1330 operate with a digital supply down to 1.8V and feature an internal charge pump to boost the supply voltage for the analog circuitry that requires 2.7V to 5.5V.

The MAX1329/MAX1330 include an internal reference with programmable buffer for the ADC, two analog external inputs as well as inputs from other internal circuitry, an internal/external temperature sensor, internal oscillator, dual single-pole, double-throw (SPDT) switches, four digital programmable I/Os, four analog programmable I/Os, and dual programmable voltage monitors.

The MAX1329 features dual 12-bit force-sense DACs with programmable reference buffer and one operational amplifier. The MAX1330 includes one 12-bit force-sense DAC with programmable reference buffer and dual op amps. DACA can be sequenced with a 16-word FIFO. The DAC buffers and op amps have internal analog switches between the output and the inverting input.

Power-On Reset

After a power-on reset, the DV_{DD} voltage supervisor is enabled with thresholds at 1.8V and 2.7V. All digital and analog programmable I/Os (DPIOs and APIOs) are configured as inputs with pullups enabled. The internal oscillator is enabled and is output at CLKIO once the 1.8V reset trip threshold has been exceeded and the subsequent timeout period has expired. See the *Register Bit Descriptions* section for the default values after a power-on reset.

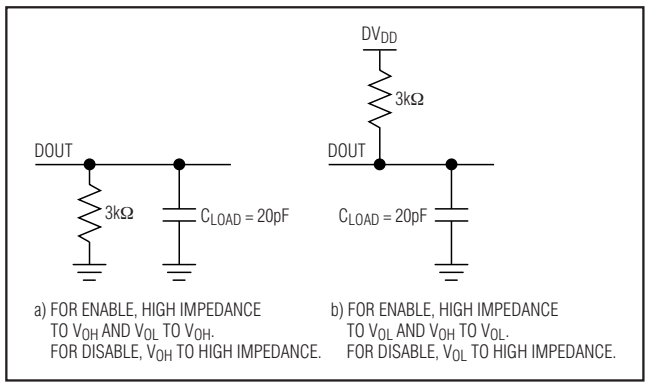


Figure 2. DOUT Enable and Disable Time Load Circuits

Power-On Setup

After applying power to AV_{DD}:

1) Write to the Reset register. This initializes the temperature sensor and voltage reference trim logic.
2) Within 3ms following the reset, configure the charge pump as desired by writing to the CP/VM Control register. The details of programming the charge pump are described in the *Charge Pump* section.

Charge Pump

Power AV_{DD} and DV_{DD} by any one of the following ways: drive AV_{DD} and DV_{DD} with a single external power supply, drive AV_{DD} and DV_{DD} with separate external power supplies, or drive DV_{DD} with an external supply and enable the internal charge pump to generate AV_{DD} or short DV_{DD} to AV_{DD} internally.