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EVALUATION KIT AVAILABLE

# 4-Channel, Automotive Class D Audio Amplifier

MAX13301

## General Description

The MAX13301 combines four high-efficiency Class D amplifiers with integrated diagnostic hardware for reliable automotive audio systems, and delivers up to 80W at 10% THD+N per channel into 4Ω when operating from a 24V supply.

The internal diagnostics evaluate each channel's output impedance to check for shorts across the outputs, to the battery, or to ground. The I²C interface allows the system to query critical device parameters such as device temperature and output clipping. The device is programmable to four different I²C addresses.

The audio amplifiers feature single-ended analog inputs with a common negative input. The MAX13301 has a fixed gain of 26dB.

The Class D amplifier has 10 programmable switching frequencies between 300kHz and 750kHz.

The BTL outputs are protected against short circuits and thermal overload. The outputs can be configured as a 2-, 3-, or 4-channel amplifier. The device provides 50V load-dump protection, and is offered in the thermally enhanced, 48-pin TSSOP-EPR package operating over the -40°C to +125°C temperature range.

## Applications

Car Stereo

Rear-Seat Entertainment Units

Discrete Amplifier Modules

Active Loudspeaker Systems

Radio Head Units

Mobile Surround Systems

***Typical Operating Circuit appears at end of data sheet.***

## Features

- **High Output Power (10% THD+N)**
  - **2 x 160W into 2Ω at 24V**
  - **4 x 80W into 4Ω at 24V**
- **2 Channels Can Be Paralleled**
- **Feedback After the Filter**
  - **Improves THD+N**
  - **Low Output Impedance**
  - **High-Frequency Response**
  - **Improved Damping of Complex Loads**
  - **Enables Low-Cost Inductors**
- **102dB SNR**
- **Low 0.04% THD+N**
- **70dB PSRR**
- **On-Board Diagnostics**
  - **Short-to-Battery/GND**
  - **Open/Shorted Load**
  - **Tweeter Detect**
- **Protection and Monitoring Functions:**
  - **Short-Circuit Protection**
  - **50V Load-Dump Protection**
  - **Programmable Clip Detection**
  - **DC Offset Detection**
  - **Open Battery/GND Tolerant**
  - **Thermal-Overload Protection**
  - **Thermal Warning Indication**
- **Four-Address I²C Control Interface**
- **Low-Power Shutdown Mode**
- **Up to 90.5% Efficiency**
- **-40°C to +125°C Ambient Operating Temperature**
- **48-Pin TSSOP-EPR (Top Side Exposed Pad) Package**
- **AEC-Q100 Qualified**

## Ordering Information

| PART | PIN-PACKAGE | SUPPLY VOLTAGE RANGE (V) |
|---|---|---|
| MAX13301AUM/V+ | 48 TSSOP-EPR* | 6 to 25.5 |

***Note:*** *The device operates over the -40°C to +125°C operating temperature range.*
*/V denotes an automotive qualified part.*
*+Denotes a lead(Pb)-free/RoHS-compliant package.*
**EPR = Top side exposed pad.*

# 4-Channel, Automotive Class D Audio Amplifier

## ABSOLUTE MAXIMUM RATINGS

PVDD to PGND ..... -0.3V to +30V
PVDD to PGND (t < 200ms) ..... -0.3V to +50V
PVDD Ramp Rate ..... 25V/ms
$V_{DD5}$, CM to PGND ..... -0.3V to +6V
CP to PGND ..... ($V_{PVDD}$ - 0.3V) to ($V_{CHOLD}$ + 0.3V)
CHOLD to PVDD ..... -0.3V to +6V
OUT_ to PGND, FB_ to PGND ..... -0.3V to ($V_{PVDD}$ + 0.3V)
$V_{DD}$ to GND ..... -0.3V to +6V
REF to GND ..... -0.3V to +6V
SCL, SDA, SYNC to GND ..... -0.3V to +6V
$\overline{MUTE\_CL1}$, $\overline{CL0}$, $\overline{FLT\_OT}$, EN to GND ..... -0.3V to +6V
IN_ to GND ..... -0.3V to +6V
GND to PGND ..... -0.3V to +0.3V
Continuous Power Dissipation (Notes 1 and 2)
TSSOP (derate 16.7mW/°C above 70°C) ..... 1333.3mW
Operating Temperature Range ..... -40°C to +125°C
Junction Temperature Range ..... -40°C to +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +240°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## PACKAGE THERMAL CHARACTERISTICS (Notes 1 and 2)

TSSOP
Junction-to-Ambient Thermal Resistance ($\theta_{JA}$) ..... 60°C/W
Junction-to-Case Thermal Resistance ($\theta_{JC}$) ..... 1°C/W

**Note 1:** Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

**Note 2:** The 48-pin TSSOP-EPR package has a top side exposed pad for enhanced thermal management. Connect this exposed pad to an external heatsink to ensure the device is adequately cooled. The maximum power dissipation in the device is a function of this external heatsink and other system parameters. See the *Thermal Information* section for more information.

## ELECTRICAL CHARACTERISTICS

($V_{PVDD}$ = 14.4V, $V_{DD}$ = $V_{DD5}$ = 5V, $V_{GND}$ = $V_{PGND}$ = 0V, $f_{SW}$ = 500kHz, MAP.COMP[2:0] = (see Table 20 for applicable setting), $T_A$ = -40°C to +125°C; typical values are at $T_A$ = +25°C, unless otherwise noted.) (Note 3)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **AMPLIFIER DC CHARACTERISTICS** | | | | | | |
| Supply Voltage Range | $V_{PVDD}$ | | 8 | | 25.5 | V |
| | | Operational | 6 | | | |
| | $V_{DD5}$ | | 4.75 | 5 | 5.5 | |
| | $V_{DD}$ | | 4.5 | 5 | 5.5 | |
| PVDD UVLO Threshold | | Falling | 5.2 | 5.35 | 5.6 | V |
| PVDD OVLO Threshold | | Rising | 26 | 27 | 30 | V |
| PVDD OVLO Response Timing | | Rising | 4 | 14 | 55 | µs |
| OUT_ and FB_ Voltage | | OV active | | $V_{PVDD}$/2 | | V |
| $V_{DD}$ UV Threshold | | Falling | | 4.2 | 4.35 | V |
| | | Rising | | 4.5 | 4.6 | |
| $V_{DD}$ UV Threshold Hysteresis | | | 0.1 | 0.2 | | V |
| $V_{DD}$ UV Threshold Deglitch | | | | 1 | | µs |
| Quiescent Supply Current | $I_{PVDD}$ | $R_L$ = ∞, play mode (CTRL2 = 0x0F) | | 70 | | µA |
| | $I_{VDD5}$ | | | 60 | 72 | mA |
| | $I_{VDD}$ | | | 50 | 75 | |

## ELECTRICAL CHARACTERISTICS (continued)

($V_{PVDD}$ = 14.4V, $V_{DD}$ = $V_{DD5}$ = 5V, $V_{GND}$ = $V_{PGND}$ = 0V, $f_{SW}$ = 500kHz, MAP.COMP[2:0] = (see Table 20 for applicable setting), $T_A$ = -40°C to +125°C; typical values are at $T_A$ = +25°C, unless otherwise noted.) (Note 3)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| PVDD Shutdown Supply Current | $I_{PVDD\_SHDN}$ | $T_A$ = +25°C, $V_{EN}$ = 0V | | 7 | | µA |
| | | $T_A$ = $T_{MIN}$ to +85°C, $V_{EN}$ = 0V | | | 17 | |
| $V_{DD5}$ Shutdown Supply Current | $I_{VDD5\_SHDN}$ | $T_A$ = +25°C, $V_{EN}$ = 0V | | 0.1 | | µA |
| | | $T_A$ = $T_{MIN}$ to +85°C, $V_{EN}$ = 0V | | | 2 | |
| $V_{DD}$ Shutdown Supply Current | $I_{VDD\_SHDN}$ | $T_A$ = +25°C, $V_{EN}$ = 0V | | 0.1 | | µA |
| | | $T_A$ = $T_{MIN}$ to +85°C, $V_{EN}$ = 0V | | | 2 | |
| Standby Supply Current | $I_{VDD5}$ | CTRL2 = 0x20, $V_{EN}$ = 5V | | 1 | | mA |
| | $I_{VDD}$ | | | 10 | | |
| Output Leakage | | $V_{OUT\_}$ = 14.4V | | | 200 | µA |
| | | $V_{OUT\_}$ = 0V | | | 1 | |
| Output Discharge Current | | CTRL3.DIS = 1 | | 8 | | mA |
| $R_{DS(ON)}$ per Output | | Excluding wire bond resistance | | 70 | | mΩ |
| FB_ Resistance | | | | 310 | | kΩ |
| Output Offset | $V_{OS}$ | $T_A$ = +25°C, mute mode (CTRL2 = 0x00), no input signal | | | 15 | mV |
| | | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | | | 100 | |
| OUT_ Output Impedance | | | | 100 | | mΩ |
| **AMPLIFIER AC CHARACTERISTICS** | | | | | | |
| Output Power | $P_{OUT}$ | THD+N = 1%, $R_L$ = 4Ω, $V_{PVDD}$ = 24V | | 66 | | W |
| | | THD+N = 10%, $R_L$ = 4Ω, $V_{PVDD}$ = 24V | | 80 | | |
| | | THD+N = 10%, $R_L$ = 2Ω, $V_{PVDD}$ = 24V, parallel mode | | 160 | | |
| Signal-Path Gain | | | | 26 | | dB |
| Channel-to-Channel Gain Tracking | | | -1 | +0.1 | +1 | dB |
| Input Resistance | | IN0+, IN1+, IN2+, IN3+ | | 20 | | kΩ |
| | | IN- | | 5 | | |
| Mute Attenuation | | Guaranteed by design, test is functional only | 90 | 100 | | dB |
| Precharge Current | | CTRL1.PRE = 1, IN- | 5 | 10 | | mA |
| | | CTRL1.PRE = 1, IN_+ | 1 | 2 | | |
| Power-Supply Rejection Ratio | | $V_{DD}$ = 4.5V to 5.5V | | 70 | | dB |
| | | $V_{PVDD}$ = $1V_{P-P}$ ripple, 100Hz to 10kHz | | 60 | | |
| | | $V_{PVDD}$ = 8V to 25.5V | | 68 | | |
| REF Voltage | | $C_{REF(MIN)}$ = 1µF | | 2.224 | | V |
| REF Output Impedance | | DC | | 800 | | Ω |
| Input Voltage Range | | AC-coupled | | | 1.2 | $V_{RMS}$ |

## ELECTRICAL CHARACTERISTICS (continued)

($V_{PVDD}$ = 14.4V, $V_{DD}$ = $V_{DD5}$ = 5V, $V_{GND}$ = $V_{PGND}$ = 0V, $f_{SW}$ = 500kHz, MAP.COMP[2:0] = (see Table 20 for applicable setting), $T_A$ = -40°C to +125°C; typical values are at $T_A$ = +25°C, unless otherwise noted.) (Note 3)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Total Harmonic Distortion Plus Noise | THD+N | $P_{OUT}$ = 10W, $R_L$ = 4Ω, BW = 22Hz to 20kHz AES17 filter, f = 1kHz | | | 0.04 | 0.14 | % |
| | | $P_{OUT}$ = 1W to 10W, $R_L$ = 4Ω, BW = 22Hz to 20kHz AES17 filter, f = 1kHz | | | 0.1 | | |
| Noise | N | A-weighted, $V_{PVDD}$ = 24V | | | 100 | | $\mu V_{RMS}$ |
| | | 22Hz to 22kHz, $V_{PVDD}$ = 24V | | | 140 | | |
| | | A-weighted, CTRL5.SS[2:0] = 110, SSEN = 1, $V_{PVDD}$ = 24V | | | 100 | | |
| Crosstalk | | $P_{OUT\_}$ = 4W, f = 1kHz to 10kHz | | | 60 | | dB |
| Efficiency | η | $R_L$ = 4Ω, $P_{OUT}$ = 20W/channel, $V_{DD5}$, $V_{DD}$ supplied from a switching power supply | | | 88 | | % |
| Internal Switching Frequency Adjust Range | | 6 to 15 clock-divider range | | 300 | | 750 | kHz |
| **ONE-TIME DIAGNOSTICS** | | | | | | | |
| Short-to-Ground Detection | | CTRL2.STBY = 0, CTRL3.SDET = 1 | | | 75 | | Ω |
| Short-to-PVDD Detection Threshold | | CTRL2.STBY = 1, CTRL3.SDET = 1 | | | 6 | | V |
| Open-Load Detection | | CTRL3.LDM = 1, power amplifier mode | | 70 | 100 | | Ω |
| | | CTRL3.LDM = 0, line-driver mode | | 200 | 300 | | |
| Low-Current Threshold | | 15kHz < f < 25kHz, $T_A$ = +25°C, CTRL3.TW = 1 | CTRL3.HCL = 0 | 160 | 291 | 500 | mA |
| | | | CTRL3.HCL = 1 | 200 | 364 | 625 | |
| High-Current Threshold | | f < 20Hz, CTRL3.TW = 0 | CTRL3.HCL = 0 | 0.65 | 1.15 | 1.85 | A |
| | | | CTRL3.HCL = 1 | 0.9 | 1.65 | 2.15 | |
| **CONTINUOUS DIAGNOSTICS** | | | | | | | |
| Differential Output Offset Voltage Threshold | | No audio in play mode | | 0.56 | 1.04 | 1.6 | V |
| Clip-Detect Threshold | | $R_L$ = 4Ω | CTRL1.CLVL[1:0] = 11 | | 1 | | %THDN |
| | | | CTRL1.CLVL[1:0] = 01 | | 3 | | |
| | | | CTRL1.CLVL[1:0] = 10 | | 5 | | |
| | | | CTRL1.CLVL[1:0] = 00 | | 10 | | |

## ELECTRICAL CHARACTERISTICS (continued)

($V_{PVDD}$ = 14.4V, $V_{DD}$ = $V_{DD5}$ = 5V, $V_{GND}$ = $V_{PGND}$ = 0V, $f_{SW}$ = 500kHz, MAP.COMP[2:0] = (see Table 20 for applicable setting), $T_A$ = -40°C to +125°C; typical values are at $T_A$ = +25°C, unless otherwise noted.) (Note 3)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Short-to-Ground/PVDD | | OUT__ shorted to ground/PVDD, CTRL1.CL_TH = 1 | CTRL3.HCL = 0 | | 1.03 | | A |
| | | | CTRL3.HCL = 1 | | 1.28 | | |
| | | OUT__ shorted to ground/PVDD, CTRL1.CL_TH = 0 | CTRL3.HCL = 0 | | 3.09 | | |
| | | | CTRL3.HCL = 1 | | 3.86 | | |
| Level 1 Output Current Limit | $I_{LIM1}$ | CTRL3.HCL = 0 | | 5.5 | 7 | | A |
| Level 2 Output Current Limit | $I_{LIM2}$ | CTRL3.HCL = 1 | | 7 | 8.75 | | A |
| **THERMAL PROTECTION** | | | | | | | |
| Thermal Warning Range 1 | | Guaranteed monotonic | | | 110 | | °C |
| Thermal Warning Range 2 | | Guaranteed monotonic | | | 120 | | °C |
| Thermal Warning Range 3 | | Guaranteed monotonic | | | 130 | | °C |
| Thermal Warning Range 4 | | Guaranteed monotonic | | | 140 | | °C |
| Thermal Shutdown Level | | Guaranteed monotonic | | 150 | 165 | | °C |
| Thermal Warning Hysteresis | | | | | 5 | | °C |
| Thermal Shutdown Hysteresis | | | | 15 | | | °C |
| **CHARGE PUMP** | | | | | | | |
| Switching Frequency | | $f_{CP}$ = $f_{SW}$ | | 300 | | 750 | kHz |
| Soft-Start Time | | | | | 100 | | µs |
| Charge-Pump Output Impedance | | Guaranteed by FET $R_{DS(ON)}$ measurement | | | 1.8 | | Ω |
| Output Voltage | | | | | $V_{PVDD}$ + 5 | | V |
| **INTERNAL OSCILLATOR** | | | | | | | |
| SYNC I/O Frequency Range | | 2x switching frequency | | 0.6 | | 1.5 | MHz |
| Frequency | | Spread-spectrum disabled | | 17.1 | 18 | 18.9 | MHz |
| **DIGITAL INTERFACE (SCL, SDA, ADDR, $\overline{CL0}$, $\overline{MUTE\_CL1}$, EN, SYNC, $\overline{FLT\_OT}$)** | | | | | | | |
| SYNC High | | CTRL1.CM[1:0] = 01, $I_{SOURCE}$ = 3mA | | 4.5 | | | V |
| SYNC Low | | CTRL1.CM[1:0] = 01, $I_{SINK}$ = 3mA | | | | 0.4 | V |
| Input Voltage High | $V_{INH}$ | | | 2.0 | | | V |
| Input Voltage Low | $V_{INL}$ | | | | | 0.8 | V |
| Input Voltage Hysteresis | | | | | 300 | | mV |
| Input Leakage Current | | SDA, SCL, $\overline{CL0}$, $\overline{MUTE\_CL1}$, $\overline{FLT\_OT}$ | | | | ±10 | µA |
| Output Low Voltage | | SDA, $\overline{CL0}$, $\overline{MUTE\_CL1}$, $I_{SINK}$ = 3mA, $\overline{FLT\_OT}$ | | | | 0.4 | V |
| Pulldown Current | | $\overline{MUTE\_CL1}$ | | | 5 | 13 | µA |
| | | EN | | | 10 | 18 | |

## ELECTRICAL CHARACTERISTICS (continued)

($V_{PVDD}$ = 14.4V, $V_{DD}$ = $V_{DD5}$ = 5V, $V_{GND}$ = $V_{PGND}$ = 0V, $f_{SW}$ = 500kHz, MAP.COMP[2:0] = (see Table 20 for applicable setting), $T_A$ = -40°C to +125°C; typical values are at $T_A$ = +25°C, unless otherwise noted.) (Note 3)

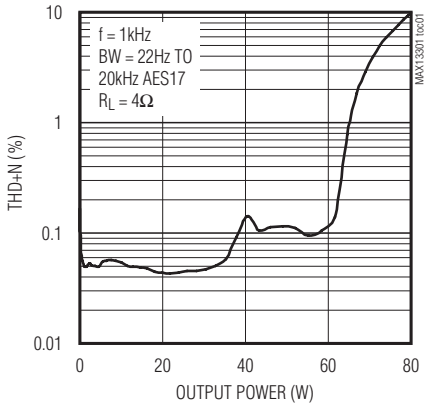
| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **I²C TIMING** | | | | | | |
| Output Fall Time | $t_{OF}$ | $C_{BUS}$ = 10pF to 400pF | | | 250 | ns |
| Pin Capacitance | | | | | 10 | pF |
| Clock Frequency | $f_{SCL}$ | | | | 400 | kHz |
| SCL Low Time | $t_{LOW}$ | | 1.3 | | | µs |
| SCL High Time | $t_{HIGH}$ | | 0.6 | | | µs |
| START Condition Hold Time | $t_{HD:STA}$ | Repeated START condition | 0.6 | | | µs |
| START Condition Setup Time | $t_{SU:STA}$ | Repeated START condition | 0.6 | | | µs |
| Data Hold Time | $t_{HD:DAT}$ | | 0 | | 900 | ns |
| Data Setup Time | $t_{SU:DAT}$ | | 100 | | | ns |
| Input Rise Time | $t_R$ | SCL, SDA | | | 300 | ns |
| Input Fall Time | $t_F$ | SCL, SDA | | | 300 | ns |
| STOP Condition Setup Time | $t_{SU:STO}$ | | 0.6 | | | µs |
| Bus Free Time | $t_{BUF}$ | Between START and STOP conditions | 1.3 | | | µs |
| Maximum Bus Capacitance | $C_{BUS}$ | Per bus line | | | 400 | pF |

**Note 3:** All units are 100% production tested at $T_A$ = +25°C. All temperature limits are guaranteed by design.

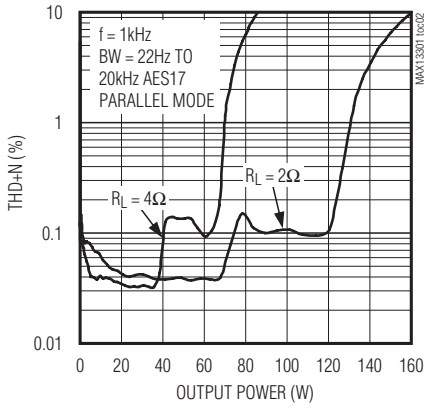
## Typical Operating Characteristics

($V_{PVDD}$ = 24V, $V_{DD}$ = $V_{DD5}$ = 5V, $V_{GND}$ = $V_{PGND}$ = 0V, $f_{SW}$ = 500kHz, MAP.COMP[2:0] = 011, see Table 32 for LC filter value, $T_A$ = +25°C, unless otherwise noted.)

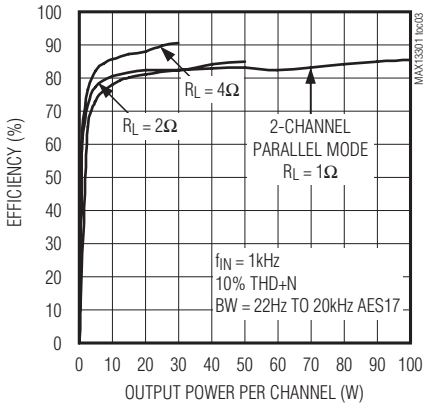
**THD+N vs. OUTPUT POWER**



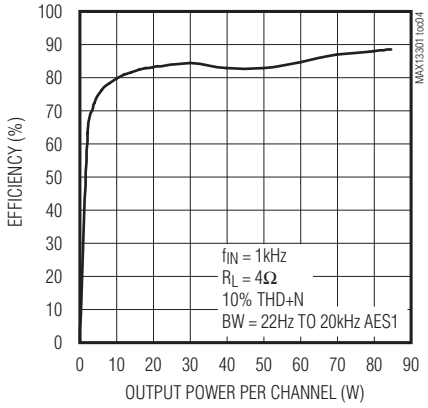

**THD+N vs. OUTPUT POWER**



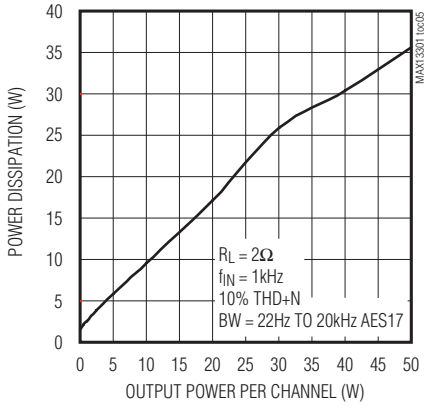

**EFFICIENCY vs. OUTPUT POWER PER CHANNEL**



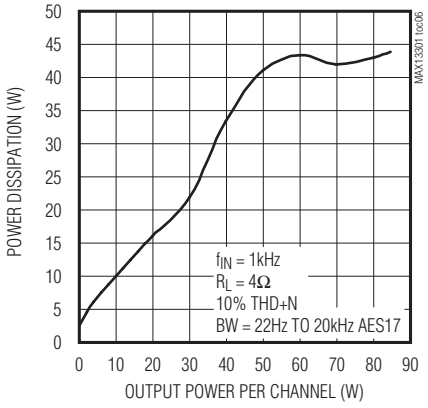

**EFFICIENCY vs. OUTPUT POWER PER CHANNEL**



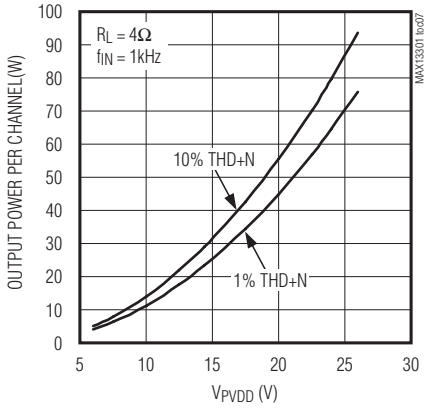

**POWER DISSIPATION vs. OUTPUT POWER PER CHANNEL**



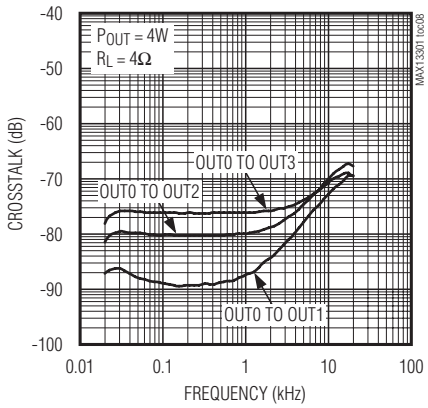

**POWER DISSIPATION vs. OUTPUT POWER PER CHANNEL**



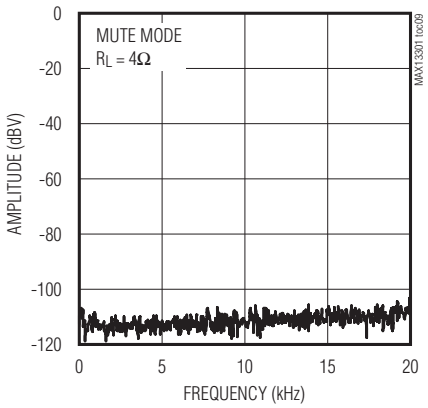

**OUTPUT POWER vs. SUPPLY VOLTAGE**




**CROSSTALK**



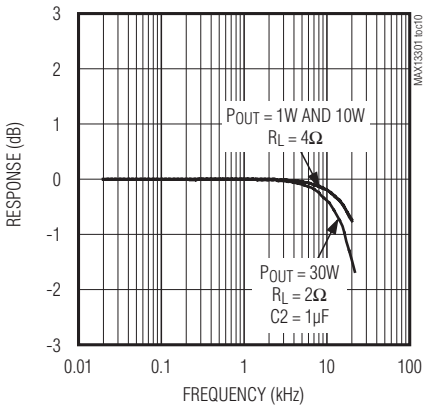

**OUTPUT FREQUENCY SPECTRUM**



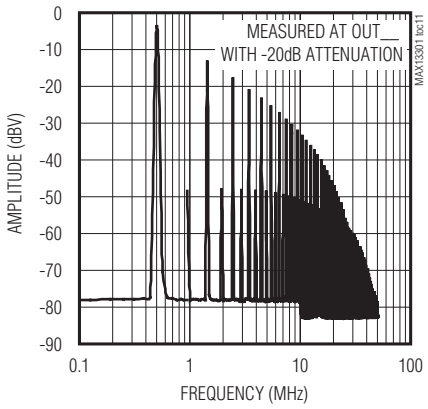
## Typical Operating Characteristics (continued)

($V_{PVDD}$ = 24V, $V_{DD}$ = $V_{DD5}$ = 5V, $V_{GND}$ = $V_{PGND}$ = 0V, $f_{SW}$ = 500kHz, MAP.COMP[2:0] = 011, see Table 32 for LC filter value, $T_A$ = +25°C, unless otherwise noted.)

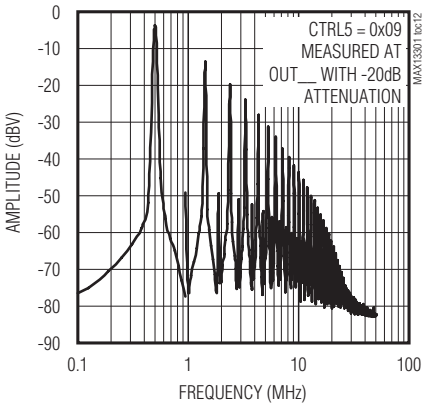
**FREQUENCY RESPONSE**



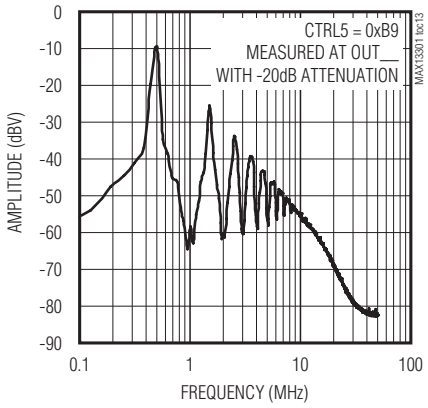

**FIXED-FREQUENCY MODULATION WIDEBAND OUTPUT SPECTRUM**



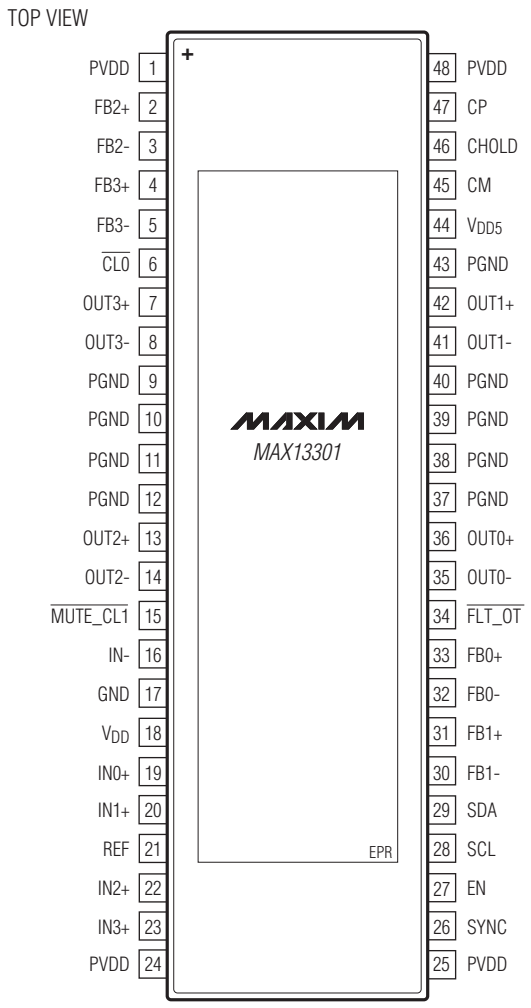

**SPREAD-SPECTRUM MODULATION WIDEBAND OUTPUT SPECTRUM**




**SPREAD-SPECTRUM MODULATION WIDEBAND OUTPUT SPECTRUM**



## Pin Configuration




**TSSOP**

## Pin Description

| PIN | NAME | FUNCTION |
|---|---|---|
| 1, 24, 25, 48 | PVDD | Audio Output Power-Supply Input. Bypass each PVDD to its PGND pair locally with 0.1µF and 4.7µF ceramic capacitors. Each PVDD/PGND pair consists of one PVDD and two PGNDs. The PVDD/PGND pairs are 1 and 9-10, 48 and 39-40, 24 and 11-12, and 25 and 37-38. Bypassing PVDD locally minimizes the area of di/dt loops. An additional 1000µF, low-ESR electrolytic capacitor should be placed from 1 and 48 to PGND and 24 and 25 to PGND. |
| 2 | FB2+ | Output 2 Positive Feedback. Connect to the LC filter's positive output through a 150Ω ±1% resistor. |
| 3 | FB2- | Output 2 Negative Feedback. Connect to the LC filter's negative output through a 150Ω ±1% resistor. |

# 4-Channel, Automotive Class D Audio Amplifier

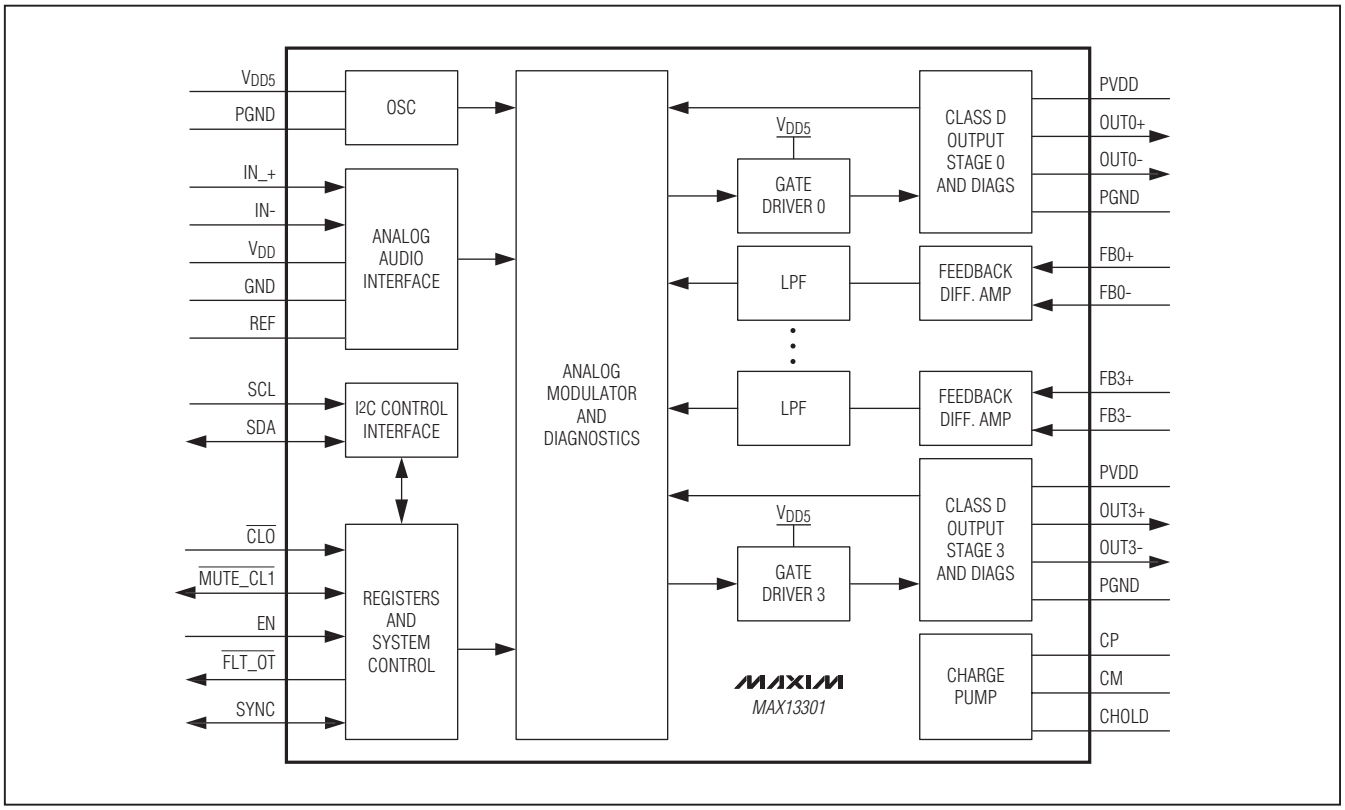
## Pin Description (continued)

| PIN | NAME | FUNCTION |
|---|---|---|
| 4 | FB3+ | Output 3 Positive Feedback. Connect to the LC filter's positive output through a 150Ω ±1% resistor. |
| 5 | FB3- | Output 3 Negative Feedback. Connect to the LC filter's negative output through a 150Ω ±1% resistor. |
| 6 | $\overline{CL0}$ | Active-Low Open-Drain Clip 0 Output. $\overline{CL0}$ is configurable to provide clipping indication for outputs 0 and 1 or for all four outputs. |
| 7 | OUT3+ | Channel 3 Power Amplifier Positive Output |
| 8 | OUT3- | Channel 3 Power Amplifier Negative Output |
| 9–12, 37–40, 43 | PGND | Audio Output Power Ground |
| 13 | OUT2+ | Channel 2 Power Amplifier Positive Output |
| 14 | OUT2- | Channel 2 Power Amplifier Negative Output |
| 15 | $\overline{MUTE\_CL1}$ | Mute Input or Active-Low Open-Drain Clip 1 Output. $\overline{MUTE\_CL1}$ is configurable as a mute input or as an open-drain clip indicator output. When configured as an input, drive $\overline{MUTE\_CL1}$ low to mute all four outputs. As an output, $\overline{MUTE\_CL1}$ provides clipping indication for outputs 2 and 3. This pin also selects the low bit of the I²C address and is latched upon the rising edge of the EN pin. $\overline{MUTE\_CL1}$ has an internal 5µA pulldown. |
| 16 | IN- | Common Audio Negative Input. IN- has 5kΩ of input resistance. Bypass to analog ground with 2µF or 4 x $C_{IN\_+}$. |
| 17 | GND | Analog Ground |
| 18 | $V_{DD}$ | 5V Analog Power-Supply Input. Bypass with a 2.2µF or larger ceramic capacitor to GND. $V_{DD}$ provides power to the analog and digital circuitry. |
| 19 | IN0+ | Channel 0 Audio Input. IN0+ has 20kΩ of input resistance. Connect a series capacitor of at least 0.47µF to IN0+. |
| 20 | IN1+ | Channel 1 Audio Input. IN1+ has 20kΩ of input resistance. Connect a series capacitor of at least 0.47µF to IN1+. |
| 21 | REF | 2.2V Reference Output. Bypass REF to GND with a 1µF ceramic capacitor. |
| 22 | IN2+ | Channel 2 Audio Input. IN2+ has 20kΩ of input resistance. Connect a series capacitor of at least 0.47µF to IN2+. |
| 23 | IN3+ | Channel 3 Audio Input. IN3+ has 20kΩ of input resistance. Connect a series capacitor of at least 0.47µF to IN3+. |
| 26 | SYNC | Sync I/O. In master mode, SYNC outputs a clock signal that is synchronized to that of the modulator. In slave mode, SYNC is a clock input and serves as the clock source for the modulator. |
| 27 | EN | Enable Input. Connect EN to $V_{DD}$ for normal operation. Connect EN to GND to place the device in a low-power mode. There is an internal 10µA pulldown on EN. |
| 28 | SCL | I²C Serial-Clock Input |
| 29 | SDA | I²C Serial-Data Input and Output |
| 30 | FB1- | Output 1 Negative Feedback. Connect to the LC filter's negative output through a 150Ω ±1% resistor. |
| 31 | FB1+ | Output 1 Positive Feedback. Connect to the LC filter's positive output through a 150Ω ±1% resistor. |
| 32 | FB0- | Output 0 Negative Feedback. Connect to the LC filter's negative output through a 150Ω ±1% resistor. |
| 33 | FB0+ | Output 0 Positive Feedback. Connect to the LC filter's positive output through a 150Ω ±1% resistor. |

## Pin Description (continued)

| PIN | NAME | FUNCTION |
|---|---|---|
| 34 | $\overline{FLT\_OT}$ | Active-Low Open-Drain Fault and Overtemperature Output. $\overline{FLT\_OT}$ provides indication of faults, overtemperature, and thermal shutdown status. |
| 35 | OUT0- | Channel 0 Power Amplifier Negative Output |
| 36 | OUT0+ | Channel 0 Power Amplifier Positive Output |
| 41 | OUT1- | Channel 1 Power Amplifier Negative Output |
| 42 | OUT1+ | Channel 1 Power Amplifier Positive Output |
| 44 | $V_{DD5}$ | 5V Power-Supply Input. Bypass with a 0.1µF capacitor to PGND. $V_{DD5}$ provides power to the gate drivers and charge pump. |
| 45 | CM | Charge-Pump Capacitor Negative Terminal |
| 46 | CHOLD | Charge-Pump Output. Connect a 1µF capacitor from CHOLD to PVDD. |
| 47 | CP | Charge-Pump Capacitor Positive Terminal |
| — | EPR | Top Side Exposed Pad. Connect this exposed pad to an external heatsink to ensure the device is adequately cooled. The maximum power dissipation in the device is a function of this external heatsink and other system parameters. See the *Thermal Information* section for more information. The top side exposed pad is electrically isolated from the die. |

## Functional Diagram



# 4-Channel, Automotive Class D Audio Amplifier

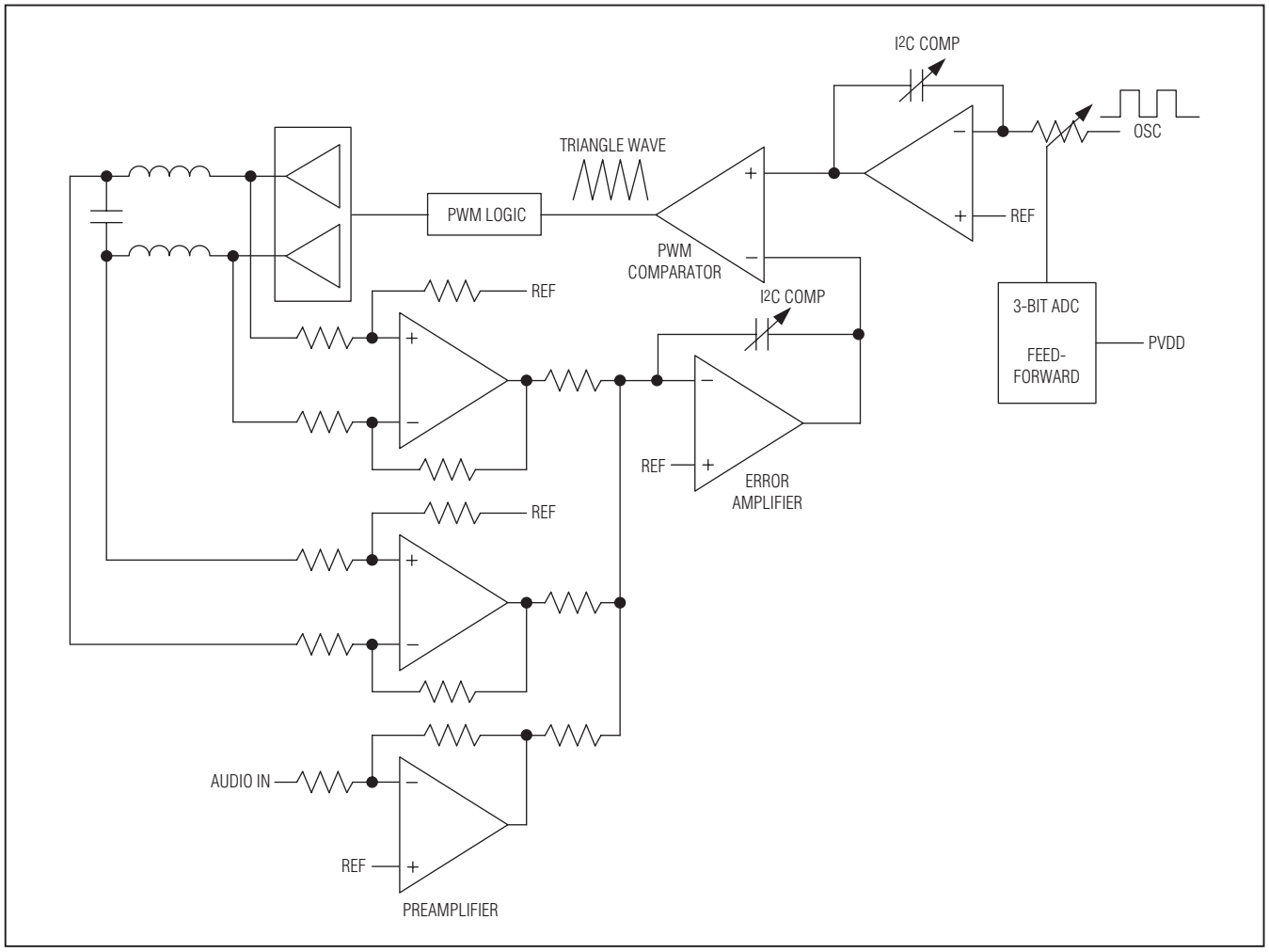



*Figure 1. Detailed Block Diagram of the MAX13301 Audio Path*

## Detailed Description

The MAX13301 4-channel, Class D audio power amplifiers is specifically designed for automotive applications. Integrated feedback from the LC filter's output improves the THD+N by reducing the distortion, providing Class AB performance while achieving efficiency up to 90.5%. The devices also support spread-spectrum modulation for AM radio compatibility.

### Description of Operation

The device emulates current-mode controllers with digital feed-forward (Figure 1). The internal oscillator creates an 18MHz square wave. The I2C controls a clock divider that divides down this high-frequency clock to a usable frequency. The resulting square wave is integrated to create a triangle wave. A 3-bit ADC converts the PVDD voltage into a code that adjusts the resistors used in the triangle-wave integrator. The triangle-wave amplitude becomes progressively larger as PVDD increases. The triangle wave is fed into the PWM comparator.

The two differential amplifiers provide both analog and digital feedback. The feedback is summed with the output of the preamplifier at the error amplifier. The output of the error amplifier is an AC replica of the inductor current (emulated current mode) and the triangle wave is therefore the slope compensation. The PWM comparator controls the full-bridge operation, turning on and off each FET pair (double-edge modulation). To ensure that the devices switch at the desired frequency, it is important to ensure that the triangle wave is greater than the error-

amplifier ramp. The design equation that must be met to ensure constant frequency is as follows:

Error-Amplifier Ramp < 2/3 Triangle-Wave Ramp

The error-amplifier ramp is fixed by the gain of the differential amplifiers used in the feedback loop and by the error-amplifier compensation capacitor programmed through I²C. To ensure the design equation for fixed frequency is met, the error-amplifier compensation capacitor tracks the integrator capacitor used to generate the triangle wave.

For optimal noise shaping, the error-amplifier capacitor should be set to a small value. This results in a broadband spectrum where the error amplifier pushes the noise created by the clock jitter and PWM sampling above the audio range. However, there is a limit. Because the triangle-wave capacitor tracks the error-amplifier capacitor, small capacitor values can clip the triangle wave as it runs out of supply. This effect is aggravated at high PVDD voltages by the ADC action that decreases the integrator resistor at higher supply voltages. Tables 20 and 21 are lookup tables to facilitate choosing the optimal setting for the error-amplifier capacitance (MAP.COMP[2:0]).

It is possible to change this setting instantaneously while playing music, but if there is no music, a slight audible click is heard at the speakers. Systems that monitor the input voltage can take advantage of this instantaneous programmability and use a smaller error-amplifier capacitor at lower PVDD voltages. Higher switching frequencies also allow the use of a smaller integrator capacitor, and thus help improve the noise performance of the amplifier.

Do not set the error-amplifier capacitor to a value less than 18pF. Doing so results in extreme distortion, as the triangle wave clips. The MAP.COMP[2:0] settings that result in this behavior are listed as reserved (Table 19).

### Advantage of Feedback After the Filter

High-fidelity audio amplifiers require very low output impedance. The device achieves this by using a dual-feedback approach. The digital feedback (feedback from OUT__ outputs) emulates current-mode enabling on chip compensation. The analog feedback (FB__ inputs) significantly reduces the output impedance of the amplifier and at the same time, compensates for the nonideal characteristics of the output filter. If the characteristics of the speaker and/or output filter change with age or temperature, the analog feedback compensates accordingly. Further inductor matching is less critical because the inductors are inside the feedback loop. Because the inductors are inside the feedback loop, the loop can dampen out any LC ringing that might occur when the amplifier is used as a line driver. The analog feedback is differential so it does not help with common-mode ringing. Thus, the Zobel (RC) networks are required on each speaker connection to damp any common-mode ringing associated with the LC output filter and speaker.

### Operating Modes

Configure the device for one of three states of activity: normal, standby, or shutdown.

#### Normal

In normal mode, the device is ready for play. Placing the device in standby reduces power consumption while keeping fault monitors and the I²C interface on to communicate fault conditions. In shutdown, the device is completely disabled and draws minimal current from the battery.

To reset the device and clear all register contents to their reset values, set CTRL5.RST to 1. After reset, this bit is automatically cleared back to 0.

#### Standby

In standby, all circuitry is disabled except the fault monitors and the I²C interface. The I²C registers retain their content and are still interactive. To place the device in standby, set the CTRL2.STBY bit to 1. In standby, the device draws 11mA from all power-supply inputs.

Before exiting standby, always set the CTRL1.CL_TH (current-limit threshold setting) bit to 1. After exiting standby, clear CTRL1.CL_TH back to 0.

## Table 1. Operating Modes

| MODE | EN | CTRL2.STBY | I²C | FAULT MONITORS | ALL OTHER CIRCUITRY |
|---|---|---|---|---|---|
| Normal | High | 0 | Enabled | On | On |
| Standby | High | 1 | Enabled | On | Off |
| Shutdown | Low | X | Off | Off | Off |

*X = Don't care*

# 4-Channel, Automotive Class D Audio Amplifier

### Shutdown

In shutdown, all circuitry including the fault monitors and I²C interface is disabled to reduce power consumption and extend battery life. Connect EN to logic-high for normal operation. Connect EN to GND to place the device in a low-power shutdown mode. In shutdown, the devices draw 17mA (typ) from the battery.

### Clock Source

The device supports fixed-frequency modulation with an internal or external clock. The modulation mode is selected through CTRL1.CM[1:0] (operating mode select bits).

### Master Configuration

In master mode, 10 modulation frequencies are available in fixed-frequency modulation mode. Program CTRL0.MDIV[3:0] (master clock-divide ratio bits) for the desired frequency.

### Slave Configuration

Configuring the device as a slave allows an external clock source to provide the switching frequency. In this case, apply the external clock signal at SYNC at double the desired switching frequency.

### Fixed-Frequency Modulation Mode

The devices supports a fixed-frequency modulation mode with 10 different selectable frequencies between 300kHz and 750kHz. The frequency is selectable through the I²C interface. The frequency spectrum consists of the fundamental switching frequency and its associated harmonics (see the wideband output spectrum graphs in the *Typical Operating Characteristics*). For applications where exact spectrum placement of the switching fundamental is important, program the switching frequency so that the harmonics do not fall within a sensitive frequency band.

### Spread Spectrum

The device features a unique spread-sprectrum mode that flattens the wideband spectral components, improving EMI emissions that can be radiated by the speaker and cables. This feature is only available in master clock mode and is enabled by setting the CTRL5.SS[2:0] and CTRL5.SSEN bits. In spread-spectrum mode, the switching frequency vaies linearly by up to 7% depending on CTRL5.SS[2:0] setting. The modulation scheme remains the same, but the period of the triangle waveform changes from cycle to cycle. Instead of a large amount of spectral energy present at multiples of the switching frequency, the energy is now spread over a bandwidth that increases with frequency. Above a few megahertz, the wideband spectrum looks like white noise for EMI purposes. A proprietary amplifier topology ensures this does not significantly increase the noise floor in the audio bandwidth.

### Efficiency

The high efficiency of a Class D amplifier is due to the switching operation of the output stage transistors. In a Class D amplifier, the output transistors act as current-steering switches and consume negligible additional power. Any power loss associated with the Class D output stage is mostly due to the I²R loss of the MOSFET on-resistance and quiescent current overhead. The theoretical best efficiency of a linear amplifier is 78% at peak output power. Under normal operating levels (typical music reproduction levels), the efficiency falls below 30%, whereas the device exhibits > 80% efficiency under the same conditions (Figure 2).

### Current Limit

The current limit of the outputs is selectable between 7A (typ) and 8.75A (typ) through the CTRL3.HCL bit.

When the current limit is exceeded, the affected output is latched off and its corresponding overcurrent indicator bit OSTAT0.$\overline{OC[3:0]}$ is set to 0. The device does not attempt to activate the output until instructed by the microcontroller to do so. After eliminating the cause of the current limit, reactivate the output by setting OSTAT0.$\overline{OC[3:0]}$ to 1.

Short to either ground or battery causes the output to be latched off and its corresponding OSTAT0.$\overline{OC[3:0]}$ bit to be set to 0. After removing the short, reactivate the output by setting OSTAT0.$\overline{OC[3:0]}$ to 1.

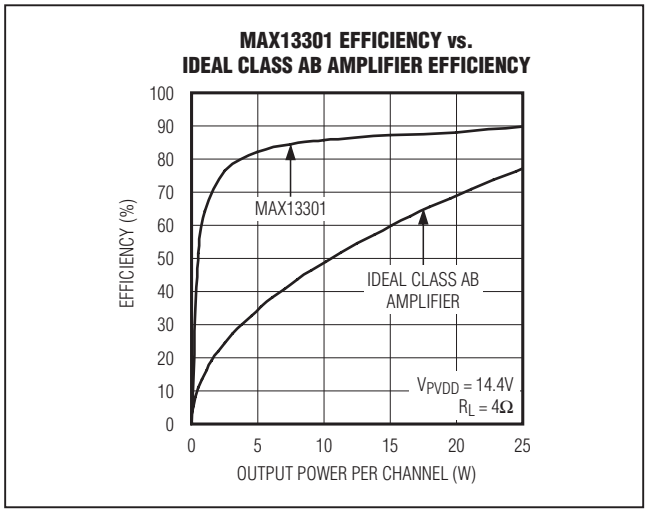



*Figure 2. Efficiency vs. Output Power of Class AB Amplifier and the MAX13301*

The device has real-time current limit for shorted outputs, outputs shorted to battery, outputs shorted to ground, and outputs shorted to adjacent channels.

For shorted outputs, the devices enter cycle-by-cycle current limit. In a BTL configuration, current flows diagonally through two of the four FETs at any instant in time. If the current in either of these FETs reaches the current-limit threshold, then both turn off and the other pair of diagonal FETs turns on for a fixed time. This creates distortion, as the music clips. The internal logic of the device counts the cycle-by-cycle current-limit events, and if too many happen in a fixed amount of time, the devices latch off the faulted channel. Current limit is programmable with the I²C. When CTRL3.HCL = 1, the peak current is limited to 8.75A (typ). With CTRL3.HCL = 0, peak current is limited to 7A (typ).

Short-to-battery and short-to-ground take advantage of the diagonal flow of current in a full bridge to detect fault conditions. The load current during normal operation should be equal in the two diagonal FETs that are actively conducting current. When an output is shorted to battery or ground, the current is no longer equal and the degree of mismatch is a measure of the severity of the fault. If the mismatch threshold is exceeded in any channel, that channel is immediately shut down and an overcurrent fault is reported. The level of mismatch is programmable through I²C. When CTRL1.CL_TH = 0, the mismatch threshold is 3.09A with CTRL3.HCL = 0 and 3.86A with CTRL3.HCL = 1. When CTRL1.CL_TH = 1, the mismatch threshold is 1.03A with CTRL3.HCL = 0 and 1.28A with CTRL3.HCL = 1. The lower setting is preferred in that it can detect a misconfigured speaker. For example, the lower setting issues a fault if a 4Ω speaker is incorrectly connected between one of the outputs and ground. At startup, when a large snubber capacitor is present, the higher setting is sometimes required to avoid false trips. When the bridge starts switching, both snubber capacitors must be charged to half the battery. The charging current mimics a short to ground. Following the startup procedure is the best way to avoid issues with overcurrent faults.

### Mute/Precharging

The device features a clickless/popless mute mode. When muted, the volume at the speaker is reduced to an inaudible level. To mute the device, configure $\overline{\text{MUTE\_CL1}}$ as a mute input by setting MAP.MCLP (clip output mapping bit) to 0. Then drive the mute input low. Use the mute function during system power-up and power-down to ensure optimum click-and-pop performance.

It is also advisable to set CTRL1.PRE (precharge bit) to 1 after taking the device out of standby mode to precharge the input DC-blocking capacitors. This action should be part of any startup routine. Precharging the DC-blocking capacitors enhances click-and-pop performance. Capacitors that are 0.47µF/2µF in series with the inputs take about 1ms to be charged.

### Output Configuration

The four FETs forming the full-bridge output of each channel can be programmed into one of four states: high-impedance (default), forced overvoltage, mute, and play through the CTRL2.MD01_[1:0] (channels 0 and 1 output mode) and CTRL2.MD23_[1:0] (channels 2 and 3 output mode) bits. Channels 0 and 1 and channels 2 and 3 always share the same configuration.

In high-impedance mode, all four FETs are turned off. In forced overvoltage state, each half-bridge output is regulated to 1/2 $V_{PVDD}$. In mute mode, the outputs continue to switch but the volume is kept to an inaudible level. In play mode, the FETs switch normally.

### I²C Interface

The device features an I²C, 2-wire serial interface consisting of a serial-data line (SDA) and a serial-clock line (SCL). SDA and SCL facilitate communication between the device and the master at clock rates up to 400kHz. When the device is used on an I²C bus with multiple devices, the $V_{DD}$ supply must stay powered on to ensure proper I²C bus operation. The master, typically a microcontroller, generates SCL and initiates data transfer on the bus. Figure 3 shows the 2-wire interface timing diagram.

A master device communicates to the IC by transmitting the proper address followed by the data word. Each transmit sequence is framed by a START (S) or repeated START (Sr) condition, and a STOP (P) condition. Each word transmitted over the bus is 8 bits long and is always followed by an acknowledge clock pulse.

The SDA line operates as both an input and an open-drain output. A pullup resistor, greater than 500Ω, is required on the SDA bus. The SCL line operates as an input only. A pullup resistor, greater than 500Ω, is required on SCL if there are multiple masters on the bus, or if the master in a single-master system has an open-drain SCL output. Series resistors in line with SDA and SCL are optional. The SCL and SDA inputs suppress noise spikes to ensure proper device operation even on a noisy bus.

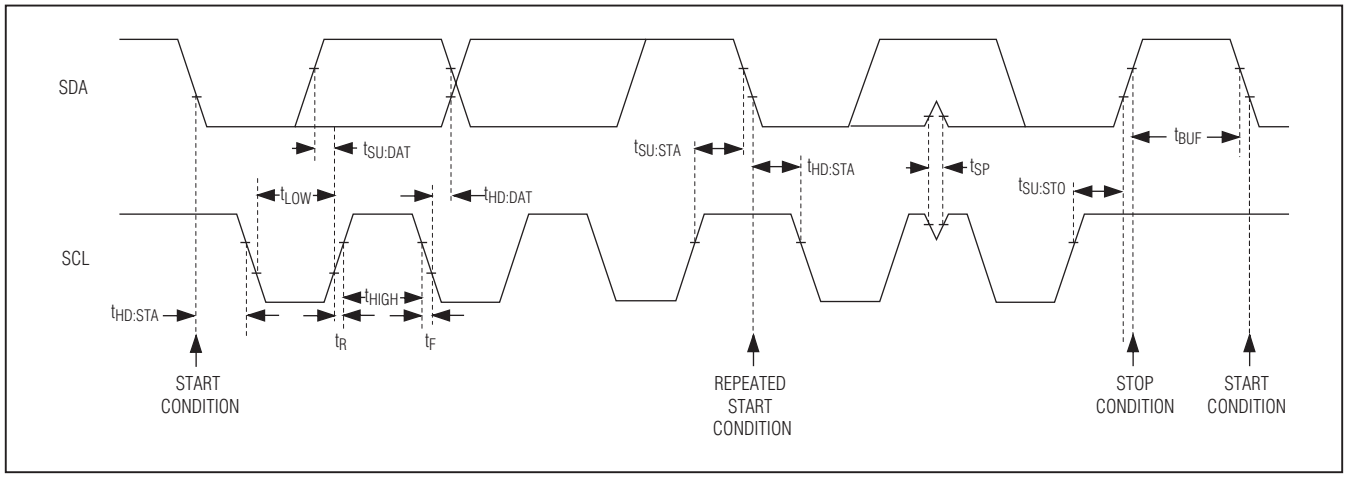



*Figure 3. 2-Wire Serial-Interface Timing Diagram*

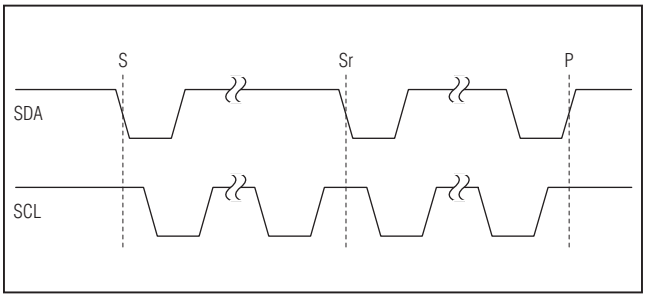



*Figure 4. START, STOP, and Repeated START Conditions*

### Bit Transfer

One data bit is transferred during each SCL cycle. The data on SDA must remain stable during the high period of the SCL pulse. Changes in SDA while SCL is high are control signals (see the *START and STOP Conditions* section). SDA and SCL idle high when the I²C bus is not busy.

### STOP and START Conditions

A master device initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA while SCL is high (Figure 4). A START condition from the master signals the beginning of a transmission to the device. The master terminates transmission and frees the bus by issuing a STOP condition. The bus remains active if a repeated START condition is generated instead of a STOP condition.

### Early STOP Condition

The device recognizes a STOP condition at any point during data transmission, except if the STOP condition occurs in the same high pulse as a START condition.

### Slave Address

Each time the device is enabled, the state of the $\overline{\text{MUTE\_CL1}}$ input is latched and determines the device's slave address. Table 2 shows the two possible hardware-defined slave addresses of the devices.

Once the device is enabled, it is programmable to one of four I²C slave addresses through CTRL4.ADDR[1:0] (I²C slave address setting bits), as shown in Table 3. When initially setting the slave address, use the default slave address as discussed in the previous paragraph and shown in Table 2. After setting the slave address, set the CTRL5.ADDR_DEF (I²C slave address definition bit) to 1. For subsequent reads and writes, use the new software-defined address. These slave addresses are unique device IDs.

The address is defined as the 7 most significant bits (MSBs) followed by the R/$\overline{\text{W}}$ bit. Set the R/$\overline{\text{W}}$ bit to 1 to configure the device to read mode. Set the R/$\overline{\text{W}}$ bit to 0 to configure the device to write mode. The address is the first byte of information sent to the device after the START condition.

## Table 2. Default Slave Address

| $\overline{\text{MUTE\_CL1}}$ | A6 | A5 | A4 | A3 | A2 | A1 | A0 | R/$\overline{W}$ | WRITE | READ |
|---|---|---|---|---|---|---|---|---|---|---|
| Low | 1 | 1 | 0 | 1 | 1 | 0 | 1 | X | 0xDA | 0xDB |
| High | 1 | 1 | 0 | 1 | 1 | 0 | 0 | X | 0xD8 | 0xD9 |

## Table 3. I²C Programmable Slave Address

| CTRL4. ADDR[1:0] | A6 | A5 | A4 | A3 | A2 | A1 | A0 | R/$\overline{W}$ | WRITE | READ |
|---|---|---|---|---|---|---|---|---|---|---|
| 00 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | X | 0xD8 | 0xD9 |
| 01 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | X | 0xDC | 0xDD |
| 10 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | X | 0xDA | 0xDB |
| 11 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | X | 0xDE | 0xDF |

### *Acknowledge*

The acknowledge bit (ACK) is a clocked 9th bit that the device uses to handshake receipt each byte of data (Figure 5). The device pulls down SDA during the master-generated 9th clock pulse. The SDA line must remain stable and low during the high period of the acknowledge clock pulse. Monitoring ACK allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master can reattempt communication.

### *Write Data Format*

A write to the device includes transmission of a START condition, the slave address with the write bit set to 0, one byte of data to register address, one byte of data to the command register, and a STOP condition. Figure 6 illustrates the proper format for one frame.

### *Read Data Format*

A read from the device includes transmission of a START condition, the slave address with the write bit set to 0, one byte of data to register address, restart condition, the slave address with read bit set to 1, one byte of data to the command register, and a STOP condition. Figure 6 illustrates the proper format for one frame.

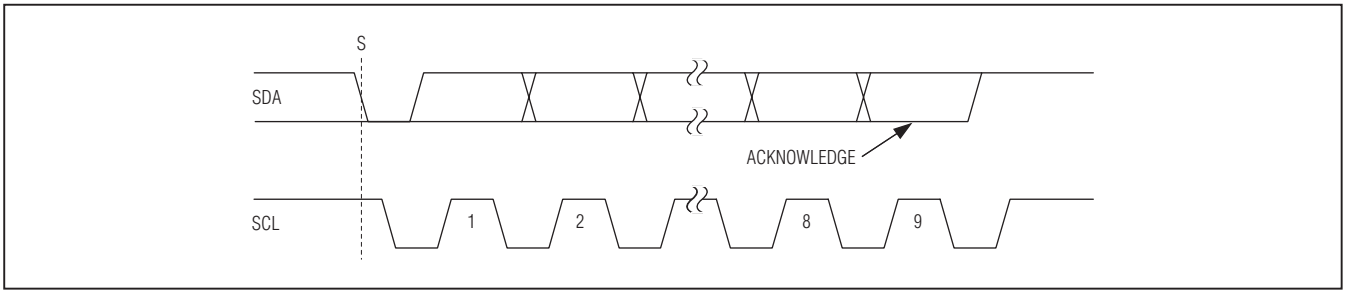



*Figure 5. Acknowledge Condition*

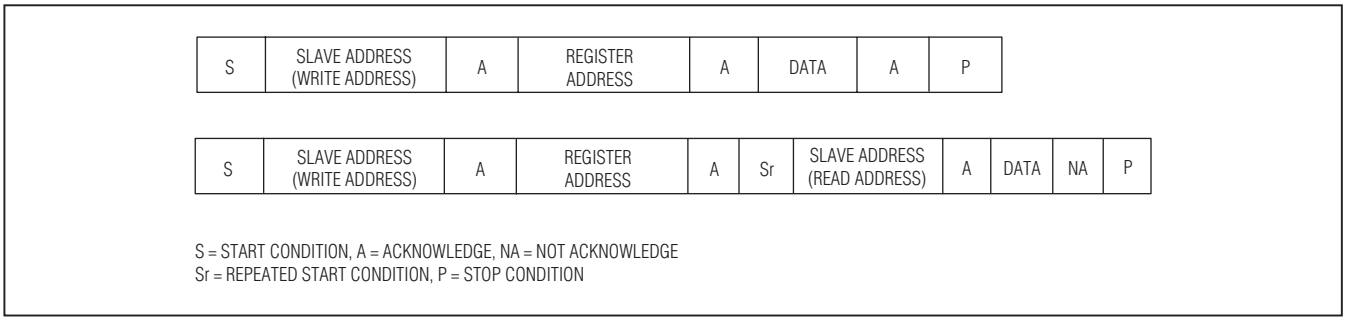



*Figure 6. Data Format of I²C Interface Write Mode Read Mode*

## Register Map

### Table 4. Register Map

| REGISTER | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 | ADDRESS | R/W | POWER-ON RESET (POR) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| CTRL0 | — | — | MDIV3 | MDIV2 | MDIV1 | MDIV0 | TW1 | TW0 | 0x00 | R/W | 0x24 |
| CTRL1 | — | CL_TH | CLVL1 | CLVL0 | — | PRE | CM1 | CM0 | 0x01 | R/W | 0x00 |
| CTRL2 | — | — | STBY | — | MD23_1 | MD23_0 | MD01_1 | MD01_0 | 0x02 | R/W | 0x20 |
| CTRL3 | TW | RDET | SDET | DIS | — | HCL | — | LDM | 0x03 | R/W | 0x00 |
| CTRL4 | — | — | ADDR1 | ADDR0 | — | — | — | — | 0x04 | R/W | 0xC0 |
| CTRL5 | SSEN | RST | SS2 | SS1 | SS0 | PAR1 | PAR0 | ADDR_DEF | 0x05 | R/W | 0x01 |
| MAP | COMP2 | COMP1 | COMP0 | OTWM | LCTM | MCLP | OTM | FLTM | 0x06 | R/W | 0x40 |
| STAT | — | $\overline{OT}$ | $\overline{OTW}$ | $\overline{OV}$ | $\overline{UV}$ | $\overline{OC}$ | $\overline{CPUV}$ | $\overline{CLIP}$ | 0x07 | R | — |
| OSTAT0 | $\overline{OC3}$ | $\overline{OC2}$ | $\overline{OC1}$ | $\overline{OC0}$ | $\overline{CLIP3}$ | $\overline{CLIP2}$ | $\overline{CLIP1}$ | $\overline{CLIP0}$ | 0x08 | R | — |
| OSTAT1 | $\overline{LDOK3}$ | $\overline{LDOK2}$ | $\overline{LDOK1}$ | $\overline{LDOK0}$ | $\overline{LOAD3}$ | $\overline{LOAD2}$ | $\overline{LOAD1}$ | $\overline{LOAD0}$ | 0x09 | R | — |
| OSTAT2 | $\overline{SBAT3}$ | $\overline{SBAT2}$ | $\overline{SBAT1}$ | $\overline{SBAT0}$ | $\overline{SGND3}$ | $\overline{SGND2}$ | $\overline{SGND1}$ | $\overline{SGND0}$ | 0x0A | R | — |
| OSTAT3 | — | — | — | VER | $\overline{VOS3}$ | $\overline{VOS2}$ | $\overline{VOS1}$ | $\overline{VOS0}$ | 0x0B | R | — |

### Table 5. Control Register 0

| CTRL0 | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **BIT #** | **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** |
| **NAME** | — | — | MDIV3 | MDIV2 | MDIV1 | MDIV0 | TW1 | TW0 |
| **POR** | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |

### Table 6. Control Register 0 Bit Description

| BIT | BIT DESCRIPTION |
|---|---|
| **MDIV[3:0]** | Master Clock-Divide Ratio. In master mode, the modulation and charge-pump frequencies are each set to 4.5MHz/(MDIV[3:0]). The device is in standby mode for MDIV[3:0] ≤ 3. The valid operating frequencies are 750kHz, 642.9kHz, 562.5kHz, 500kHz, 450kHz, 409.1kHz, 375kHz, 346.2kHz, 321.4kHz, and 300kHz. Switching frequencies below 450kHz compromises noise, as a larger integrator and triangle-wave capacitor trim setting is required.<br><br>In slave mode, the modulation and charge-pump frequency are always set to $f_{SYNC}/2$, where $f_{SYNC}$ is the frequency of the clock signal applied to the SYNC input. |
| **TW[1:0]** | Thermal Warning Threshold. This threshold determines the temperature at which the status bit STAT.$\overline{OTW}$ asserts.<br>00 = Junction temperature exceeds 110°C.<br>01 = Junction temperature exceeds 120°C.<br>10 = Junction temperature exceeds 130°C.<br>11 = Junction temperature exceeds 140°C. |

## Table 7. Control Register 1

| CTRL1 | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **BIT #** | **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** |
| **NAME** | — | CL_TH | CLVL1 | CLVL0 | — | PRE | CM1 | CM0 |
| **POR** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

## Table 8. Control Register 1 Bit Description

| BIT | BIT DESCRIPTION |
|---|---|
| **CL_TH** | Selects the current threshold for the real-time short-to-ground and short-to-battery detection diagnostics. Set this bit to 0 before exiting high-Z mode to prevent false triggering of short-to-ground and short-to-battery faults during startup. Set this bit to 1 after the device has entered mute or play mode.<br>0 = High threshold<br>1 = Normal threshold |
| **CLVL[1:0]** | Clip Level. The clip level provides an indication of the amount of total harmonic distortion in the output signal.<br>00 = THD exceeds 10%<br>10 = THD exceeds 5%<br>01 = THD exceeds 3%<br>11 = THD exceeds 1% |
| **PRE** | Precharge. Use PRE to precharge the input DC-blocking capacitors. Set this bit to 1 as part of the startup procedure. A 2µF capacitor for IN- and 0.47µF input blocking capacitors require a 1ms precharge to avoid startup pop.<br>0 = Disable precharging<br>1 = Enable precharging |
| **CM[1:0]** | Clock Mode. Before selecting the operating mode, three-state all outputs.<br>00 = Master fixed frequency, switching frequency set by the master clock-divide ratio (CTRL0.MDIV[3:0]) bits, SYNC output disabled<br>01 = Master fixed frequency, switching frequency set by the master clock-divide ratio (CTRL0.MDIV[3:0]) bits, SYNC output enabled<br>10 = Reserved<br>11 = Slave fixed frequency, SYNC input enabled |

## Table 9. Control Register 2

| CTRL2 | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **BIT #** | **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** |
| **NAME** | — | — | STBY | — | MD23_1 | MD23_0 | MD01_1 | MD01_0 |
| **POR** | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |

## Table 10. Control Register 2 Bit Description

| BIT | BIT DESCRIPTION |
|---|---|
| **STBY** | Standby Mode. Wait 50ms after exiting standby mode to allow the charge pump and reference to stabilize before entering mute or play mode.<br>0 = Normal mode<br>1 = Standby mode. The charge pump, preamplifier, and modulator are disabled. Fault monitors and I²C are still active. |
| **MD23_[1:0]** | Channels 2 and 3 Output Mode. Channels 2 and 3 are always in the same configuration. MD23_[1:0] determines the state of outputs 2 and 3.<br>00 = High-Z<br>01 = Mute<br>10 = Forced overvoltage. In this state, both differential outputs are charged to 1/2 $V_{PVDD}$.<br>11 = Play |
| **MD01_[1:0]** | Channels 0 and 1 Output Mode. Channels 0 and 1 are always in the same mode. MD01_[1:0] determines the state of outputs 0 and 1.<br>00 = High-Z<br>01 = Mute<br>10 = Force overvoltage. In this state, both differential outputs are charged to 1/2 $V_{PVDD}$.<br>11 = Play |

## Table 11. Control Register 3

| CTRL3 | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **BIT #** | **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** |
| **NAME** | TW | RDET | SDET | DIS | — | HCL | — | LDM |
| **POR** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

## Table 12. Control Register 3 Bit Description

| BIT | BIT DESCRIPTION |
|---|---|
| **TW** | Tweeter-Detect Current Threshold Setting<br>0 = The current threshold at which OSTAT1.$\overline{\text{LOAD[3:0]}}$ (load indicator bit) asserts is set equal to the shorted-load current threshold (see the *Electrical Characteristics* table). Use this setting when running shorted-load diagnostic.<br>1 = The current threshold at which OSTAT1.$\overline{\text{LOAD[3:0]}}$ asserts is set equal to the tweeter detect current threshold. This threshold is approximately 25% of the default value to facilitate tweeter detection. Use this setting when the running tweeter diagnostic or for detecting the presence of a speaker. |
| **RDET** | Open-Load Diagnostic Enable. Upon detecting an open load on any of the outputs, the corresponding OSTAT1.$\overline{\text{LDOK[3:0]}}$ (load OK indicator bit) asserts. Always perform short-to-ground and short-to-battery diagnosis before entering RDET mode. If a short-to-battery is detected, do not enter RDET mode. After performing the short-to-battery test, discharge both outputs by setting CTRL3.DIS to 1 for 200µs, then reset CTRL3.DIS back to 0. Failure to follow this procedure can result in a loud pop at the speaker.<br>Because the results are not latched, read $\overline{\text{LDOK[3:0]}}$ before clearing RDET. Wait a minimum of 200µs before reading these status bits. RDET can only be set after three-stating all four outputs. When performing the open-load diagnostic, set the CTRL3.SDET (short-to-ground/battery enable) bit to 0.<br>0 = Disable open-load diagnostic<br>1 = Enable open-load diagnostic |
| **SDET** | Short-to-Ground/Battery Diagnostic Enable. Upon detecting a short-to-ground or battery on any of the outputs, the corresponding OSTAT2.$\overline{\text{SBAT[3:0]}}$ (short-to-battery) and OSTAT2.$\overline{\text{SGND[3:0]}}$ (short-to-ground) bits assert. Because the results are not latched, read OSTAT2.$\overline{\text{SBAT[3:0]}}$ and OSTAT2.$\overline{\text{SGND[3:0]}}$ before clearing SDET. Wait a minimum of 200µs before reading these status bits. Before setting SDET to 1, three-state all four outputs and set the CTRL3.DIS (discharge output enable) bit to 1 and then reset back to 0. Before performing the short-to-ground/battery diagnostic, set the CTRL3.RDET (open-load diagnostic enable) bit to 0. To test for short-to-ground, set CTRL2.STBY to 0, and to test for short-to-battery, set CTRL2.STBY to 1.<br>0 = Disable short-to-ground/battery diagnostic<br>1 = Enable short-to-ground/battery diagnostic |
| **DIS** | Discharge Output Enable. Set DIS to 1 to discharge all outputs with 15mA current sources. Use DIS to discharge all outputs before performing the short-to-ground/battery diagnostic (SDET) to avoid a loud pop on the speaker. DIS can only be set to 1 after three-stating all four outputs.<br>0 = Output discharge is disabled.<br>1 = Output discharge is enabled. |
| **HCL** | Current-Limit Level. HCL sets the current-limit threshold of the outputs during normal operation.<br>0 = 7A (typ) current limit<br>1 = 8.75A (typ) current limit |
| **LDM** | Line-Driver Mode. Use LDM to set the load resistance threshold required to assert the OSTAT1.$\overline{\text{LDOK[3:0]}}$ (load-okay indicator bit). Any load with a resistance greater than the threshold is interpreted as an open output.<br>0 = Line-driver mode, OSTAT1.$\overline{\text{LDOK[3:0]}}$ = 1 if $R_L$ > 300Ω<br>1 = Power amplifier mode, OSTAT1.$\overline{\text{LDOK[3:0]}}$ = 1 if $R_L$ > 100Ω |

## Table 13. Control Register 4

| CTRL4 | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **BIT #** | **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** |
| **NAME** | — | — | ADDR1 | ADDR0 | — | — | — | — |
| **POR** | 1 | 1 | 0 | 0 | X | X | X | X |

## Table 14. Control Register 4 Bit Description

| BIT | BIT DESCRIPTION |
|---|---|
| **ADDR[1:0]** | I²C Slave Address Setting. Use ADDR[1:0] to set the slave address of the device. After setting the slave address, set CTRL5.ADDR_DEF (I²C slave address definition bit) to 1 to make the new address effective.<br>00 = Slave address set to 1101100 R/$\overline{W}$<br>01 = Slave address set to 1101110 R/$\overline{W}$<br>10 = Slave address set to 1101101 R/$\overline{W}$<br>11 = Slave address set to 1101111 R/$\overline{W}$ |

## Table 15. Control Register 5

| CTRL5 | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **BIT #** | **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** |
| **NAME** | SSEN | RST | SS2 | SS1 | SS0 | PAR1 | PAR0 | ADDR_DEF |
| **POR** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

## Table 16. Control Register 5 Bit Description

| BIT | BIT DESCRIPTION |
|---|---|
| **SSEN** | Spread-Spectrum Modulation Enable.<br>0: Spread-spectrum disabled; SSEN = 1 and SS[2:0] > 0: Spread-spectrum enabled |
| **RST** | Reset. Setting RST to 1 resets the device. In reset, all register bits are reset to their POR values. RST is automatically cleared back to 0 after device reset.<br>0 = Not in reset<br>1 = Reset |
| **SS[2:0]** | Spread-Spectrum Modulation Control. Spread-spectrum modulation is enabled when SSEN = 1 and SS[2:0] > 0, once enabled the switching frequency varies from +2% to +7% (see Table 17). |
| **PAR[1:0]** | Parallel Mode. The four outputs can be paralleled in one of four ways. To parallel outputs, connect the positive outputs together and connect the negative outputs together. In parallel mode, only the feedback inputs corresponding to the slaved input IN0+ or IN2+ are used. Connect the other feedback inputs to ground.<br>00 = 4-channel output<br>01 = 2.1-channel output. Outputs 0 and 1 are paralleled and slaved to input IN0+. Channels 2 and 3 are unaffected.<br>10 = 2.1-channel output. Outputs 2 and 3 are paralleled and slaved to input IN2+. Channels 0 and 1 are unaffected.<br>11 = 2-channel output. Outputs 0 and 1 are paralleled and slaved to input IN0+. Outputs 2 and 3 are paralleled and slaved to input IN2+. |
| **ADDR_DEF** | I²C Slave Address Definition. This bit determines whether the I²C slave address is hardware or software-defined.<br>0 = Slave address is defined by CTRL4.ADDR[1:0] (I²C slave address setting bits).<br>1 = Slave address is set to the default address as defined by the state of the $\overline{\text{MUTE\_CL1}}$ input when the enable input EN is pulled high. |

## Table 17. Spread-Spectrum Modulation Table

| SSEN | SS2 | SS1 | SS0 | SPREAD (%) |
|---|---|---|---|---|
| 0 | X | X | X | Disabled |
| 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 2 |
| 1 | 0 | 1 | 0 | 3 |
| 1 | 0 | 1 | 1 | 4 |
| 1 | 1 | 0 | 0 | 5 |
| 1 | 1 | 0 | 1 | 6 |
| 1 | 1 | 1 | 0 | 7 |
| 1 | 1 | 1 | 1 | Reserved |

## Table 18. Mapping Register

| MAP | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **BIT #** | **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** |
| **NAME** | COMP2 | COMP1 | COMP0 | OTWM | LCTM | MCLP | OTM | FLTM |
| **POR** | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

## Table 19. Mapping Register Bit Description

| BIT | BIT DESCRIPTION |
|---|---|
| **COMP[2:0]** | Integrator and Triangle-Wave Capacitor Trim. A smaller integrator capacitor pushes noise out of the audio band yielding the lowest noise. If distortion rises at high output powers, lower switching frequencies, or higher PVDD voltages then use a larger capacitor setting. See Table 20 for choosing minimum capacitor settings based on PVDD and the switching frequency. Larger capacitor values can be used.<br><br>If all 4 channels of the amplifier are used to drive subwoofers, the capacitor settings can be relaxed because a smaller capacitor setting helps to eliminate high-frequency noise (greater than 10kHz). Systems with multiple tweeters benefit the most from proper COMP[2:0] selection. Lower switching frequencies are possible when this high-frequency noise is not a concern as with systems that lack tweeters.<br><br>000 = 43pF<br>001 = 37pF<br>010 = 31pF<br>011 = 25pF<br>100 = 18pF<br>101 = Reserved<br>110 = Reserved<br>111 = Reserved |
| **OTWM** | Overtemperature Warning Mapping Bit<br>0 = STAT.$\overline{\text{OTW}}$ (overtemperature warning bit) is unmapped to the $\overline{\text{FLT\_OT}}$ open-drain output.<br>1 = STAT.$\overline{\text{OTW}}$ is mapped to $\overline{\text{FLT\_OT}}$ when MAP.OTM = 1. |
| **LCTM** | Low-Current Threshold Mapping Bit. The current thresholds used in tweeter and shorted load diagnostics are lower than the current limit. When the threshold is exceeded in running either diagnostic, OSTAT1.$\overline{\text{LOAD[3:0]}}$ (load indicator bit) asserts. Hardware indication is also possible by using LCTM to map OSTAT1.$\overline{\text{LOAD[3:0]}}$ to the $\overline{\text{CL0}}$ and $\overline{\text{MUTE\_CL1}}$ outputs.<br>0 = OSTAT1.$\overline{\text{LOAD[3:0]}}$ (load indicator bit used for tweeter and shorted load diagnostics) is unmapped to the $\overline{\text{CL0}}$ and $\overline{\text{MUTE\_CL1}}$ outputs.<br>1 = OSTAT1.$\overline{\text{LOAD[3:0]}}$ is mapped to the $\overline{\text{CL0}}$ and $\overline{\text{MUTE\_CL1}}$ outputs. Use this setting only when running tweeter or shorted load diagnostic. |
| **MCLP** | Clip Output Mapping. MCLP determines which open-drain outputs ($\overline{\text{CL0}}$ and $\overline{\text{MUTE\_CL1}}$) are used to indicate clipping on an audio output. $\overline{\text{CL0}}$ is always used as a clip indicator, while $\overline{\text{MUTE\_CL1}}$ is configurable as a clip indicator output or as a mute input.<br>0 = $\overline{\text{CL0}}$ provides clip indication for all audio outputs; $\overline{\text{MUTE\_CL1}}$ is configured as a mute input.<br>1 = $\overline{\text{CL0}}$ provides clip indication for audio outputs 0 and 1; $\overline{\text{MUTE\_CL1}}$ is configured as a clip indicator output for audio outputs 2 and 3. |
| **OTM** | Overtemperature Shutdown Map<br>0 = STAT.$\overline{\text{OT}}$ (overtemperature shutdown bit) is unmapped to the open-drain $\overline{\text{FLT\_OT}}$ output.<br>1 = STAT.$\overline{\text{OT}}$ is mapped to the $\overline{\text{FLT\_OT}}$ output. |
| **FLTM** | Fault Mapping Bit<br>0 = Faults are unmapped to the open-drain $\overline{\text{FLT\_OT}}$ output.<br>1 = Any fault condition (as indicated by the status bits $\overline{\text{OV}}$, $\overline{\text{UV}}$, $\overline{\text{OC}}$) causes $\overline{\text{FLT\_OT}}$ to assert low. |

## Table 20. COMP[2:0] Setting Lookup Table

| $f_{SW}/V_{PVDD}$ | < 8V | 8V to 9.5V | 9.5V to 12.65V | 12.65V to 15.6V | 15.6V to 18.65V | 18.65V to 21.1V | > 21.1V |
|---|---|---|---|---|---|---|---|
| 300k | 100 | 100 | 100 | 011 | 011 | 010 | 001 |
| 320k | 100 | 100 | 100 | 011 | 011 | 010 | 010 |
| 346k | 100 | 100 | 100 | 100 | 011 | 010 | 010 |
| 375k | 100 | 100 | 100 | 100 | 011 | 011 | 010 |
| 409k | 100 | 100 | 100 | 100 | 100 | 011 | 011 |
| 450k | 100 | 100 | 100 | 100 | 100 | 011 | 011 |
| 475k | 100 | 100 | 100 | 100 | 100 | 100 | 011 |
| 500k | 100 | 100 | 100 | 100 | 100 | 100 | 011 |
| 530k | 100 | 100 | 100 | 100 | 100 | 100 | 011 |
| 562k | 100 | 100 | 100 | 100 | 100 | 100 | 100 |
| 600k | 100 | 100 | 100 | 100 | 100 | 100 | 100 |
| 643k | 100 | 100 | 100 | 100 | 100 | 100 | 100 |
| 675k | 100 | 100 | 100 | 100 | 100 | 100 | 100 |
| 700k | 100 | 100 | 100 | 100 | 100 | 100 | 100 |
| 725k | 100 | 100 | 100 | 100 | 100 | 100 | 100 |
| 750k | 100 | 100 | 100 | 100 | 100 | 100 | 100 |

## Table 21. Status Register

| STAT | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **BIT #** | **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** |
| **NAME** | — | $\overline{OT}$ | $\overline{OTW}$ | $\overline{OV}$ | $\overline{UV}$ | $\overline{OC}$ | $\overline{CPUV}$ | $\overline{CLIP}$ |

## Table 22. Status Register Bit Description

| BIT | BIT DESCRIPTION |
|---|---|
| **$\overline{OT}$** | Overtemperature Shutdown. The device goes into thermal shutdown when the junction temperature exceeds +150°C.<br>0 = Device is in thermal shutdown.<br>1 = Device is not in thermal shutdown. |
| **$\overline{OTW}$** | Overtemperature Warning. $\overline{OTW}$ asserts when the junction temperature exceeds the thermal warning threshold programmed in CTRL0.TW[1:0].<br>0 = Junction temperature is greater than the programmed thermal warning threshold.<br>1 = Junction temperature is less than the programmed thermal warning threshold. |
| **$\overline{OV}$** | Overvoltage Indicator<br>0 = $V_{PVDD}$ is greater than the PVDD overvoltage lockout (OVLO) threshold as defined in the *Electrical Characteristics* table.<br>1 = $V_{PVDD}$ is less than the OVLO threshold. |
| **$\overline{UV}$** | Undervoltage Indicator<br>0 = $V_{PVDD}$ is less than the PVDD undervoltage lockout (UVLO) threshold as defined in the *Electrical Characteristics* table.<br>1 = $V_{PVDD}$ is greater than the UVLO threshold. |