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19-5159; Rev 1; 12/10

MAXIM

16-Bit, Data-Acquisition System with ADC, DACs, UPIOs, RTC, Voltage Monitors, and Temp Sensor

General Description

The MAX1358B smart data-acquisition system (DAS) is based on a 16-bit, sigma-delta analog-to-digital converter (ADC) and system-support functionality for a microprocessor (µP)-based system. This device integrates an ADC, DACs, operational amplifiers, internal selectable-voltage reference, temperature sensors, analog switches, a 32kHz oscillator, a real-time clock (RTC) with alarm, a high-frequency-locked loop (FLL) clock, four user-programmable I/Os, an interrupt generator, and 1.8V and 2.7V voltage monitors in a single chip.

The MAX1358B has dual 10:1 differential input multiplexers (muxes) that accept signal levels from 0 to AV_{DD}. An on-chip 1x to 8x programmable-gain amplifier (PGA) allows measuring low-level signals and reduces external circuitry required.

The MAX1358B operates from a single +1.8V to +3.6V supply and consumes only 1.15mA in normal mode and only 3µA in sleep mode. The MAX1358B has two DACs with one uncommitted op amp.

The serial interface is compatible with either SPI™/QSPI™ or MICROWIRE™, and is used to power up, configure, and check the status of all functional blocks.

The MAX1358B is available in a space-saving, 40-pin TQFN package and is specified over the commercial (0°C to +70°C) and the extended (-40°C to +85°C) temperature ranges.

Applications

Battery-Powered and Portable Devices

Electrochemical and Optical Sensors

Medical Instruments

Industrial Control

Data-Acquisition Systems

SPI/QSPI are trademarks of Motorola, Inc.
MICROWIRE is a trademark of National Semiconductor Corp.

Features

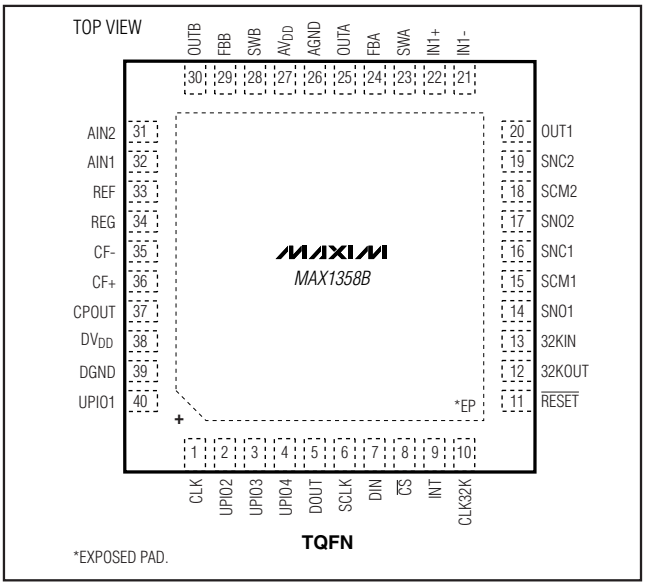
- **+1.8V to +3.6V Single-Supply Operation**
- **Multichannel, 16-Bit, Sigma-Delta ADC**
  - **10sps to 477sps Programmable Conversion Rate**
  - **Self- and System Offset and Gain Calibration**
  - **PGA with Gains of 1, 2, 4, or 8**
  - **Unipolar and Bipolar Modes**
  - **10-Input Differential Multiplexer**
- **10-Bit Force-Sense DACs**
- **Uncommitted Op Amps**
- **Dual SPDT and SPST Analog Switches**
- **Selectable References**
  - **1.25V, 2.048V, and 2.5V**
- **Internal Charge Pump**
- **System Support**
  - **RTC and Alarm Register**
  - **Internal/External Temperature Sensor**
  - **Internal Oscillator with Clock Output**
  - **User-Programmable I/O and Interrupt Generator**
  - **V_{DD} Monitors**
- **SPI/QSPI/MICROWIRE, 4-Wire Serial Interface**
- **Space-Saving (6mm x 6mm x 0.8mm), 40-Pin TQFN Package**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX1358BCTL+	0°C to +70°C	40 TQFN-EP*
MAX1358BETL+	-40°C to +85°C	40 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Pin Configuration



16-Bit, Data-Acquisition System with ADC, DACs, UPIOs, RTC, Voltage Monitors, and Temp Sensor

ABSOLUTE MAXIMUM RATINGS

AV_{DD} to AGND .....-0.3V to +4V
DV_{DD} to DGND .....-0.3V to +4V
AV_{DD} to DV_{DD} .....-4V to +4V
AGND to DGND.....-0.3V to +0.3V
CLK32K to DGND .....-0.3V to (DV_{DD} + 0.3V)
UPIO_ to DGND.....-0.3V to +4V
Digital Inputs to DGND .....-0.3V to +4V
Analog Inputs to AGND .....-0.3V to (AV_{DD} + 0.3V)
Digital Output to DGND.....-0.3V to (DV_{DD} + 0.3V)
Analog Outputs to AGND.....-0.3V to (AV_{DD} + 0.3V)
CPOUT.....(DV_{DD} - 0.3V) to +4V
Continuous Current Into Any Pin.....50mA
Continuous Power Dissipation (T_A = +70°C)
40-Pin TQFN (derate 25.6mW/°C above +70°C) 2051.3mW
Operating Temperature Range
MAX1358BCTL+ .....0°C to +70°C
MAX1358BETL+ .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Soldering Temperature (reflow) .....+260°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(AV_{DD} = DV_{DD} = +1.8V to +3.6V, V_{REF} = +1.25V, external reference, f_{CLK32K} = 32.768kHz (external clock), C_{REG} = 10µF, C_{CPOUT} = 10µF, 10µF between CF+ and CF-, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ADC DC ACCURACY						
Noise-Free Resolution		Data rate = 10sps, PGA gain = 2; data rate = 10sps to 60sps, PGA gain = 1; no missing codes, Table 1 (Note 2)	16			Bits
Conversion Rate		No missing codes, Table 1	10		477	sps
Output Noise		No missing codes		Table 1		
Integral Nonlinearity	INL	Unipolar mode, AV_{DD} = 3V, PGA gain = 1, data rate = 40sps		±0.0046		%FSR
Unipolar Offset Error (Note 3) or Bipolar Zero Error (Note 2, 3)		Uncalibrated		±1.0		%FSR
		PGA gain = 1, calibrated, T_A = +25°C, data rate = 10sps			±0.003	
Unipolar Offset-Error or Bipolar Zero-Error Temperature Drift (Note 4)		Bipolar		1		µV/°C
		Unipolar		1		
Gain Error (Notes 3, 5)		Uncalibrated		±0.6		%FSR
		PGA = 1, calibrated, data rate = 10sps		±0.003		
Gain-Error Temperature Coefficient		(Notes 4, 6)		2		ppm/°C
DC Positive Power-Supply Rejection Ratio	PSRR	PGA gain = 1, unipolar mode, measured by full-scale error with AV_{DD} = 1.8V to 3.6V		85		dB
ADC ANALOG INPUTS (AIN1, AIN2)						
DC Input Common-Mode Rejection Ratio	CMRR	PGA gain = 1, unipolar mode		85		dB

ELECTRICAL CHARACTERISTICS (continued)

(AV_{DD} = DV_{DD} = +1.8V to +3.6V, V_{REF} = +1.25V, external reference, f_{CLK32K} = 32.768kHz (external clock), C_{REG} = 10µF, C_{CPOUT} = 10µF, 10µF between CF+ and CF-, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Normal-Mode 60Hz Rejection Ratio		PGA gain = 1, unipolar mode, data rate = 40sps (Note 2)	100			dB
Normal-Mode 50Hz Rejection Ratio		Data rate = 10sps or 40sps, PGA gain = 1, unipolar mode (Note 2)	100			dB
Absolute Input Range			V_{AGND}		AV_{DD}	V
Differential Input Range		Unipolar mode	-0.05/ Gain		V_{REF}/ Gain	V
		Bipolar mode	-V_{REF}/ Gain		V_{REF}/ Gain	
DC Input Current (Note 7)		ADC not in measurement mode, mux enabled, $T_A \le +55°C$, inputs = +0.1V to (AV_{DD} - 0.1V)			±1	nA
		T_A = +85°C			±5	
Input Sampling Capacitance	C_{IN}			5		pF
Input Sampling Rate	f_{SAMPLE}			21.94		kHz
External Source Impedance at Input				Table 3		
FORCE-SENSE DAC (R_L = 10kΩ and C_L = 200pF, FBA = OUTA, unless otherwise noted)						
Resolution		Guaranteed monotonic	10			Bits
Differential Nonlinearity	DNL	Code 3D hex to 3FF hex			±1	LSB
Integral Nonlinearity	INL	Code 3D hex to 3FF hex			±4	LSB
Offset Error		Reference to code 52 hex			±20	mV
Offset-Error Tempco				5		µV/°C
Gain Error		Excludes offset and voltage reference error			±5	LSB
Gain-Error Tempco		Excludes offset and reference drift		5.6		ppm/°C
Input Leakage Current at SWA/B		Switches open (Notes 7, 8)			±1	nA
Input Leakage Current at FBA/B		V_{FBA} = +0.3V to (AV_{DD} - 0.3V) (Note 7), T_A = -40°C to +85°C			±1	nA
		V_{FBA} = +0.3V to (AV_{DD} - 0.3V) (Note 7), T_A = 0°C to +70°C			±600	pA
		V_{FBA} = +0.3V to (AV_{DD} - 0.3V) (Note 7), T_A = 0°C to +50°C			±400	
DAC Output Buffer Leakage Current		DAC buffer disabled (Note 7)			±75	nA
Input Common-Mode Voltage		At FBA	0		AV_{DD} - 0.35	V
Line Regulation		AV_{DD} = +1.8V to +3.6V, T_A = +25°C		40	175	µV/V
Load Regulation		I_{OUT} = ±2mA, C_L = 1000pF (Note 2)			0.5	µV/µA
Output Voltage Range			V_{AGND}		AV_{DD}	V

16-Bit, Data-Acquisition System with ADC, DACs, UPIOs, RTC, Voltage Monitors, and Temp Sensor

ELECTRICAL CHARACTERISTICS (continued)

(AV_{DD} = DV_{DD} = +1.8V to +3.6V, V_{REF} = +1.25V, external reference, f_{CLK32K} = 32.768kHz (external clock), C_{REG} = 10µF, C_{CPOUT} = 10µF, 10µF between CF+ and CF-, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Slew Rate		52 hex to 3FF hex code swing rising or falling, R_L = 10kΩ, C_L = 100pF			50		V/ms
Output-Voltage Settling Time		10% to 90% rising or falling to ±0.5 LSB			65		µs
Input-Voltage Noise		Referred to FBA, excludes reference noise	f = 0.1Hz to 10Hz		40		$µV_{P-P}$
			f = 10Hz to 10kHz		100		
Output Short-Circuit Current		OUTA shorted to AGND			20		mA
		OUTA shorted to AV_{DD}			18		
Input-Output SWA/SWB Switch Resistance		Between SW_ and OUT_, HFCLK enabled (Note 2)				150	Ω
SWA/SWB Switch Turn-On/Off Time		HFCLK enabled			100		ns
Power-On Time		Excluding reference			12		µs
EXTERNAL REFERENCE (REF)							
Input Voltage Range				V_{AGND}		AV_{DD}	V
Input Resistance		DAC on, internal REF and ADC off			2.5		MΩ
DC Input Leakage Current		Internal REF, DAC, and ADC off (Note 7)				100	nA
INTERNAL VOLTAGE REFERENCE (C_{REF} = 4.7µF)							
Reference Output Voltage	V_{REF}	AV_{DD} ≥ +1.8V, T_A = +25°C		1.213	1.25	1.288	V
		AV_{DD} ≥ +2.2V, T_A = +25°C		1.987	2.048	2.109	
		AV_{DD} ≥ +2.7V, T_A = +25°C		2.425	2.5	2.575	
Output-Voltage Temperature Coefficient (Note 7)	TC	T_A = -40°C to +85°C			25		ppm/°C
		T_A = 0°C to +70°C			13		
Output Short-Circuit Current	I_{RSC}	REF shorted to AGND			65		mA
		REF shorted to AV_{DD}			90		µA
Line Regulation					25		µV/V
Load Regulation		T_A = +25°C, V_{REF} = 1.25V	I_{SOURCE} = 0 to 500µA			1.2	µV/µA
			I_{SINK} = 0 to 50µA		1.7		

ELECTRICAL CHARACTERISTICS (continued)

(AV_{DD} = DV_{DD} = +1.8V to +3.6V, V_{REF} = +1.25V, external reference, f_{CLK32K} = 32.768kHz (external clock), C_{REG} = 10µF, C_{CPOUT} = 10µF, 10µF between CF+ and CF-, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Long-Term Stability		(Note 9)			150		ppm/1000hrs
Output Noise Voltage		f = 0.1Hz to 10Hz, AV_{DD} = 3V			50		μV_{P-P}
		f = 10Hz to 10kHz, AV_{DD} = 3V			200		
Turn-On Settling Time		Buffer only, settle to 0.1% of final value			100		µs
TEMPERATURE SENSOR							
Temperature Measurement Resolution		10sps			0.11		°C/LSB
Internal Temperature-Sensor Measurement Error (Note 10)		External voltage reference, two-current method	T_A = 0°C to +50°C		±0.5		°C
			T_A = -40°C to +85°C		±1		
External Temperature-Sensor Measurement Error (Note 11)		T_A = +25°C			±0.5		°C
		T_A = 0°C to +50°C			±0.5		
		T_A = -40°C to +85°C			±1.0		
Temperature Measurement Noise					0.18		$°C_{RMS}$
Temperature Measurement Power-Supply Rejection Ratio					0.2		°C/V
OP AMP							
Input Offset Voltage	V_{OS}	V_{CM} = 0.5V			±1	±15	mV
Offset-Error Tempco					6.2		µV/°C
Input Bias Current (Note 7)	I_{BIAS}	IN1+	T_A = -40°C to +85°C		0.006	±1	nA
			T_A = 0°C to +70°C		4	±300	pA
			T_A = 0°C to +50°C		2	±200	
		IN1-	T_A = -40°C to +85°C		0.025	±1	nA
			T_A = 0°C to +70°C		20	±600	pA
			T_A = 0°C to +50°C			±400	
Input Offset Current	I_{OS}	$V_{IN1\_}$ = +0.3V to (AV_{DD} - 0.3V) (Note 7)				±1	nA
Input Common-Mode Voltage Range	CMVR			0		AV_{DD} - 0.35	V
Common-Mode Rejection Ratio	CMRR	0 ≤ V_{CM} ≤ 75mV			60		dB
		75mV < V_{CM} ≤ AV_{DD} - 0.5V, T_A = +25°C		60	75		
		AV_{DD} - 0.5V ≤ V_{CM} ≤ AV_{DD} - 0.35V			75		

16-Bit, Data-Acquisition System with ADC, DACs, UPIOs, RTC, Voltage Monitors, and Temp Sensor

ELECTRICAL CHARACTERISTICS (continued)

(AV_{DD} = DV_{DD} = +1.8V to +3.6V, V_{REF} = +1.25V, external reference, f_{CLK32K} = 32.768kHz (external clock), C_{REG} = 10µF, C_{CPOUT} = 10µF, 10µF between CF+ and CF-, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Power-Supply Rejection Ratio	PSRR	AV_{DD} = +1.8V to +3.6V, T_A = +25°C		76.5	100		dB
Large-Signal Voltage Gain	A_{VOL}	100mV ≤ $V_{OUT\_}$ ≤ AV_{DD} - 100mV (Note 12)		90	116		dB
Output-Voltage Drop (Note 2)	ΔV_{OUT}	Sourcing	I_{SOURCE} = 10µA			0.005	V
			I_{SOURCE} = 50µA			0.025	
			I_{SOURCE} = 100µA			0.05	
			I_{SOURCE} = 500µA			0.25	
			I_{SOURCE} = 2mA			0.5	
		Sinking	I_{SINK} = 10µA			0.005	
			I_{SINK} = 50µA			0.025	
			I_{SINK} = 100µA			0.05	
			I_{SINK} = 500µA			0.25	
			I_{SINK} = 2mA			0.5	
Gain Bandwidth Product	GBW	Unity-gain configuration, C_L = 1nF			80		kHz
Phase Margin		Unity-gain configuration, C_L = 1nF (Note 12)			60		Degrees
Output Slew Rate	SR	C_L = 200pF			0.05		V/µs
Input-Voltage Noise		Unity-gain configuration	f = 0.1Hz to 10Hz		50		μV_{P-P}
			f = 10Hz to 10kHz		100		
Output Short-Circuit Current		$V_{OUT\_}$ shorted to AGND			20		mA
		$V_{OUT\_}$ shorted to AV_{DD}			18		
Power-On Time					12		µs
SPDT SWITCHES (SNO_, SNC_, SCM_, HFCLK enabled)							
On-Resistance (Note 2)	R_{ON}	$V_{SCM\_}$ = 0V	T_A = 0°C to +50°C			45	Ω
		$V_{SCM\_}$ = 0.5V	T_A = 0°C to +50°C			50	
		$V_{SCM\_}$ = 0.5V to AV_{DD}	T_A = -40°C to +85°C			150	
SNO_, SNC_ Off-Leakage Current	$I_{SNO\_(OFF)}$ $I_{SNC\_(OFF)}$	$V_{SNO\_}$, $V_{SNC\_}$ = +0.5V, +1.5V; $V_{SCM\_}$ = +1.5V, +0.5V (Note 7)	T_A = -40°C to +85°C			±1	nA
			T_A = 0°C to +70°C			±600	pA
			T_A = 0°C to +50°C			±400	
SCM_ Off-Leakage Current	$I_{SCM\_(OFF)}$	$V_{SNO\_}$, $V_{SNC\_}$ = +0.5V, +1.5V; $V_{SCM\_}$ = +1.5V, +0.5V (Note 7)	T_A = -40°C to +85°C			±2	nA
			T_A = 0°C to +70°C			±1.2	
			T_A = 0°C to +50°C			±0.8	
SCM_ On-Leakage Current	$I_{SCM\_(ON)}$	$V_{SNO\_}$, $V_{SNC\_}$ = +0.5V, +1.5V, or unconnected; $V_{SCM\_}$ = +1.5V, +0.5V (Note 7)	T_A = -40°C to +85°C			±2	nA
			T_A = 0°C to +70°C			±1.2	
			T_A = 0°C to +50°C			±0.8	
Input Voltage Range				V_{AGND}		AV_{DD}	V
Turn-On/Off Time	t_{ON}/t_{OFF}	Break-before-make			100		ns

ELECTRICAL CHARACTERISTICS (continued)

(AV_{DD} = DV_{DD} = +1.8V to +3.6V, V_{REF} = +1.25V, external reference, f_{CLK32K} = 32.768kHz (external clock), C_{REG} = 10µF, C_{CPOUT} = 10µF, 10µF between CF+ and CF-, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Capacitance		SNO_, SNC_, or SCM_ = AV_{DD} or AGND; switch connected to enabled mux input		2.5		pF
CHARGE PUMP						
Maximum Output Current	I_{OUT}		10			mA
Output Voltage		No load	3.2	3.3	3.6	V
		I_{OUT} = 10mA	3.0			
Output-Voltage Ripple		I_{OUT} = 10mA, excluding ESR of external capacitor (Note 2)			50	mV_{P-P}
Load Regulation		I_{OUT} = 10mA, excluding ESR of external capacitor		15	20	mV/mA
REG Input Voltage Range		Internal linear regulator disabled (Note 2)	1.6		1.8	V
REG Input Current		Linear regulator off, charge pump off		3		nA
CPOUT Input Voltage Range		Charge pump disabled	1.8		3.6	V
CPOUT Input Leakage Current		Charge pump disabled		2		nA
SIGNAL-DETECT COMPARATOR						
Differential Input-Detection Threshold Voltage		TSEL[2:0] = 0 hex		0		mV
		TSEL[2:0] = 4 hex		50		
		TSEL[2:0] = 5 hex		100		
		TSEL[2:0] = 6 hex		150		
		TSEL[2:0] = 7 hex		200		
Differential Input-Detection Threshold Error				±10		mV
Common-Mode Input Voltage Range			V_{AGND}		AV_{DD}	V
Turn-On Time				45		µs
VOLTAGE MONITORS						
DV_{DD} Monitor Supply Voltage Range		For valid reset (Note 7)	1.4		3.6	V
Trip Threshold (DV_{DD} Falling)			1.80	1.85	1.95	V
DV_{DD} Monitor Timeout Reset Period				1.5		s
DV_{DD} Monitor Hysteresis		HYSE bit set to logic 1		225		mV
		HYSE bit set to logic 0		40		

16-Bit, Data-Acquisition System with ADC, DACs, UPIOs, RTC, Voltage Monitors, and Temp Sensor

ELECTRICAL CHARACTERISTICS (continued)

(AV_{DD} = DV_{DD} = +1.8V to +3.6V, V_{REF} = +1.25V, external reference, f_{CLK32K} = 32.768kHz (external clock), C_{REG} = 10µF, C_{CPOUT} = 10µF, 10µF between CF+ and CF-, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DV_{DD} Monitor Turn-On Time				5		ms
CPOUT Monitor Supply Voltage Range		(Note 7)	1.4		3.6	V
CPOUT Monitor Trip Threshold			2.7	2.8	2.9	V
CPOUT Monitor Hysteresis				35		mV
CPOUT Monitor Turn-On Time				5		ms
Internal Power-On Reset Voltage					1.7	V
32kHz OSCILLATOR (32KIN, 32KOUT)						
Clock Frequency		DV_{DD} = 2.7V		32.768		kHz
Stability		DV_{DD} = 1.8V to 3.6V, excluding crystal		25		ppm
Oscillator Startup Time				1500		ms
Crystal Load Capacitance				6		pF
LOW-FREQUENCY CLOCK INPUT/OUTPUT (CLK32K)						
Output Clock Frequency				32.768		kHz
Absolute Input to Output Clock Jitter		Cycle to cycle		5		ns
Input to Output Rise/Fall Time		10% to 90%, 30pF load		5		ns
Input Duty Cycle			40		60	%
Output Duty Cycle				54		%
HIGH-FREQUENCY CLOCK OUTPUT (CLK)						
FLL Output Clock Frequency		f_{OUT} = f_{FLL}	4.8660	4.9152	4.9644	MHz
		f_{OUT} = f_{FLL}/2, power-up default	2.4330	2.4576	2.4822	MHz
		f_{OUT} = f_{FLL}/4	1.2165	1.2288	1.2411	MHz
		f_{OUT} = f_{FLL}/8	608.25	614.4	620.54	kHz
Absolute Clock Jitter		Cycle to cycle, FLL off		0.1		ns
		Cycle to cycle, FLL on		0.5		ns
Rise and Fall Time	t_R/t_F	10% to 90%, 30pF load			10	ns
Duty Cycle		f_{OUT} = 4.9152MHz	40		60	%
		f_{OUT} = 2.4576MHz, 1.2288MHz, 614.4kHz	45		55	%
Uncalibrated CLK Frequency Error		FLL calibration not performed			±35	%
DIGITAL INPUTS (SCLK, DIN, $\overline{CS}$, UPIO_, CLK32K)						
Input High Voltage	V_{IH}		0.7 x DV_{DD}			V
Input Low Voltage	V_{IL}				0.3 x DV_{DD}	V

ELECTRICAL CHARACTERISTICS (continued)

(AV_{DD} = DV_{DD} = +1.8V to +3.6V, V_{REF} = +1.25V, external reference, f_{CLK32K} = 32.768kHz (external clock), C_{REG} = 10µF, C_{CPOUT} = 10µF, 10µF between CF+ and CF-, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
UPIO_ Input High Voltage		DV_{DD} supply voltage	0.7 x DV_{DD}			V
		CPOUT supply voltage	0.7 x V_{CPOUT}			
UPIO_ Input Low Voltage		DV_{DD} supply voltage			0.3 x DV_{DD}	V
		CPOUT supply voltage			0.3 x V_{CPOUT}	
Input Hysteresis	V_{HYS}	DV_{DD} = 3.0V		200		mV
Input Current	I_{IN}	V_{IN} = V_{DGND} or DV_{DD} (Note 7)		±0.01	±100	nA
Input Capacitance		V_{IN} = V_{DGND} or DV_{DD}		4		pF
UPIO_ Input Current (Note 2)		V_{IN} = DV_{DD} or V_{CPOUT}, pullup enabled		±0.01	1	µA
		V_{IN} = DV_{DD} or V_{CPOUT} or 0V, pullup disabled			1	
UPIO_ Pullup Current		V_{IN} = 0V, pullup enabled, unconnected UPIO_ inputs are pulled up to DV_{DD} or CPOUT with pullup enabled (Note 2)	0.1	2	5	µA
DIGITAL OUTPUTS (DOUT, $\overline{RESET}$, UPIO_, CLK32K, INT, CLK)						
Output Low Voltage	V_{OL}	I_{SINK} = 1mA			0.4	V
Output High Voltage	V_{OH}	I_{SOURCE} = 500µA	0.8 x DV_{DD}			V
DOUT Three-State Leakage Current	I_L			±0.01	±1	µA
DOUT Three-State Output Capacitance	C_{OUT}			4.5		pF
$\overline{RESET}$ Output Low Voltage	V_{OL}	I_{SINK} = 1mA			0.4	V
$\overline{RESET}$ Output Leakage Current		Open-drain output, $\overline{RESET}$ deasserted (Note 7)			0.1	µA
UPIO_ Output Low Voltage	V_{OL}	I_{SINK} = 1mA, UPIO_ referenced to DV_{DD}			0.4	V
		I_{SINK} = 4mA, UPIO_ referenced to CPOUT			0.4	
UPIO_ Output High Voltage	V_{OH}	I_{SOURCE} = 500µA, UPIO_ referenced to DV_{DD}	0.8 x DV_{DD}			V
		I_{SOURCE} = 4mA, UPIO_ referenced to CPOUT	V_{CPOUT} - 0.4			
POWER REQUIREMENT						
Analog Supply Voltage Range	AV_{DD}		1.8		3.6	V
Digital Supply Voltage Range	DV_{DD}		1.8		3.6	V

16-Bit, Data-Acquisition System with ADC, DACs, UPIOs, RTC, Voltage Monitors, and Temp Sensor

ELECTRICAL CHARACTERISTICS (continued)

(AV_{DD} = DV_{DD} = +1.8V to +3.6V, V_{REF} = +1.25V, external reference, f_{CLK32K} = 32.768kHz (external clock), C_{REG} = 10µF, C_{CPOUT} = 10µF, 10µF between CF+ and CF-, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Total Supply Current (Note 2)	I_{MAX}	Everything on, charge pump unloaded, no digital pins, sinking/sourcing current, e.g., $\overline{RST}$, UPIO_, and CLK32K, max internal temp-sensor current, clock output buffers unloaded, ADC at 477sps	AV_{DD} = DV_{DD} = 3.6V		1.2	2.0	mA
			AV_{DD} = DV_{DD} = 2.7V		1.15	1.4	
	I_{NORMAL}	All on except charge pump and temp sensor, ADC at 477sps, CLK output buffer enabled, clock output buffers unloaded			1.15	1.5	
Sleep-Mode Supply Current (I_{AVDD} + I_{DVDD})	I_{SLEEP}	T_A = -40°C to +85°C	AV_{DD} = DV_{DD} = 2.7V		3.0	5.2	µA
			AV_{DD} = DV_{DD} = 3.6V			6.7	
		T_A = +25°C	AV_{DD} = DV_{DD} = 2.7V		3.0		
			AV_{DD} = DV_{DD} = 3.6V		4.5		
Shutdown Supply Current (I_{AVDD} + I_{DVDD})	I_{SHDN}	All off	T_A = -40°C to +85°C			2.5	µA
			T_A = +25°C		1.2		

Note 1: Devices are production tested at T_A = room temperature. Specifications to T_A = -40°C and T_A = +85°C are guaranteed by design.

Note 2: Guaranteed by design or characterization.

Note 3: The offset and gain errors are corrected by self-calibration or system calibration. For accurate calibrations, perform calibration at the lowest rate. The calibration error is therefore in the order of peak-to-peak noise for the selected rate.

Note 4: Eliminate drift errors by recalibration at the new temperature.

Note 5: The gain error excludes reference error, offset error (unipolar), and zero error (bipolar).

Note 6: Gain-error drift does not include unipolar-offset drift or bipolar zero-error drift. It is effectively the drift of the part if zero-scale error is removed.

Note 7: These specifications are obtained from characterization during design or from initial product evaluation. Not production tested or guaranteed.

Note 8: V_{OUTA} = +0.5V or +1.5V, V_{SWA} = +1.5V or +0.5V, T_A = 0°C to +50°C.

Note 9: Long-term stability is characterized using five to six parts. The bandgaps are turned on for 1000hrs at room temperature with the parts running continuously. Daily measurements are taken and any obvious outlying data points are discarded.

Note 10: Temperature error is the difference in the calculated temperature using the internal circuit vs. measurements made using precision external voltage and current meters. The same diode and diode equation are used for both measurements.

Note 11: All the stated temperature accuracies assume that 1) the external diode characteristic is precisely known (i.e., ideal) and 2) the ADC reference voltage is exactly equal to 1.25V. Any variations to this known reference characteristic and voltage caused by temperature, loading, or power supply results in errors in the temperature measurement. The actual temperature calculation is performed externally by the µC.

Note 12: Values based on simulation results and are not production tested or guaranteed.

Table 1. Output Noise (Notes 13 and 14)

RATE (sps)	OUTPUT NOISE (μV_{RMS})			
	GAIN = 1	GAIN = 2	GAIN = 4	GAIN = 8
10	1.75	1.75	1.75	1.75
40	2.92	2.92	2.92	2.92
50	3.23	3.23	3.23	3.23
60	3.60	3.60	3.60	3.60
200	56.06	56.06	56.06	56.06
240	102.36	102.36	102.36	102.36
400	587.06	587.06	587.06	587.06
477	951.07	951.07	951.07	951.07

Note 13: V_{REF} = +1.25V, bipolar mode, V_{IN} = 1.24912V, PGA gain = 1, T_A = +25°C.
Note 14: Assume ±3 sigma peak-to-peak variation; noise-free resolution means no code flicker at given bits' LSB.

Table 2. Peak-to-Peak Resolution

RATE (sps)	PEAK-TO-PEAK RESOLUTION (BITS)			
	GAIN = 1	GAIN = 2	GAIN = 4	GAIN = 8
10	17.57	16.57	15.57	14.57
40	16.83	15.83	14.83	13.83
50	16.68	15.68	14.68	13.68
60	16.53	15.53	14.53	13.53
200	12.57	11.57	10.57	9.57
240	11.70	10.70	9.70	8.70
400	9.18	8.18	7.18	6.18
477	8.48	7.48	6.48	5.48

Table 3. Maximum External Source Impedance Without 16-Bit Gain Error

PARAMETER	EXTERNAL CAPACITANCE (pF)					
	0 (Note 15)	50	100	500	1000	5000
Resistance (kΩ)	350	60	30	10	4	1

Note 15: 2pF parasitic capacitance is assumed, which represents pad and any other parasitic capacitance.

16-Bit, Data-Acquisition System with ADC, DACs, UPIOs, RTC, Voltage Monitors, and Temp Sensor

TIMING CHARACTERISTICS (Figures 1 and 19)

(AV_{DD} = DV_{DD} = +1.8V to +3.6V, external V_{REF} = +1.25V, f_{CLK32K} = 32.768kHz (external clock), C_{REG} = 10µF, C_{CPOUT} = 10µF, 10µF between CF+ and CF-, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLK Operating Frequency	f_{SCLK}		0		10	MHz
SCLK Cycle Time	t_{CYC}		100			ns
SCLK Pulse-Width High	t_{CH}		40			ns
SCLK Pulse-Width Low	t_{CL}		40			ns
DIN to SCLK Setup	t_{DS}		30			ns
DIN to SCLK Hold	t_{DH}		0			ns
SCLK Fall to DOUT Valid	t_{DO}	C_L = 50pF, Figure 2			40	ns
$\overline{CS}$ Fall to DOUT Enable	t_{DV}	C_L = 50pF, Figure 2			48	ns
$\overline{CS}$ Rise to DOUT Disable	t_{TR}	C_L = 50pF, Figure 2			48	ns
$\overline{CS}$ to SCLK Rise Setup	t_{CSS}		20			ns
$\overline{CS}$ to SCLK Rise Hold	t_{CSH}		0			ns
DV_{DD} Monitor Timeout Period	t_{DSLP}	(Note 16)		1.5		s
Wake-Up (WU) Pulse Width	t_{WU}	Minimum pulse width required to detect a wake-up event		1		µs
Shutdown Delay	t_{DPU}	The delay for $\overline{SHDN}$ to go high after a valid wake-up event		1		µs
HFCLK Turn-On Time (Note 2)	t_{DFON}	The turn-on time for the high-frequency clock and FLL (FLLE = 1) (Note 17)			10	ms
		If FLLE = 0, the turn-on time for the high-frequency clock (Notes 7, 18)			10	µs
CRDY to $\overline{INT}$ Delay	t_{DFI}	The delay for CRDY to go low after the HFCLK clock output has been enabled (Note 19)		7.82		ms
HFCLK Disable Delay	t_{DFOF}	The delay after a shutdown command has asserted and before HFCLK is disabled (Note 20)		1.95		ms
$\overline{SHDN}$ Assertion Delay	t_{DPD}	(Note 21)		2.93		ms

Note 16: The delay for the sleep voltage monitor output, $\overline{RESET}$, to go high after V_{DD} rises above the reset threshold. This is largely driven by the startup of the 32kHz oscillator.

Note 17: FLLE is gated by an AND function with three inputs—the external $\overline{RESET}$ signal, the internal DV_{DD} monitor output, and the external $\overline{SHDN}$ signal. The time delay is timed from the internal LOV_{DD} going high or the external $\overline{RESET}$ going high, whichever happens later. HFCLK always starts in the low state.

Note 18: If FLLE = 0, the internal signal CRDY is not generated by the FLL block and $\overline{INT}$ or INT is deasserted.

Note 19: CRDY is used as an interrupt signal to inform the µC that the high-frequency clock has started. Only valid if FLLE = 1.

Note 20: t_{DFOF} gives the µC time to clean up and go into sleep-override mode properly.

Note 21: t_{DPD} is greater than the HFCLK delay to clean up before losing power.

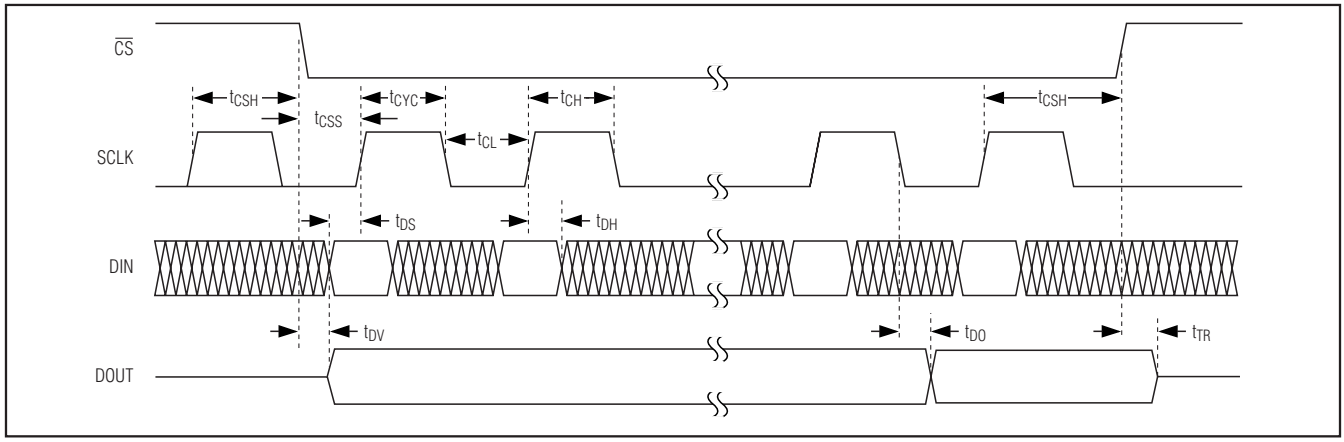


Figure 1. Detailed Serial-Interface Timing

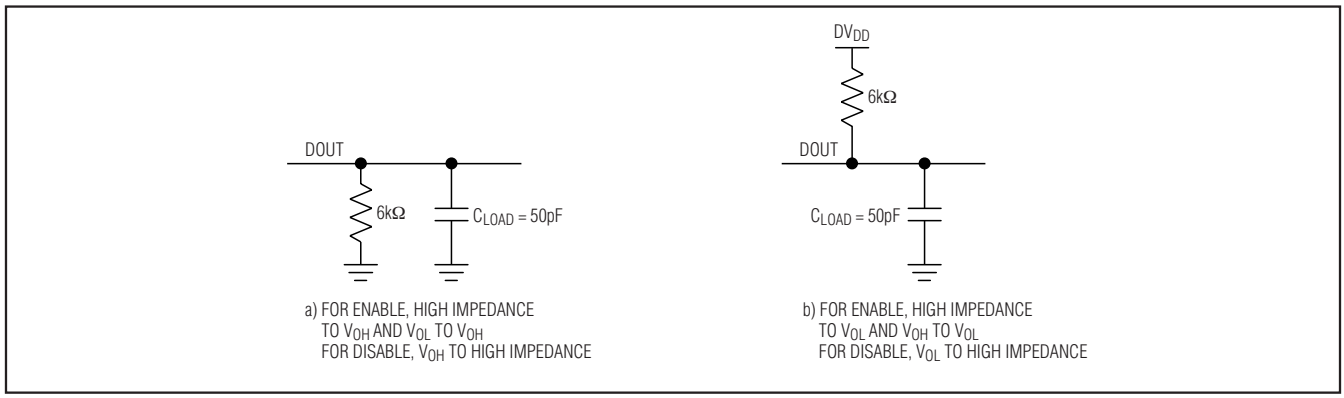
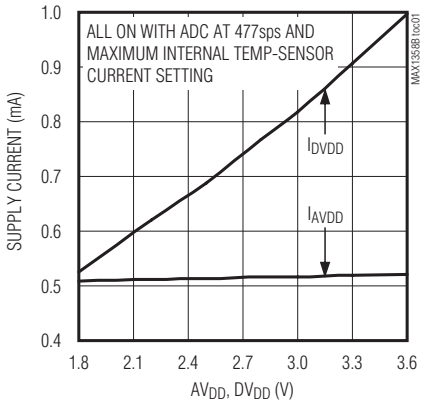


Figure 2. DOUT Enable and Disable Time Load Circuits

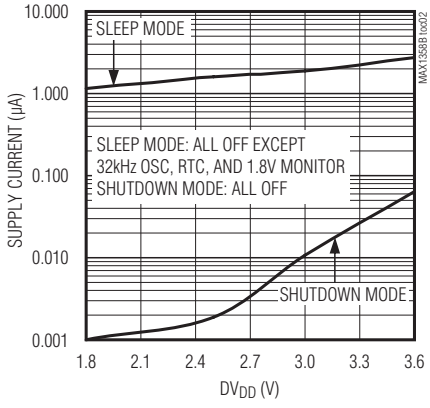
Typical Operating Characteristics

(DVDD = AVDD = 1.8V, VREF = +1.25V, CCPOUT = 10µF, TA = +25°C, unless otherwise noted.)

SUPPLY CURRENT vs. SUPPLY VOLTAGE



DVDD SUPPLY CURRENT vs. DVDD SUPPLY VOLTAGE

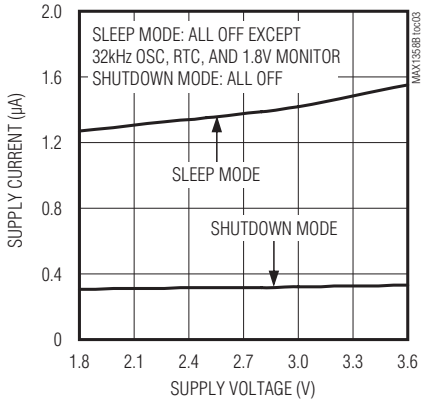


16-Bit, Data-Acquisition System with ADC, DACs, UPIOs, RTC, Voltage Monitors, and Temp Sensor

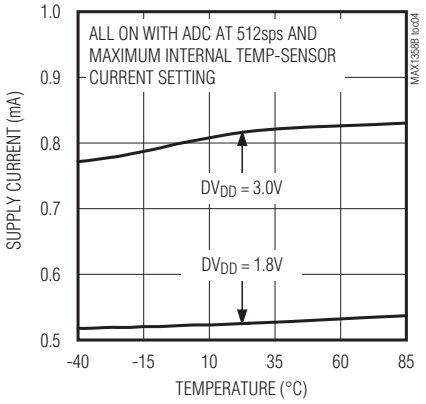
Typical Operating Characteristics (continued)

(DV_{DD} = AV_{DD} = 1.8V, V_{REF} = +1.25V, C_{CPOUT} = 10µF, T_A = +25°C, unless otherwise noted.)

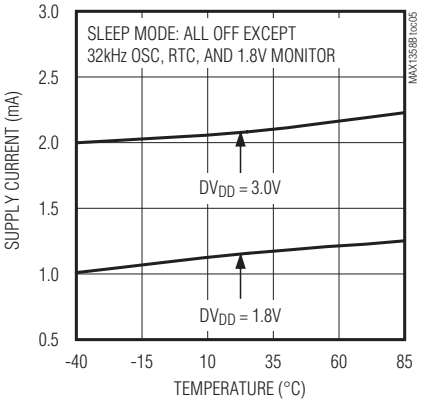
AV_{DD} SUPPLY CURRENT vs. AV_{DD} SUPPLY VOLTAGE



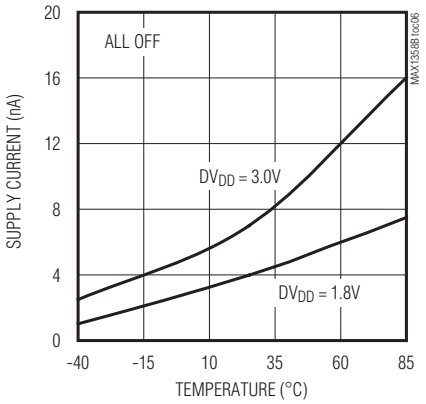
DV_{DD} SUPPLY CURRENT vs. TEMPERATURE



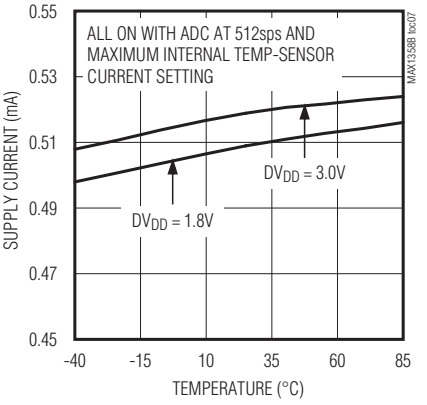
DV_{DD} SUPPLY CURRENT vs. TEMPERATURE



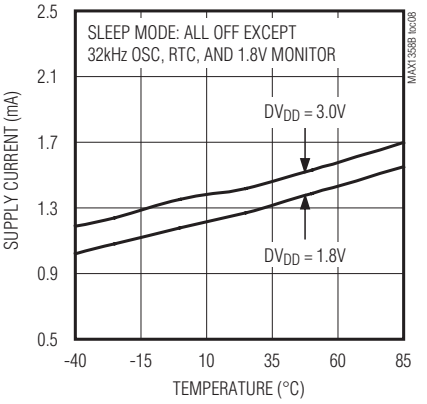
DV_{DD} SUPPLY CURRENT vs. TEMPERATURE



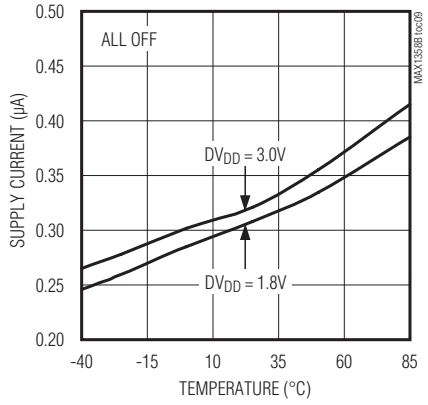
AV_{DD} SUPPLY CURRENT vs. TEMPERATURE



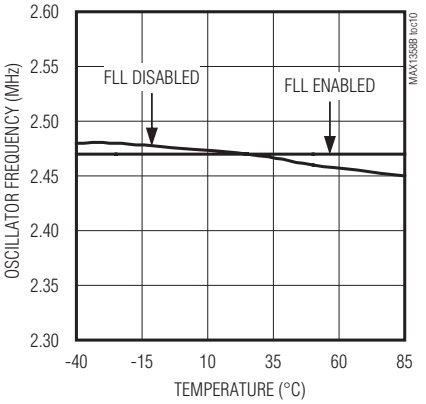
AV_{DD} SUPPLY CURRENT vs. TEMPERATURE



AV_{DD} SUPPLY CURRENT vs. TEMPERATURE



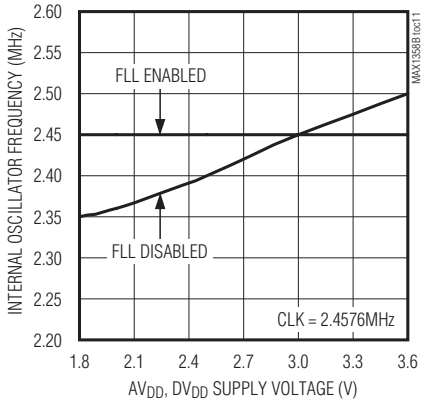
INTERNAL OSCILLATOR FREQUENCY vs. TEMPERATURE



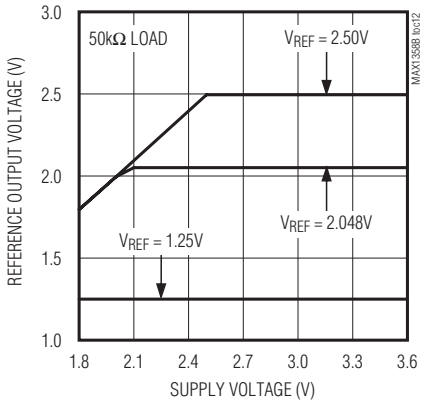
Typical Operating Characteristics (continued)

(DV_{DD} = AV_{DD} = 1.8V, V_{REF} = +1.25V, C_{CPOUT} = 10µF, T_A = +25°C, unless otherwise noted.)

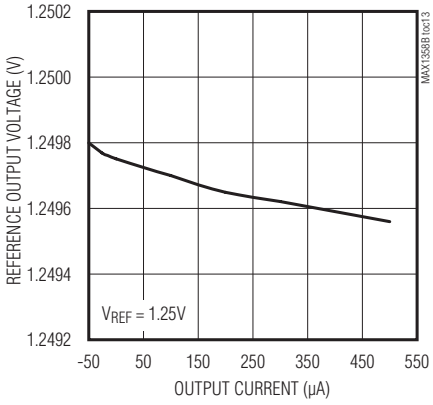
INTERNAL OSCILLATOR FREQUENCY vs. SUPPLY VOLTAGE



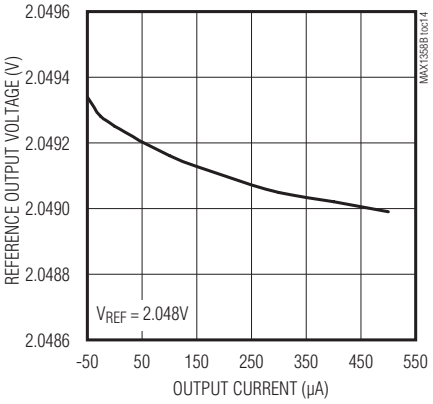
REFERENCE OUTPUT VOLTAGE vs. SUPPLY VOLTAGE



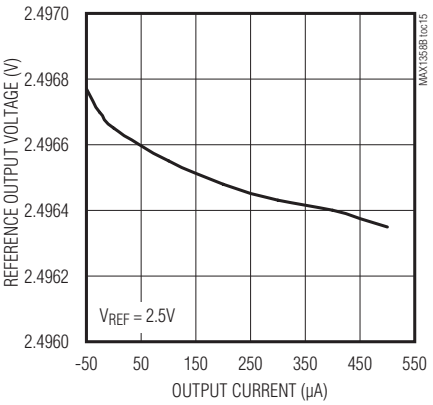
REFERENCE OUTPUT VOLTAGE vs. OUTPUT CURRENT



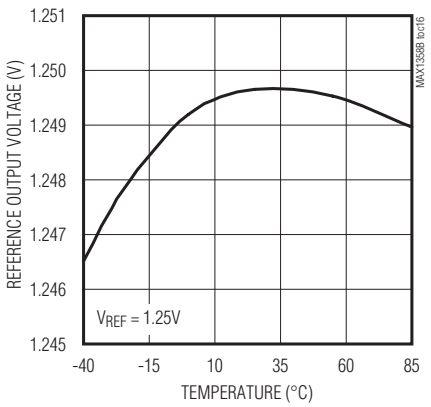
REFERENCE OUTPUT VOLTAGE vs. OUTPUT CURRENT



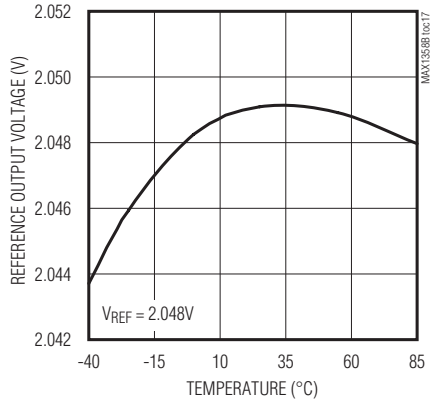
REFERENCE OUTPUT VOLTAGE vs. OUTPUT CURRENT



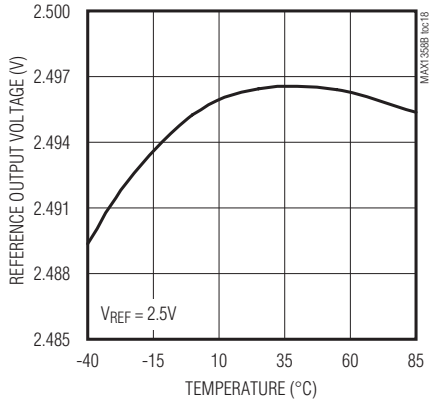
REFERENCE OUTPUT VOLTAGE vs. TEMPERATURE



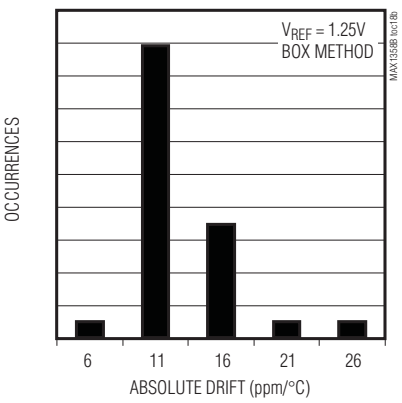
REFERENCE OUTPUT VOLTAGE vs. TEMPERATURE



REFERENCE OUTPUT VOLTAGE vs. TEMPERATURE



REFERENCE DRIFT (0°C TO 50°C)

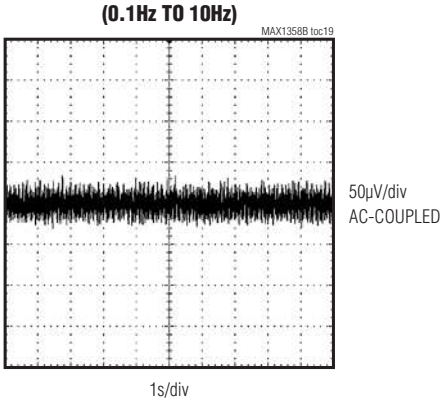


16-Bit, Data-Acquisition System with ADC, DACs, UPIOs, RTC, Voltage Monitors, and Temp Sensor

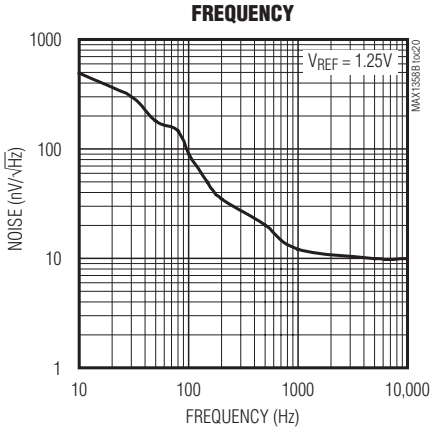
Typical Operating Characteristics (continued)

(DV_{DD} = AV_{DD} = 1.8V, V_{REF} = +1.25V, C_{CPOUT} = 10µF, T_A = +25°C, unless otherwise noted.)

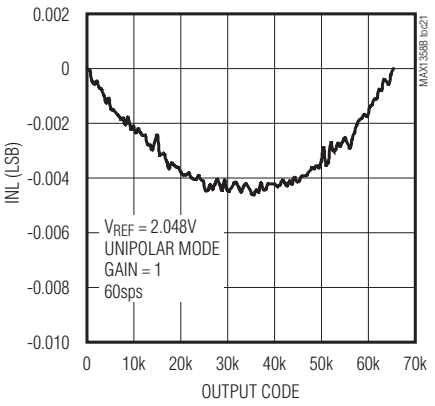
REFERENCE VOLTAGE OUTPUT NOISE (0.1Hz TO 10Hz)



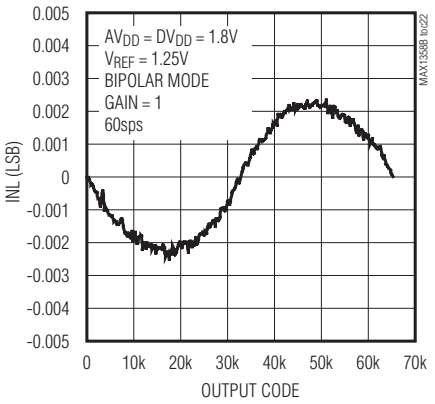
REFERENCE NOISE DENSITY vs. FREQUENCY



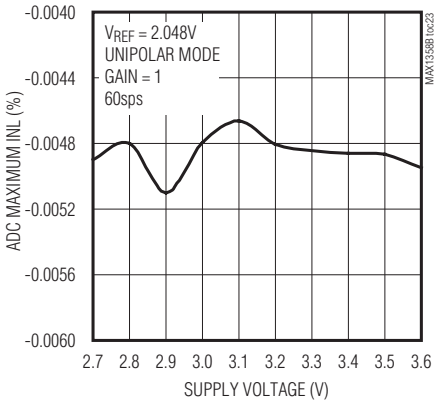
ADC INL vs. OUTPUT CODE



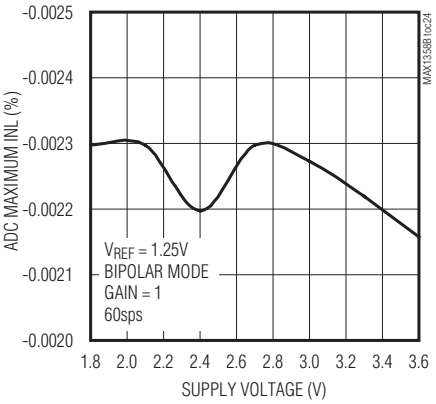
ADC INL vs. OUTPUT CODE



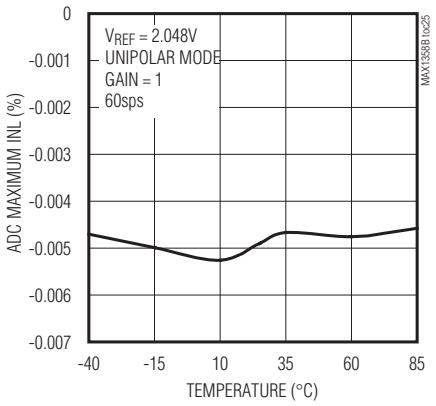
ADC MAXIMUM INL vs. SUPPLY VOLTAGE



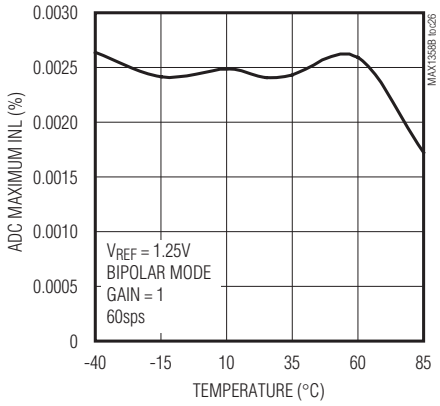
ADC MAXIMUM INL vs. SUPPLY VOLTAGE



ADC MAXIMUM INL vs. TEMPERATURE



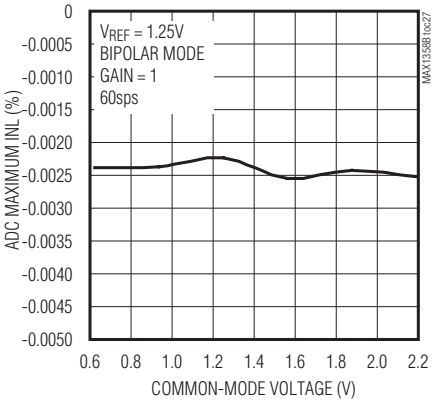
ADC MAXIMUM INL vs. TEMPERATURE



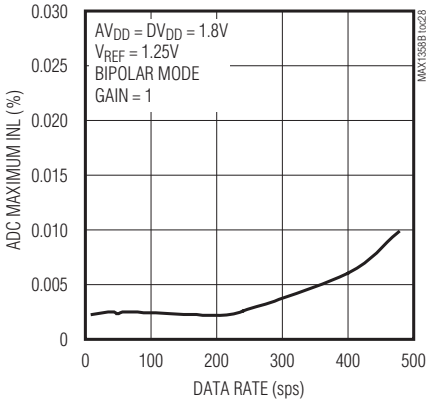
Typical Operating Characteristics (continued)

(DV_{DD} = AV_{DD} = 1.8V, V_{REF} = +1.25V, C_{CPOUT} = 10µF, T_A = +25°C, unless otherwise noted.)

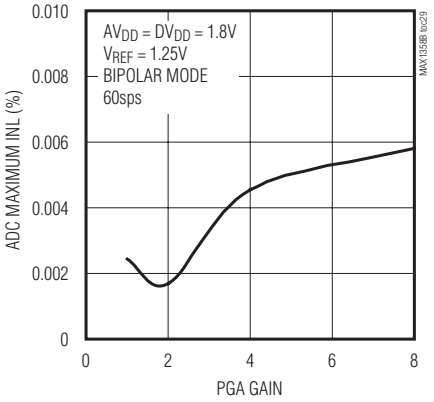
ADC MAXIMUM INL vs. COMMON-MODE INPUT VOLTAGE



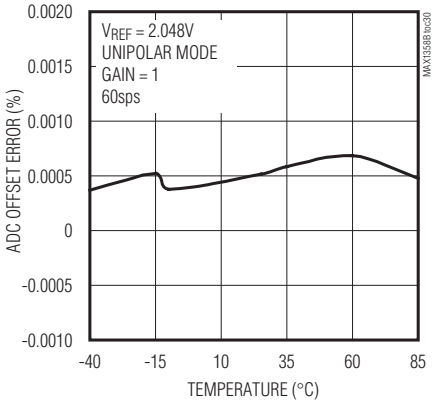
ADC MAXIMUM vs. OUTPUT DATA RATE



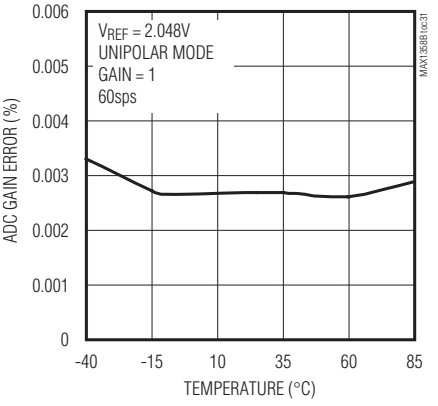
ADC MAXIMUM INL vs. PGA GAIN



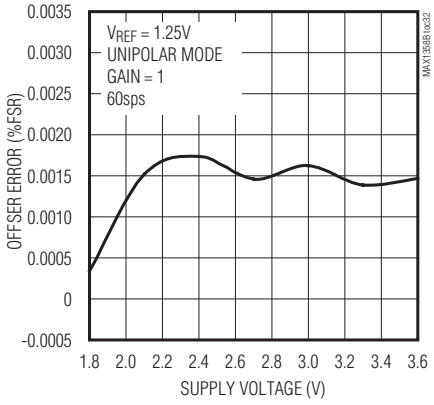
ADC OFFSET ERROR vs. TEMPERATURE



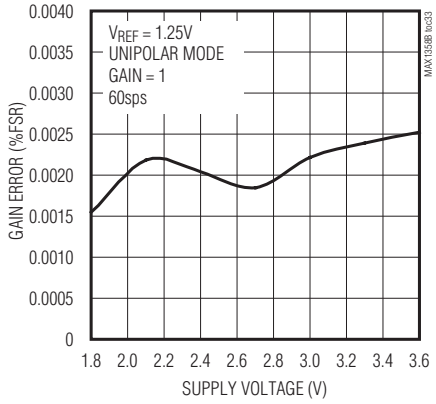
ADC GAIN ERROR vs. TEMPERATURE



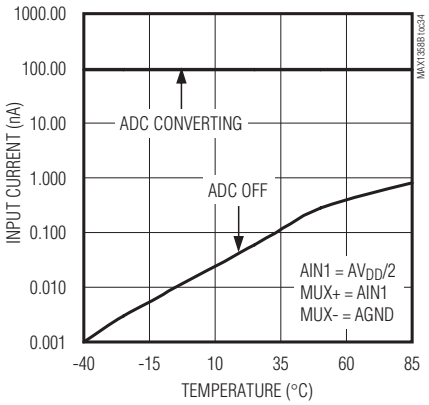
ADC OFFSET ERROR vs. SUPPLY VOLTAGE



ADC GAIN ERROR vs. SUPPLY VOLTAGE



ADC MUX INPUT DC CURRENT vs. TEMPERATURE

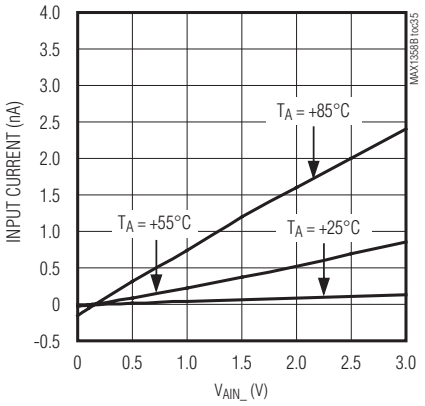


16-Bit, Data-Acquisition System with ADC, DACs, UPIOs, RTC, Voltage Monitors, and Temp Sensor

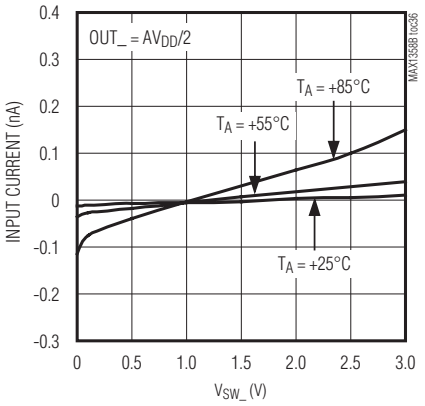
Typical Operating Characteristics (continued)

(DV_{DD} = AV_{DD} = 1.8V, V_{REF} = +1.25V, C_{CPOUT} = 10µF, T_A = +25°C, unless otherwise noted.)

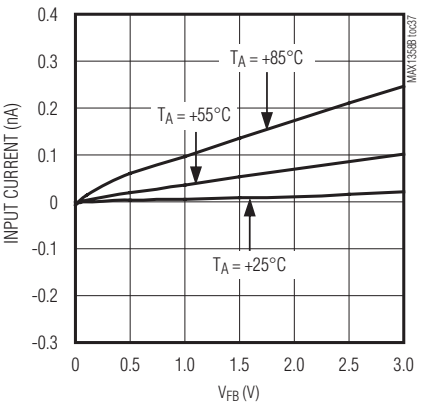
AIN_ LEAKAGE CURRENT vs. INPUT VOLTAGE



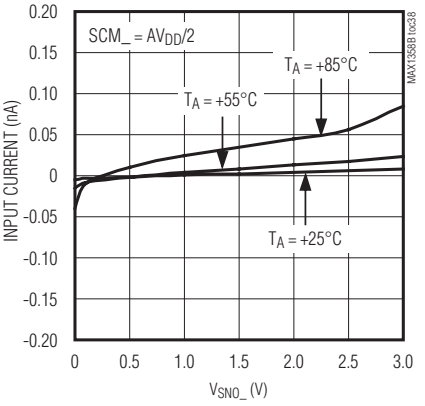
SW_ LEAKAGE CURRENT vs. INPUT VOLTAGE



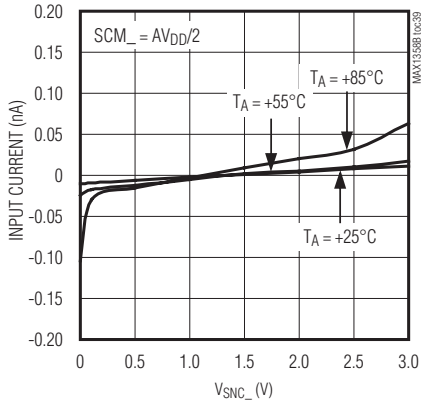
FB LEAKAGE CURRENT vs. INPUT VOLTAGE



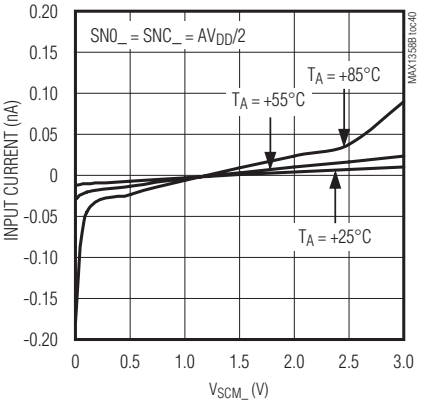
SNO_ LEAKAGE CURRENT vs. INPUT VOLTAGE



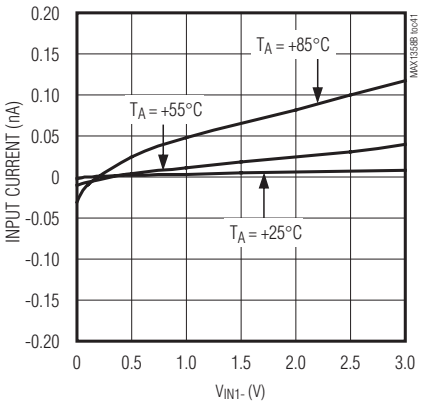
SNC_ LEAKAGE CURRENT vs. INPUT VOLTAGE



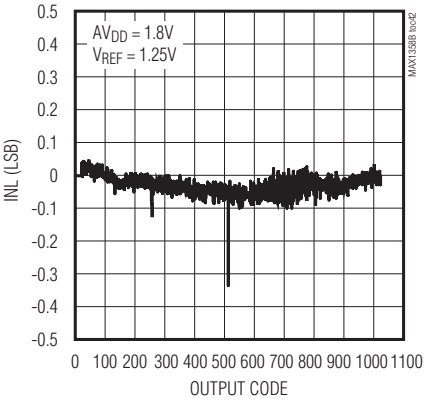
SCM_ LEAKAGE CURRENT vs. INPUT VOLTAGE



IN1- LEAKAGE CURRENT vs. INPUT VOLTAGE



DAC INL vs. OUTPUT CODE

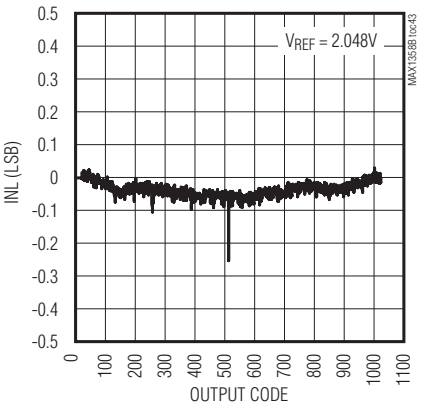


16-Bit, Data-Acquisition System with ADC, DACs, UPIOs, RTC, Voltage Monitors, and Temp Sensor

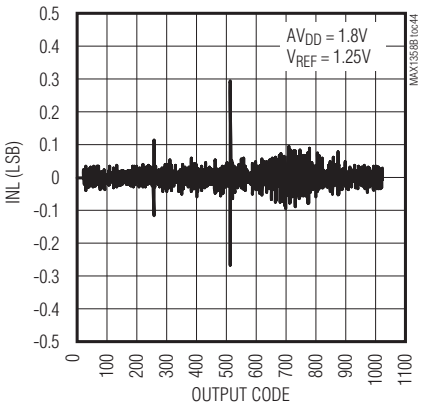
Typical Operating Characteristics (continued)

(DV_{DD} = AV_{DD} = 1.8V, V_{REF} = +1.25V, C_{CPOUT} = 10µF, T_A = +25°C, unless otherwise noted.)

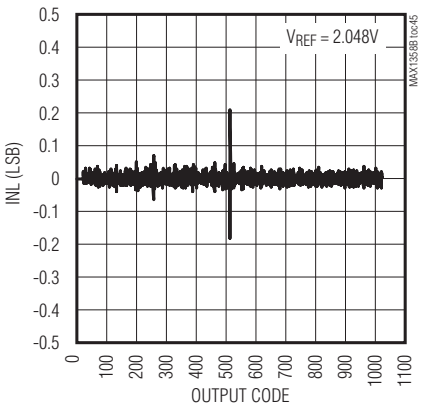
DAC INL vs. OUTPUT CODE



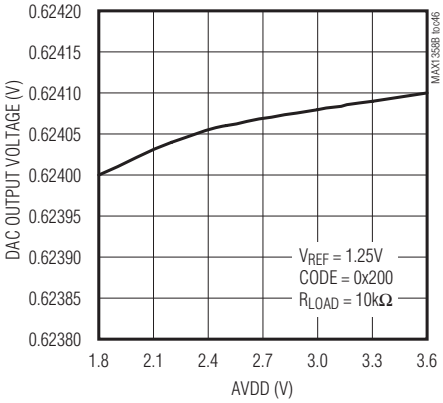
DAC DNL vs. OUTPUT CODE



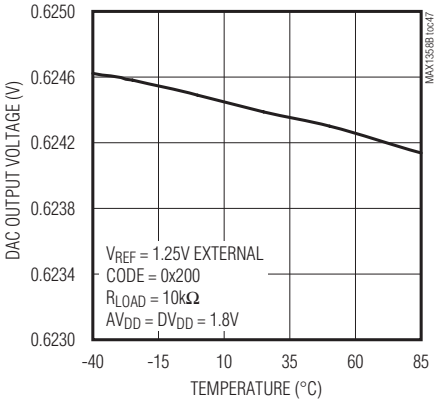
DAC DNL vs. OUTPUT CODE



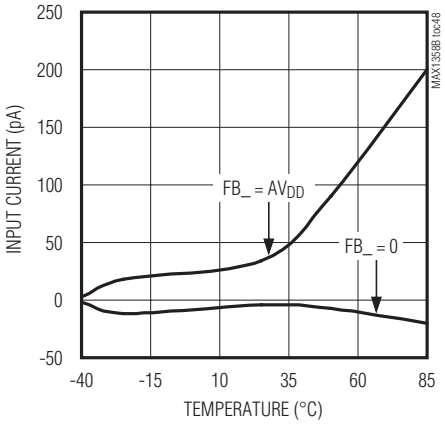
DAC OUTPUT VOLTAGE vs. ANALOG SUPPLY VOLTAGE



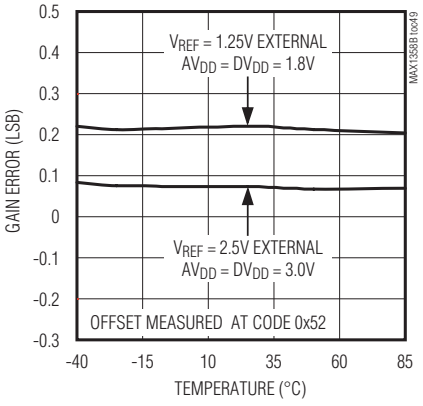
DAC OUTPUT VOLTAGE vs. TEMPERATURE



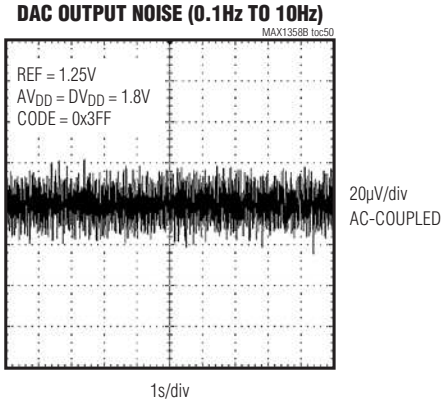
DAC FB_ INPUT BIAS CURRENT vs. TEMPERATURE



DAC GAIN ERROR vs.TEMPERATURE



DAC OUTPUT NOISE (0.1Hz TO 10Hz)

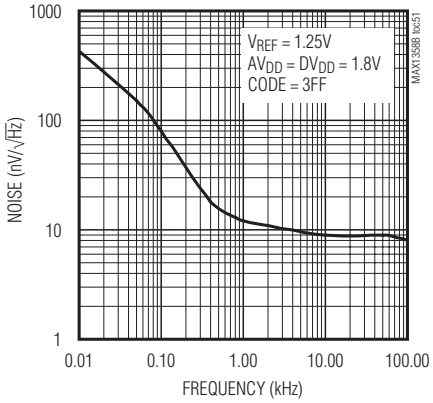


16-Bit, Data-Acquisition System with ADC, DACs, UPIOs, RTC, Voltage Monitors, and Temp Sensor

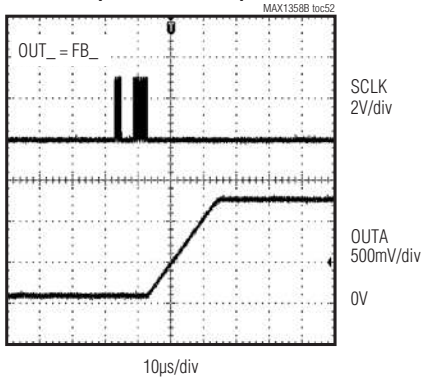
Typical Operating Characteristics (continued)

(DV_{DD} = AV_{DD} = 1.8V, V_{REF} = +1.25V, C_{CPOUT} = 10µF, T_A = +25°C, unless otherwise noted.)

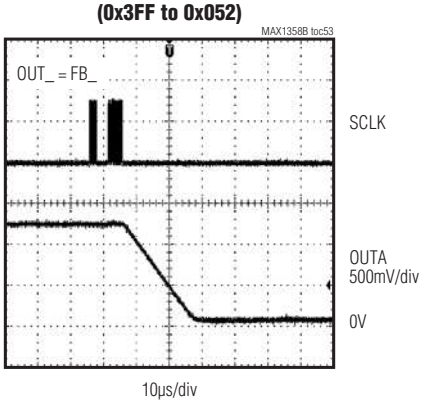
DAC OUTPUT-NOISE DENSITY vs. FREQUENCY



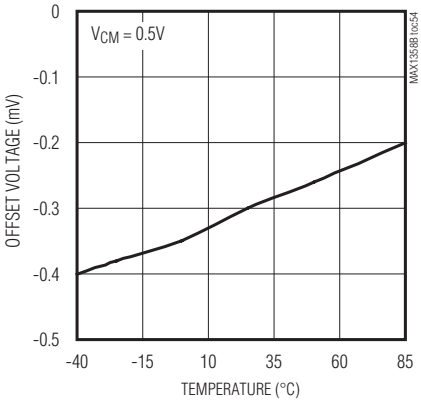
DAC LARGE-SIGNAL STEP RESPONSE (0x052 TO 0x3FF)



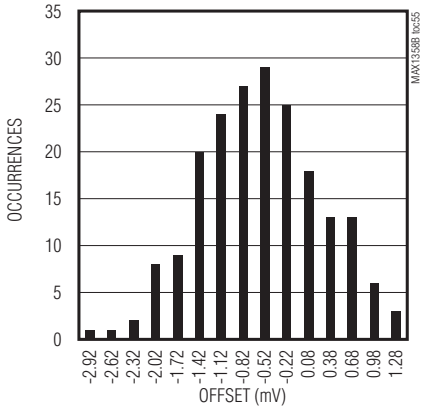
DAC LARGE-SIGNAL STEP RESPONSE (0x3FF to 0x052)



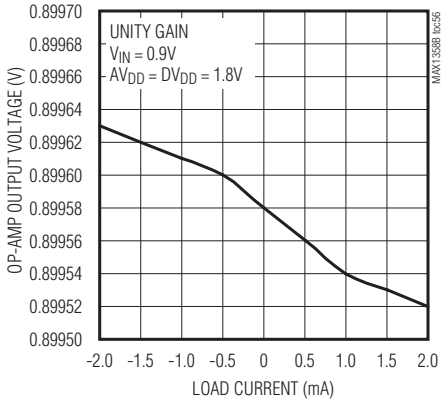
OP-AMP INPUT OFFSET VOLTAGE vs. TEMPERATURE



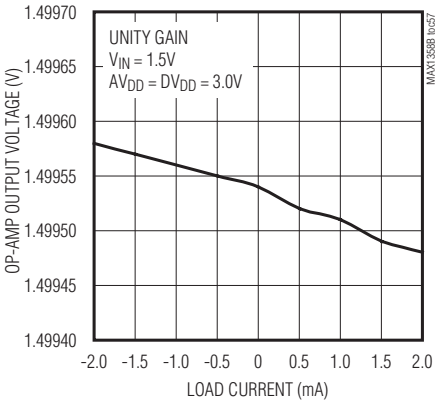
OP-AMP INPUT OFFSET HISTOGRAM



OP-AMP OUTPUT VOLTAGE vs. LOAD CURRENT



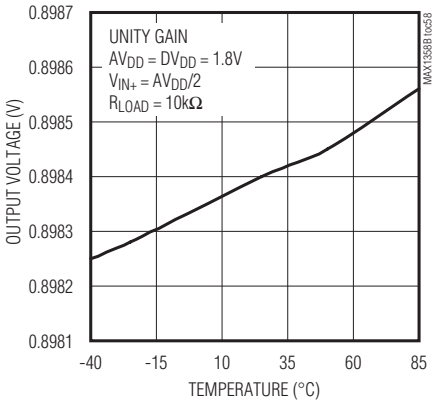
OP-AMP OUTPUT VOLTAGE vs. LOAD CURRENT



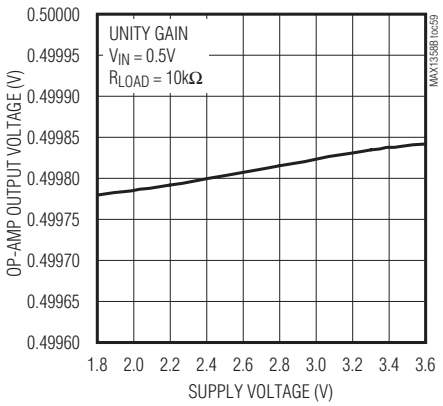
Typical Operating Characteristics (continued)

(DV_{DD} = AV_{DD} = 1.8V, V_{REF} = +1.25V, C_{CPOUT} = 10µF, T_A = +25°C, unless otherwise noted.)

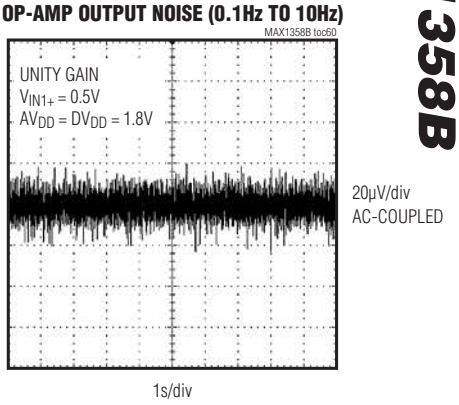
OP-AMP OUTPUT VOLTAGE vs. TEMPERATURE



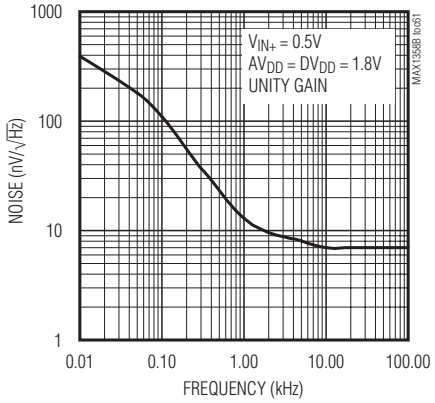
OP-AMP OUTPUT VOLTAGE vs. SUPPLY VOLTAGE



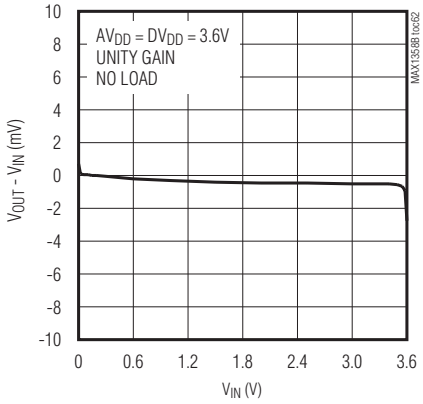
OP-AMP OUTPUT NOISE (0.1Hz TO 10Hz)



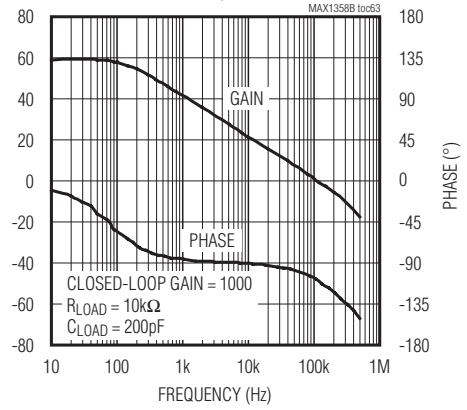
OP-AMP OUTPUT-NOISE DENSITY vs. FREQUENCY



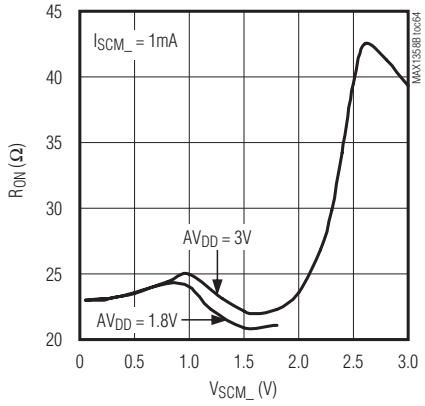
OP-AMP UNITY-GAIN INPUT RANGE



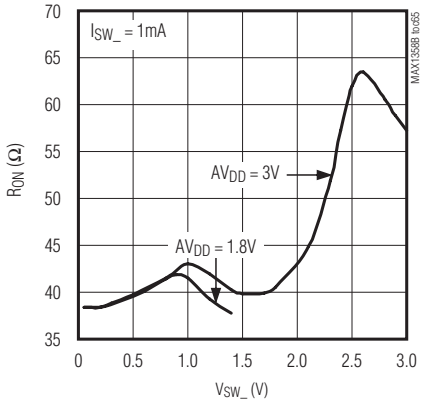
CLOSED-LOOP OP-AMP GAIN AND PHASE vs. FREQUENCY



SPDT ON-RESISTANCE vs. SCM_ VOLTAGE



SPST ON-RESISTANCE vs. SW_ VOLTAGE

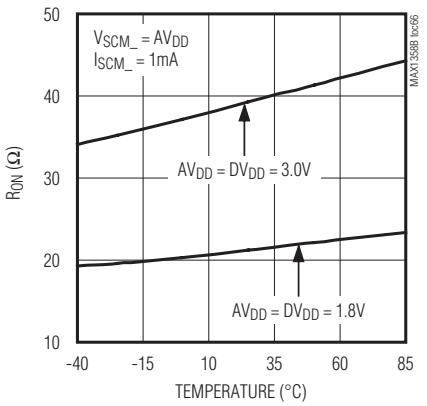


16-Bit, Data-Acquisition System with ADC, DACs, UPIOs, RTC, Voltage Monitors, and Temp Sensor

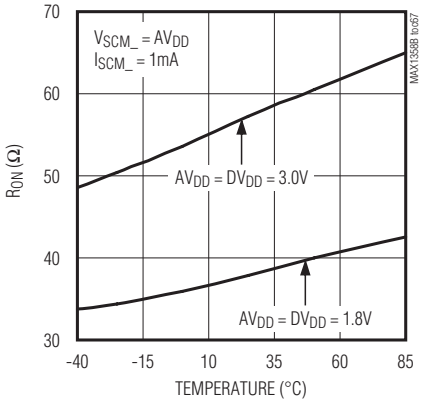
Typical Operating Characteristics (continued)

(DV_{DD} = AV_{DD} = 1.8V, V_{REF} = +1.25V, C_{CPOUT} = 10µF, T_A = +25°C, unless otherwise noted.)

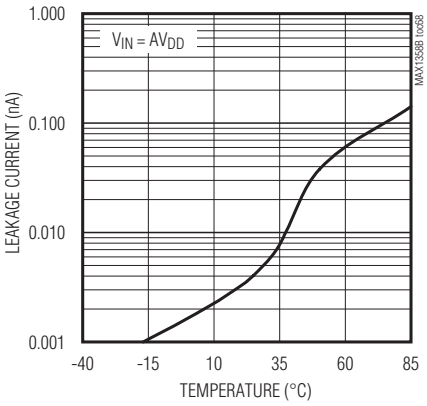
SPDT ON-RESISTANCE vs. TEMPERATURE



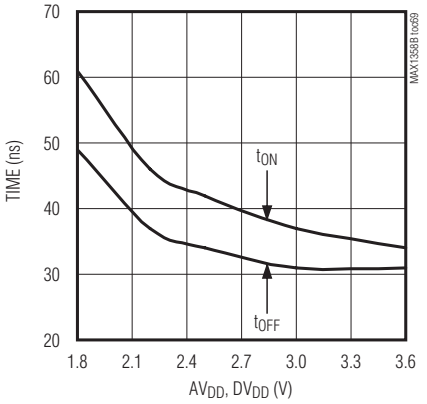
SPDT ON-RESISTANCE vs. TEMPERATURE



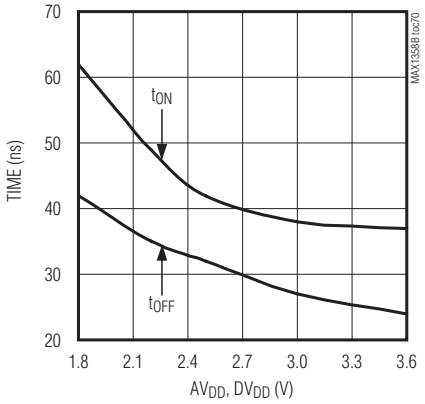
SPST LEAKAGE CURRENT vs. TEMPERATURE



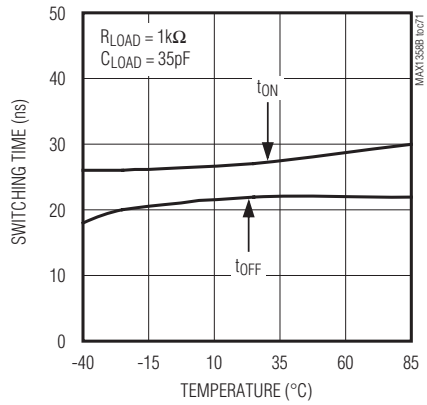
SPDT SWITCHING TIME vs. SUPPLY VOLTAGE



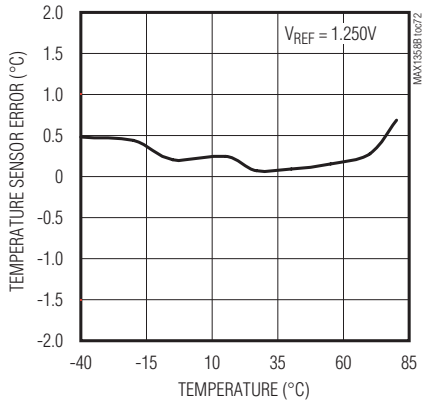
SPST SWITCHING TIME vs. SUPPLY VOLTAGE



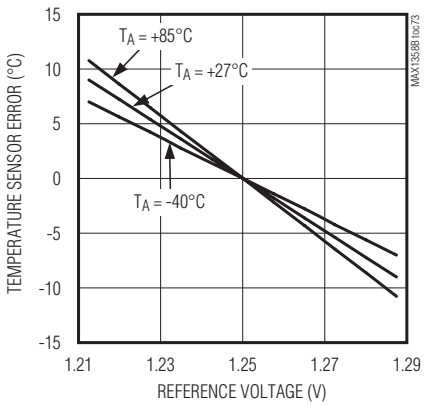
SPDT/SPST SWITCHING TIME vs. TEMPERATURE



INTERNAL TEMPERATURE SENSOR ERROR vs. AMBIENT TEMPERATURE



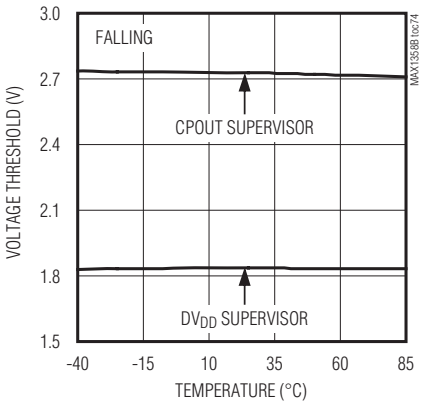
INTERNAL TEMPERATURE SENSOR ERROR vs. REFERENCE VOLTAGE



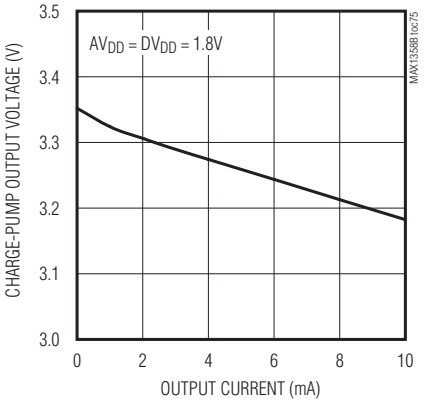
Typical Operating Characteristics (continued)

(DV_{DD} = AV_{DD} = 1.8V, V_{REF} = +1.25V, C_{CPOUT} = 10µF, T_A = +25°C, unless otherwise noted.)

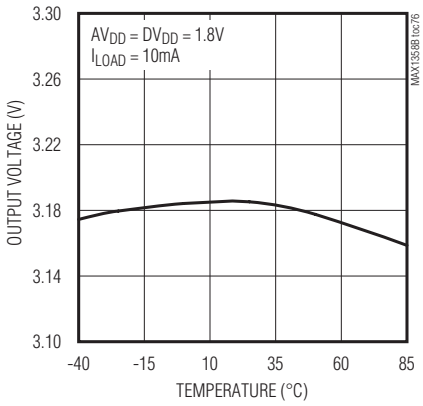
VOLTAGE SUPERVISOR THRESHOLD vs. TEMPERATURE



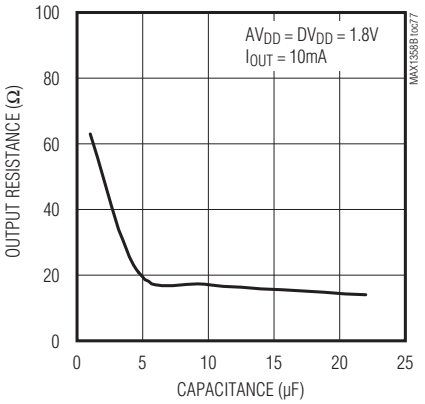
CHARGE-PUMP OUTPUT VOLTAGE vs. OUTPUT CURRENT



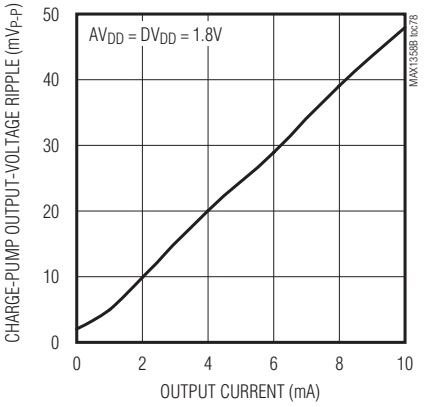
CHARGE-PUMP OUTPUT VOLTAGE vs. TEMPERATURE



CHARGE-PUMP OUTPUT RESISTANCE vs. CAPACITANCE



CHARGE-PUMP OUTPUT-VOLTAGE RIPPLE vs. OUTPUT CURRENT



16-Bit, Data-Acquisition System with ADC, DACs, UPIOs, RTC, Voltage Monitors, and Temp Sensor

Pin Description

PIN	NAME	FUNCTION
1	CLK	Clock Output. Default is 2.457MHz output clock for the µC.
2	UPIO2	User-Programmable Input/Output 2. See the *UPIO2_CTRL Register* section for functionality.
3	UPIO3	User-Programmable Input/Output 3. See the *UPIO3_CTRL Register* section for functionality.
4	UPIO4	User-Programmable Input/Output 4. See the *UPIO4_CTRL Register* section for functionality.
5	DOUT	Serial-Data Output. Data is clocked out on SCLK's falling edge. High impedance when $\overline{CS}$ is high, when UPIO/SPI pass-through mode is enabled, DOUT mirrors the state of UPIO1.
6	SCLK	Serial-Clock Input. Clocks data in and out of the serial interface.
7	DIN	Serial-Data Input. Data is clocked in on SCLK's rising edge.
8	$\overline{CS}$	Active-Low Chip-Select Input. Data is not clocked into DIN unless $\overline{CS}$ is low. When $\overline{CS}$ is high, DOUT is high impedance. High impedance when $\overline{CS}$ is high; when UPIO/SPI pass-through mode is enabled, DOUT mirrors the state of UPIO1.
9	INT	Programmable Active-High/Low Interrupt Output. ADC, UPIO wake-up, alarm, and voltage-monitor events.
10	CLK32K	32kHz Clock Input/Output. Outputs 32kHz clock for the µC. Can be programmed as an input by enabling the IO32E bit to accept an external 32kHz input clock. The RTC, PWM, and watchdog timer always use the internal 32kHz clock derived from the 32kHz crystal.
11	$\overline{RESET}$	Active-Low, Open-Drain Reset Output. Remains low while DV_{DD} is below the 1.8V voltage threshold and stays low for a timeout period (t_{DSLP}) after DV_{DD} rises above the 1.8V threshold. $\overline{RESET}$ also pulses low when the watchdog timer times out and holds low during POR until the 32kHz oscillator stabilizes.
12	32KOUT	32kHz Crystal Output. Connect an external 32kHz watch crystal between 32KIN and 32KOUT.
13	32KIN	32kHz Crystal Input. Connect an external 32kHz watch crystal between 32KIN and 32KOUT.
14	SNO1	Analog Switch 1 Normally Open Terminal. Analog input to mux.
15	SCM1	Analog Switch 1 Common Terminal. Analog input to mux.
16	SNC1	Analog Switch 1 Normally Closed Terminal. Analog input to mux (open on POR).
17	SNO2	Analog Switch 2 Normally Open Terminal. Analog input to mux.
18	SCM2	Analog Switch 2 Common Terminal. Analog input to mux (open on POR).
19	SNC2	Analog Switch 2 Normally Closed Terminal. Analog input to mux.
20	OUT1	Amplifier 1 Output. Analog input to mux.
21	IN1-	Amplifier 1 Inverting Input. Analog input to mux.
22	IN1+	Amplifier 1 Noninverting Input

Pin Description (continued)

PIN	NAME	FUNCTION
23	SWA	DACA SPST Shunt Switch Input. Connects to OUTA through an SPST switch.
24	FBA	DACA Force-Sense Feedback Input. Analog input to mux.
25	OUTA	DACA Force-Sense Output. Analog input to mux.
26	AGND	Analog Ground
27	AV_{DD}	Analog Supply Voltage. Also ADC reference voltage during AV_{DD} measurement. Bypass to AGND with 10µF and 0.1µF capacitors in parallel as close to the pin as possible.
28	SWB	DACB SPST Shunt Switch Input. Connects to OUTB through an SPST switch.
29	FBB	DACB Force-Sense Feedback Input. Analog input to mux.
30	OUTB	Force-Sense DACB Ouput. Analog input to mux.
31	AIN2	Analog Input 2. Analog input to mux. Inputs have internal programmable current source for external temperature measurement.
32	AIN1	Analog Input 1. Analog input to mux. Inputs have internal programmable current source for external temperature measurement.
33	REF	Reference Input/Output. Output of the reference buffer amplifier or external reference input. Disabled at power-up to allow external reference. Reference voltage for ADC and DACs.
34	REG	Linear Voltage-Regulator Output. Charge-pump-doubler input voltage. Bypass REG with a 10µF capacitor to DGND for charge-pump regulation.
35	CF-	Charge-Pump Flying Capacitor Terminals. Connect an external 10µF (typ) capacitor between CF+ and CF-.
36	CF+	
37	CPOUT	Charge-Pump Output. Connect an external 10µF (typ) reservoir capacitor between CPOUT and DGND. There is a low threshold diode between DV_{DD} and CPOUT. When the charge pump is disabled, CPOUT is pulled up within 300mV (typ) of DV_{DD}.
38	DV_{DD}	Digital Supply Voltage. Bypass to DGND with 10µF and 0.1µF capacitors in parallel as close to the pin as possible.
39	DGND	Digital Ground. Also ground for cascaded linear voltage regulator and charge-pump doubler.
40	UPIO1	User-Programmable Input/Output 1. See the *UPIO1_CTRL Register* for functionality.
—	EP	Exposed Pad. Leave unconnected or connect to AGND.