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EVALUATION KIT AVAILABLE

Dual RF LDMOS Bias Controllers with I²C/SPI Interface

General Description

The MAX1385/MAX1386 set and control bias conditions for dual RF LDMOS power devices found in cellular base stations. Each device includes a high-side current-sense amplifier with programmable gains of 2, 10, and 25 to monitor LDMOS drain current over the 20mA to 5A range. Two external diode-connected transistors monitor LDMOS temperatures while an internal temperature sensor measures the local die temperature of the MAX1385/MAX1386. A 12-bit ADC converts the programmable-gain amplifier (PGA) outputs, external/internal temperature readings, and two auxiliary inputs.

The two gate-drive channels, each consisting of 8-bit coarse and 10-bit fine DACs and a gate-drive amplifier, generate a positive gate voltage to bias the LDMOS devices. The MAX1385 includes a gate-drive amplifier with a gain of 2 and the MAX1386 gate-drive amplifier provides a gain of 4. The 8-bit coarse and 10-bit fine DACs allow up to 18 bits of resolution. The MAX1385/MAX1386 include autocalibration features to minimize error over time, temperature, and supply voltage.

The MAX1385/MAX1386 feature an I²C/SPI™-compatible serial interface. Both devices operate from a 4.75V to 5.25V analog supply (3.2mA supply current), a 2.7V to 5.25V digital supply (3.1mA supply current), and a 4.75V to 11.0V gate-drive supply (4.5mA supply current). The MAX1385/MAX1386 are available in a 48-pin thin QFN package.

Applications

RF LDMOS Bias Control in Cellular Base Stations

Industrial Process Control

Features

- **Integrated High-Side Drain Current-Sense PGA with Gain of 2, 10, or 25**
- **±0.5% Accuracy for Sense Voltage Between 75mV and 250mV**
- **Full-Scale Sense Voltage of 100mV with Gain of 25**
- **Full-Scale Sense Voltage of 250mV with Gain of 10**
- **Common-Mode Range of 5V to 30V Drain Voltage for LDMOS**
- **Adjustable Low Noise 0 to 5V, 0 to 10V Output Gate-Bias Voltage Ranges with ±10mA Gate Drive**
- **Fast Clamp to 0V for LDMOS Protection**
- **8-Bit DAC Control of Gate-Bias Voltage**
- **10-Bit DAC Control of Gate-Bias Offset with Temperature**
- **Internal Die Temperature Measurement**
- **External Temperature Measurement by Diode-Connected Transistor (2N3904)**
- **Internal 12-Bit ADC Measurement of Temperature, Current, and Voltages**
- **Selectable I²C-/SPI-Compatible Serial Interface**
  - **400kHz/1.7MHz/3.4MHz I²C-Compatible Control for Settings and Data Measurement**
  - **16MHz SPI-Compatible Control for Settings and Data Measurement**
- **Internal 2.5V Reference**
- **Three Address Inputs to Control Eight Devices in I²C Mode**

Ordering Information/Selector Guide

PART	TEMP RANGE	PIN-PACKAGE	TEMP ERROR (°C)	V_{GATE} (V)
MAX1385AETM+**	-40°C to +85°C	48 Thin QFN-EP*	±1	5
MAX1385BETM+	-40°C to +85°C	48 Thin QFN-EP*	±2	5
MAX1386AETM+**	-40°C to +85°C	48 Thin QFN-EP*	±1	10
MAX1386BETM+**	-40°C to +85°C	48 Thin QFN-EP*	±2	10

**EP = Exposed pad.*
***Future product—contact factory for availability.*
+Denotes a lead(Pb)-free/RoHS-compliant package.

Pin Configuration and Typical Operating Circuit (I²C Mode) appear at end of data sheet.

SPI is a trademark of Motorola, Inc.

Dual RF LDMOS Bias Controllers with I²C/SPI Interface

ABSOLUTE MAXIMUM RATINGS

AV_{DD} to AGND .....-0.3V to +6V
DV_{DD} to DGND.....-0.3V to +6V
AGND to DGND.....-0.3V to +0.3V
CS1+, CS1-, CS2+, CS2- to GATEGND.....-0.3V to +32V
CS1- to CS1+, CS2- to CS2+ .....-6V to +0.3V
$GATEV_{DD}$ to GATEGND .....-0.3V to +12V
GATE1, GATE2 to GATEGND.....-0.3V to ($GATEV_{DD}$ + 0.3V)
SAFE1, SAFE2 to GATEGND.....-0.3V to +6V
GATEGND to AGND.....-0.3V to +0.3V
All Other Analog Inputs
to AGND .....-0.3V to the lower of +6V and (AV_{DD} + 0.3V)
Digital Inputs
to DGND.....-0.3V to the lower of +6V and (DV_{DD} + 0.3V)
SDA/DIN, SCL to DGND.....-0.3V to +6V
Digital Outputs to DGND .....-0.3V to (DV_{DD} + 0.3V)
Maximum Continuous Current into Any Pin 50mA
Continuous Power Dissipation (T_A = +70°C)
48-Pin, 7mm x 7mm, Thin QFN (derate 27.8 mW/°C above +70°C).....2222mW
Maximum Junction Temperature .....+150°C
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

($GATEV_{DD}$ = +5.5V for the MAX1385, $GATEV_{DD}$ = +11V for the MAX1386, AV_{DD} = DV_{DD} = +5V, external V_{REFADC} = +2.5V, external V_{REFDAC} = +2.5V, C_{REF} = 0.1µF, unless otherwise noted. T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
HIGH-SIDE CURRENT SENSE WITH PGA						
Common-Mode Input Voltage Range	V_{CS+}, V_{CS-}		5		30	V
Common-Mode Rejection Ratio	CMRR	11V < V_{CS+} < 30V		90		dB
Input-Bias Current	I_{CS+}	V_{SENSE} < 100mV over the common-mode range		120	195	µA
	I_{CS-}			0.002	±2	
Full-Scale Sense Voltage Range	V_{SENSE} = VCS_+ - VCS_-	PGA gain = 25	0		100	mV
		PGA gain = 10	0		250	
		PGA gain = 2	0		1250	
Sense Voltage Range for Accuracy of ±0.5% V_{SENSE}		PGA gain = 25	75		100	mV
		PGA gain = 10	75		250	
		PGA gain = 2	75		1250	
Sense Voltage Range for Accuracy of ±2% V_{SENSE}		PGA gain = 25	20		100	mV
		PGA gain = 10	20		250	
		PGA gain = 2	20		1250	
Total PGAOUT Voltage Error		V_{SENSE} = 75mV		±0.1	±0.5	%
PGAOUT Capacitive Load	C_{PGAOUT}				100	pF
PGAOUT Settling Time	t_{HSCS}	Settles to within ±0.5% of final value, R_S = 50Ω, C_{GATE} = 15pF		< 25		µs
Saturation Recovery Time		Settles to within ±0.5% accuracy; from V_{SENSE} = 3 x full scale		< 45		µs
Sense-Amplifier Slew Rate		A_{VPGA} = 2		0.5		V/µs
		A_{VPGA} = 10		2		
		A_{VPGA} = 25		2		

ELECTRICAL CHARACTERISTICS (continued)

($GATEV_{DD}$ = +5.5V for the MAX1385, $GATEV_{DD}$ = +11V for the MAX1386, AV_{DD} = DV_{DD} = +5V, external V_{REFADC} = +2.5V, external V_{REFDAC} = +2.5V, C_{REF} = 0.1µF, unless otherwise noted. T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Sense-Amplifier Bandwidth		AV_{PGA} = 2		900		kHz
		AV_{PGA} = 10		720		
		AV_{PGA} = 25		290		
LDMOS GATE DRIVER (GAIN = 2 and 4)						
Output Gate-Drive Voltage Range	V_{GATE}	I_{GATE} = ±1mA	0.75		$GATEV_{DD}$ - 0.75	V
		I_{GATE} = ±10mA	1		$GATEV_{DD}$ - 1	
Output Impedance	R_{GATE}	Measured at DC		0.1		Ω
V_{GATE} Settling Time	t_{GATE}	Settles to within ±0.5% of final value; R_{SERIES} = 50Ω, C_{GATE} = 15µF		10		ms
Output Capacitive Load (Note 1)	C_{GATE}	No series resistance, R_{SERIES} = 0Ω	0		10	nF
		R_{SERIES} = 50Ω	0		25,000	
V_{GATE} Noise		RMS noise; 1kHz - 1MHz		250		$nV/\sqrt{Hz}$
Maximum Power-On Transient				±100		mV
Output Short-Circuit Current Limit	I_{SC}	1s, sinking or sourcing		±25		mA
Total Unadjusted Error No Autocalibration and Offset Removal (Note 2)	TUE	MAX1385, LOCODE = 128, HICODE = 180		±6	±20	mV
		MAX1386, LOCODE = 128, HICODE = 180		±12	±40	
Total Adjusted Error With Autocalibration and Offset Removal	TUE	MAX1385, LOCODE = 128, HICODE = 180		±1	±8	mV
		MAX1386, LOCODE = 128, HICODE = 180		±2	±16	
Drift		MAX1385, V_{GATE} > 1V		±15		µV/°C
		MAX1386, V_{GATE} > 1V		±30		
Clamp to Zero Delay				1		µs
Output Safe Switch On-Resistance	R_{OPSW}	GATE_ clamped to AGND (Note 3)			500	Ω
Amplifier Bandwidth		MAX1385		300		kHz
		MAX1386		150		
Amplifier Slew Rate				0.375		V/µs
MONITOR ADC DC ACCURACY						
Resolution	N_{ADC}		12			Bits
Differential Nonlinearity	DNL_{ADC}			±0.5	±2	LSB
Integral Nonlinearity	INL_{ADC}	(Note 4)		±0.6	±2	LSB
Offset Error				±2	±4	LSB
Gain Error		(Note 5)		±2	±4	LSB
Gain Temperature Coefficient				±0.4		ppm/°C
Offset Temperature Coefficient				±0.4		ppm/°C

Dual RF LDMOS Bias Controllers with I²C/SPI Interface

ELECTRICAL CHARACTERISTICS (continued)

($GATEV_{DD}$ = +5.5V for the MAX1385, $GATEV_{DD}$ = +11V for the MAX1386, AV_{DD} = DV_{DD} = +5V, external V_{REFADC} = +2.5V, external V_{REFDAC} = +2.5V, C_{REF} = 0.1µF, unless otherwise noted. T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Channel-to-Channel Offset Matching				±0.1		LSB
Channel-to-Channel Gain Matching				±0.1		LSB
MONITOR ADC DYNAMIC ACCURACY (1kHz sine-wave input, 2.5V_{P-P}, up to 94.4ksps)						
Signal-to-Noise Plus Distortion	SINAD			70		dB
Total Harmonic Distortion	THD	Up to the 5th harmonic		-82		dB
Spurious-Free Dynamic Range	SFDR			86		dB
Intermodulation Distortion	IMD	f_{IN1} = 0.99kHz, f_{IN2} = 1.02kHz		76		dB
Full-Power Bandwidth		-3dB point		10		MHz
Full-Linear Bandwidth		S/(N + D) > 68dB		100		kHz
MONITOR ADC CONVERSION RATE						
Power-Up Time	t_{PU}	External reference		0.8		µs
		Internal reference		70		
Conversion Time	t_{CONV}	Internally clocked		7.5	10	µs
MONITOR ADC ANALOG INPUT (ADCIN1, ADCIN2)						
Input Range	V_{ADCIN}	Relative to AGND (Note 6)	0		V_{REF}	V
Input Leakage Current		V_{IN} = 0V and V_{IN} = AV_{DD}		±0.01	±1	µA
Input Capacitance	C_{ADCIN}			34		pF
TEMPERATURE MEASUREMENTS						
Internal Sensor Measurement Error (Note 1)		MAX1385A/MAX1386A, T_A = +25°C		±0.25		°C
		MAX1385A/MAX1386A, T_A = T_{MIN} to T_{MAX}	-1.0	±0.25	+1.0	
		MAX1385B/MAX1386B, T_A = +25°C		±0.25		
		MAX1385B/MAX1386B, T_A = T_{MIN} to T_{MAX}	-2.0	±0.35	+2.0	
External Sensor Measurement Error (Notes 1, 7)		T_A = +25°C		±0.4		°C
		T_A = T_{MIN} to T_{MAX}	-3	±0.75	+3	
Temperature Resolution				1/8		°C/LSB
External Diode Drive			2.8		85	µA
Drive Current Ratio		(Note 8)		16.5		
INTERNAL REFERENCE						
REFADC/REFDAC Output Voltage	V_{REFADC}	T_A = +25°C	2.494	2.500	2.506	V
	V_{REFDAC}	T_A = +25°C	2.494	2.500	2.506	
REFADC/REFDAC Output Temperature Coefficient	TC_{REFADC}, TC_{REFDAC}			±14		ppm/°C
REFADC/REFDAC Output Impedance				6.5		kΩ

ELECTRICAL CHARACTERISTICS (continued)

($GATEV_{DD}$ = +5.5V for the MAX1385, $GATEV_{DD}$ = +11V for the MAX1386, AV_{DD} = DV_{DD} = +5V, external V_{REFADC} = +2.5V, external V_{REFDAC} = +2.5V, C_{REF} = 0.1µF, unless otherwise noted. T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Capacitive Bypass at REF			270			nF
Power-Supply Rejection Ratio	PSRR	AV_{DD} = +5V ±5%		70		dB
EXTERNAL REFERENCE						
REFADC Input Voltage Range	V_{REFADC}	Limited code test	1.0		AV_{DD}	V
REFADC Input Current	I_{REFADC}	V_{REF} = 2.5V, f_{SAMPLE} = 174ksps		60	80	µA
		Acquisition/between conversions		±0.01	±1	
REFDAC Input Voltage Range	V_{REFDAC}	(Note 9)	0.5		2.5	V
REFDAC Input Current		Static current when no DAC calibration		0.1		µA
GATE-DRIVER COARSE-DAC DC ACCURACY						
Resolution	N_{CDAC}		8			Bits
Integral Nonlinearity	INL_{CDAC}	Measured at GATE; fine DAC set at full scale		±0.15	±1	LSB
Differential Nonlinearity	DNL_{CDAC}	Guaranteed monotonic		±0.05	±0.5	LSB
GATE-DRIVER FINE-DAC DC ACCURACY						
Resolution	N_{FDAC}		10			Bits
Integral Nonlinearity	INL_{FDAC}	Measured at GATE; coarse DAC set at full scale		±0.25	±4	LSB
Differential Nonlinearity	DNL_{FDAC}	Guaranteed monotonic		±0.1	±1	LSB
POWER SUPPLIES (Note 10)						
Analog Supply Voltage	AV_{DD}		4.75		5.25	V
Digital Supply Voltage	DV_{DD}		2.7		AV_{DD} + 0.3	V
Gate-Drive Supply Voltage	$V_{GATEVDD}$		4.75		11.00	V
Analog Supply Current	I_{AVDD}	AV_{DD} = 5V		3.2	4	mA
Digital Supply Current	I_{DVDD}	DV_{DD} = 2.7V to 5.25V		3.1	4.3	mA
$GATEV_{DD}$ Supply Current	$I_{GATEVDD}$		3	4.5	7	mA
Shutdown Current (Note 11)	I_{PD}	I_{AVDD}		0.1	2	µA
		I_{DVDD}		0.1	2	
		$I_{VDDGATE}$		0.1	2	

ELECTRICAL CHARACTERISTICS (continued)

($GATEV_{DD}$ = +5.5V for the MAX1385, $GATEV_{DD}$ = +11V for the MAX1386, AV_{DD} = DV_{DD} = +5V, external V_{REFADC} = +2.5V, external V_{REFDAC} = +2.5V, C_{REF} = 0.1µF, unless otherwise noted. T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{IH} AND V_{IL} FOR SDA/DIN AND SCL IN I²C OPERATION ONLY						
Input High Voltage	V_{IH}		0.7 x DV_{DD}			V
Input Low Voltage	V_{IL}				0.3 x DV_{DD}	V
Input Hysteresis	V_{HYS}		0.1 x DV_{DD}			V
V_{IH} AND V_{IL} FOR OPSAFE1 AND OPSAFE2						
Input High Voltage	V_{IH}		2.4			V
Input Low Voltage	V_{IL}				0.4	V
V_{IH} AND V_{IL} FOR ALL OTHER DIGITAL INPUTS						
Input High Voltage	V_{IH}		2.2			V
Input Low Voltage	V_{IL}				0.7	V
V_{OH} AND V_{OL} FOR A1/DOUT (SPI), SDA/DIN, ALARM						
Output Low Voltage	V_{OL}	I_{SINK} = 3mA			0.4	V
Output High Voltage	V_{OH}	I_{SOURCE} = 2mA	DV_{DD} - 0.5			V
V_{OH} AND V_{OL} FOR SAFE1, SAFE2, BUSY						
Output Low Voltage	V_{OL}	I_{SINK} = 0.5mA			0.4	V
Output High Voltage	V_{OH}	I_{SOURCE} = 0.5mA	DV_{DD} - 0.5			V

I²C SLOW-/FAST-MODE TIMING CHARACTERISTICS (Note 12, see Figure 1)

(GATEV_{DD} = +5.5V for MAX1385, GATEV_{DD} = +11V for MAX1386, AV_{DD} = +5V, DV_{DD} = 2.7V to 5.25V, external V_{REFADC} = +2.5V, external V_{REFDAC} = +2.5V, C_{REF} = 0.1µF, T_A = -40°C to +85°C, unless otherwise noted).

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Serial-Clock Frequency	f_{SCL}		0		400	kHz
Bus Free Time Between STOP and START Condition	t_{BUF}		1.3			µs
Hold Time Repeated START Condition	$t_{HD;STA}$	After this period, the first clock pulse is generated	0.6			µs
SCL Pulse-Width Low	t_{LOW}		1.3			µs
SCL Pulse-Width High	t_{HIGH}		0.6			µs
Setup Time Repeated START Condition	$t_{SU;STA}$		0.6			µs
Data Hold Time	$t_{HD;DAT}$	(Note 13)	0		0.9	µs
Data Setup Time	$t_{SU;DAT}$		100			ns
Rise Time of Both SDA and SCL Signals, Receiving	t_R	(Note 14)	0		300	ns
Fall Time of Both SDA and SCL Signals, Receiving	t_F	(Note 14)	0		300	ns
Fall Time of SDA Signal, Transmitting	t_F	(Notes 14, 15)	$20 + 0.1C_b$		250	ns
Setup Time for STOP Condition	$t_{SU;STO}$		0.6			µs
Capacitive Load for Each Bus Line	C_b				400	pF
Pulse Width of Spikes Suppressed by the Input Filter	t_{SP}	(Note 16)	0		50	ns

I²C HIGH-SPEED-MODE TIMING CHARACTERISTICS (Note 12, see Figure 2)

($GATEV_{DD}$ = +5.5V for MAX1385, $GATEV_{DD}$ = +11V for MAX1386, AV_{DD} = +5V, DV_{DD} = 2.7V to 5.25V, external V_{REFADC} = +2.5V, external V_{REFDAC} = +2.5V, C_{REF} = 0.1µF, T_A = -40°C to +85°C, unless otherwise noted).

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Serial-Clock Frequency	f_{SCL}		0		3.4	MHz
Setup Time Repeated START Condition	$t_{SU;STA}$		160			ns
Hold Time Repeated START Condition	$t_{HD;STA}$		160			ns
SCL Pulse-Width Low	t_{LOW}		160			ns
SCL Pulse-Width High	t_{HIGH}		60			ns
Data Setup Time	$t_{SU;DAT}$		10			ns
Data Hold Time	$t_{HD;DAT}$	(Note 17)	0		70	ns
Rise Time of SCL Signal, Receiving	t_{RCL}		10		40	ns
Rise Time of SCL Signal After a Repeated START Condition and After an Acknowledge Bit, Receiving	t_{RCL1}		10		80	ns
Fall Time of SCL Signal, Receiving	t_{FCL}		10		40	ns
Rise Time of SDA Signal, Receiving	t_{RDA}		10		80	ns
Fall Time of SDA Signal, Transmitting	t_{FDA}		10		80	ns
Setup Time for STOP Condition	$t_{SU;STO}$		160			ns
Capacitive Load for Each Bus Line	C_b	(Note 18)			100	pF
Pulse Width of Spikes That are Suppressed by the Input Filter	t_{SP}		0		10	ns

SPI TIMING CHARACTERISTICS (Note 12, See Figure 3)

($GATEV_{DD}$ = +5.5V for the MAX1385, $GATEV_{DD}$ = +11V for the MAX1386, AV_{DD} = +5V, DV_{DD} = 2.7V to 5.25V, external V_{REFADC} = +2.5V, external V_{REFDAC} = +2.5V, C_{REF} = 0.1µF, T_A = -40°C to +85°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Clock Period	t_{CP}		62.5			ns
SCL High Time	t_{CH}		25			ns
SCL Low Time	t_{CL}		25			ns
DIN Setup Time	t_{DS}		10			ns
DIN Hold Time	t_{DH}		0			ns
SCL Fall to DOUT Transition	t_{DO}	C_{LOAD} = 30pF			20	ns
$\overline{CSB}$ Fall to DOUT Enable	t_{DV}	C_{LOAD} = 30pF			40	ns
$\overline{CSB}$ Rise to DOUT Disable	t_{TR}	C_{LOAD} = 30pF (Note 12)			100	ns
$\overline{CSB}$ Rise or Fall to SCL Rise	t_{CSS}		25			ns
$\overline{CSB}$ Pulse-Width High	t_{CSW}		100			ns
Last Clock Rise to $\overline{CSB}$ Rise	t_{CSH}		50			ns

Note 1: Guaranteed by design.

Note 2: Total unadjusted errors are for the entire gain drive channel including the 8- and 10-bit DACs and the gate driver. They are all measured at the GATE1 and GATE2 outputs. Offset removal refers to presetting the drain current after a room temperature calibration by the user. This effectively removes the channel offset.

Note 3: During power-on reset, the output safe switch is closed. The output safe switch opens once both AV_{DD} and DV_{DD} supply voltages are established.

Note 4: Integral nonlinearity is the deviation of the analog value at any code from its theoretical value after the gain and offset errors have been removed.

Note 5: Offset nulled.

Note 6: Absolute range for analog inputs is from 0 to AV_{DD}.

Note 7: The MAX1385/MAX1386 and external sensor are at the same temperature. External sensor measurement error is tested with a diode-connected 2N3904.

Note 8: The drive current ratio is defined as the large drive current divided by the small drive current in a temperature measurement. See the *Temperature Measurements* section for further details.

Note 9: Guaranteed monotonicity. Accuracy might be degraded at lower V_{REFDAC}.

Note 10: Supply current limits are valid only when digital inputs are at DV_{DD} or DGND. Timing specifications are only guaranteed when inputs are driven rail-to-rail.

Note 11: Shutdown supply currents are typically 0.1µA. Maximum specification is limited by automated test equipment.

Note 12: All timing specifications referred to V_{IH} or V_{IL} levels.

Note 13: A master device must provide a hold time of at least 300ns for the SDA signal (referred to V_{IL} of SCL) to bridge the undefined region of SCL's falling edge.

Note 14: C_b = total capacitance of one bus line in pF; t_R and t_F are measured between 0.3 x DV_{DD} and 0.7 x DV_{DD}.

Note 15: For a device operating in an I²C-compatible system.

Note 16: Input filters on the SDA and SCL inputs suppress noise spikes less than 50ns.

Note 17: A device must provide a data hold time to bridge the undefined part between V_{IH} and V_{IL} of the falling edge of the SCL signal. An input circuit with a threshold as low as possible for the falling edge of the SCL signal minimizes this hold time.

Note 18: Cb = total capacitance of one bus line in pF. For bus loads between 100pF and 400pF, the timing parameters should be linearly interpolated.

Dual RF LDMOS Bias Controllers with I²C/SPI Interface

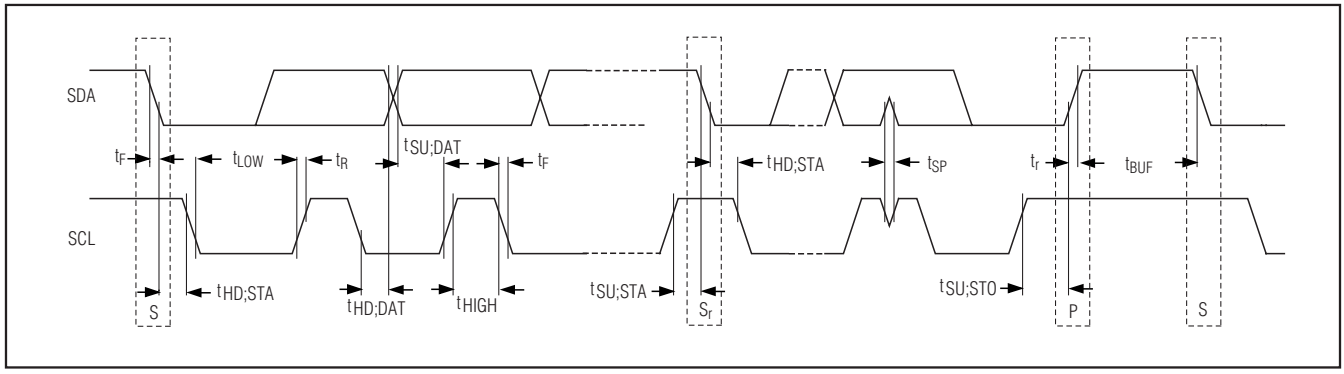


Figure 1. I²C Slow-/Fast-Mode Timing Diagram

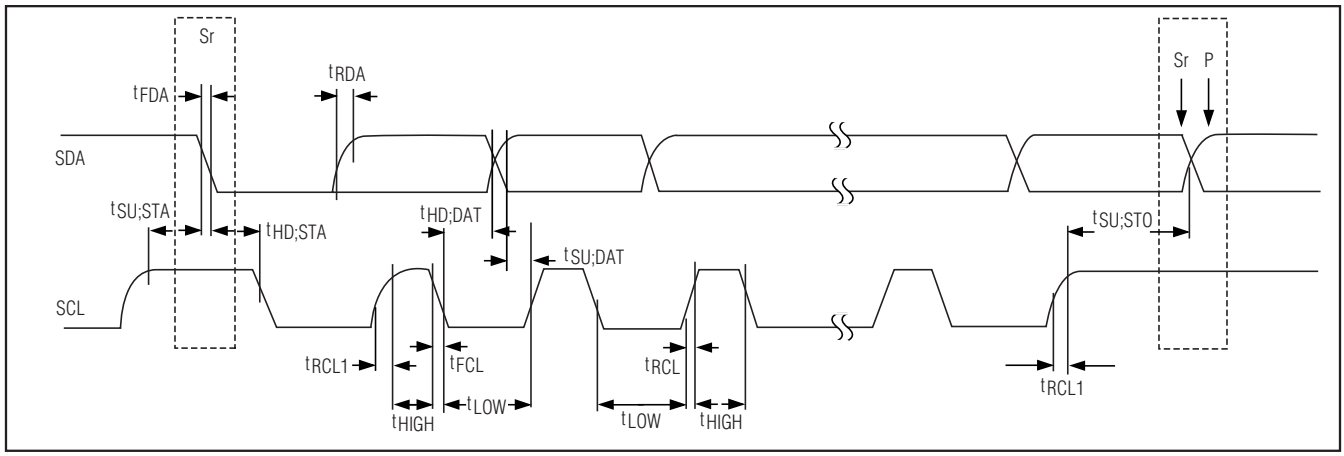


Figure 2. I²C High-Speed-Mode Timing Diagram

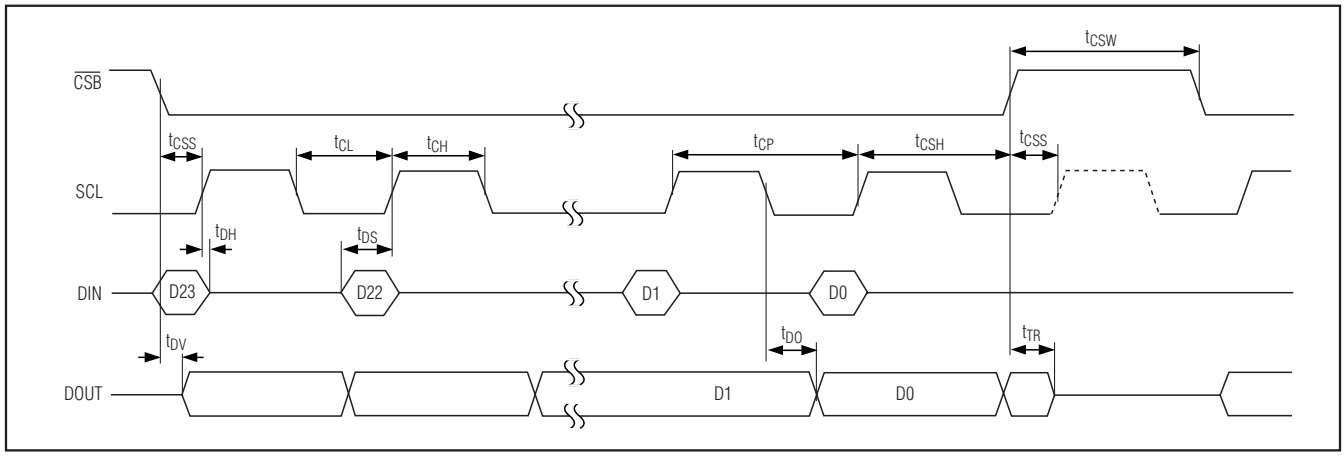
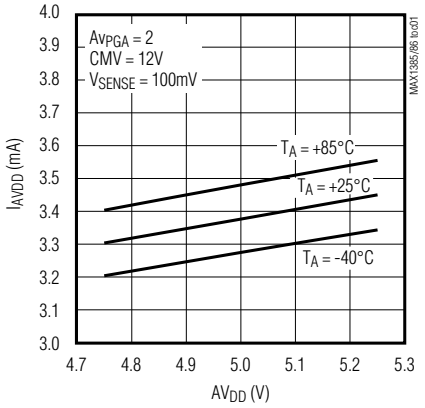


Figure 3. SPI Timing Diagram

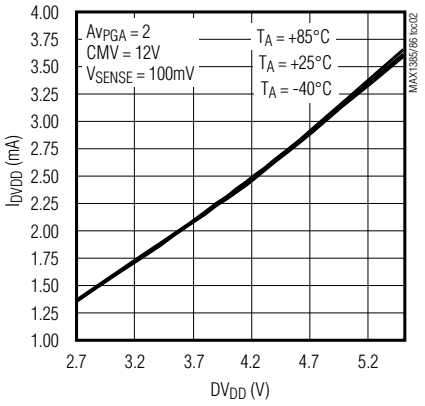
Typical Operating Characteristics

($GATEV_{DD}$ = +5.5V for the MAX1385, $GATEV_{DD}$ = +11V for the MAX1386, AV_{DD} = DV_{DD} = +5V, external V_{REFADC} = +2.5V, external V_{REFDAC} = +2.5V, C_{REF} = 0.1µF, T_A = +25°C, unless otherwise noted.)

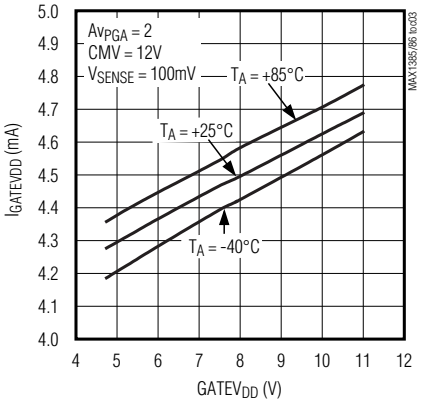
AV_{DD} SUPPLY CURRENT vs. AV_{DD} VOLTAGE



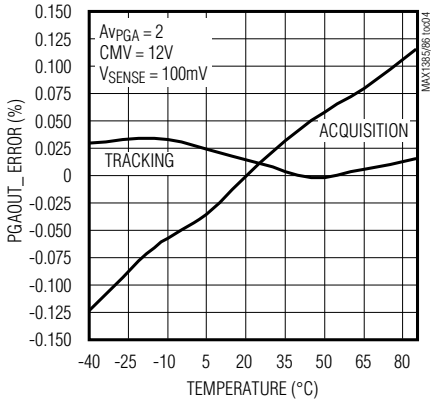
DV_{DD} SUPPLY CURRENT vs. DV_{DD} VOLTAGE



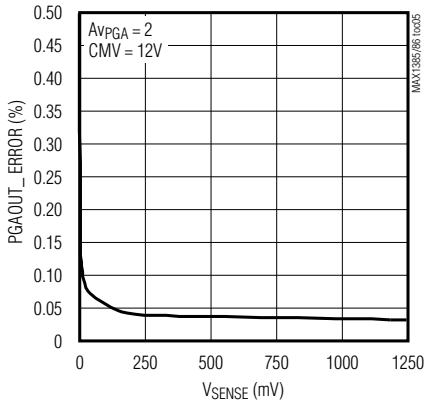
$GATEV_{DD}$ SUPPLY CURRENT vs. $GATEV_{DD}$ VOLTAGE



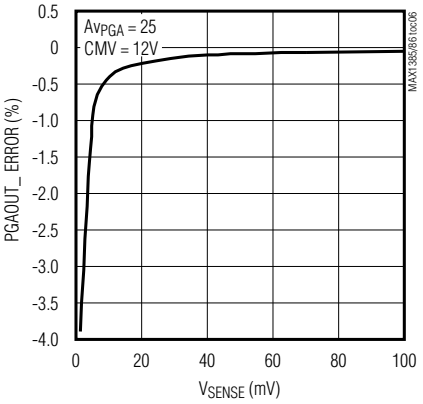
TOTAL PGAOUT_ ERROR vs. TEMPERATURE



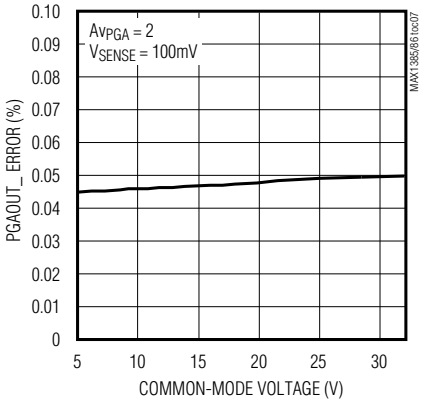
TOTAL PGAOUT_ ERROR vs. V_{SENSE}



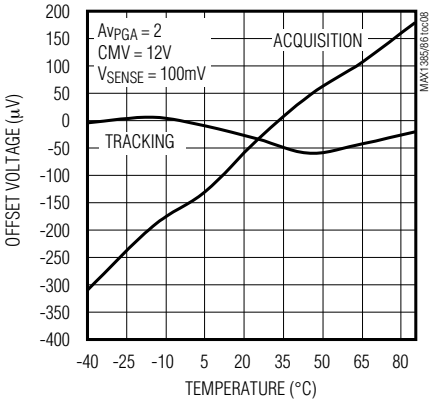
TOTAL PGAOUT_ ERROR vs. V_{SENSE}



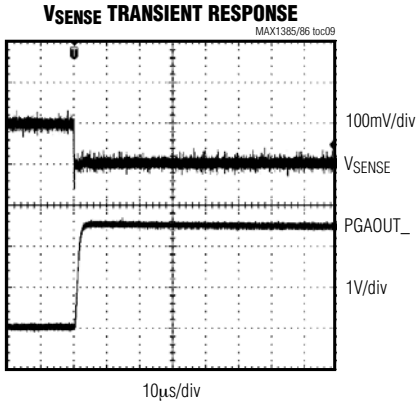
TOTAL PGAOUT_ ERROR vs. COMMON-MODE VOLTAGE



PGAOUT_ OFFSET VOLTAGE vs. TEMPERATURE



V_{SENSE} TRANSIENT RESPONSE

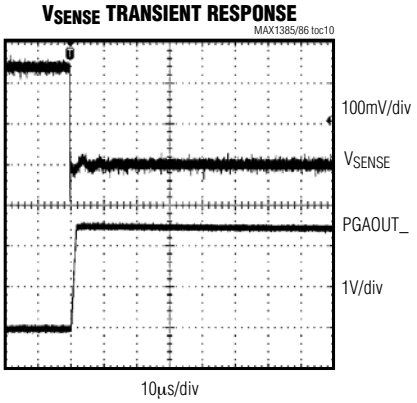


Dual RF LDMOS Bias Controllers with I²C/SPI Interface

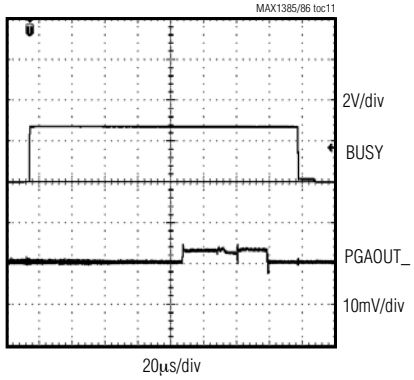
Typical Operating Characteristics (continued)

($GATEV_{DD}$ = +5.5V for the MAX1385, $GATEV_{DD}$ = +11V for the MAX1386, AV_{DD} = DV_{DD} = +5V, external V_{REFADC} = +2.5V, external V_{REFDAC} = +2.5V, C_{REF} = 0.1µF, T_A = +25°C, unless otherwise noted.)

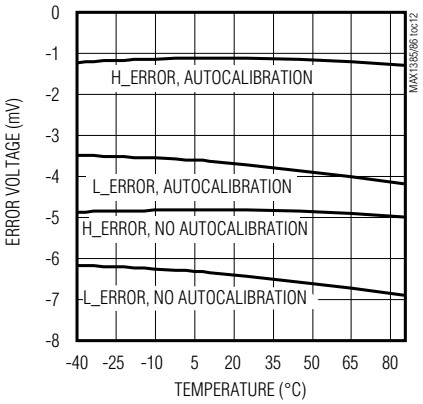
PGAOUT_ 0mV TO 250mV V_{SENSE} TRANSIENT RESPONSE



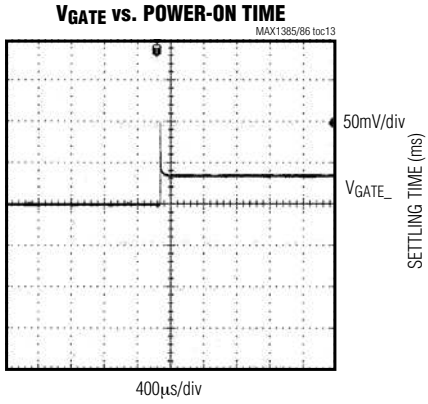
PGAOUT_ PEDESTAL ERROR DURING CALIBRATION



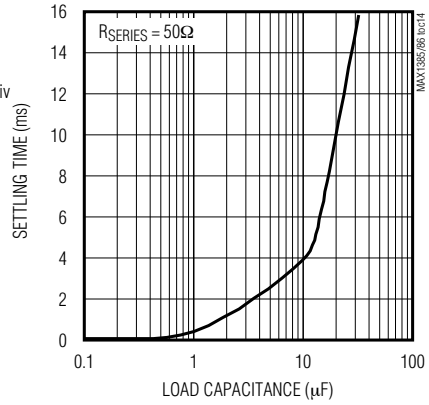
GATE_ OFFSET COMPENSATED ERROR vs. TEMPERATURE



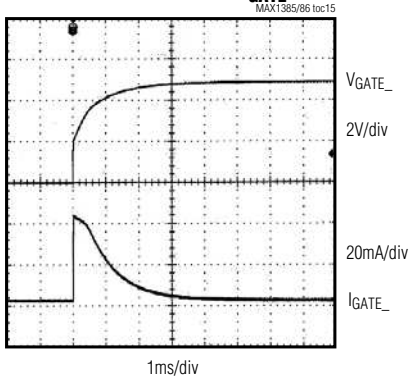
V_{GATE} vs. POWER-ON TIME



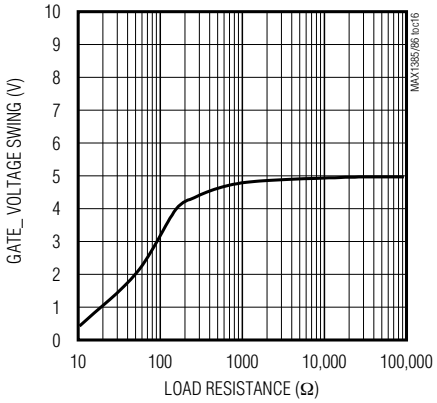
GATE_ SETTLING TIME vs. LOAD CAPACITANCE



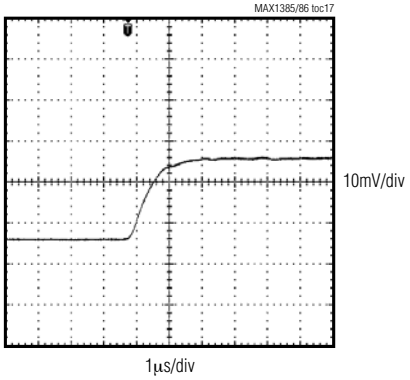
CHARGE CURRENT vs. V_{GATE}



GATE_ VOLTAGE SWING vs. LOAD RESISTANCE



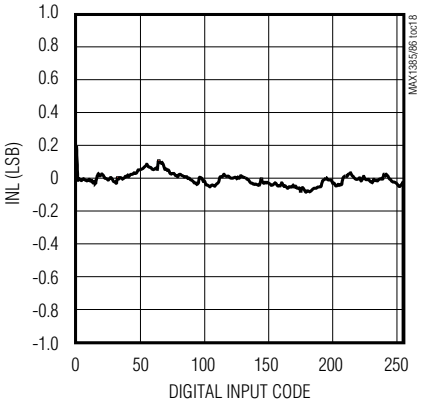
GLITCH ENERGY



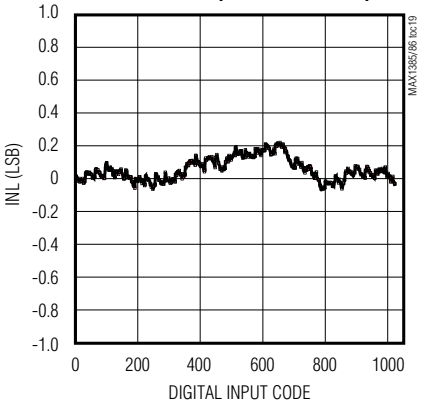
Typical Operating Characteristics (continued)

($GATEV_{DD}$ = +5.5V for the MAX1385, $GATEV_{DD}$ = +11V for the MAX1386, AV_{DD} = DV_{DD} = +5V, external V_{REFADC} = +2.5V, external V_{REFDAC} = +2.5V, C_{REF} = 0.1µF, T_A = +25°C, unless otherwise noted.)

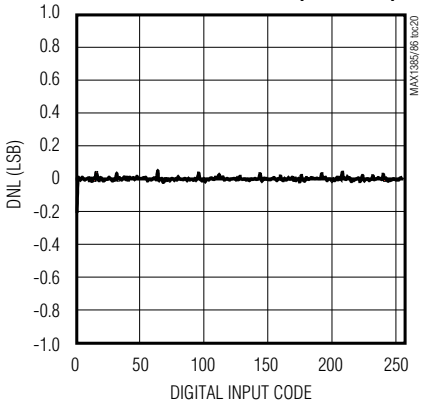
INTEGRAL NONLINEARITY vs. DIGITAL INPUT CODE (8-BIT COARSE DAC)



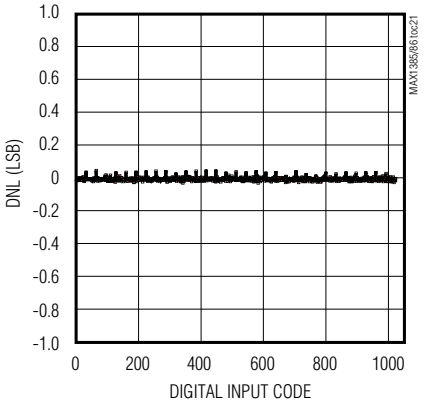
INTEGRAL NONLINEARITY vs. DIGITAL INPUT CODE (10-BIT FINE DAC)



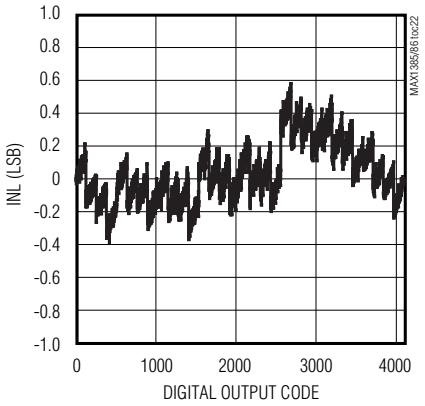
DIFFERENTIAL NONLINEARITY vs. DIGITAL INPUT CODE (8-BIT DAC)



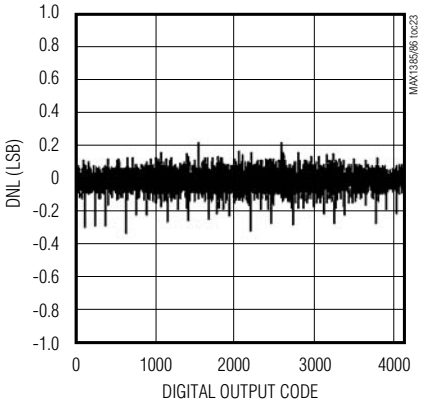
DIFFERENTIAL NONLINEARITY vs. DIGITAL INPUT CODE (10-BIT FINE DAC)



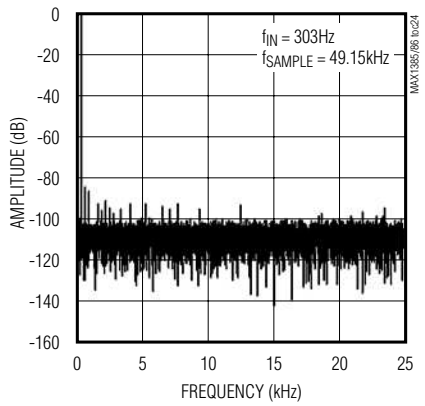
INTEGRAL NONLINEARITY vs. DIGITAL OUTPUT CODE (ADC)



DIFFERENTIAL NONLINEARITY vs. DIGITAL OUTPUT CODE (ADC)



FFT PLOT

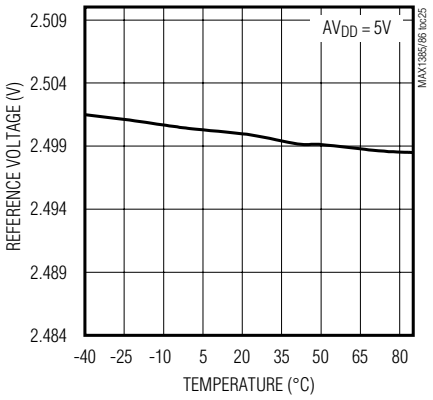


Dual RF LDMOS Bias Controllers with I²C/SPI Interface

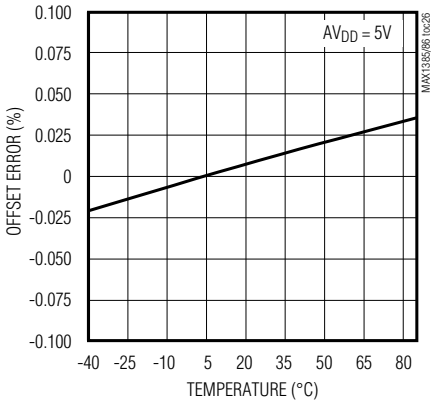
Typical Operating Characteristics (continued)

(GATEV$_{DD}$ = +5.5V for the MAX1385, GATEV$_{DD}$ = +11V for the MAX1386, AV$_{DD}$ = DV$_{DD}$ = +5V, external V$_{REFADC}$ = +2.5V, external V$_{REFDAC}$ = +2.5V, C$_{REF}$ = 0.1µF, T$_A$ = +25°C, unless otherwise noted.)

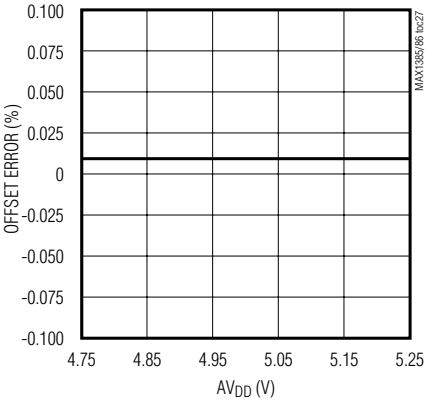
INTERNAL REFERENCE vs. TEMPERATURE



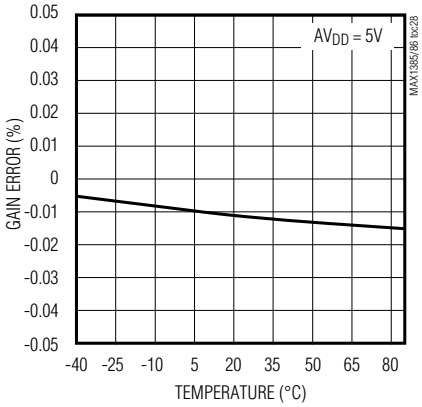
ADC OFFSET ERROR vs. TEMPERATURE



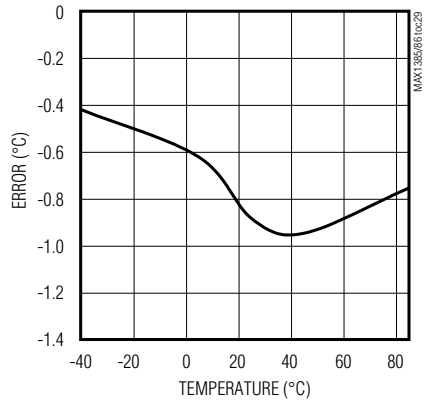
ADC OFFSET ERROR vs. AV$_{DD}$ VOLTAGE



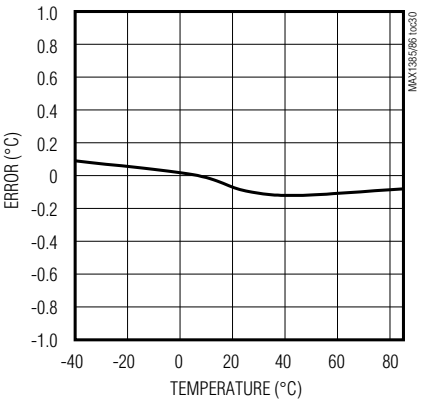
ADC GAIN ERROR vs. TEMPERATURE



INTERNAL TEMPERATURE SENSOR ERROR vs. TEMPERATURE



EXTERNAL TEMPERATURE SENSOR ERROR vs. TEMPERATURE



Pin Description

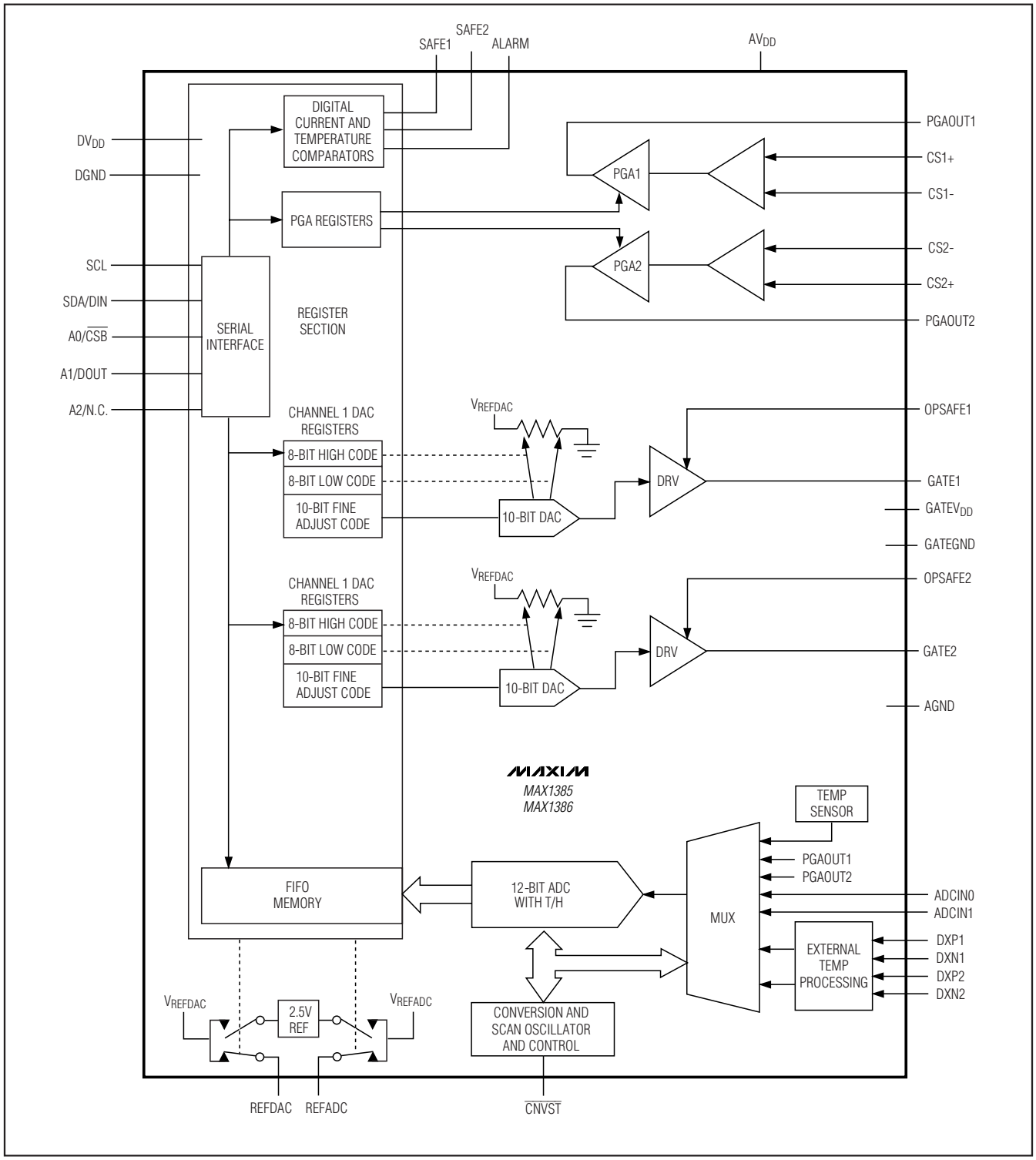
PIN	NAME	FUNCTION
1	DGND	Digital Ground
2	SAFE1	Safe Status Channel 1 Output. Programmable active-high or active-low. SAFE1 asserts when programmed channel 1 temperature threshold or current threshold has been reached.
3	A0/$\overline{CSB}$	I²C-Compatible Address 0/ SPI-Compatible Chip Select. See the *Digital Serial Interface* section. In SPI mode, drive A0/$\overline{CSB}$ low to select the device.
4	$\overline{CNVST}$	Active-Low Conversion-Start Input. Drive $\overline{CNVST}$ low to start a conversion (clock modes 01 and 11). Connect $\overline{CNVST}$ to DV_{DD} when initiating conversions through the serial interface (clock mode 00).
5	SEL	Mode Select. Connect SEL to DGND to select I²C mode. Connect SEL to DV_{DD} to select SPI mode.
6	ALARM	Alarm Output. Program ALARM for comparator or interrupt output modes (see the *Alarm Modes* section). Program ALARM to assert on any combination of channel temperature or current thresholds.
7	SAFE2	Safe Status Channel 2 Output. Programmable active-high or active-low. SAFE2 asserts when programmed channel 2 temperature threshold or current threshold has been reached.
8, 19, 25, 28, 35–39, 42, 46	N.C.	No Connection. Not internally connected.
9	REFDAC	DAC Reference Input/Output
10	REFADC	ADC Reference Input/Output
11	DXP1	Diode Positive Input 1. Connect to anode of temperature diode or the base and collector of an npn transistor.
12	DXN1	Diode Negative Input 1. Connect to cathode of temperature diode or the emitter of an npn transistor.
13	DXP2	Diode Positive Input 2. Connect to anode of temperature diode or the base and collector of an npn transistor.
14	DXN2	Diode Negative Input 2. Connect to cathode of temperature diode or the emitter of an npn transistor.
15	ADCIN1	ADC Input 1
16	ADCIN2	ADC Input 2
17	PGAOUT2	Programmable-Gain Amplifier Output 2
18	AV_{DD}	Analog Power-Supply Input
20, 21, 22	AGND	Analog Ground

Dual RF LDMOS Bias Controllers with I²C/SPI Interface

Pin Description (continued)

PIN	NAME	FUNCTION
23	GATEGND	Gate-Drive Amplifier Ground
24	$GATEV_{DD}$	Gate-Drive Amplifier Supply Input
26	OPSAFE2	Operating Safe Channel 2 Input. Drive OPSAFE2 high to clamp GATE2 to AGND.
27	CS2+	Current-Sense Positive Input 2. CS2+ is the external sense resistor connection to the LDMOS 2 supply.
29	CS2-	Current-Sense Negative Input 2. CS2- is the external sense resistor connection to the LDMOS 2 drain.
30	GATE2	Channel 2 Gate-Drive Amplifier Output
31	GATE1	Channel 1 Gate-Drive Amplifier Output
32	CS1-	Current-Sense Negative Input 1. CS1- is the external sense resistor connection to the LDMOS 1 drain.
33	CS1+	Current-Sense Positive Input 1. CS1+ is the external sense resistor connection to the LDMOS 1 supply.
34	OPSAFE1	Operating Safe Channel 1 Input. Drive OPSAFE1 high to clamp GATE1 to AGND.
40	PGAOUT1	Programmable-Gain Amplifier Output 1
41	A2/N.C.	I²C-Compatible Address 2. See the *Digital Serial Interface* section.
		No Connection. Leave unconnected in SPI mode.
43	SCL	Digital Serial Clock Input
44	SDA/DIN	I²C-Compatible Serial Data Input/Output
		SPI-Compatible Serial Data Input
45	A1/DOUT	I²C-Compatible Address 1. See the *Digital Serial Interface* section.
		SPI-Compatible Serial Data Output
47	BUSY	Device Busy Output. See the *BUSY Output* section
48	DV_{DD}	Digital Supply Input
—	EP	Exposed Pad. Connect to AGND. Internally connected to analog ground.

Functional Diagram



Dual RF LDMOS Bias Controllers with I²C/SPI Interface

Detailed Description

The MAX1385/MAX1386 set and control bias conditions for dual RF LDMOS power devices found in cellular base stations. Each device includes a high-side current-sense amplifier with programmable gains of 2, 10, and 25 to monitor the LDMOS drain current over the 20mA to 5A range. Two external diode-connected transistors monitor the LDMOS temperatures while an internal temperature sensor measures the local die temperature of the MAX1385/MAX1386. A 12-bit ADC converts the programmable-gain amplifier (PGA) outputs, external/internal temperature readings, and two auxiliary inputs.

The two gate-drive channels, each consisting of 8-bit coarse and 10-bit fine DACs and a gate-drive amplifier, generate a positive gate voltage to bias the LDMOS devices. The MAX1385 includes a gate-drive amplifier with a gain of 2 and the MAX1386 gate-drive amplifier provides a gain of 4. The 8-bit coarse and 10-bit fine DACs allow up to 18 bits of resolution. The MAX1385/MAX1386 include autocalibration modes to minimize error over time, temperature, and supply voltage.

The MAX1385/MAX1386 feature an I²C-/SPI-compatible serial interface. Both devices operate from a 4.75V to 5.25V analog supply (3.2mA supply current), a 2.7V to 5.25V digital supply (3.1mA supply current), and a 4.75V to 11.0V gate-drive supply (4.5mA supply current).

Power-On Reset

On power-up, the MAX1385/MAX1386 are in full power-down mode (see the *SSHUT (Write)* section). To change to normal power mode, write two commands to the Software Shutdown register. The first command sets FULLPD to 0 (other bits in the Software Shutdown register are ignored). A second command is needed to activate any internal blocks. The recommended sequence of commands to ensure reliable startup following the application of power, is given in the *Appendix: Recommended Power-Up Code Sequence* section.

ADC Description

The MAX1385/MAX1386 ADC uses a fully differential successive approximation register (SAR) conversion technique and on-chip track-and-hold (T/H) circuitry to convert temperature and voltage signals into 12-bit digital results. The analog inputs accept single-ended input signals. Single-ended signals are converted using a unipolar transfer function. See the ADC transfer function of Figure 25 for more information.

The internal ADC block converts the results of the die temperature, remote diode temperature readings, PGAOUT1, PGAOUT2, ADCIN1, or ADCIN2 voltages according to which bits are set in the ADC Conversion register (see the *ADCCON (Write)* section). The results of the conversions are written to FIFO memory. The FIFO holds up to 15 words (each word is 16 bits) with channel tags to indicate which channel the 12-bit data comes from. The FIFO indicates an overflow condition and an underflow condition (read of an empty FIFO) by the Flag register (see the *RDFLAG (Read)* section) and channel tags. The FIFO always stores the most recent conversion results and allows the oldest data to be overwritten. Read the latest result stored in the FIFO by sending the appropriate read command byte (see the *FIFO (Read)* section).

Read the data stored in the FIFO through the FIFO Read register. The *FIFO (Read)* section details which channel is being read and whether the FIFO has overflowed.

Analog-to-Digital Conversion Scheduling

The MAX1385/MAX1386 ADC multiplexer scans selected inputs in the order shown in Table 1. The ADC multiplexer skips over the items that are not selected in the Analog-to-Digital Conversion register. When writing a conversion command before a conversion is complete, the pending conversion may be canceled. In addition, using the serial interface while the ADC is converting may degrade the performance of the ADC.

ADC Clock Modes

The MAX1385/MAX1386 offer three different conversion/acquisition modes (known as clock modes) selectable through the Device Configuration register (see the *DCFIG (Read/Write)* section). Clock Mode 10 is reserved and cannot be used. For conversion/acquisition examples and timing diagrams, see the *Applications Information* section.

If the analog-to-digital conversion requires the internal reference (temperature measurement or voltage measurement with internal reference selected) and the reference has not been previously forced on, the device inserts a worst-case delay of 81µs, for the reference to settle, before commencing the analog-to-digital conversion. The reference remains powered up while there are pending conversions. If the reference is not forced on, it automatically powers down at the end of a scan or when CONCONV in the Analog-to-Digital Conversion register is set back to 0.

Clock Mode 00

In clock mode 00, power-up, acquisition, conversion, and power-down are all initiated by writing to the Analog-to-Digital Conversion register and performed automatically using the internal oscillator. This is the default clock mode. The ADC sets the BUSY output high, powers up, scans all requested channels, stores the results in the FIFO, and then powers down. After the scan is complete, BUSY is pulled low and the results for all the commanded channels are available in the FIFO.

Clock Mode 01

In clock mode 01, power-up, acquisition, conversion, and power-down are all initiated by setting $\overline{CNVST}$ low for at least 40ns. Conversions are performed automatically using the internal oscillator. The ADC sets the BUSY output high, powers up, scans all requested channels, stores the results in the FIFO, and then powers down. After the scan is complete, BUSY is pulled low and the results for all the commanded channels are available in the FIFO.

Clock Mode 11

In clock mode 11, conversions are initiated one at a time through $\overline{CNVST}$ in the order shown in Table 1 and performed using the internal oscillator. In this mode, the acquisition time is controlled by the time $\overline{CNVST}$ is brought low. $\overline{CNVST}$ is resynchronized by the internal oscillator, which means there is a one-clock-cycle uncertainty (typically 320ns) in the exact sampling instant. Different timing parameters apply depending whether the conversion is temperature, voltage, using the external reference, or using the internal reference.

Table 1. Order of ADC Conversion Scan

ORDER OF SCAN	DESCRIPTION OF CONVERSION
1	Internal device temperature
2	External diode 1 temperature
3	PGAOUT1 for current sense
4	ADCIN1
5	External diode 2 temperature
6	PGAOUT2 for current sense
7	ADCIN2

For a temperature conversion, set $\overline{CNVST}$ low for at least 40ns. The BUSY output goes high and the temperature conversion results are available after an additional 94µs (when BUSY goes low again). Thus, the worst-case conversion time of the initial temperature sensor scan (allowing the internal reference to settle) is 175µs. Subsequent temperature scans only take 85µs worst case as the internal reference and temperature sensor circuits are already powered.

For a voltage conversion while using an internal or external reference, set $\overline{CNVST}$ low for at least 2µs but less than 6.7µs. The BUSY output goes high and the conversion results are available after an additional 7.5µs (typ) when BUSY goes low again.

Continuous conversion is not supported in this clock mode (see the *ADCCON (Write)* section).

Changing Clock Modes During ADC Conversions

If a change is made to the clock mode in the Device Configuration register while the ADC is already performing a conversion (or series of conversions), the following descriptions show how the MAX1385/MAX1386 respond:

- **CKSEL = 00 and is then changed to another value**

  The ADC completes the already triggered series of conversions and then goes idle. The BUSY output remains high until the conversions are completed. The MAX1385/MAX1386 then respond in accordance with the new CKSEL mode.

- **CKSEL = 01 and is then changed to another value**

  If waiting for the initial external trigger, the MAX1385/MAX1386 immediately exit clock mode 01, power down the ADC, and go idle. The BUSY output stays low and waits for the external trigger. If a conversion sequence has started, the ADC completes the requested conversions and then goes idle. The BUSY output remains high until the conversions are completed. The MAX1385/MAX1386 then respond in accordance with the new CKSEL mode.

- **CKSEL = 11 and is then changed to another value**

  If waiting for an external trigger, the MAX1385/MAX1386 immediately exit clock mode 11, power down the ADC, and go idle. The BUSY output stays low and waits for the external trigger.

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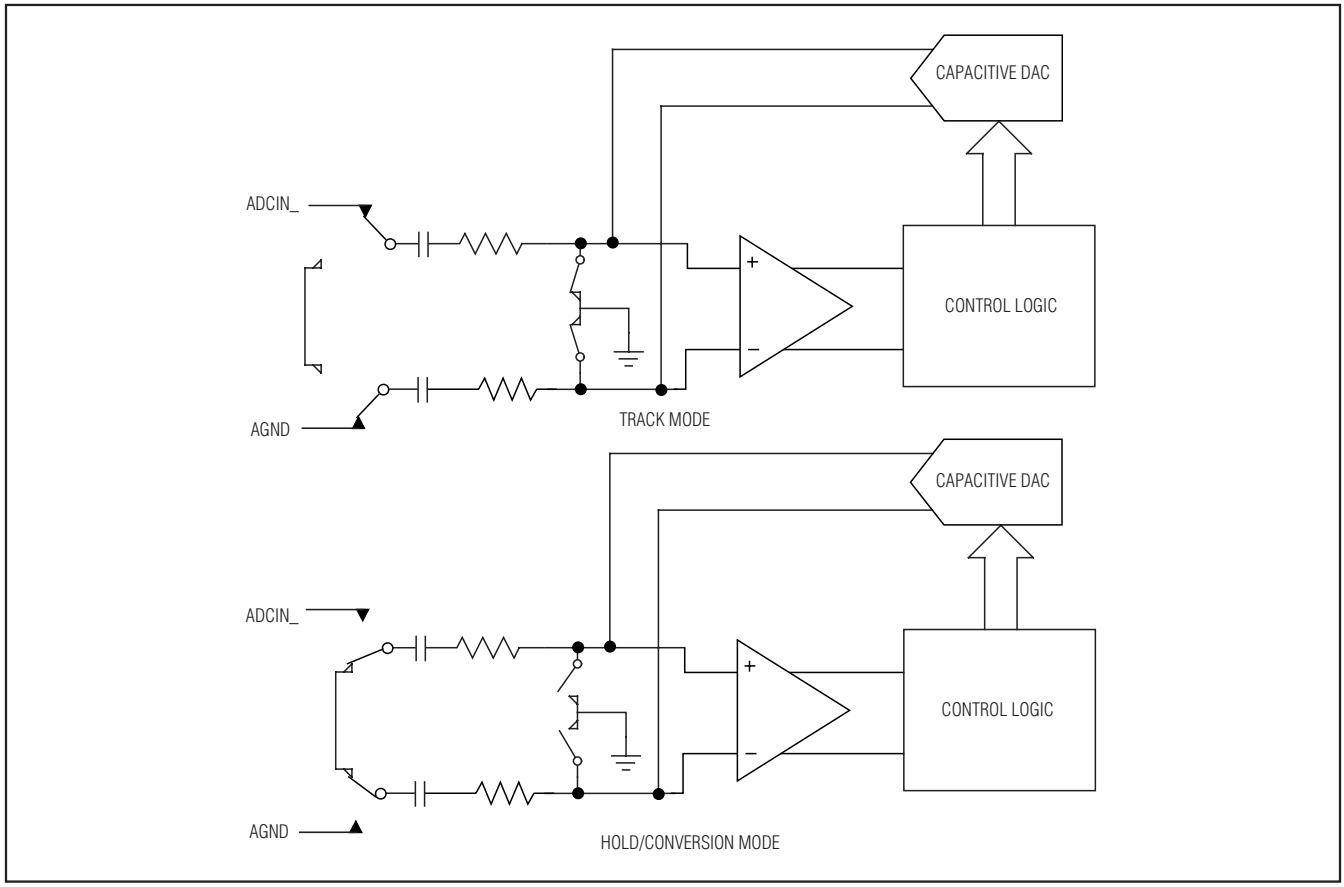

Figure 4. Equivalent ADC Input Circuit

Analog Input Track and Hold

The equivalent circuit (Figure 4) shows the MAX1385/MAX1386 ADC input architecture. In track mode, a positive input capacitor is connected to ADCIN_ and a negative input capacitor is connected to AGND. After the T/H enters hold mode, the difference between the sampled positive and negative input voltages is converted. The input capacitance charging rate determines the time required for the T/H to acquire an input signal. If the input signal's source impedance is high, the required acquisition time lengthens.

Any source impedance below 300Ω does not significantly affect the ADC's AC performance. A high-impedance source can be accommodated either by lengthening t_{ACQ} or by placing a 1µF capacitor between the positive input and AGND. The combination of the analog input source impedance and the capacitance at the analog input creates an RC filter that limits the analog-input bandwidth.

Analog-Input Bandwidth

The ADC's input-tracking circuitry has a 10MHz bandwidth to digitize high-speed transient events. Anti-alias prefiltering of the input signals is necessary to avoid high-frequency signals aliasing into the frequency band of interest.

Analog-Input Protection

Internal ESD protection diodes clamp all analog inputs to AV_{DD} and AGND, allowing the inputs to swing from AGND - 0.3V to AV_{DD} + 0.3V without damage. If an analog input voltage exceeds the supplies, limit the input current to 2mA.

DAC Description

The MAX1385/MAX1386 include two 8-bit and 10-bit DAC blocks to independently control the voltage on each LDMOS gate. Both 10-bit and 8-bit DACs can be automatically calibrated to minimize output error over time, temperature, and supply voltage. The 8-bit and 10-bit DACs have unipolar transfer functions and have a relationship to the output voltage by the following equation:

$$V_{DACOUT} = \frac{V_{REF}}{2^8} \times LOCODE + \frac{V_{REF}}{2^8} \times [HICODE - LOCODE] \times \frac{FINECODE}{2^{10}}$$

where LOCODE, HICODE, and FINECODE are the low wiper (8 bits), high wiper (8 bits), and fine DAC (10 bits) values written to the DAC by the user. LOCODE, HICODE, and FINECODE represent the values in the DAC input registers and may or may not be the actual values in the DAC output registers depending whether autocalibration is used or not (see the 8-Bit *Coarse-DAC Adjustment* section). To find the actual voltage at GATE_, multiply the V_{DACOUT} result by 2 (MAX1385) or 4 (MAX1386). Due to the buffer amplifiers, the voltage at GATE_ cannot be set below 100mV above AGND. It is recommended that the LOCODE for DAC1 and DAC2 are set so that the minimum possible output at GATE_ is 200mV (MAX1385) and 400mV (MAX1386).

The DACs can be operated to produce an 18-bit monotonic DAC with 12-bit (typ) INL. Write to either HICODE or LOCODE in a leapfrog fashion, without commanding autocalibration, to configure the 18-bit monotonic DAC. When LOCODE > HICODE, invert the value of FINECODE.

8-Bit Coarse-DAC Adjustment

Each DAC control block contains a resistor string with wipers that serve as an 8-bit coarse DAC. Wipers are set by writing to the appropriate DAC input registers and/or using the Load DAC Control register (LDAC) commands. The output of a coarse DAC is not updated until the appropriate DAC output register(s) have been set. See Figure 5 for the relationship between DAC input registers, DAC output registers, and wipers.

DAC output registers are not directly accessible to the user. Choose which input register to write to based on whether automatic low or high calibration is desired, or if updates to the output of the DAC need to be initiated immediately. In the case of automatic low or high calibration, a correction code is added to or subtracted from the 10-bit fine-DAC input register. Transfers from the DAC input registers to DAC output registers can occur immediately after a write to the appropriate DAC input register or on a software command through the Software LDAC register. See the *Register Descriptions* section for bit-level descriptions of these registers.

10-Bit Fine-DAC Adjustment

Each DAC control block contains a 10-bit fine DAC that operates between the high and low wiper positions from the 8-bit coarse DAC. The 10-bit fine DAC also has an optional automatic calibration mode and can be updated immediately or on a software-issued command in the Software LDAC register. Writing to the appropriate fine-DAC input register determines whether automatic calibration is used and/or when the DAC is updated. See Figure 6 for the relationship between DAC input registers, DAC output registers, and the Software LDAC register.

The fine-DAC output registers are not directly accessible. Choose which DAC input register to write to based on whether automatic fine calibration is desired, or whether updates to the output of the DAC need to be initiated immediately. In the case of automatic fine calibration, a correction code is added to or subtracted from the input register code and transferred to the appropriate fine-DAC output register. Transfers from a fine-DAC input register to a fine-DAC output register can occur immediately after a write to the appropriate DAC input register or on a software command through the Software LDAC register. See the *Register Descriptions* section for bit-level detail of these registers.

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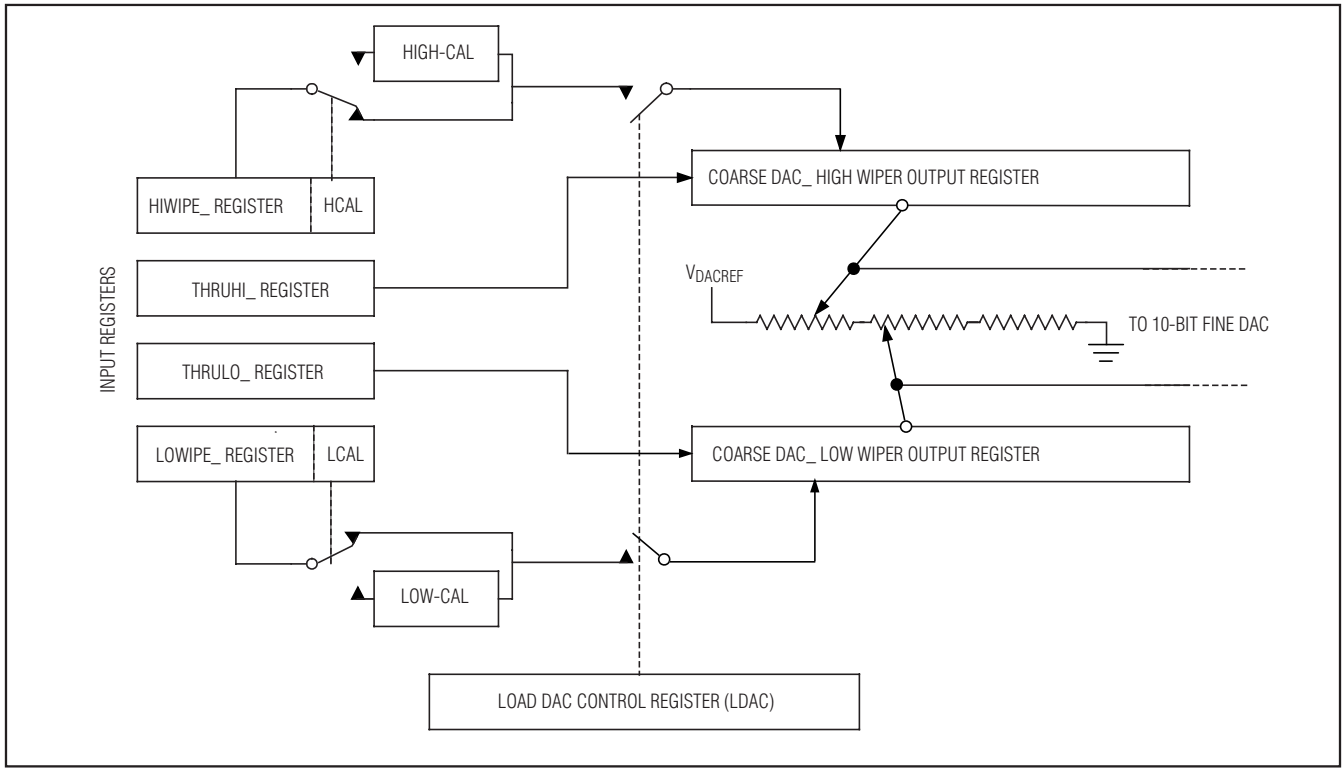

Figure 5. Coarse-DAC Register Diagram

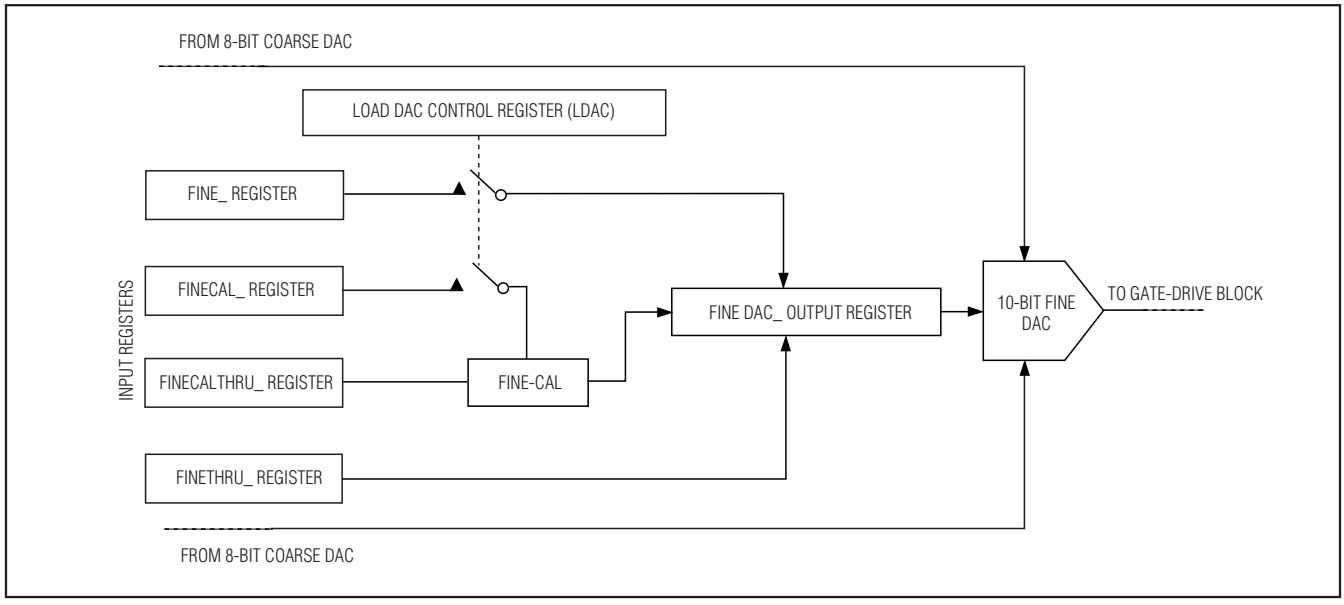

Figure 6. Fine-DAC Register Diagram

ADC/DAC References

The MAX1385/MAX1386 provide an internal low-noise 2.5V reference for the ADCs, DACs, and temperature sensor. See the *Device Configuration Register* section for information on configuring the device for external or internal reference. Connect a voltage source to REFADC in the 1V to AV_{DD} range when using an external ADC reference. Connect a voltage source to REFDAC in the 0.5V to 2.5V range when using an external DAC reference. When using an external voltage reference, bypass the reference pin with a 0.1µF capacitor to AGND.

The internal reference has a lowpass filter to reduce noise. The device allows 60µs (typ) and 81µs (typ) worst case for the reference to settle before permitting an analog-to-digital conversion. If reference mode 11 is selected, the required settling time is longer. In this case, the user should set at least one of DAC1PD, DAC2PD, or FBGON in the Software Shutdown register, any of which forces the reference to be permanently powered up.

Temperature Measurements

The MAX1385/MAX1386 measure the internal die temperature and two external remote-diode temperature sensors. Set up a temperature conversion by writing to the Analog-to-Digital Conversion register (see the *ADCCON (Write)* section). Optionally program SAFE1 and SAFE2 outputs to depend on programmed temperature thresholds.

The MAX1385/MAX1386 can perform temperature measurements with an internal diode-connected transistor. The diode bias current changes from 66µA to 4µA to produce a temperature-dependent bias voltage difference. The second conversion result at 4µA is subtracted from the first at 66µA to calculate a digital value that is proportional to the absolute temperature. The stored data result is the aforementioned digital code minus an offset to adjust from Kelvin to Celsius.

The reference voltage for the temperature measurements is always derived from the internal reference source. Temperature results are in degrees Celsius (two's-complement form).

The temperature-sensing circuits power up for the first temperature measurement in an analog-to-digital conversion scan. The temperature-sensing circuits remain powered until the end of the scan to avoid a possible 67µs delay of internal reference power-up time for each individual temperature channel. If the continuous convert bit CONCONV is set high and the current ADC channel selection includes a temperature channel, the temperature-sensor circuits remain powered up until the CONCONV bit is set low.

The external temperature-sensor drive current ratio has been optimized for a 2N3904 npn transistor with an ideality factor of 1.0065. The nonideality offset is removed internally by a preset digital coefficient. Use of a transistor with a different ideality factor produces a proportionate difference in the absolute measured temperature. More details on this topic and others related to using an external temperature sensor can be found in Maxim Application Note 1057: *Compensating for Ideality and Series Resistance Differences Between Thermal Sense Diodes* and Application Note 1944: *Temperature Monitoring Using the MAX1253/MAX1254 and MAX1153/MAX1154*.

High-Side Current-Sense PGAs

The MAX1385/MAX1386 provide two high-side current-sense amplifiers with programmable gain. The current-sense amplifiers are unidirectional and provide a 5V to 30V input common-mode range. Both CS1+ and CS2+ must be within the specified common-mode range for proper operation of each amplifier.

The sense amplifiers measure the load current, I_{LOAD}, through an external sense resistor, $R_{SENSE\_}$, between the CS_+ and CS_- inputs. The full-scale sense voltage range ($V_{SENSE\_} = V_{CS\_+} - V_{CS\_-}$) depends on the programmed gain, $Av_{PGA\_}$ (see the *DCFIG (Read/Write)* section). The sense amplifiers provide a voltage output at PGAOUT_ according to the following equation:

$$V_{PGAOUT\_} = Av_{PGA\_} \times (V_{CS\_+} - V_{CS\_-})$$

These outputs are also routed to the internal 12-bit ADC so that a digital representation of the amplified voltages can be read through the FIFO.

The PGA scales the sensed voltages to fit the input range of the ADC. Program the PGA with gains of 2, 10, and 25 by setting the PGSET_ bits (see the *DCFIG (Read/Write)* section). The input stages have nominal input offset voltages of 0mV that can be adjusted by a trim DAC (not shown in the *Functional Diagram*) over the -3mV to +3mV range in 25µV steps. Autocalibration can be used to control the trim DAC to minimize the effective channel input offset voltage (see the *PGACAL (Write)* section). The PGA feedback network is referenced to AGND.

ALARM Output

The state of ALARM is logically equivalent to the inclusive OR of SAFE1 and SAFE2. The exception to this statement is when ALARM is configured for output interrupt mode (see the *Alarm Modes* section). When in output-interrupt mode, ALARM stays in its asserted state until its associated flag is cleared by reading from the

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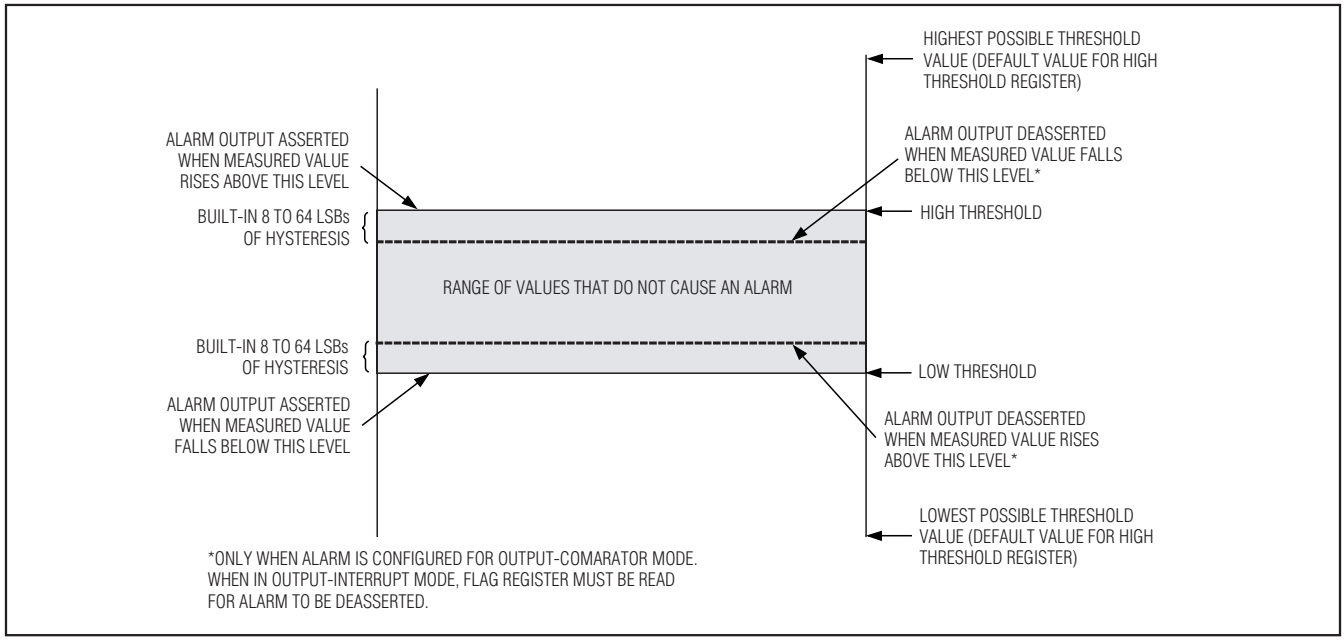

Figure 7. Window-Threshold-Mode Diagram

Flag register. Configure ALARM for open-drain/push-pull and active-high/active-low by setting the respective bits in the Hardware Alarm Configuration register.

SAFE1/SAFE2 Outputs

Set up the SAFE1 and SAFE2 outputs to allow Wired-OR/AND-type logic functions or to create additional interrupt-type signals to replace or supplement the existing ALARM output. SAFE1 and SAFE2 do not have any internal pullup/pulldown devices.

The SAFE1 and SAFE2 output buffers are CMOS-compatible, noninverting, output buffers capable of driving to within 0.5V of either digital rail. The SAFE1 and SAFE2 outputs power up as active-high CMOS outputs with standard logic levels. Configure the SAFE1 and SAFE2 outputs for open-drain or push-pull by setting the appropriate bits in the Hardware Alarm Configuration register. When configuring SAFE1 and SAFE2 as open-drain outputs, an external pullup resistor is required.

BUSY Output

The BUSY output is forced high to show that the MAX1385/MAX1386 are busy for a variety of reasons:

- The ADC is in the middle of a user-commanded conversion cycle (but not in continuous convert mode)
- The ADC is in the middle of an internally triggered conversion cycle (for a self-calibration measurement)
- The device is in the middle of DAC calibration calculations
- The device is in the middle of power-up initialization
- One of the PGA channels is undergoing self-calibration

The serial interface remains active regardless of the state of the BUSY output. Wait until BUSY goes low to read the current conversion data from the FIFO. When BUSY is high as a result of an ADC conversion, do not enter a second conversion command until BUSY has gone low to indicate the previous conversion is complete. The rising edge of BUSY occurs on the next internal oscillator clock after the start of a new conversion (either by $\overline{CNVST}$ or an interface command).

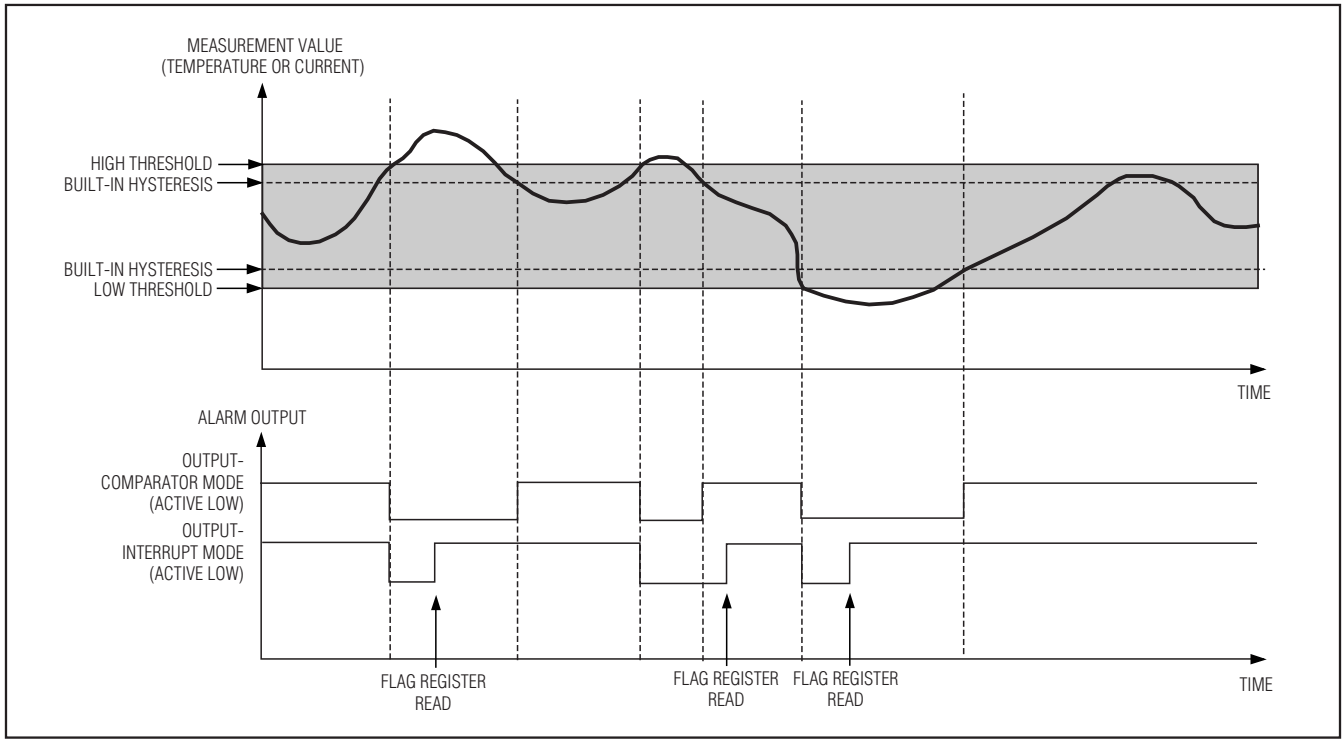

Figure 8. Window-Threshold-Mode Timing Diagram

In single-conversion mode (CKSEL = 11), the BUSY signal remains high until the ADC has completed the current conversion (not the entire scan, just the current conversion), the data has been moved into the FIFO, and the alarm limits for the channel have been checked (if enabled). In multiple-conversion mode (CKSEL = 01 or CKSEL = 00), the BUSY signal remains high until all channels have been scanned and the data from the final channel has been moved into the FIFO and checked for alarm limits (if enabled). In continuous-conversion mode (CONCONV = 1), the BUSY signal does not go high as a result of ADC conversions; however, BUSY does go high when CONCONV is removed and remains high until the current scan is complete and the ADC sequence halts.

After commanding any of the DAC autocalibration components, wait for BUSY to go low before setting OSCPD to 1.

Alarm Modes

The MAX1385/MAX1386 contain several programmable modes for configuring outputs ALARM, SAFE1, and SAFE2 behavior. Window-threshold mode allows SAFE_ to assert when the temperature/current is too high or too low (outside the window). Hysteresis-threshold mode allows SAFE_ to assert when the temperature/current is too high, and then to deassert when the temperature/current falls back to an appropriate level. ALARM asserts when SAFE1 and/or SAFE2 asserts. Program ALARM for output-comparator mode to stay asserted after an alarm condition until temperature/current levels are back below programmed thresholds. Program ALARM for output-interrupt mode to stay asserted after an alarm condition until the Flag register is read.

Window-Threshold Mode

In window-threshold mode, ADC readings of current/temperature are compared to the configured current/temperature low/high thresholds that are programmed to cause an alarm condition. If an ADC reading falls out of the configured window and ALARM is configured for output-comparator mode, ALARM asserts until the current/temperature reading falls back into the window (past the built-in hysteresis). If an ADC reading falls out of the configured window and ALARM is configured for output-interrupt mode, ALARM asserts until the Flag register is read. Set the amount of built-in hysteresis from 8 LSBs to 64 LSBs (see the *ALMSCFG (Read/Write)* section). See Figures 7 and 8.