Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

19-1481; Rev 1; 7/02

EVALUATION KIT AVAILABLE

+3V, 18-Bit, Low-Power, Multichannel, Oversampling (Sigma-Delta) ADC

General Description

The MAX1403 18-bit, low-power, multichannel, serial-output analog-to-digital converter (ADC) features matched 200µA current sources for sensor excitation. This ADC uses a sigma-delta modulator with a digital decimation filter to achieve 16-bit accuracy. The digital filter's user-selectable decimation factor allows the conversion resolution to be reduced in exchange for a higher output data rate. True 16-bit performance is achieved at an output data rate of up to 480sps. In addition, the modulator sampling frequency may be optimized for either lowest power dissipation or highest throughput rate. The MAX1403 operates from +3V.

This device offers three fully differential input channels that may be independently programmed with a gain between +1V/V and +128V/V. Furthermore, it can compensate an input-referred DC offset up to 117% of the selected full-scale range. These three differential channels may also be configured to operate as five pseudo-differential input channels. Two additional, fully differential system-calibration channels are provided for gain and offset error correction.

The MAX1403 can be configured to sequentially scan all signal inputs and provide the results via the serial interface with minimum communications overhead. When used with a 2.4576MHz or 1.024MHz master clock, the digital decimation filter can be programmed to produce zeros in its frequency response at the line frequency and associated harmonics, ensuring excellent line rejection without the need for further postfiltering.

The MAX1403 is available in a 28-pin SSOP package.

Applications

Portable Industrial Instruments

Portable Weigh Scales

Loop-Powered Systems

Pressure Transducers

Ordering Information

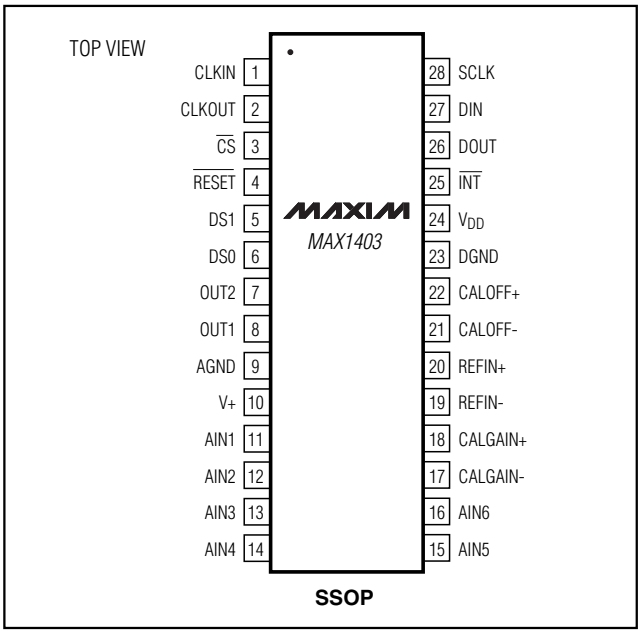
PART	TEMP RANGE	PIN-PACKAGE
MAX1403CAI	0°C to +70°C	28 SSOP
MAX1403EAI	-40°C to +85°C	28 SSOP

SPI and QSPI are trademarks of Motorola, Inc.

Features

- **18-Bit Resolution, Sigma-Delta ADC**
- **16-Bit Accuracy with No Missing Codes to 480sps**
- **Matched On-Board Current Sources (200µA) for Sensor Excitation**
- **Low Quiescent Current**
  250µA (operating mode)
  2µA (power-down mode)
- **3 Fully Differential or 5 Pseudo-Differential Signal Input Channels**
- **2 Additional, Fully Differential Calibration Channels/Auxiliary Input Channels**
- **Programmable Gain and Offset**
- **Fully Differential Reference Inputs**
- **Converts Continuously or On Command**
- **Automatic Channel Scanning and Continuous Data Output Mode**
- **Operates with Analog and Digital Supplies from +2.7V to +3.6V**
- **SPI™/QSPI™-Compatible 3-Wire Serial Interface**
- **28-Pin SSOP Package**

Pin Configuration



+3V, 18-Bit, Low-Power, Multichannel, Oversampling (Sigma-Delta) ADC

ABSOLUTE MAXIMUM RATINGS

V+ to AGND, DGND .....-0.3V to +6V
V_{DD} to AGND, DGND .....-0.3V to +6V
AGND to DGND .....-0.3V to +0.3V
Analog Inputs to AGND .....-0.3V to (V+ + 0.3V)
Analog Outputs to AGND .....-0.3V to (V+ + 0.3V)
Reference Inputs to AGND .....-0.3V to (V+ + 0.3V)
CLKIN and CLKOUT to DGND .....-0.3V to (V_{DD} + 0.3V)
All Other Digital Inputs to DGND .....-0.3V to +6V
All Digital Outputs to DGND .....-0.3V to (V_{DD} + 0.3V)

Maximum Current Input into Any Pin 50mA
Continuous Power Dissipation (T_A = +70°C)
28-Pin SSOP (derate 9.52mW/°C above +70°C) 524mW
Operating Temperature Ranges
MAX1403CAI .....0°C to +70°C
MAX1403EAI .....-40°C to +85°C
Storage Temperature Range .....-60°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = +2.7V to +3.6V, V_{DD} = +2.7V to +3.6V, V_{REFIN+} = +1.25V, REFIN- = AGND, f_{CLKIN} = 2.4576MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC PERFORMANCE						
Noise-Free Resolution		No missing codes guaranteed by design; for filter settings with FS1 = 0	16			Bits
Output Noise		Depends on filter setting and selected gain		(Tables 16a, 16b)		
Integral Nonlinearity (Note 1)	INL	Bipolar mode; FS1 = 0; MF1, MF0 = 0	-0.0015		0.0015	%FSR
		FS1 = 0; MF1, MF0 = 1, 2, 3		±0.001		
Nominal Gain (Note 2)				0.98		
Unipolar Offset Error		Relative to nominal of 1% FSR	-1		2	%FSR
Unipolar Offset Drift		For gains of 1, 2, 4		0.5		µV/°C
		For gains of 8, 16, 32, 64, 128		0.3		
Bipolar Zero Error			-2.0		2.0	%FSR
Bipolar Zero Drift		For gains of 1, 2, 4		0.8		µV/°C
		For gains of 8, 16, 32, 64, 128		0.3		
Positive Full-Scale Error (Note 3)		For gains of 1, 2, 4, 8, 16, 32, 64	-2.5		2.5	%FSR
		For gain of 128	-3.5		3.5	
Full-Scale Drift (Note 4)		For gains of 1, 2, 4		0.8		µV/°C
		For gains of 8, 16, 32, 64, 128		0.3		
Gain Error (Note 5)		For gains of 1, 2, 4, 8, 16, 32, 64	-2		2	%FSR
		For gain of 128	-3		3	
Gain-Error Drift (Note 6)		For gains of 1, 2, 4, 8, 16, 32, 64		1		ppm/°C
		For gain of 128		5		
Bipolar Negative Full-Scale Error		For gains of 1, 2, 4, 8, 16, 32, 64	-2.5		2.5	%FSR
		For gain of 128	-3.5		3.5	
Bipolar Negative Full-Scale Drift		For gains of 1, 2, 4		0.8		µV/°C
		For gains of 8, 16, 32, 64, 128		0.3		

ELECTRICAL CHARACTERISTICS (continued)

(V+ = +2.7V to +3.6V, V_{DD} = +2.7V to +3.6V, V_{REFIN+} = +1.25V, REFIN- = AGND, f_{CLKIN} = 2.4576MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
OFFSET DAC							
Offset DAC Range (Note 7)		Unipolar mode		-116.7		116.7	%FSR
		Bipolar mode		-58.35		58.35	
Offset DAC Resolution		Unipolar mode			16.7		%FSR
		Bipolar mode			8.35		
Offset DAC Full-Scale Error		Input referred	Gain = 1, 2, 4, 8, 16, 32, 64	-2.5		+2.5	%FSR
			Gain = 128	-3.5		+3.5	
Offset DAC Zero-Scale Error					0		%FSR
Additional Noise from Offset DAC (Note 8)		DAC code = 0000			0		μV_{RMS}
ANALOG INPUTS/REFERENCE INPUTS (Specifications for AIN and REFIN, unless otherwise noted.)							
Common-Mode Rejection	CMR	At DC		90			dB
		For filter notch 50Hz, ±0.02 · f_{NOTCH}, MF1 = 0, MF0 = 0, f_{CLKIN} = 2.4576MHz (Note 9)		150			
		For filter notch 60Hz, ±0.02 · f_{NOTCH}, MF1 = 0, MF0 = 0, f_{CLKIN} = 2.4576MHz (Note 9)		150			
Normal Mode 50Hz Rejection (Note 9)	NMR	For filter notch 50Hz, ±0.02 · f_{NOTCH}, MF1 = 0, MF0 = 0, f_{CLKIN} = 2.4576MHz		100			dB
Normal Mode 60Hz Rejection (Note 9)	NMR	For filter notch 60Hz, ±0.02 · f_{NOTCH}, MF1 = 0, MF0 = 0, f_{CLKIN} = 2.4576MHz		100			dB
Common-Mode Voltage Range (Note 10)		REFIN and AIN for BUFF = 0		V_{AGND}		V+	V
Absolute Input Voltage Range		REFIN and AIN for BUFF = 0		V_{AGND} - 30mV		V+ + 30mV	V
Absolute and Common-Mode AIN Voltage Range		BUFF = 1		V_{AGND} + 200mV		V+ - 1.5	V
DC Input Leakage Current (Note 11)		REFIN and AIN for BUFF = 0	T_A = +25°C		40		pA
			T_A = T_{MIN} to T_{MAX}			10	nA
AIN Input Current (Note 11)		BUFF = 1				10	nA
AIN Input Capacitance (Notes 12)		BUFF = 0	Gain = 1		34		pF
			Gain = 2		38		
			Gain = 4		45		
			Gain = 8, 16, 32, 64, 128		60		
		BUFF = 1, all gains			30		
AIN Differential Voltage Range (Note 13)		Unipolar input range (U/$\overline{B}$ bit = 1)		0 to V_{REF} / gain			V
		Bipolar input range (U/$\overline{B}$ bit = 0)		±V_{REF} / gain			

+3V, 18-Bit, Low-Power, Multichannel, Oversampling (Sigma-Delta) ADC

ELECTRICAL CHARACTERISTICS (continued)

(V+ = +2.7V to +3.6V, V_{DD} = +2.7V to +3.6V, V_{REFIN+} = +1.25V, REFIN- = AGND, f_{CLKIN} = 2.4576MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
AIN and REFIN Input Sampling Frequency	f_S			(Table 15)		Hz
REFIN+ - REFIN- Voltage (Note 14)		±5% for specified performance; functional with lower V_{REF}			1.25	V
LOGIC INPUTS						
Input Current	I_{IN}		-10		+10	µA
Input Low Voltage	V_{IL}	All inputs except CLKIN			0.4	V
		CLKIN only			0.4	
Input High Voltage	V_{IH}	All inputs except CLKIN	2			V
		CLKIN only	2.4			
Input Hysteresis	V_{HYS}	All inputs except CLKIN		200		mV
LOGIC OUTPUTS						
Output Low Voltage (Note 15)	V_{OL}	DOUT and $\overline{INT}$, I_{SINK} = 100µA			0.4	V
		CLKOUT, I_{SINK} = 10µA			0.4	
Output High Voltage (Note 15)	V_{OH}	DOUT and $\overline{INT}$, I_{SOURCE} = 100µA	V_{DD} - 0.3			V
		CLKOUT, I_{SOURCE} = 10µA	V_{DD} - 0.3			
Floating-State Leakage Current	I_L		-10		10	µA
Floating-State Output Capacitance	C_O			9		pF
TRANSDUCER BURN-OUT (Note 16)						
Current	I_{BO}			0.1		µA
Initial Tolerance				±10		%
Drift				±0.05		%/°C
TRANSDUCER EXCITATION CURRENTS						
Current	I_{EXC}			200		uA
Initial Tolerance					15	%
Drift				100		ppm/°C
Match		OUT1 to OUT2			±1	%
Drift Match				5		ppm/°C
Compliance Voltage Range			V_{AGND}		V+ - 1.0	V
POWER REQUIREMENTS						
V+ Voltage	V+	For specified performance	2.7		3.6	V
V_{DD} Voltage	V_{DD}		2.7		3.6	V
Power-Supply Rejection V+ (Note 17)	PSR			(Note 18)		dB

ELECTRICAL CHARACTERISTICS (continued)

(V+ = +2.7V to +3.6V, V_{DD} = +2.7V to +3.6V, V_{REFIN+} = +1.25V, REFIN- = AGND, f_{CLKIN} = 2.4576MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
ANALOG POWER-SUPPLY CURRENT (Measured with digital inputs at either DGND or V_{DD}, external CLKIN, burn-out and transducer excitation currents disabled, X2CLK = 0, CLK = 0 for 1.024MHz, CLK = 1 for 2.4576MHz.)								
V+ Standby Current (Note 19)		PD bit = 1, external clock stopped				1	10	µA
V+ Current	I_{V+}	Normal mode, MF1 = 0, MF0 = 0	1.024MHz	Buffers off		175	210	µA
				Buffers on		370	420	
			2.4576MHz	Buffers off		250	300	
				Buffers on		610	700	
		2X mode, MF1 = 0, MF0 = 1	1.024MHz	Buffers off		245		
				Buffers on		610		
			2.4576MHz	Buffers off		0.42	0.55	mA
				Buffers on		1.2	1.5	
		4X mode, MF1 = 1, MF0 = 0	1.024MHz	Buffers off		0.42		
				Buffers on		1.2		
			2.4576MHz	Buffers off		1.8	2.2	
				Buffers on		4.8	6	
		8X mode, MF1 = 1, MF0 = 1	1.024MHz	Buffers off		1.8		
				Buffers on		4.8		
			2.4576MHz	Buffers off		1.8	2.2	
				Buffers on		4.8	6	
DIGITAL POWER-SUPPLY CURRENT (Measured with digital inputs at either DGND or V_{DD}, external CLKIN, burn-out and transducer excitation currents disabled, X2CLK = 0, CLK = 0 for 1.024MHz, CLK = 1 for 2.4576MHz.)								
V_{DD} Standby Current (Note 19)		PD bit = 1, external clock stopped				1	10	µA
Digital Supply Current	I_{DD}	Normal mode, MF1 = 0, MF0 = 0	1.024MHz			70	200	µA
			2.4576MHz			150	300	
		2X mode, MF1 = 0, MF0 = 1	1.024MHz			0.08		mA
			2.4576MHz			0.17	0.35	
		4X mode, MF1 = 1, MF0 = 0	1.024MHz			0.11		
			2.4576MHz			0.22	0.40	
		8X mode, MF1 = 1, MF0 = 1	1.024MHz			0.15		
			2.4576MHz			0.32	0.50	

+3V, 18-Bit, Low-Power, Multichannel, Oversampling (Sigma-Delta) ADC

ELECTRICAL CHARACTERISTICS (continued)

(V+ = +2.7V to +3.6V, V_{DD} = +2.7V to +3.6V, V_{REFIN+} = +1.25V, REFIN- = AGND, f_{CLKIN} = 2.4576MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
POWER DISSIPATION (V+ = V_{DD} = +3.3V, digital inputs = 0 or V_{DD}, external CLKIN, burn-out and transducer excitation currents disabled, X2CLK = 0, CLK = 0 for 1.024MHz, CLK = 1 for 2.4576MHz.)								
Power Dissipation	PD	Normal mode, MF1 = 0, MF0 = 0	1.024MHz	Buffers off		0.81	1.36	mW
				Buffers on		1.45	2.05	
			2.4576MHz	Buffers off		1.32	1.98	
				Buffers on		2.51	3.30	
		2X mode, MF1 = 0, MF0 = 1	1.024MHz	Buffers off		1.08		
				Buffers on		2.28		
			2.4576MHz	Buffers off		1.95	2.97	
				Buffers on		4.53	6.11	
		4X mode, MF1 = 1, MF0 = 0	1.024MHz	Buffers off		1.75		
				Buffers on		4.32		
			2.4576MHz	Buffers off		6.67	8.58	
				Buffers on		16.6	21.2	
		8X mode, MF1 = 1, MF0 = 1	1.024MHz	Buffers off		6.44		
				Buffers on		16.4		
			2.4576MHz	Buffers off		7.0	8.91	
				Buffers on		16.9	21.45	
Standby Power Dissipation		(Note 19)				7	70	µW

Note 1: Contact factory for INL limits applicable with FS1 = 0 and MF1, MF0 = 1, 2, or 3.

Note 2: Nominal gain is 0.98. This ensures a full-scale input voltage may be applied to the part under all conditions without causing saturation of the digital output data.

Note 3: Positive Full-Scale Error includes zero-scale errors (unipolar offset error or bipolar zero error) and applies to both unipolar and bipolar input ranges. This error does not include the nominal gain of 0.98.

Note 4: Full-Scale Drift includes zero-scale drift (unipolar offset drift or bipolar zero drift) and applies to both unipolar and bipolar input ranges.

Note 5: Gain Error does not include zero-scale errors. It is calculated as (full-scale error - unipolar offset error) for unipolar ranges and as (full-scale error - bipolar zero error) for bipolar ranges. This error does not include the nominal gain of 0.98.

Note 6: Gain-Error Drift does not include unipolar offset drift or bipolar zero drift. It is effectively the drift of the part if zero-scale error is removed.

Note 7: Use of the offset DAC does not imply that any input may be taken below AGND.

Note 8: Additional noise added by the offset DAC is dependent on the filter cutoff, gain, and DAC setting. No noise is added for a DAC code of 0000.

Note 9: Guaranteed by design or characterization; not production tested.

Note 10: The absolute input voltage must be within the input voltage range specification.

Note 11: All AIN and REFIN pins have identical input structures. Leakage is production tested only for the AIN3, AIN4, AIN5, CALGAIN, and CALOFF inputs.

Note 12: The dynamic load presented by the MAX1403 analog inputs for each gain setting is discussed in detail in the *Switching Network* section. Values are provided for the maximum allowable external series resistance.

Note 13: The input voltage range for the analog inputs is with respect to the voltage on the negative input of its respective differential or pseudo-differential pair. Table 5 shows which inputs form differential pairs.

Note 14: V_{REF} = V_{REFIN+} - V_{REFIN-}.

Note 15: These specifications apply to CLKOUT only when driving a single CMOS load.

Note 16: The burn-out currents require a 500mV overhead between the analog input voltage and both V+ and AGND to operate correctly.

Note 17: Measured at DC in the selected passband. PSR at 50Hz will exceed 120dB with filter notches of 25Hz or 50Hz and FAST bit = 0. PSR at 60Hz will exceed 120dB with filter notches of 20Hz or 60Hz and FAST bit = 0.

Note 18: PSR depends on gain. For a gain of +1V/V, PSR is 70dB typical. For a gain of +2V/V, PSR is 75dB typical. For a gain of +4V/V, PSR is 80dB typical. For gains of +8V/V to +128V/V, PSR is 85dB typical.

Note 19: Standby power-dissipation and current specifications are valid only with CLKIN driven by an external clock and with the external clock stopped. If the clock continues to run in standby mode, the power dissipation will be considerably higher. When used with a resonator or crystal between CLKIN and CLKOUT, the actual power dissipation and I_{DD} in standby mode will depend on the resonator or crystal type.

TIMING CHARACTERISTICS

($V+$ = +2.7V to +3.6V, V_{DD} = +2.7V to +3.6V, AGND = DGND, f_{CLKIN} = 2.4576MHz, input logic 0 = 0V, logic 1 = V_{DD}, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Notes 20, 21, 22)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Master Clock Frequency	f_{CLKIN}	Crystal oscillator or clock externally supplied for specified performance (Notes 23, 24)	X2CLK = 0	0.4		2.5	MHz
			X2CLK = 1	0.8		5.0	
Master Clock Input Low Time	$f_{CLKIN\ LO}$	t_{CLKIN} = 1 / f_{CLKIN}, X2CLK = 0		0.4 • t_{CLKIN}			ns
Master Clock Input High Time	$f_{CLKIN\ HI}$	t_{CLKIN} = 1 / f_{CLKIN}, X2CLK = 0		0.4 • t_{CLKIN}			ns
$\overline{INT}$ High Time	$t_{\overline{INT}}$	X2CLK = 0, N = $2^{(2 \cdot MF1 + MF0)}$		280 / N • t_{CLKIN}			ns
		X2CLK = 1, N = $2^{(2 \cdot MF1 + MF0)}$		560 / N • t_{CLKIN}			
$\overline{RESET}$ Pulse Width Low	t_2			100			ns
SERIAL-INTERFACE READ OPERATION							
$\overline{INT}$ to $\overline{CS}$ Setup Time (Note 9)	t_3			0			ns
SCLK Setup to Falling Edge $\overline{CS}$	t_4			30			ns
$\overline{CS}$ Falling Edge to SCLK Falling Edge Setup Time	t_5			30			ns
SCLK Falling Edge to Data Valid Delay (Notes 25, 26)	t_6			0		100	ns
SCLK High Pulse Width	t_7			100			ns
SCLK Low Pulse Width	t_8			100			ns
$\overline{CS}$ Rising Edge to SCLK Rising Edge Hold Time (Note 22)	t_9			0			ns
Bus Relinquish Time After SCLK Rising Edge (Note 27)	t_{10}			10		100	ns
SCLK Rising Edge to $\overline{INT}$ High (Note 28)	t_{11}					200	ns
SERIAL-INTERFACE WRITE OPERATION							
SCLK Setup to Falling Edge $\overline{CS}$	t_{12}			30			ns

+3V, 18-Bit, Low-Power, Multichannel, Oversampling (Sigma-Delta) ADC

TIMING CHARACTERISTICS (continued)

(V+ = +2.7V to +3.6V, V_{DD} = +2.7V to +3.6V, AGND = DGND, f_{CLKIN} = 2.4576MHz, input logic 0 = 0V, logic 1 = V_{DD}, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Notes 20, 21, 22)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{CS}$ Falling Edge to SCLK Falling Edge Setup Time	t_{13}		30			ns
Data Valid to SCLK Rising Edge Setup Time	t_{14}		30			ns
Data Valid to SCLK Rising Edge Hold Time	t_{15}		0			ns
SCLK High Pulse Width	t_{16}		100			ns
SCLK Low Pulse Width	t_{17}		100			ns
$\overline{CS}$ Rising Edge to SCLK Rising Edge Hold Time	t_{18}		0			ns
AUXILIARY DIGITAL INPUTS (DS0 and DS1)						
DS0/DS1 to SCLK Falling Edge Setup Time (Notes 21, 29)	t_{19}		40			ns
DS0/DS1 to SCLK Falling Edge Hold Time (Notes 21, 29)	t_{20}		0			ns

Note 20: All input signals are specified with t_r = t_f = 5ns (10% to 90% of V_{DD}) and timed from a voltage level of 1.6V.

Note 21: See Figure 4.

Note 22: Timings shown in tables are for the case where SCLK idles high between accesses. The part may also be used with SCLK idling low between accesses, provided $\overline{CS}$ is toggled. In this case SCLK in the timing diagrams should be inverted and the terms “SCLK Falling Edge” and “SCLK Rising Edge” exchanged in the specification tables. If $\overline{CS}$ is permanently tied low, the part should only be operated with SCLK idling high between accesses.

Note 23: CLKIN duty cycle range is 45% to 55%. CLKIN must be supplied whenever the MAX1403 is not in standby mode. If no clock is present, the device can draw higher current than specified.

Note 24: The MAX1403 is production tested with f_{CLKIN} at 2.5MHz (1MHz for some I_{DD} tests).

Note 25: Measured with the load circuit of Figure 1 and defined as the time required for the output to cross the V_{OL} or V_{OH} limits.

Note 26: For read operations, SCLK active edge is falling edge of SCLK.

Note 27: Derived from the time taken by the data output to change 0.5V when loaded with the circuit of Figure 1. The number is then extrapolated back to remove effects of charging or discharging the 50pF capacitor. This ensures that the times quoted in the timing characteristics are true bus-relinquish times and are independent of external bus loading capacitances.

Note 28: $\overline{INT}$ returns high after the first read after an output update. The same data can be read again while $\overline{INT}$ is high, but be careful not to allow subsequent reads to occur close to the next output update.

Note 29: Auxiliary inputs DS0 and DS1 are latched on the first falling edge of SCLK during a data-read cycle.

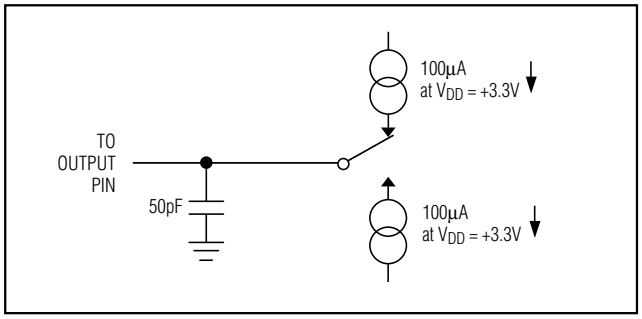


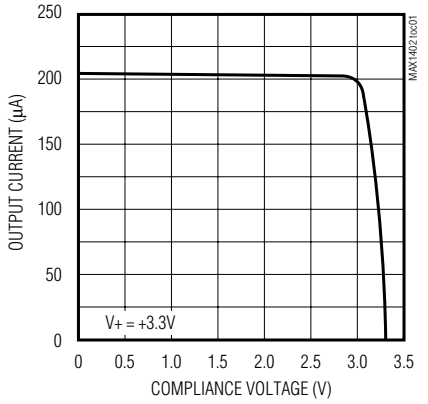
Figure 1. Load Circuit for Bus-Relinquish Time and V_{OL} and V_{OH} Levels

+3V, 18-Bit, Low-Power, Multichannel, Oversampling (Sigma-Delta) ADC

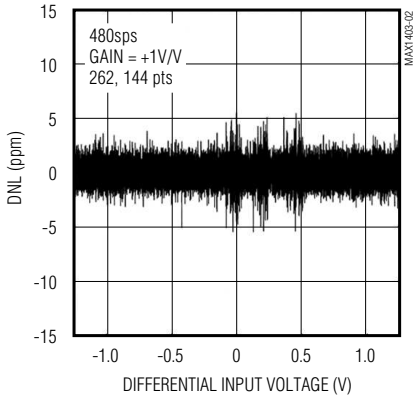
Typical Operating Characteristics

(V+ = +3V, V_{DD} = +3V, V_{REFIN+} = +1.25V, REFIN- = AGND, f_{CLKIN} = 2.4576MHz, transducer excitation currents disabled, T_A = +25°C, unless otherwise noted.)

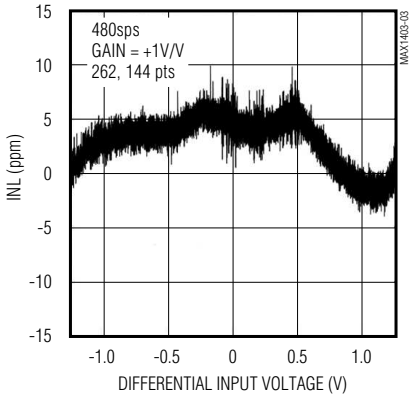
OUT1 AND OUT2 COMPLIANCE



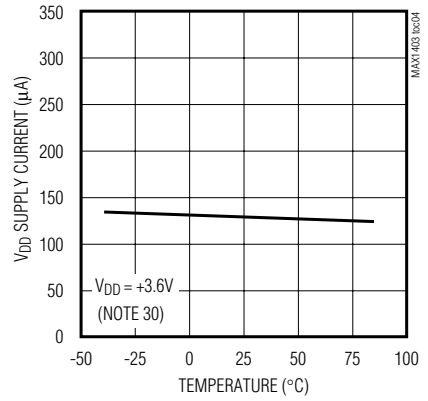
DIFFERENTIAL NONLINEARITY



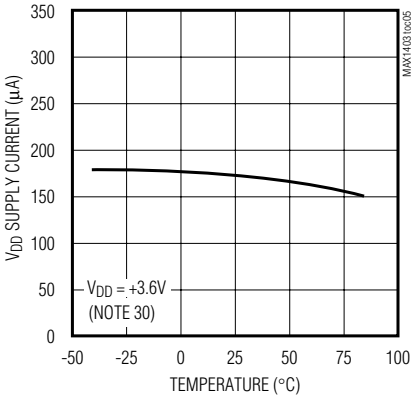
INTEGRAL NONLINEARITY



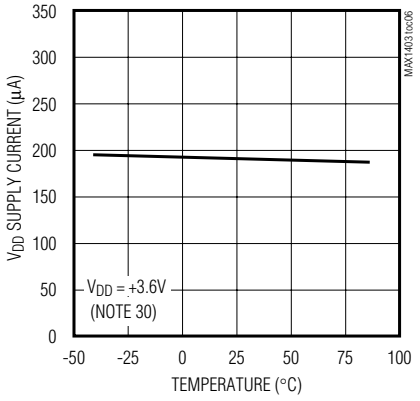
V_{DD} SUPPLY CURRENT vs. TEMPERATURE (20sps OUTPUT DATA RATE UNBUFFERED)



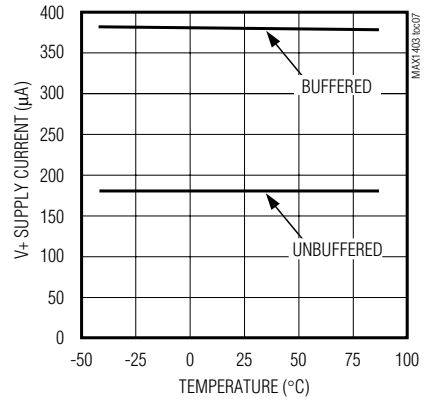
V_{DD} SUPPLY CURRENT vs. TEMPERATURE (60sps OUTPUT DATA RATE UNBUFFERED)



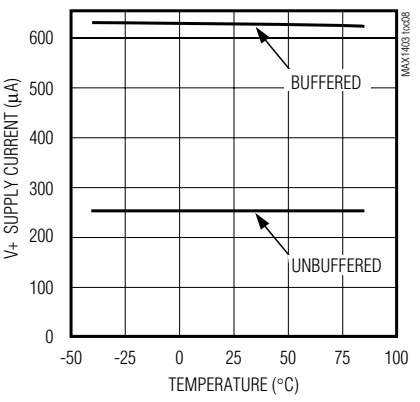
V_{DD} SUPPLY CURRENT vs. TEMPERATURE (120sps OUTPUT DATA RATE UNBUFFERED)



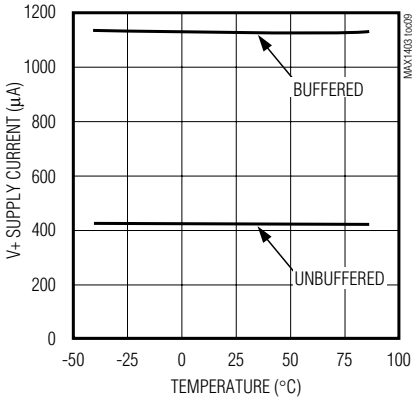
V+ SUPPLY CURRENT vs. TEMPERATURE (20sps OUTPUT DATA RATE)



V+ SUPPLY CURRENT vs. TEMPERATURE (60sps OUTPUT DATA RATE)



V+ SUPPLY CURRENT vs. TEMPERATURE (120sps OUTPUT DATA RATE)

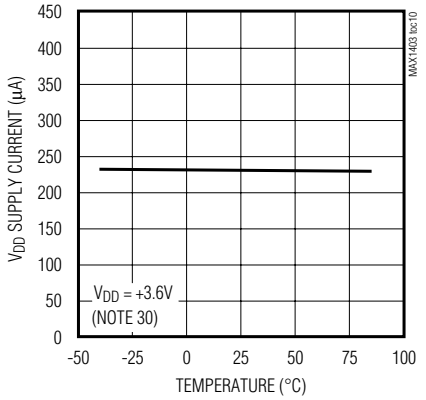


+3V, 18-Bit, Low-Power, Multichannel, Oversampling (Sigma-Delta) ADC

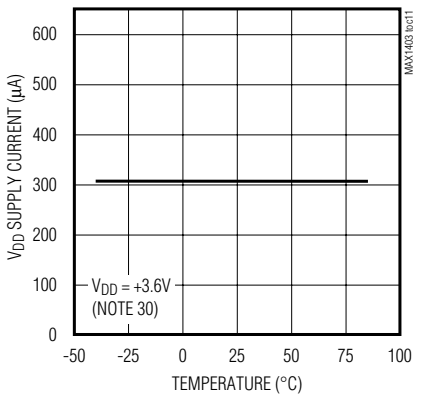
Typical Operating Characteristics (continued)

(V+ = +3V, V_{DD} = +3V, V_{REFIN+} = +1.25V, REFIN- = AGND, f_{CLKIN} = 2.4576MHz, transducer excitation currents disabled, T_A = +25°C, unless otherwise noted.)

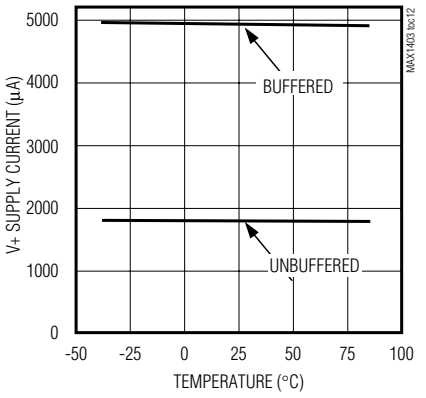
V_{DD} SUPPLY CURRENT vs. TEMPERATURE (240sps OUTPUT DATA RATE UNBUFFERED)



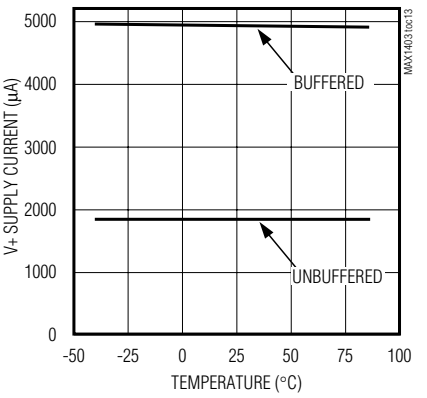
V_{DD} SUPPLY CURRENT vs. TEMPERATURE (480sps OUTPUT DATA RATE UNBUFFERED)



V+ SUPPLY CURRENT vs. TEMPERATURE (240sps OUTPUT DATA RATE)



V+ SUPPLY CURRENT vs. TEMPERATURE (480sps OUTPUT DATA RATE)



Note 30: Minimize capacitive loading at CLKOUT for lowest V_{DD} supply current. *Typical Operating Characteristics* show V_{DD} supply current with CLKOUT loaded by 120pF.

Pin Description

PIN	NAME	FUNCTION
1	CLKIN	Clock Input. A crystal can be connected across CLKIN and CLKOUT. Alternatively, drive CLKIN with a CMOS-compatible clock at a nominal frequency of 2.4576MHz or 1.024MHz, and leave CLKOUT unconnected. Frequencies of 4.9152MHz and 2.048MHz may be used if the X2CLK control bit is set to 1.
2	CLKOUT	Clock Output. When deriving the master clock from a crystal, connect the crystal between CLKIN and CLKOUT. In this mode, the on-chip clock signal is not available at CLKOUT. Leave CLKOUT unconnected when CLKIN is driven with an external clock.
3	$\overline{CS}$	Chip-Select Input. This active-low logic input is used to enable the digital interface. With $\overline{CS}$ hard-wired low, the MAX1403 operates in its 3-wire interface mode with SCLK, DIN, and DOUT used to interface to the device. $\overline{CS}$ is used either to select the device in systems with more than one device on the serial bus, or as a frame-synchronization signal for the MAX1403, when a continuous SCLK is used.
4	$\overline{RESET}$	Active-Low Reset Input. Drive low to reset the control logic, interface logic, digital filter, and analog modulator to power-on status. $\overline{RESET}$ must be high and CLKIN must be toggling in order to exit reset.
5	DS1	Digital Input for Auxiliary Data Input Bit 1. The status of this bit is reflected in the output data by bit D4. Used to communicate the status of DS1 via the serial interface.
6	DS0	Digital Input for Auxiliary Data Input Bit 0. The status of this bit is reflected in the output data by bit D3. Used to communicate the status of DS0 via the serial interface.
7	OUT2	Transducer Excitation Current Source 2
8	OUT1	Transducer Excitation Current Source 1
9	AGND	Analog Ground. Reference point for the analog circuitry. AGND connects to the IC substrate.
10	V+	Analog Positive Supply Voltage (+2.7V to +3.6V).
11	AIN1	Analog Input Channel 1. May be used as a pseudo-differential input with AIN6 as common, or as the positive input of the AIN1/AIN2 differential analog input pair (see *On-Chip Registers* section).
12	AIN2	Analog Input Channel 2. May be used as a pseudo-differential input with AIN6 as common, or as the negative input of the AIN1/AIN2 differential analog input pair (see *On-Chip Registers* section).
13	AIN3	Analog Input Channel 3. May be used as a pseudo-differential input with AIN6 as common, or as the positive input of the AIN3/AIN4 differential analog input pair (see *On-Chip Registers* section).
14	AIN4	Analog Input Channel 4. May be used as a pseudo-differential input with AIN6 as common, or as the negative input of the AIN3/AIN4 differential analog input pair (see *On-Chip Registers* section).
15	AIN5	Analog Input Channel 5. Used as a differential or pseudo-differential input with AIN6 (see *On-Chip Registers* section).
16	AIN6	Analog Input 6. May be used as a common point for AIN1 through AIN5 in pseudo-differential mode, or as the negative input of the AIN5/AIN6 differential analog input pair (see *On-Chip Registers* section).
17	CALGAIN-	Negative Gain Calibration Input. Used for system gain calibration. It forms the negative input of a fully differential input pair with CALGAIN+. Normally these inputs are connected to reference voltages in the system. When system gain calibration is not required and the auto-sequence mode is used, the CALGAIN+/CALGAIN- input pair provides an additional fully differential input channel.
18	CALGAIN+	Positive Gain Calibration Input. Used for system gain calibration. It forms the positive input of a fully differential input pair with CALGAIN-. Normally these inputs are connected to reference voltages in the system. When system gain calibration is not required and the auto-sequence mode is used, the CALGAIN+/CALGAIN- input pair provides an additional fully differential input channel.

+3V, 18-Bit, Low-Power, Multichannel, Oversampling (Sigma-Delta) ADC

Pin Description (continued)

PIN	NAME	FUNCTION
19	REFIN-	Negative Differential Reference Input. Bias REFIN- between V+ and AGND, provided that REFIN+ is more positive than REFIN-.
20	REFIN+	Positive Differential Reference Input. Bias REFIN+ between V+ and AGND, provided that REFIN+ is more positive than REFIN-.
21	CALOFF-	Negative Offset Calibration Input. Used for system offset calibration. It forms the negative input of a fully differential input pair with CALOFF+. Normally these inputs are connected to zero-reference voltages in the system. When system offset calibration is not required and the auto-sequence mode is used, the CALOFF+/CALOFF- input pair provides an additional fully differential input channel.
22	CALOFF+	Positive Offset Calibration Input. Used for system offset calibration. It forms the positive input of a fully differential input pair with CALOFF-. Normally these inputs are connected to zero-reference voltages in the system. When system offset calibration is not required and the auto-sequence mode is used, the CALOFF+/CALOFF- input pair provides an additional fully differential input channel.
23	DGND	Digital Ground. Reference point for digital circuitry.
24	V_{DD}	Digital Supply Voltage (+2.7V to +3.6V)
25	$\overline{INT}$	Interrupt Output. A logic low indicates that a new output word is available from the data register. $\overline{INT}$ returns high upon completion of a full output word read operation. $\overline{INT}$ also returns high for short periods (determined by the filter and clock control bits) if no data read has taken place. A logic high indicates internal activity, and a read operation should not be attempted under this condition. $\overline{INT}$ can also provide a strobe to indicate valid data at DOUT (MDOUT = 1).
26	DOUT	Serial Data Output. DOUT outputs data from the internal shift register containing information from the Communications Register, Global Setup Registers, Transfer Function Registers, or Data Register. DOUT can also provide the digital bit stream directly from the Σ-Δ modulator (MDOUT = 1).
27	DIN	Serial Data Input. Data on DIN is written to the input shift register and later transferred to the Communications Register, Global Setup Registers, Special Function Register, or Transfer Function Registers, depending on the register selection bits in the Communications Register.
28	SCLK	Serial Clock Input. Apply an external serial clock to transfer data to and from the MAX1403. This serial clock can be continuous, with data transmitted in a train of pulses, or intermittently. If $\overline{CS}$ is used to frame the data transfer, then SCLK may idle high or low between conversions and $\overline{CS}$ determines the desired active clock edge (see *Selecting Clock Polarity*). If $\overline{CS}$ is tied permanently low, SCLK must idle high between data transfers.

Detailed Description

Circuit Description

The MAX1403 is a low-power, multichannel, serial-output, sigma-delta ADC designed for applications with a wide dynamic range, such as weigh scales and pressure transducers. The functional block diagram in Figure 2 contains a switching network, a modulator, a PGA, two buffers, an oscillator, an on-chip digital filter, two matched transducer excitation current sources, and a bidirectional serial communications port.

Three fully differential input channels feed into the switching network. Each channel may be independently programmed with a gain between +1V/V and +128V/V. These three differential channels may also be configured to operate as five pseudo-differential input channels. Two additional, fully differential system-calibration channels allow system gain and offset error to be measured. These system-calibration channels can be used as additional differential signal channels when dedicated gain and offset error correction channels are not required.

Two chopper-stabilized buffers are available to isolate the selected inputs from the capacitive loading of the PGA and modulator. Three independent DACs provide compensation for the DC component of the input signal on each of the differential input channels.

The sigma-delta modulator converts the input signal into a digital pulse train whose average duty cycle represents the digitized signal information. The pulse train is then processed by a digital decimation filter, resulting in a conversion accuracy exceeding 16 bits. The digital filter's decimation factor is user-selectable, which allows the conversion result's resolution to be reduced to achieve a higher output data rate. When used with 2.4576MHz or 1.024MHz master clocks, the decimation filter can be programmed to produce zeros in its frequency response at the line frequency and associated harmonics. This ensures excellent line rejection without the need for further postfiltering. In addition, the modulator sampling frequency can be optimized for either lowest power dissipation or highest output data rate.

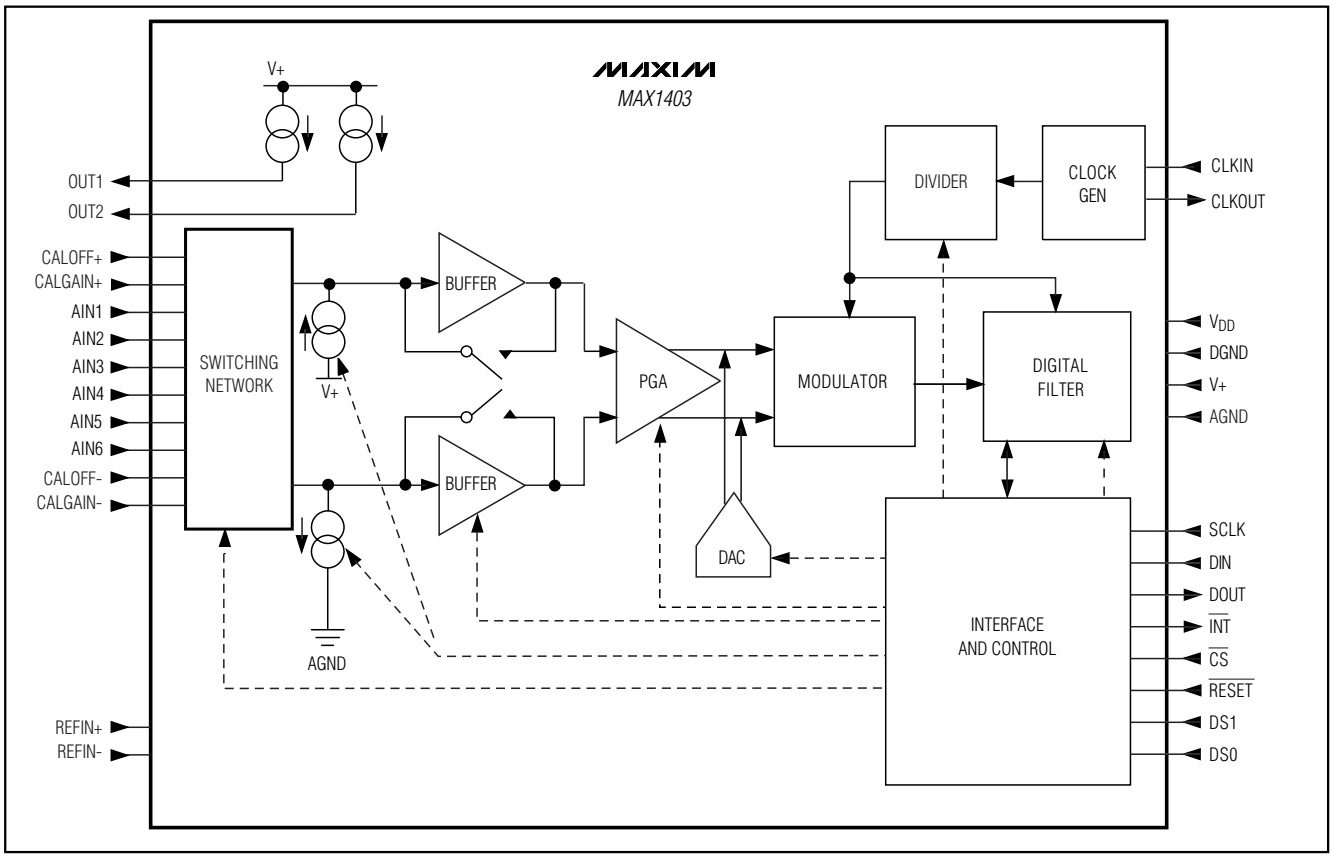


Figure 2. Functional Diagram

+3V, 18-Bit, Low-Power, Multichannel, Oversampling (Sigma-Delta) ADC

The MAX1403 can be configured to sequentially scan all signal inputs and to transmit the results through the serial interface with minimum communications overhead. The output word contains a channel identification tag to indicate the source of each conversion result.

Serial Digital Interface

The serial digital interface provides access to eight on-chip registers (Figure 3). All serial-interface commands begin with a write to the communications register (COMM). On power-up, system reset, or interface reset, the part expects a write to its communications register. The COMM register access begins with a 0 start bit. The COMM register R/$\overline{W}$ bit selects a read or write operation, and the register select bits (RS2, RS1, RS0) select the register to be addressed. Hold DIN high when not writing to COMM or another register (Table 1).

The serial interface consists of five signals: $\overline{CS}$, SCLK, DIN, DOUT, and $\overline{INT}$. Clock pulses on SCLK shift bits into DIN and out of DOUT. $\overline{INT}$ provides an indication that data is available. $\overline{CS}$ is a device chip-select input as well as a clock polarity select input (Figure 4).

Using $\overline{CS}$ allows the SCLK, DIN, and DOUT signals to be shared among several SPI-compatible devices. When short on I/O pins, connect $\overline{CS}$ low and operate the serial digital interface in CPOL = 1, CPHA = 1 mode using SCLK, DIN, and DOUT. This 3-wire interface mode is ideal for opto-isolated applications. Furthermore, a microcontroller (such as a PIC16C54 or 80C51) can use a single bidirectional I/O pin for both sending to DIN and receiving from DOUT (see *Applications Information*), because the MAX1403 drives DOUT only during a read cycle.

Additionally, connecting the $\overline{INT}$ signal to a hardware interrupt allows faster throughput and reliable, collision-free data flow.

Table 1. Control-Register Addressing

RS2	RS1	RS0	TARGET REGISTER
0	0	0	Communications Register
0	0	1	Global Setup Register 1
0	1	0	Global Setup Register 2
0	1	1	Special Function Register
1	0	0	Transfer Function Register 1
1	0	1	Transfer Function Register 2
1	1	0	Transfer Function Register 3
1	1	1	Data Register

The MAX1403 features a mode where the raw modulator data output is accessible. In this mode, the DOUT and $\overline{INT}$ functions are reassigned (see the *Modulator Data Output* section).

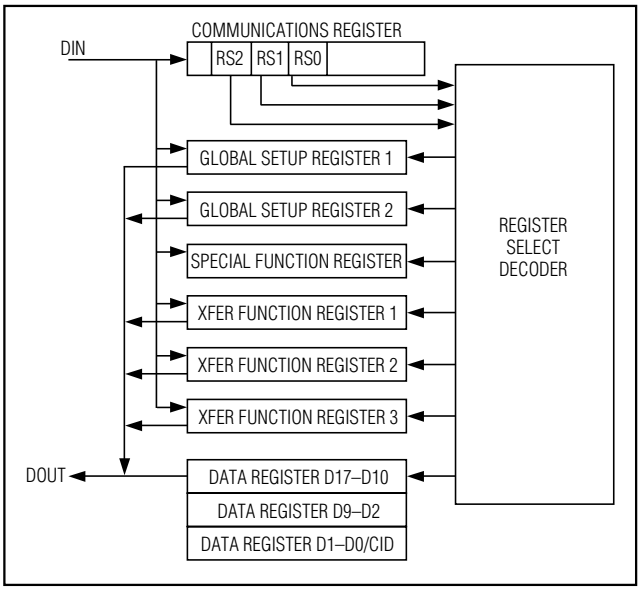


Figure 3. Register Summary

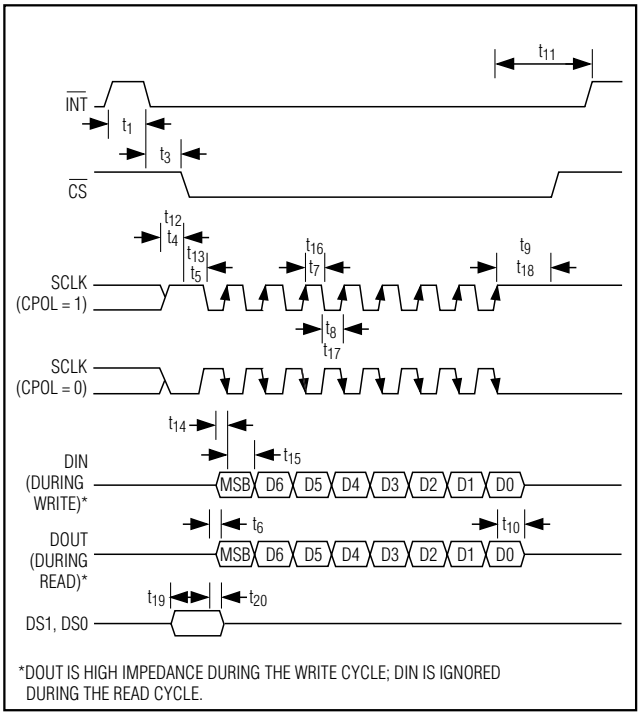


Figure 4. Serial-Interface Timing

Selecting Clock Polarity

The serial interface can be operated with the clock idling either high or low. This is compatible with Motorola's SPI interface operated in CPOL = 1, CPHA = 1 mode or CPOL = 0, CPHA = 1 mode. The clock polarity is determined by the state of SCLK at the falling edge of $\overline{CS}$. Ensure that the setup times t_4/t_{12} and t_5/t_{13} are not violated. If $\overline{CS}$ is connected to ground, resulting in no falling edge on $\overline{CS}$, SCLK must idle high (CPOL = 1, CPHA = 1).

Data-Ready Signal (DRDY bit true or $\overline{INT}$ = low)

The data-ready signal indicates that new data may be read from the 24-bit data register. After the end of a successful data register read, the data-ready signal becomes false. If a new measurement completes before the data is read, the data-ready signal becomes false. The data-ready signal becomes true again when new data is available in the data register.

The MAX1403 provides two methods of monitoring the data-ready signal. $\overline{INT}$ provides a hardware solution (active low when data is ready to be accessed), while the DRDY bit in the COMM register provides a software solution (active high).

Read data as soon as possible once data-ready becomes true. This becomes increasingly important for faster measurement rates. If the data read is delayed significantly, a collision may result. A collision occurs when a new measurement completes during a data-register read operation. After a collision, information in the data register is invalid. The failed read operation must be completed even though the data is invalid.

Resetting the Interface

Reset the serial interface by clocking in 32 1s. Resetting the interface does not affect the internal registers.

If continuous data output mode is in use, clock in eight 0s followed by 32 1s. More than 32 1s may be clocked in, since a leading 0 is used as the start bit for all operations.

Continuous Data Output Mode

When scanning the input channels (SCAN = 1), the serial interface allows the data register to be read repeatedly without requiring a write to the COMM register. The initial COMM write (01111000) is followed by 24 clocks (DIN = high) to read the 24-bit data register. Once the data register has been read, it can be read again after the next conversion by writing another 24 clocks (DIN = high). Terminate the continuous data output mode by writing to the COMM register with any valid access.

Modulator Data Output (MDOUT = 1)

Single-bit, raw modulator data is available at DOUT for custom filtering when MDOUT = 1. $\overline{INT}$ provides a modulator clock for data synchronization. Data is valid on the falling edge of $\overline{INT}$. Write operations can still be performed; however, read operations are disabled. After MDOUT is returned to 0, valid data is accessed by the normal serial-interface read operation.

On-Chip Registers

Communications Register

0/DRDY: (Default = 0) Data Ready Bit. On a write, this bit must be reset to 0 to signal the start of the Communications Register data word. On a read, a 1 in this location (0/DRDY) signifies that valid data is available in the data register. This bit is reset after the data register is read or, if data is not read, 0/DRDY will go low at the end of the next measurement.

RS2, RS1, RS0: (Default = 0, 0, 0) Register Select Bits. These bits select the register to be accessed (Table 1).

R/$\overline{W}$: (Default = 0) Read/Write Bit. When set high, the selected register is read; when R/$\overline{W}$ = 0, the selected register is written.

RESET: (Default = 0) Software Reset Bit. Setting this bit high causes the part to be reset to its default power-up condition (RESET = 0).

STDBY: (Default = 0) Standby Power-Down Bit. Setting the STDBY bit places the part in "standby" condition, shutting down everything except the serial interface and the CLK oscillator.

FSYNC: (Default = 0) Filter Sync Bit. When FSYNC = 0, conversions are automatically performed at a data rate determined by CLK, FS1, FS0, MF1, and MF0 bits. When FSYNC = 1, the digital filter and analog modulator

Communications Register

First Bit (MSB) **(LSB)**

FUNCTION	DATA RDY	REGISTER SELECT BITS						
Name	0/DRDY	RS2	RS1	RS0	R/$\overline{W}$	RESET	STDBY	FSYNC
Defaults	0	0	0	0	0	0	0	0

+3V, 18-Bit, Low-Power, Multichannel, Oversampling (Sigma-Delta) ADC

are held in reset, inhibiting normal self-timed operation. This bit may be used to convert on command to minimize the settling time to valid output data, or to synchronize operation of a number of MAX1403s. FSYNC does not reset the serial interface or the 0/DRDY flag. To clear the 0/DRDY flag while FSYNC is active, simply read the data register.

Global Setup Register 1

A1, A0: (Default = 0, 0) Channel-Selection Control Bits. These bits (combined with the state of the DIFF, M1, and M0 bits) determine the channel selected for conversion according to Tables 8, 9, and 10. These bits are ignored if the SCAN bit is set.

MF1, MF0: (Default = 0, 0) Modulator Frequency Bits. MF1 and MF0 determine the ratio of CLKIN oscillator frequency to modulator operating frequency. They affect the output data rate, the position of the digital filter notch frequencies, and the power dissipation of the device. Achieve lowest power dissipation with MF1 = 0 and MF0 = 0. Highest power dissipation and fastest output data rate occur with these bits set to 1, 1 (Table 2).

CLK: (Default = 1) CLK Bit. The CLK bit is used in conjunction with X2CLK to tell the MAX1403 the frequency of the CLKIN input signal. If CLK = 0, a CLKIN input frequency of 1.024MHz (2.048MHz for X2CLK = 1) is expected. If CLK = 1, a CLKIN input frequency of 2.4576MHz (4.9152MHz for X2CLK = 1) is expected. This bit affects the decimation factor in the digital filter and thus the output data rate (Table 2).

FS1, FS0: (Default = 0, 1) Filter Selection Bits. These bits (in conjunction with the CLK bit) control the decimation ratio of the digital filter. They determine the output data rate, the position of the digital filter frequency response notches, and the noise present in the output result (Table 2).

FAST: (Default 0) Fast Bit. FAST = 0 causes the digital filter to perform a $SINC^3$ filter function on the modulator data stream. The output data rate will be determined by the values in the CLK, FS1, FS0, MF1, and MF0 bits (Table 2). The settling time for $SINC^3$ function is $3 \cdot [1 / (\text{output data rate})]$. In $SINC^3$ mode, the MAX1403 automatically holds the DRDY signal false (after any significant configuration change) until settled data is available. FAST = 1 causes the digital filter to perform a $SINC^1$ filter function on the modulator data stream. The signal-to-noise ratio achieved with this filter function is less than that of the $SINC^3$ filter; however, $SINC^1$ settles in a single output sample period rather than a minimum of three output sample periods for $SINC^3$. When switching from $SINC^1$ to $SINC^3$ mode, the DRDY flag will be deasserted and reasserted after the filter has fully settled. This mode change requires a minimum of three samples.

Global Setup Register 2

SCAN: (Default = 0) Scan Bit. Setting this bit to a 1 causes sequential scanning of the input channels as determined by DIFF, M1, and M0 (see *Scanning (Scan-Mode)* section). When SCAN = 0, the MAX1403 repeatedly measures the unique channel selected by A1, A0, DIFF, M1, and M0 (Table 4).

M1, M0: (Default 0, 0) Mode Control Bits. These bits control access to the calibration channels CALOFF and CALGAIN. When SCAN = 0, setting M1 = 0 and M0 = 1 selects the CALOFF input, and M1 = 1 and M0 = 0 selects the CALGAIN input (Table 3). When SCAN = 1 and M1 ≠ M0, the scanning sequence includes both CALOFF and CALGAIN inputs (Table 4). When SCAN is set to 1 and the device is scanning the available input channels, selection of either calibration mode (01 or 10) will cause the scanning sequence to be extended to include a conversion on both the CALGAIN+/CALGAIN- input pair and the CALOFF+/CALOFF-input pair. The

Global Setup Register 1

First Bit (MSB) **(LSB)**

FUNCTION	CHANNEL SELECTION		MODULATOR FREQUENCY			FILTER SELECTION		
Name	A1	A0	MF1	MF0	CLK	FS1	FS0	FAST
Defaults	0	0	0	0	1	0	1	0

Global Setup Register 2

First Bit (MSB) **(LSB)**

FUNCTION		MODE CONTROL						
Name	SCAN	M1	M0	BUFF	DIFF	BOUT	IOUT	X2CLK
Defaults	0	0	0	0	0	0	0	0

exact sequence depends on the state of the DIFF bit (Table 4). When scanning, the calibration channels use the PGA gain, format, and DAC settings defined by the contents of Transfer Function Register 3.

BUFF: (Default = 0) The BUFF bit controls operation of the input buffer amplifiers. When this bit is 0, the internal buffers are bypassed and powered down. When this bit is set high, the buffers drive the input sampling capacitors and minimize the dynamic input load.

DIFF: (Default = 0) Differential/Pseudo-Differential Bit. When DIFF = 0, the part is in pseudo-differential mode, and AIN1–AIN5 are measured respective to AIN6, the analog common. When DIFF = 1, the part is in differential mode with the analog inputs defined as AIN1/AIN2, AIN3/AIN4, and AIN5/AIN6. The available input channels for each mode are tabulated in Table 5. Note that DIFF also affects the scanning sequence when the part is placed in SCAN mode (Table 4).

BOUT: (Default = 0) Burn-Out Current Bit. Setting BOUT = 1 connects 100nA current sources to the selected analog input channel. This mode is used to check that a transducer has not burned out or opened circuit. The burn-out current source must be turned off (BOUT = 0) before measurement to ensure best linearity.

IOUT: (Default = 0) The IOUT bit controls the Transducer Excitation Currents. A 0 in this bit disables OUT1 and OUT2, effectively making these pins high-impedance. A 1 in this location activates both IOUT1 and IOUT2, causing each pin to source 200µA.

X2CLK: (Default = 0) Times-Two Clock Bit. Setting this bit to 1 selects a divide-by-2 prescaler in the clock signal path. This allows use of a higher frequency crystal or clock source and improves immunity to asymmetric clock sources.

Table 2. Data Output Rate vs. CLK, Filter Select, and Modulator Frequency Bits

CLKIN FREQUENCY, f_{CLKIN} (MHz)		CLK	MF1	MF0	AVAILABLE OUTPUT DATA RATES (sps)			
X2CLK = 0	X2CLK = 1				FS1, FS0* (0, 0)	FS1, FS0* (0, 1)	FS1, FS0 (1, 0)	FS1, FS0 (1, 1)
1.024	2.048	0	0	0	20	25	100	200
1.024	2.048	0	0	1	40	50	200	400
1.024	2.048	0	1	0	80	100	400	800
1.024	2.048	0	1	1	160	200	800	1600
2.4576	4.9152	**1**	**0**	**0**	50	**60**	300	600
2.4576	4.9152	1	0	1	100	120	600	1200
2.4576	4.9152	1	1	0	200	240	1200	2400
2.4576	4.9152	1	1	1	400	480	2400	4800

** Data rates offering noise-free 16-bit resolution.*

Note: *When FAST = 0, $f_{-3dB} = 0.262 \cdot$ Data Rate. When FAST = 1, $f_{-3dB} = 0.443 \cdot$ Data Rate.*

Note: *Default condition is in bold print.*

Table 3. Special Modes Controlled by M1, M0 (SCAN = 0)

M1	M0	DESCRIPTION
0	0	**Normal Mode:** The device operates normally.
0	1	**Calibrate Offset:** In this mode, the MAX1403 converts the voltage applied across CALOFF+ and CALOFF-. The PGA gain, DAC, and format settings of the selected channel (defined by DIFF, A1, A0) are used.
1	0	**Calibrate Gain:** In this mode, the MAX1403 converts the voltage applied across CALGAIN+ and CALGAIN-. The PGA gain, DAC, and format settings of the selected channel (defined by DIFF, A1, A0) are used.
1	1	**Reserved:** Do not use.

+3V, 18-Bit, Low-Power, Multichannel, Oversampling (Sigma-Delta) ADC

Table 4. SCAN Mode Scanning Sequences (SCAN = 1)

DIFF	M1	M0	SEQUENCE
0	0	0	AIN1–AIN6, AIN2–AIN6, AIN3–AIN6, AIN4–AIN6, AIN5–AIN6
0	0	1	AIN1–AIN6, AIN2–AIN6, AIN3–AIN6, AIN4–AIN6, AIN5–AIN6, CALOFF, CALGAIN
0	1	0	AIN1–AIN6, AIN2–AIN6, AIN3–AIN6, AIN4–AIN6, AIN5–AIN6, CALOFF, CALGAIN
1	0	0	AIN1–AIN2, AIN3–AIN4, AIN5–AIN6
1	0	1	AIN1–AIN2, AIN3–AIN4, AIN5–AIN6, CALOFF, CALGAIN
1	1	0	AIN1–AIN2, AIN3–AIN4, AIN5–AIN6, CALOFF, CALGAIN

Note: *All other combinations reserved.*

Table 5. Available Input Channels (SCAN = 0)

DIFF	M1	M0	AVAILABLE CHANNELS
0	0	0	AIN1–AIN6, AIN2–AIN6, AIN3–AIN6, AIN4–AIN6
0	0	1	CALOFF
0	1	0	CALGAIN
1	0	0	AIN1–AIN2, AIN3–AIN4, AIN5–AIN6
1	0	1	CALOFF
1	1	0	CALGAIN

Special Function Register (Write-Only)

MDOUT: (Default = 0) Modulator Out Bit. MDOUT = 0 enables data readout on the DOUT pin, the normal condition for the serial interface. MDOUT = 1 changes the function of the DOUT and $\overline{INT}$ pins, providing raw, single-bit modulator output instead of the normal serial-data interface output. This allows custom filtering directly on the modulator output, without going through the on-chip digital filter. The $\overline{INT}$ pin provides a clock to indicate when the modulator data at DOUT should be sampled (falling edge of $\overline{INT}$). Note that in this mode, the on-chip digital filter continues to operate normally. When MDOUT is returned to 0, valid data may be accessed through the normal serial-interface read operation.

FULLPD: (Default = 0) Complete Power-Down Bit. FULLPD = 1 forces the part into a complete power-down condition, which includes the clock oscillator. The serial interface continues to operate. The part requires a hardware reset to recover correctly from this condition.

Note: Changing the reserved bits in the special-function register from the default status of all 0s will select one of the reserved modes and the part will not operate as expected. This register is a write-only register. However, in the event that this register is mistakenly read, clock 24 bits of data out of the part to restore it to the normal interface-idle state.

Transfer-Function Registers

The three transfer-function registers control the method used to map the input voltage to the output codes. All of the registers have the same format. The mapping of control registers to associated channels depends on the mode of operation and is affected by the state of M1, M0, DIFF, and SCAN (Tables 8, 9, and 10).

Special Function Register (Write-Only)

First Bit (MSB) **(LSB)**

FUNCTION	RESERVED BITS			RESERVED BITS				
Name	0	0	MDOUT	0	0	0	0	FULLPD
Defaults	0	0	0	0	0	0	0	0

Transfer-Function Register

First Bit (MSB) **(LSB)**

FUNCTION	PGA GAIN CONTROL				OFFSET CORRECTION			
Name	G2	G1	G0	U/$\overline{B}$	D3	D2	D1	D0
Defaults	0	0	0	0	0	0	0	0

Analog Inputs AIN1 to AIN6

Inputs AIN1 and AIN2 map to transfer-function register 1, regardless of scanning mode (SCAN = 1) or single-ended vs. differential (DIFF) modes. Likewise, AIN3 and AIN4 inputs always map to transfer-function register 2. Finally, AIN5 always maps to transfer-function register 3 (input AIN6 is analog common).

CALGAIN and CALOFF

When not in scan mode (SCAN = 0), A1 and A0 select which transfer function applies to CALGAIN and CALOFF. In scan mode (SCAN = 1), CALGAIN and CALOFF are always mapped to transfer-function register 3. Note that when scanning while M1 ≠ M0, the scan sequence includes both CALGAIN and CALOFF channels (Table 4). CALOFF always precedes CALGAIN, even though both channels share the same channel ID tag (Table 11).

Note that changing the status of any **active** channel control bits will cause $\overline{INT}$ to immediately transition high and the modulator/filter to be reset. $\overline{INT}$ will reassert after the appropriate digital-filter settling time. The control settings of the inactive channels may be changed freely without affecting the status of $\overline{INT}$ or causing the filter/modulator to be reset.

PGA Gain

Bits G2–G0 control the PGA gain according to Table 6.

Unipolar/Bipolar Mode

The U/$\overline{B}$ bit places the channel in either bipolar or unipolar mode. A 0 selects bipolar mode, and a 1 selects unipolar mode. This bit does not affect the analog-signal conditioning. The modulator always accepts bipolar inputs and produces a bitstream with 50% ones-density when the selected inputs are at the same potential. This bit controls the processing of the digital-filter output, such that the available output bits are mapped to the correct output range. Note that U/$\overline{B}$ must be set before a conversion is performed; it will not affect any data already held in the output register.

Selecting bipolar mode does not imply that any input may be taken below AGND. It simply changes the gain and offset of the part. All inputs must remain within their specified operating voltage range.

Offset-Correction DACs

Bits D3–D0 control the offset-correction DAC. The DAC range depends on the PGA gain setting and is expressed as a percentage of the available full-scale input range (Table 7).

D3 is a sign bit, and D2–D0 represent the DAC magnitude. Note that when a DAC value of 0000 is programmed (the default), the DAC is disconnected from the modulator inputs. This prevents the DAC from degrading noise performance when offset correction is not required.

Transfer-Function Register Mapping

Tables 8, 9, and 10 show the channel-control register mapping in the various operating modes.

Table 6. PGA Gain Codes

G2	G1	G0	PGA GAIN
0	0	0	x1
0	0	1	x2
0	1	0	x4
0	1	1	x8
1	0	0	x16
1	0	1	x32
1	1	0	x64
1	1	1	x128

Table 7. DAC Code vs. DAC Value

D3	D2	D1	D0	BIPOLAR DAC VALUE (% of FSR)	UNIPOLAR DAC VALUE (% of FSR)
0	0	0	0	DAC not connected	
0	0	0	1	+8.3	+16.7
0	0	1	0	+16.7	+33.3
0	0	1	1	+25	+50
0	1	0	0	+33.3	+66.7
0	1	0	1	+41.6	+83.3
0	1	1	0	+50	+100
0	1	1	1	+58.3	+116.7
1	0	0	0	DAC not connected	
1	0	0	1	-8.3	-16.7
1	0	1	0	-16.7	-33.3
1	0	1	1	-25	-50
1	1	0	0	-33.3	-66.7
1	1	0	1	-41.6	-83.3
1	1	1	0	-50	-100
1	1	1	1	-58.3	-116.7

+3V, 18-Bit, Low-Power, Multichannel, Oversampling (Sigma-Delta) ADC

Table 8. Transfer-Function Register Mapping—Normal Mode (M1 = 0, M0 = 0)

SCAN	DIFF	A1	A0	CHANNEL	TRANSFER-FUNCTION REGISTER
0	0	0	0	AIN1–AIN6	1
0	0	0	1	AIN2–AIN6	1
0	0	1	0	AIN3–AIN6	2
0	0	1	1	AIN4–AIN6	2
0	1	0	0	AIN1–AIN2	1
0	1	0	1	AIN3–AIN4	2
0	1	1	0	AIN5–AIN6	3
0	1	1	1	Do Not Use	
1	0	X	X	AIN1–AIN6	1
1	0	X	X	AIN2–AIN6	1
1	0	X	X	AIN3–AIN6	2
1	0	X	X	AIN4–AIN6	2
1	0	X	X	AIN5–AIN6	3
1	1	X	X	AIN1–AIN2	1
1	1	X	X	AIN3–AIN4	2
1	1	X	X	AIN5–AIN6	3
1	1	1	1	Do Not Use	

X = Don't care

Table 9. Transfer-Function Register Mapping—Offset-Calibration Mode (M1 = 0, M0 = 1)

SCAN	DIFF	A1	A0	CHANNEL	TRANSFER-FUNCTION REGISTER
0	0	0	0	CALOFF+–CALOFF-	1
0	0	0	1	CALOFF+–CALOFF-	1
0	0	1	0	CALOFF+–CALOFF-	2
0	0	1	1	CALOFF+–CALOFF-	2
0	1	0	0	CALOFF+–CALOFF-	1
0	1	0	1	CALOFF+–CALOFF-	2
0	1	1	0	CALOFF+–CALOFF-	3
0	1	1	1	Do Not Use	
1	0	X	X	AIN1–AIN6	1
1	0	X	X	AIN2–AIN6	1
1	0	X	X	AIN3–AIN6	2
1	0	X	X	AIN4–AIN6	2
1	0	X	X	AIN5–AIN6	3
1	0	X	X	CALOFF+–CALOFF-	3
1	0	X	X	CALGAIN+–CALGAIN-	3
1	1	X	X	AIN1–AIN2	1
1	1	X	X	AIN3–AIN4	2
1	1	X	X	AIN5–AIN6	3
1	1	X	X	CALOFF+–CALOFF-	3
1	1	X	X	CALGAIN+–CALGAIN-	3
1	1	1	1	Do Not Use	

Table 10. Transfer-Function Register Mapping—Gain-Calibration Mode (M1 = 1, M0 = 0)

SCAN	DIFF	A1	A0	CHANNEL	TRANSFER-FUNCTION REGISTER
0	0	0	0	CALGAIN+–CALGAIN-	1
0	0	0	1	CALGAIN+–CALGAIN-	1
0	0	1	0	CALGAIN+–CALGAIN-	2
0	0	1	1	CALGAIN+–CALGAIN-	2
0	1	0	0	CALGAIN+–CALGAIN-	1
0	1	0	1	CALGAIN+–CALGAIN-	2
0	1	1	0	CALGAIN+–CALGAIN-	3
0	1	1	1	Do Not Use	
1	0	X	X	AIN1–AIN6	1
1	0	X	X	AIN2–AIN6	1
1	0	X	X	AIN3–AIN6	2
1	0	X	X	AIN4–AIN6	2
1	0	X	X	AIN5–AIN6	3
1	0	X	X	CALOFF+–CALOFF-	3
1	0	X	X	CALGAIN+–CALGAIN-	3
1	1	X	X	AIN1–AIN2	1
1	1	X	X	AIN3–AIN4	2
1	1	X	X	AIN5–AIN6	3
1	1	X	X	CALOFF+–CALOFF-	3
1	1	X	X	CALGAIN+–CALGAIN-	3
1	1	1	1	Do Not Use	

X = Don't care

Data Register (Read-Only)

The data register is a 24-bit, read-only register. Any attempt to write data to this location will have no effect. If a write operation is attempted, 8 bits of data must be clocked into the part before it will return to its normal idle mode, expecting a write to the communications register.

Data is output MSB first, followed by one reserved 0 bit, two auxiliary data bits, and a 3-bit channel ID tag indicating the channel from which the data originated.

D17–D0: The conversion result. D17 is the MSB. The result is in offset binary format. 00 0000 0000 0000 0000 represents the minimum value, and 11 1111 1111 1111 1111 represents the maximum value. Inputs exceeding the available input range are limited to the corresponding minimum or maximum output values.

0: This reserved bit will always be 0.

Data Register (Read-Only) Bits

First Bit (Data MSB)

DATA BITS							
D17	D16	D15	D14	D13	D12	D11	D10

DATA BITS							
D9	D8	D7	D6	D5	D4	D3	D2

(Data LSB) **(LSB)**

DATA BITS		RESERVED	AUXILIARY DATA		CHANNEL ID TAG		
D1	D0	'0'	DS1	DS0	CID2	CID1	CID0

+3V, 18-Bit, Low-Power, Multichannel, Oversampling (Sigma-Delta) ADC

Table 11. Channel ID Tag Codes

CID2	CID1	CID0	CHANNEL
0	0	0	AIN1–AIN6
0	0	1	AIN2–AIN6
0	1	0	AIN3–AIN6
0	1	1	AIN4–AIN6
1	0	0	AIN1–AIN2
1	0	1	AIN3–AIN4
1	1	0	AIN5–AIN6
1	1	1	Calibration

DS1, DS0: The status of the auxiliary data input pins. These are latched on the first falling edge of the SCLK signal for the current data register read access.

CID2–0: Channel ID tag (Table 11).

Switching Network

A switching network provides selection between three fully differential input channels or five pseudo-differential channels, using AIN6 as a shared common. The switching network provides two additional fully differential input channels intended for system calibration, which may be used as extra fully differential signal channels. Table 12 shows the channel configurations available for both operating modes.

Scanning (SCAN-Mode)

To sample and convert the available input channels sequentially, set the SCAN control bit in the global setup register. The sequence is determined by DIFF (fully differential or pseudo-differential) and by the mode control bits M1 and M0 (Tables 8, 9, 10). With SCAN set, the device automatically sequences through each available channel, transmitting a single conversion result before proceeding to the next channel. The MAX1403 automatically allows sufficient time for each conversion to fully settle, to ensure optimum resolution before asserting the data-ready signal and moving to the next available channel. The scan rate is, therefore, dependent on the clock bit (CLK), the filter control bits (FS1, FS0), and the modulator frequency selection bits (MF1, MF0).

Burn-Out Currents

The input circuitry also provides two “burn-out” currents. These small currents may be used to test the integrity of the selected transducer. They can be selectively enabled or disabled by the BOUT bit in the global setup register.

Table 12. Input Channel Configuration in Fully Differential and Pseudo-Differential Mode (SCAN = 0)

M1	M0	DIFF	A1	A0	MODE	HIGH INPUT	LOW INPUT
0	0	0	0	0	Pseudo-Differential	AIN1	AIN6
0	0	0	0	1		AIN2	AIN6
0	0	0	1	0		AIN3	AIN6
0	0	0	1	1		AIN4	AIN6
0	0	X	X	X		AIN5*	AIN6*
0	1	X	X	X		CALOFF+**	CALOFF-**
1	0	X	X	X		CALGAIN+**	CALGAIN-**
0	0	1	0	0	Fully Differential	AIN1	AIN2
0	0	1	0	1		AIN3	AIN4
0	0	1	1	0		AIN5	AIN6
0	1	X	X	X		CALOFF+**	CALOFF-**
1	0	X	X	X		CALGAIN+**	CALGAIN-**

X = Don’t care

** This combination is available only in pseudo-differential mode when using the internal scanning logic.*

*** These combinations are only available in the calibration modes.*

Transducer Excitation Currents

The MAX1403 provides two matched 200µA transducer excitation currents at OUT1 and OUT2. These currents have low absolute temperature coefficients and tight TC matching. These characteristics enable accurate compensation of errors due to IR drops in long transducer cable runs. They may be enabled or disabled using a single register control bit (IOUT).

Dynamic Input Impedance at the Channel Selection Network

When used in unbuffered mode (BUFF = 0), the analog inputs present a dynamic load to the driving circuitry. The size of the sampling capacitor and the input sampling frequency (Figure 5) determine the dynamic load seen by the driving circuitry. The MAX1403 samples at a constant rate for all gain settings. This provides a maximum time for the input to settle at a given data rate. The dynamic load presented by the inputs varies with the gain setting. For gains of +2V/V, +4V/V, and +8V/V, the input sampling capacitor increases with the chosen gain. Gains of +16V/V, +32V/V, +64V/V, and +128V/V present the same input load as the x8 gain setting.

When designing with the MAX1403, as with any other switched-capacitor ADC input, consider the advantages and disadvantages of series input resistance. A series resistor reduces the transient-current impulse to the external driving amplifier. This improves the amplifier phase margin and reduces the possibility of ringing. The resistor spreads the transient-load current from the sampler over time due to the RC time constant of the circuit. However, an improperly chosen series resistance can hinder performance in fast 16-bit converters. The settling time of the RC network can limit the speed at which the converter can operate properly, or reduce the settling accuracy of the sampler. In practice, this means ensuring that the RC time constant—resulting from the product of the driving source impedance and the capacitance presented by both the MAX1403's input and any external capacitances—is sufficiently small to allow settling to the desired accuracy. Tables 13a–13d summarize the maximum allowable series resistance vs. external capacitance for each MAX1403 gain setting in order to ensure 16-bit performance in unbuffered mode.

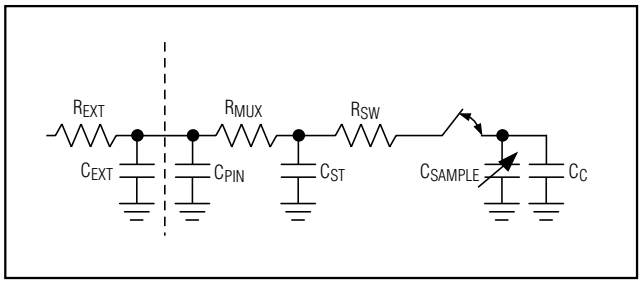


Figure 5. Analog Input, Unbuffered Mode (BUFF = 0)

Table 13a. R_{EXT}, C_{EXT} Values for Less than 16-Bit Gain Error in Unbuffered (BUFF = 0) Mode—1x Modulator Sampling Frequency (MF1, MF0 = 00); X2CLK = 0; CLKIN = 2.4576MHz

PGA GAIN	EXTERNAL RESISTANCE, R_{EXT} (kΩ)					
	C_{EXT} = 0pF	C_{EXT} = 50pF	C_{EXT} = 100pF	C_{EXT} = 500pF	C_{EXT} = 1000pF	C_{EXT} = 5000pF
1	34	15	9.8	2.9	1.6	0.43
2	34	15	9.8	2.9	1.6	0.43
4	25	13	8.7	2.7	1.5	0.40
8, 16, 32, 64, 128	17	10	7.3	2.4	1.4	0.37

Table 13b. R_{EXT}, C_{EXT} Values for Less than 16-Bit Gain Error in Unbuffered (BUFF = 0) Mode—2x Modulator Sampling Frequency (MF1, MF0 = 01); X2CLK = 0; CLKIN = 2.4576MHz

PGA GAIN	EXTERNAL RESISTANCE, R_{EXT} (kΩ)					
	C_{EXT} = 0pF	C_{EXT} = 50pF	C_{EXT} = 100pF	C_{EXT} = 500pF	C_{EXT} = 1000pF	C_{EXT} = 5000pF
1	17	7.5	4.9	1.4	0.81	0.22
2	17	7.5	4.9	1.4	0.81	0.22
4	13	6.4	4.4	1.3	0.76	0.20
8, 16, 32, 64, 128	8.4	5.0	3.7	1.2	0.70	0.18

+3V, 18-Bit, Low-Power, Multichannel, Oversampling (Sigma-Delta) ADC

Table 13c. R_{EXT}, C_{EXT} Values for Less than 16-Bit Gain Error in Unbuffered (BUFF = 0) Mode—4x Modulator Sampling Frequency (MF1, MF0 = 10); X2CLK = 0; CLKIN = 2.4576MHz

PGA GAIN	EXTERNAL RESISTANCE, R_{EXT} (kΩ)					
	C_{EXT} = 0pF	C_{EXT} = 50pF	C_{EXT} = 100pF	C_{EXT} = 500pF	C_{EXT} = 1000pF	C_{EXT} = 5000pF
1	8.3	3.7	2.4	0.72	0.40	0.11
2	8.3	3.7	2.4	0.72	0.40	0.11
4	6.2	3.2	2.2	0.67	0.38	0.10
8, 16, 32, 64, 128	4.1	2.5	1.8	0.60	0.35	0.09

Table 13d. R_{EXT}, C_{EXT} Values for Less than 16-Bit Gain Error in Unbuffered (BUFF = 0) Mode—8x Modulator Sampling Frequency (MF1, MF0 = 11); X2CLK = 0; CLKIN = 2.4576MHz

PGA GAIN	EXTERNAL RESISTANCE, R_{EXT} (kΩ)					
	C_{EXT} = 0pF	C_{EXT} = 50pF	C_{EXT} = 100pF	C_{EXT} = 500pF	C_{EXT} = 1000pF	C_{EXT} = 5000pF
1	4.1	1.8	1.2	0.35	0.20	0.05
2	4.1	1.8	1.2	0.35	0.20	0.05
4	3.0	1.5	1.1	0.32	0.18	0.05
8, 16, 32, 64, 128	2.0	1.2	0.88	0.29	0.17	0.04

Input Buffers

The MAX1403 provides a pair of input buffers to isolate the inputs from the capacitive load presented by the PGA/modulator (Figure 6). The buffers are chopper stabilized to reduce the effect of their DC offsets and low-frequency noise. Since the buffers can represent more than 50% of the total analog power dissipation, they may be shut down in applications where minimum power dissipation is required and the capacitive input load is not a concern. Disable the buffers in applications where the inputs must operate close to AGND or V+.

When used in buffered mode, the buffers isolate the inputs from the sampling capacitors. The sampling-related gain error is dramatically reduced in this mode. A small dynamic load remains from the chopper stabilization. The multiplexer exhibits a small input leakage current of up to 10nA. With high source resistances, this leakage current may result in a DC offset.

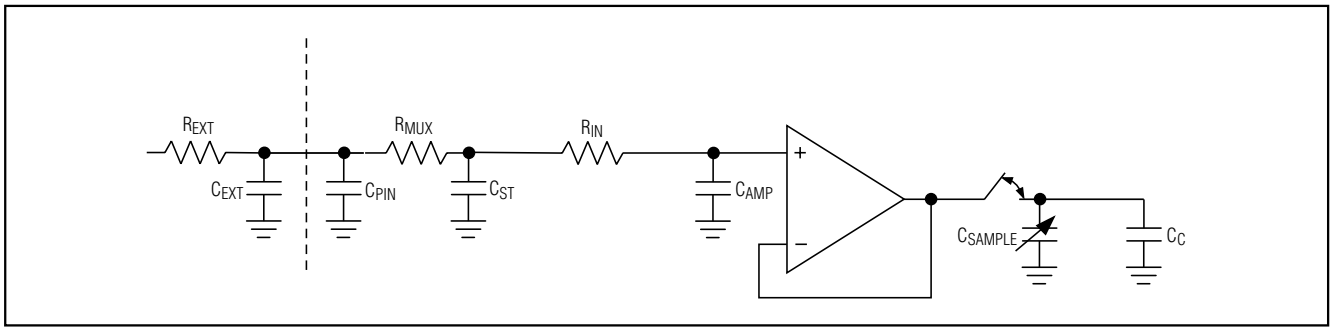


Figure 6. Analog Input, Buffered Mode (BUFF = 1)

Table 14. R_{EXT}, C_{EXT} Values for Less than 16-Bit Gain Error in Buffered (BUFF = 1) Mode—All Modulator Sampling Frequencies (MF1, MF0 = XX); X2CLK = 0; CLKIN = 2.4576MHz

PGA GAIN	EXTERNAL RESISTANCE, R_{EXT} (kΩ)					
	C_{EXT} = 0pF	C_{EXT} = 50pF	C_{EXT} = 100pF	C_{EXT} = 500pF	C_{EXT} = 1000pF	C_{EXT} = 5000pF
1	10	10	10	10	10	10
2	10	10	10	10	10	10
4	10	10	10	10	10	10
8	10	10	10	10	10	10
16	10	10	10	10	10	10
32	10	10	10	10	10	10
64	10	10	10	10	10	10
128	10	10	10	10	10	10

Reference Input

The MAX1403 is optimized for ratiometric measurements and includes a fully differential reference input. Apply the reference voltage across REFIN+ and REFIN-, ensuring that REFIN+ is more positive than REFIN-. REFIN+ and REFIN- must be between AGND and V+. The MAX1403 is specified with a +1.25V reference.

Modulator

The MAX1403 performs analog-to-digital conversion using a single-bit, second-order, switched-capacitor modulator. A single comparator within the modulator quantizes the input signal at a much higher sample rate than the bandwidth of the signal to be converted. The quantizer then presents a stream of 1s and 0s to the digital filter for processing, to remove the frequency-shaped quantization noise.

The MAX1403 modulator provides 2nd-order frequency shaping of the quantization noise resulting from the single bit quantizer. The modulator is fully differential for maximum signal-to-noise ratio and minimum susceptibility to power-supply noise.

The modulator operates at one of a total of eight different sampling rates (f_M) determined by the master clock frequency (f_{CLKIN}), the X2CLK bit, the CLK bit, and the modulator frequency control bits MF1 and MF0. Power dissipation is optimized for each of these modes by controlling the bias level of the modulator. Table 15 shows the input and reference sample rates.

PGA

A programmable gain amplifier (PGA) with a user-selectable gain of x1, x2, x4, x8, x16, x32, x64, or x128 (Table 6) precedes the modulator. Figure 8 shows the default bipolar transfer function with the following illustrated codes: 1) PGA = 0, DAC = 0; 2) PGA = 3, DAC = 0; or 3) PGA = 3, DAC = 3.

Output Noise

Tables 16a and 16b show the rms noise for typical output frequencies (notches) and -3dB frequencies for the MAX1403 with f_{CLKIN} = 2.4576MHz. The numbers given are for the bipolar input ranges with V_{REF} = +1.25V, with no buffer (BUFF = 0), and with the buffer inserted (BUFF = 1). These numbers are typical and are generated at a differential analog input voltage of 0. Figure 7 shows graphs of Effective Resolution vs. Gain and Notch Frequency. The effective resolution values were derived from the following equation:

$$\text{Effective Resolution} = (SNR_{dB} - 1.76dB) / 6.02$$

The maximum possible signal divided by the noise of the device, SNR_{dB}, is defined as the ratio of the input full-scale voltage (i.e., $2 \cdot V_{REFIN}$ / GAIN) to the output rms noise. Note that it is not calculated using peak-to-peak output noise numbers. Peak-to-peak noise numbers can be up to 6.6 times the rms numbers, while effective resolution numbers based on peak-to-peak noise can be 2.5 bits below the effective resolution based on rms noise, as quoted in the tables.

The noise shown in Tables 16a and 16b is composed of device noise and quantization noise. The device noise is relatively low, but becomes the limiting noise source for high gain settings. The quantization noise is dependent on the notch frequency and becomes the dominant noise source as the notch frequency is increased.