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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

19-2229; Rev 0; 10/01

MAXIM

Low-Power, 16-Bit Multichannel DAS with Internal Reference,10-Bit DACs, and RTC

General Description

The MAX1407/MAX1408/MAX1409/MAX1414 are low-power, general-purpose, multichannel data-acquisition systems (DAS). These devices are optimized for low-power applications. All the devices operate from a single +2.7V to +3.6V power supply and consume a maximum of 1.15mA in Run mode and only 2.5µA in Sleep mode.

The MAX1407/MAX1408/MAX1414 feature a differential 8:1 input multiplexer to the ADC, a programmable three-state digital output, an output to shutdown an external power supply, and a data ready output from the ADC. The MAX1408 has eight auxiliary analog inputs, while the MAX1407/MAX1414 include four auxiliary analog inputs and two 10-bit force/sense DACs. The MAX1414 features a 50mV trip threshold for the signal-detect comparator while the others have a 0mV trip threshold. The MAX1409 is a 20-pin version of the DAS family with a differential 4:1 input multiplexer to the ADC, one auxiliary analog input, and one 10-bit force/sense DAC.

The MAX1407/MAX1408/MAX1414 are available in space-saving 28-pin SSOP packages, while the MAX1409 is available in a 20-pin SSOP package.

Applications

Medical Instruments

Industrial Control Systems

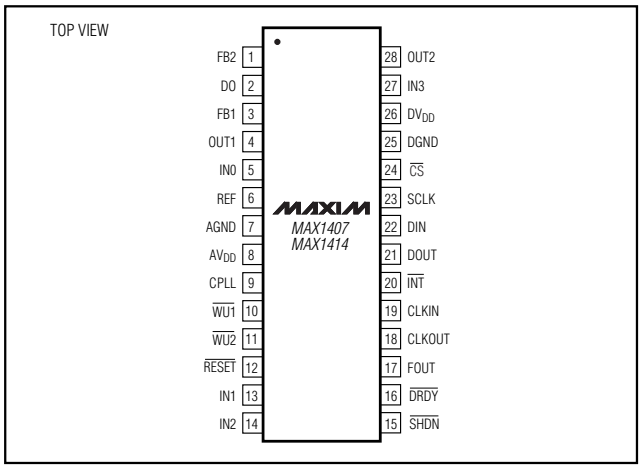
Portable Equipment

Data-Acquisition System

Automatic Testing

Robotics

Pin Configurations



Features

- **+2.7V to +3.6V Supply Voltage Range in Standby, Idle, and Run Mode (Down to 1.8V in Sleep Mode)**
- **1.15mA Run Mode Supply Current**
- **2.5µA Sleep Mode Supply Current (Wake-Up, RTC, and Voltage Monitor Active)**
- **Multichannel 16-Bit Sigma-Delta ADC**
  - **±1.5 LSB (typ) Integral Nonlinearity**
  - **30Hz or 60Hz Continuous Conversion Rate**
  - **Buffered or Unbuffered Mode**
  - **Gain of +1/3, +1, or +2V/V**
  - **Unipolar or Bipolar Mode**
  - **On-Chip Offset Calibration**
- **10-Bit Force/Sense DACs**
- **Buffered 1.25V, 18ppm/°C (typ) Bandgap Reference Output**
- **SPI™/QSPI™ or MICROWIRE™-Compatible Serial Interface**
- **System Support Functions**
  - **RTC (Valid til 9999) and Alarm**
  - **High-Frequency PLL Clock Output (2.4576MHz)**
  - **+1.8V and +2.7V RESET and Power-Supply Voltage Monitors**
  - **Signal Detect Comparator**
  - **Interrupt Generator (INT and DRDY)**
  - **Three-State Digital Output**
  - **Wake-Up Circuitry**
- **28-Pin SSOP (MAX1407/MAX1408/MAX1414), 20-Pin SSOP (MAX1409)**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1407CAI	0°C to +70°C	28 SSOP
MAX1408CAI	0°C to +70°C	28 SSOP
MAX1409CAP	0°C to +70°C	20 SSOP
MAX1414CAI	0°C to +70°C	28 SSOP

Pin Configurations continued at end of data sheet.
Typical Operating Circuit appears at end of data sheet.

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MICROWIRE is a trademark of National Semiconductor Corp.

Low-Power, 16-Bit Multichannel DAS with Internal Reference,10-Bit DACs, and RTC

ABSOLUTE MAXIMUM RATINGS

AV_{DD} to AGND .....-0.3V to +6V
AV_{DD} to DV_{DD} ..... -0.3V to +0.3V
Analog Inputs to AGND .....-0.3V to +(AV_{DD} + 0.3V)
Digital Inputs to DGND.....-0.3V to +6V
Maximum Current Input Into Any Pin 50mA
Continuous Power Dissipation (T_A = +70°C)
20-Pin SSOP (derate 8.0mW/°C above +70°C) 640mW
28-Pin SSOP (derate 9.52mW/°C above +70°C) 762mW
DV_{DD} to DGND.....-0.3V to +6V
AGND to DGND.....-0.3V to +0.3V
Analog Outputs to AGND .....-0.3V to +(AV_{DD} + 0.3V)
Digital Outputs to DGND .....-0.3V to +(AV_{DD} + 0.3V)
REF to AGND.....-0.3V to +(AV_{DD} + 0.3V)
Operating Temperature Range:
MAX14__CA_ .....0°C to +70°C
MAX14__EA_ .....-40°C to +85°C
Lead Temperature (soldering, 10s) .....+300 °C
Storage Temperature Range .....-65°C to +150°C
Junction Temperature.....+150°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(DV_{DD} = AV_{DD} = +2.7V to 3.6V, 4.7µF at REF, internal V_{REF}, 18nF between CPLL and AV_{DD}, 32.768kHz crystal across CLKIN and CLKOUT, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ADC ACCURACY							
Resolution (No Missing Codes)	RES			16			Bits
Integral Nonlinearity	INL	Unbuffered mode, Unipolar mode, gain = 1, V_{NEG} = 0.2V, fully differential input (Note 7)			1.5	3.5	LSB
		Unbuffered mode, Unipolar mode, gain = 2, V_{NEG} = 0.625V, pseudo-differential input			1.75		
		Unbuffered mode, Bipolar mode, gain = 1, V_{NEG} = 0.625V, fully differential input			1.70		
		Buffered mode, Bipolar mode, gain = 2, V_{NEG} = 0.625V, fully differential input			2.50		
Output RMS Noise (Note 1)		Unipolar	Gain = 2		±5		μV_{RMS}
			Gain = 1		±10		
			Gain = 1/3		±30		
		Bipolar Mode	Gain = 2		±8		
			Gain = 1		±16.5		
			Gain = 1/3		±48.5		
Offset Error		On-chip calibration removes this error				±1	% of FSR
Offset Drift					±0.5		µV/°C
Gain Error		Excludes offset and reference errors				±1	% of FSR
Gain Drift		Excludes offset and reference errors			±1		ppm/°C

ELECTRICAL CHARACTERISTICS (continued)

(DV_{DD} = AV_{DD} = +2.7V to 3.6V, 4.7µF at REF, internal V_{REF}, 18nF between CPLL and AV_{DD}, 32.768kHz crystal across CLKIN and CLKOUT, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
PGA Gain		See *PGA Gain* section			1/3		V/V
					1		
					2		
Power-Supply Rejection Ratio		Gain = 1, unipolar and buffered mode			70		dB
Output Update Rate		Continuous conversion	RATE bit = 0		30		Hz
			RATE bit = 1		60		
Turn-On Time		Excluding reference			50		µs
SIGNAL DETECT COMPARATOR							
Differential Input-Detection Threshold Voltage		MAX1407/MAX1408/MAX1409		-10	0	10	mV
		MAX1414		44	50	56	
Common-Mode Input Voltage				0		0.8	V
Turn-On Time					10		µs
ANALOG INPUTS							
Differential Input Voltage Range		Unipolar mode	ADC gain = 1	0		V_{REF}	V
			ADC gain = 2	0		$V_{REF/2}$	
			ADC gain = 1/3	0		AV_{DD}	
		Bipolar mode	ADC gain = 1	$-V_{REF}$		V_{REF}	
			ADC gain = 2	$-V_{REF/2}$		$V_{REF/2}$	
			ADC gain = 1/3	$-AV_{DD}$		AV_{DD}	
Absolute Input Voltage Range		Unbuffered		-0.05		AV_{DD}	V
		Buffered		0.05		1.40	
Common-Mode Input Voltage Range		Unbuffered		AGND		AV_{DD}	V
		Buffered		0.05		1.40	
Common-Mode Rejection Ratio		Gain = 1, unipolar and buffered mode			90		dB
Input Sampling Rate		FOUT = 2.4576MHz	30Hz data rate		15.360		kHz
			60Hz data rate		30.720		
Input Current		Buffered mode			±0.5		nA
Input Capacitance					15		pF
FORCE-SENSE DAC (all measurements made with FB1(2) shorted to OUT1(2), unless otherwise noted). (MAX1407/MAX1409/MAX1414 only)							
Resolution				10			Bits
Differential Nonlinearity		Guaranteed monotonic (Note 2)				±1.0	LSB
Integral Nonlinearity		(Note 2)				±1.0	LSB
Offset Error		(Note 3)				±20	mV
Offset Drift					±5		µV/°C
Gain Error		Excludes offset and reference drift				3.6	mV
Gain Drift		Excludes offset and reference drift			10		ppm/°C
Line Regulation					190		µV/V
Current into FB1(2)					±0.5		nA

Low-Power, 16-Bit Multichannel DAS with Internal Reference,10-Bit DACs, and RTC

ELECTRICAL CHARACTERISTICS (continued)

(DV_{DD} = AV_{DD} = +2.7V to 3.6V, 4.7µF at REF, internal V_{REF}, 18nF between CPLL and AV_{DD}, 32.768kHz crystal across CLKIN and CLKOUT, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Slew Rate		010hex to 3FFhex and 3FFhex to 010hex code swing, R_L = 12kΩ, C_L = 200pF			18.0		V/ms
Output Settling Time		To ±1/2 LSB (at 10-bit accuracy) of full-scale with code transition from 010hex to 3FFhex, R_L = 12kΩ, C_L = 200pF			65		µs
Turn-On Time					100		µs
OUT1, OUT2 Output Range		No Load (Note 4)		0.05		AV_{DD} - 0.2	V
EXTERNAL REFERENCE (internal reference powered down)							
Input Voltage Range					1.25 ±0.10		V
Input Resistance					540		kΩ
Input Current					2.3		µA
INTERNAL REFERENCE (AV_{DD} = 3V, unless otherwise noted)							
Output Voltage		T_A = +25°C		1.225	1.25	1.275	V
Output Voltage Temperature Coefficient					18		ppm/°C
Output Short-Circuit Current					3.4		mA
Line Regulation	$\Delta V_{REF}/\Delta V_{DD}$	2.7<AV_{DD}<3.6V			80		µV/V
Load Regulation		I_{SOURCE} = 0µA to 500µA, T_A = +25°C				1	µV/µA
		I_{SINK} = 0µA to 50µA, T_A = +25°C				2	
Noise Voltage	e_{OUT}	0.1Hz to 10Hz			40		µVp-p
		10Hz to 10kHz			400		
Power-Supply Rejection Ratio		±100mV, f = 120Hz			70		dB
Turn-On Time					3		ms
µP RESET							
Supply Voltage Range		For valid $\overline{RESET}$		1		3.6	V
$\overline{RESET}$ Trip Threshold Low	V_{TH}	AV_{DD} falling	Bit VM = 1	1.800	1.865	1.930	V
			Bit VM = 0	2.70	2.75	2.80	
Low AV_{DD} Trip Threshold		For Normal, Idle, and Standby modes, AV_{DD} falling		2.70	2.75	2.80	V
$\overline{RESET}$ Output Low Voltage (Open-Drain Output)		I_{SINK} = 1mA, AV_{DD} = 1.8V				0.4	V

ELECTRICAL CHARACTERISTICS (continued)

(DV_{DD} = AV_{DD} = +2.7V to 3.6V, 4.7µF at REF, internal V_{REF}, 18nF between CPLL and AV_{DD}, 32.768kHz crystal across CLKIN and CLKOUT, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{RESET}$ Output Leakage		$AV_{DD} \geq V_{TH}$, $\overline{RESET}$ deasserted		0.002	0.1	µA
Turn-On Time				2		ms
CRYSTAL OSCILLATOR						
Crystal Frequency		AV_{DD} = +3V		32.768		kHz
Crystal Load Capacitance				6		pF
Oscillator Stability		AV_{DD} = +1.8V to +3.6V, excluding crystal		0		ppm/V
Oscillator Startup Time				1.5		s
PLL						
FOUT Frequency		AV_{DD} = +3V		2.4576		MHz
Absolute Clock Jitter		Cycle-to-cycle		10		ns
Frequency Tolerance/Stability		Overtemperature excluding crystal, T_A = T_{MIN} to T_{MAX}		0		ppm/°C
		Oversupply voltage, +2.7V< AV_{DD}< +3.6V		0		ppm/mV
FOUT Rise/Fall Time		20% to 80% waveform, C_L = 30pF		15	30	ns
Duty Cycle			40	50	60	%
DIGITAL INPUTS (DIN, SCLK, $\overline{CS}$, $\overline{WU1}$, $\overline{WU2}$)						
Input High Voltage		DV_{DD} = +1.8V to +3.6V	0.7 x DV_{DD}			V
Input Low Voltage		DV_{DD} = +1.8V to +3.6V			0.3 x DV_{DD}	V
Input Hysteresis		DV_{DD} = +3V		200		mV
DIN, SCLK, $\overline{CS}$, Input Current		V_{IN} = 0 or V_{IN} = DV_{DD}		±0.01	±10	µA
$\overline{WU1}$, $\overline{WU2}$ Input Current		V_{IN} = AV_{DD}		0.01	10	µA
$\overline{WU1}$, $\overline{WU2}$ Pullup Current		V_{IN} = 0		10		µA
Input Capacitance				10		pF
DIGITAL OUTPUTS (DOUT, FOUT, $\overline{INT}$, $\overline{DRDY}$, $\overline{SHDN}$, D0)						
DOUT, FOUT, $\overline{DRDY}$, $\overline{INT}$ Output Low Voltage	V_{OL}	I_{SINK} = 1mA, DV_{DD} = +1.8V to +3.6V			0.4	V
DOUT, FOUT, $\overline{DRDY}$, $\overline{INT}$, $\overline{SHDN}$ Output High Voltage	V_{OH}	I_{SOURCE} = 0.2mA, DV_{DD} = +1.8V to +3.6V	0.8 x DV_{DD}			V
DOUT Three-State Leakage				±0.01	±10	µA
DOUT Three-State Capacitance				15		pF
$\overline{SHDN}$ Output Low Voltage (MAX1407/MAX1408/MAX1414 only)		I_{SINK} = 1mA, DV_{DD} = +1.8V to +3.6V			0.4	V
		I_{SINK} = 50µA, DV_{DD} = +1.8V to +3.6V			0.04 x DV_{DD}	

ELECTRICAL CHARACTERISTICS (continued)

(DV_{DD} = AV_{DD} = +2.7V to 3.6V, 4.7µF at REF, internal V_{REF}, 18nF between CPLL and AV_{DD}, 32.768kHz crystal across CLKIN and CLKOUT, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
D0 Output Low Voltage (MAX1407/MAX1408/MAX1414 only)		I_{SINK} = 200µA, DV_{DD} = +2.7V to +3.6V				0.7	mV
D0 Output High Voltage (MAX1407/MAX1408/MAX1414 only)		I_{SOURCE} = 2mA, DV_{DD} = +2.7V to +3.6V		DV_{DD} - 0.1			V
POWER REQUIREMENTS							
Supply Voltage Range	V_{DD}	Run, Idle, and Standby mode		2.7		3.6	V
		Sleep mode		1.8		3.6	
Supply Current (Note 5)	I_{DD}	Run mode	MAX1407/MAX1414			1.15	mA
			MAX1408			1.03	
			MAX1409			1.09	
		Idle mode	MAX1407/MAX1414			650	µA
			MAX1408			530	
			MAX1409			590	
		Standby mode	MAX1407/MAX1408/ MAX1409/MAX1414			330	
		Sleep mode V_{DD} = 2.7V	MAX1407/MAX1408/ MAX1409/MAX1414		1.7	2.5	

TIMING CHARACTERISTICS

(MAX1407/MAX1408/MAX1409/MAX1414: AV_{DD} = DV_{DD} = 2.7V to 3.6V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TIMING PARAMETERS						
SCLK Operating Frequency	f_{SCLK}				2.1	MHz
SCLK Cycle Time	t_{CYC}		476			ns
SCLK Pulse Width High	t_{CH}		190			ns
SCLK Pulse Width Low	t_{CL}		190			ns
DIN to SCLK Setup	t_{DS}		100			ns
DIN to SCLK Hold	t_{DH}		0			ns
SCLK Fall to Output Data Valid	t_{DO}	C_L = 50pF (see load circuit)			200	ns
$\overline{CS}$ Fall to Output Enable	t_{DV}	C_L = 50pF (see load circuit)			240	ns
$\overline{CS}$ Rise to Output Disable	t_{TR}	C_L = 50pF (see load circuit)			240	ns
$\overline{CS}$ to SCLK Rise Setup	t_{CSS}		100			ns
$\overline{CS}$ to SCLK Rise Hold	t_{CSH}		0			ns

TIMING CHARACTERISTICS (continued)

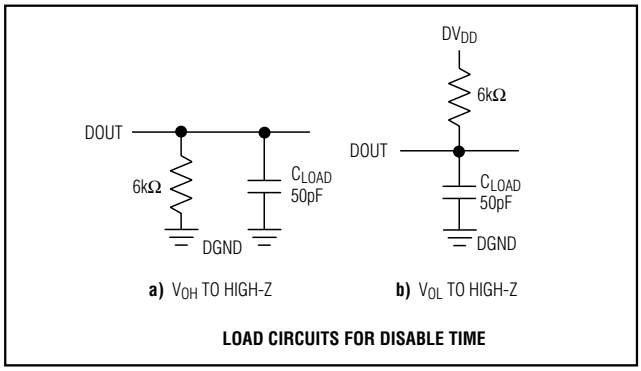
(MAX1407/MAX1408/MAX1409/MAX1414: AV_{DD} = DV_{DD} = 2.7V to 3.6V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

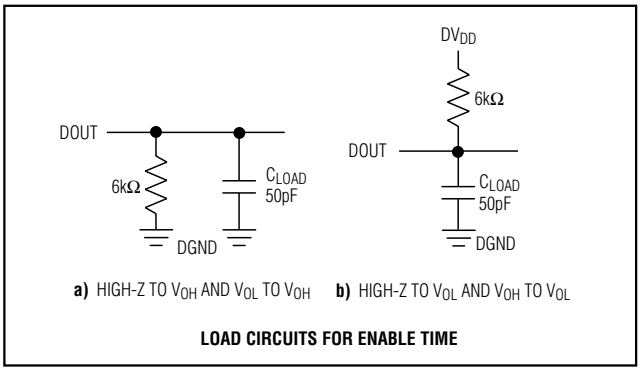
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TYPICAL TIMING PARAMETERS						
OUT1/OUT2 Turn-Off Time		Input impedance > 1MΩ (MAX1407/MAX1409/MAX1414 only)		100		µs
Sleep Voltage Monitor Timeout Period	t_{DSLP}	The delay for the sleep voltage monitor output, $\overline{RESET}$, to go high after AV_{DD} rises above the reset threshold (+1.8V when bit VM = 1 and +2.7V, when bit VM = 0); this is largely driven by the startup of the 32kHz oscillator		1.54		s
$\overline{WU1}$ or $\overline{WU2}$ Pulse Width	t_{WU}	Minimum pulse width required to detect a wake-up event		1		µs
Shutdown Deassert Delay	t_{DPU}	The delay for $\overline{SHDN}$ to go high after a valid wake-up event		1		µs
FOUT Turn-On Time	t_{DFON}	The turn-on time for the high-frequency clock; it is gated by an AND function with three signals—the $\overline{RESET}$ signal, the internal low voltage V_{DD} monitor signal, and the assertion of the PLL; the time delay is timed from when the low-voltage monitor trips or the $\overline{RESET}$ going high, whichever happens later; FOUT always starts in the low state		31.25		ms
$\overline{INT}$ Delay	t_{DFI}	The delay for $\overline{INT}$ to go low after the FOUT clock output has been enabled; $\overline{INT}$ is used as an interrupt signal to inform the µP the high-frequency clock has started		7.82		ms
FOUT Disable Delay	t_{DFOF}	The delay after a shutdown command has asserted and before FOUT is disabled; this gives the microcontroller time to clean up and go into Sleep mode properly		1.95		ms
$\overline{SHDN}$ Assertion Delay	t_{DPD}	The delay after a shutdown command has asserted and before $\overline{SHDN}$ is pulled low (turning off the DC-DC converter) (Note 6)		2.93		ms

Note 1: Single conversion.
Note 2: DNL and INL are measured between code 010hex and 3FFhex.
Note 3: Offset error is referenced to code 010hex.
Note 4: Output swing is a function of external gain-setting feedback resistors and REF voltage.
Note 5: Measured with no load on FOUT, DOUT, and the DAC amplifiers. SCLK is idle, and all digital inputs are at DGND or DV_{DD}.
Note 6: $\overline{SHDN}$ stays high if the PLL is on.
Note 7: Actual worst-case performance is ±2.5LSB. Guaranteed limit of ±3.5LSB is due to production test limitation.
Note 8: Guaranteed by design. Not production tested.

Low-Power, 16-Bit Multichannel DAS with Internal Reference,10-Bit DACs, and RTC

Load Circuits

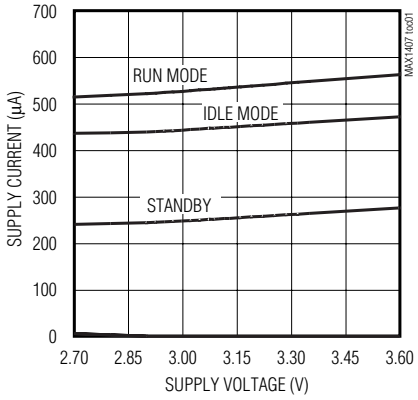




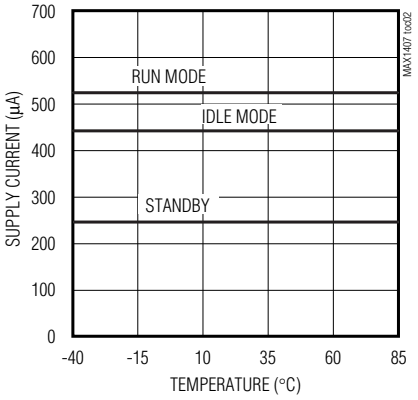
Typical Operating Characteristics

(AVDD = DVDD = 3V, MAX1407 used, TA = +25°C, unless otherwise noted.)

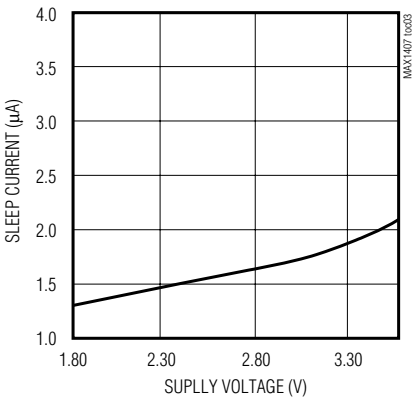
SUPPLY CURRENT vs. SUPPLY VOLTAGE



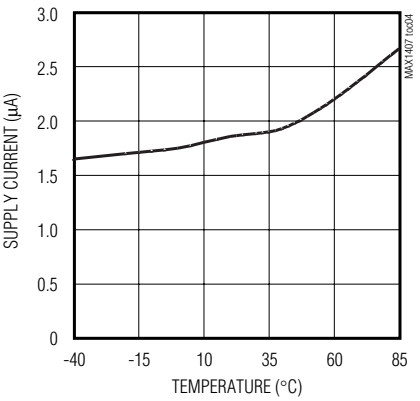
SUPPLY CURRENT vs. TEMPERATURE



SLEEP CURRENT vs. FALLING V_{DD}



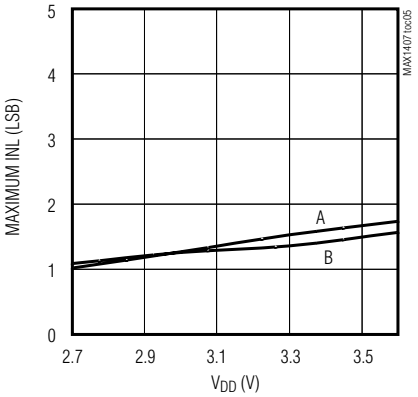
SLEEP MODE SUPPLY CURRENT vs. TEMPERATURE



Typical Operating Characteristics (continued)

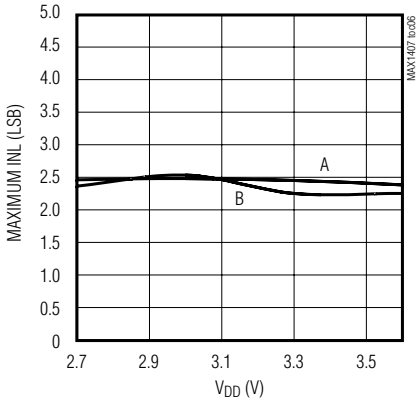
(A_{VDD} = D_{VDD} = 3V, MAX1407 used, T_A = +25°C, unless otherwise noted.)

MAXIMUM INL vs. V_{DD} (UNIPOLAR MODE, T = +25°C, PSEUDO-DIFFERENTIAL INPUT)



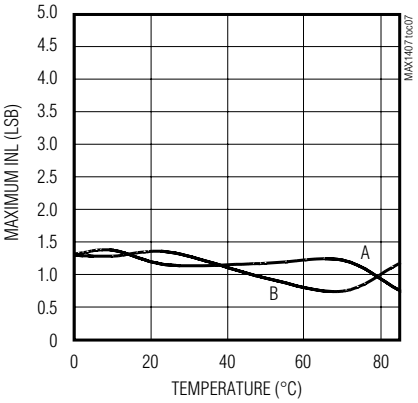
A: GAIN = 1, UNBUFFERED MODE, 60sps
B: GAIN = 1, UNBUFFERED MODE, 30sps

MAXIMUM INL vs. V_{DD} (BIPOLAR MODE, T = +25°C, FULLY DIFFERENTIAL INPUT)



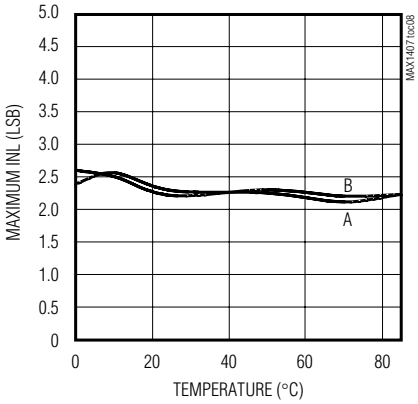
A: GAIN = 2, BUFFERED MODE, 60sps
B: GAIN = 2, BUFFERED MODE, 30sps

MAXIMUM INL vs. TEMPERATURE (UNIPOLAR MODE, V_{DD} = 3V, PSEUDO-DIFFERENTIAL INPUT)



A: GAIN = 1, UNBUFFERED MODE, 60sps
B: GAIN = 1, UNBUFFERED MODE, 30sps

MAXIMUM INL vs. TEMPERATURE (BIPOLAR MODE, V_{DD} = 3V, FULLY DIFFERENTIAL INPUT)



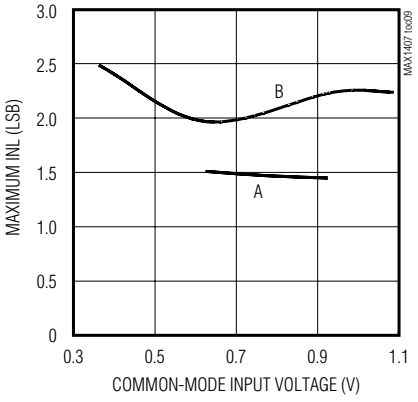
A: GAIN = 2, BUFFERED MODE, 60sps
B: GAIN = 2, BUFFERED MODE, 30sps

Low-Power, 16-Bit Multichannel DAS with Internal Reference,10-Bit DACs, and RTC

Typical Operating Characteristics (continued)

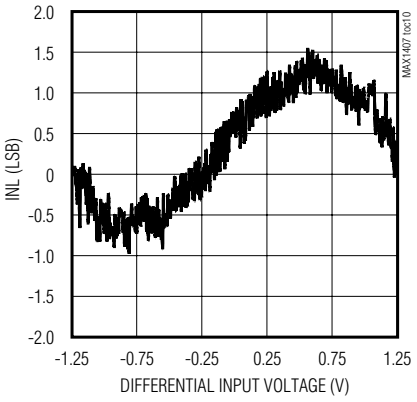
(A_{VDD} = D_{VDD} = 3V, MAX1407 used, T_A = +25°C, unless otherwise noted.)

MAXIMUM INL vs. COMMON-MODE INPUT VOLTAGE (BIPOLAR MODE, BUFFERED MODE, V_{DD} = 2.7V, 30sps, FULLY DIFFERENTIAL INPUT, T = +25°C)

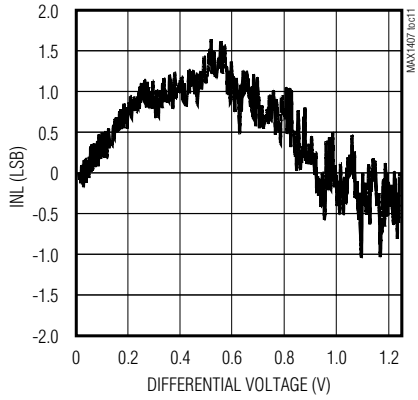


A: GAIN = 1
B: GAIN = 2

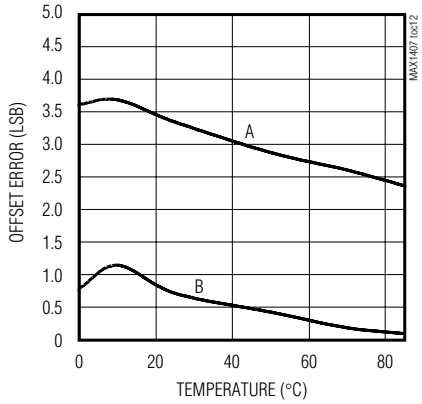
INL vs. FULLY DIFFERENTIAL INPUT VOLTAGE (BIPOLAR MODE, GAIN = 1, UNBUFFERED MODE, V_{CM} = 0.625V, V_{DD} = 3V, T = +25°C)



INL vs. PSEUDO-DIFFERENTIAL INPUT VOLTAGE RANGE (UNIPOLAR MODE, GAIN = 1, UNBUFFERED MODE, V_{NEG} = 0, V_{DD} = 3V, T = +25°C)



UNCORRECTED OFFSET ERROR vs. TEMPERATURE (UNBUFFERED MODE, V_{DD} = 3V)

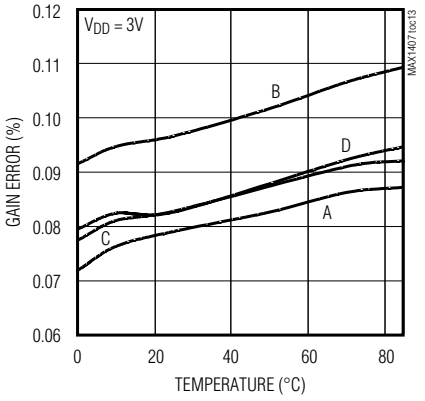


A: GAIN = 1, UNIPOLAR MODE
B: GAIN = 2, BIPOLAR MODE

Typical Operating Characteristics (continued)

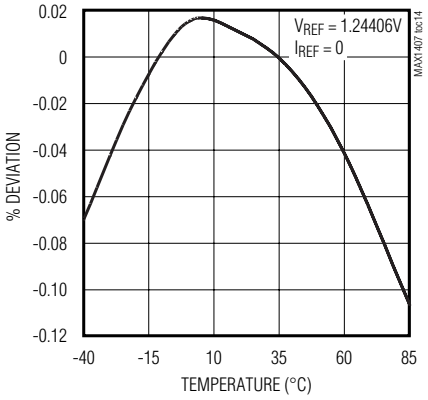
(A_{VDD} = D_{VDD} = 3V, MAX1407 used, T_A = +25°C, unless otherwise noted.)

GAIN ERROR vs. TEMPERATURE

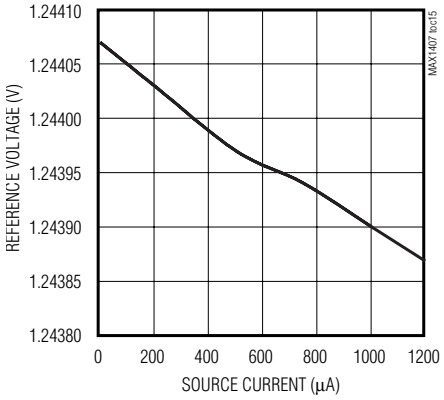


A: GAIN = 1, UNIPOLAR MODE, UNBUFFERED MODE
B: GAIN = 1, BIPOLAR MODE, UNBUFFERED MODE
C: GAIN = 2, UNIPOLAR MODE, BUFFERED MODE
D: GAIN = 2, BIPOLAR MODE, BUFFERED MODE

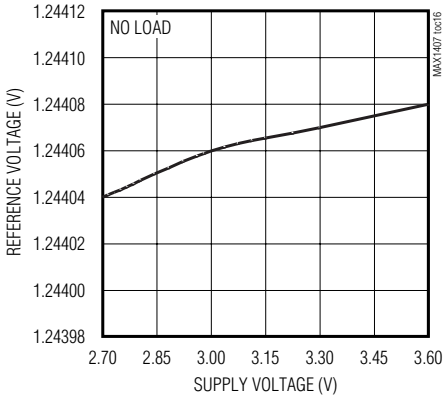
REFERENCE VOLTAGE vs. TEMPERATURE



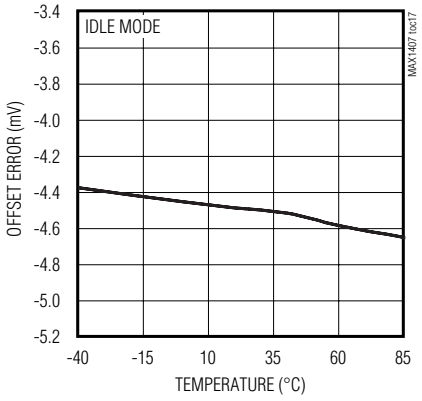
REFERENCE VOLTAGE vs. OUTPUT SOURCE CURRENT



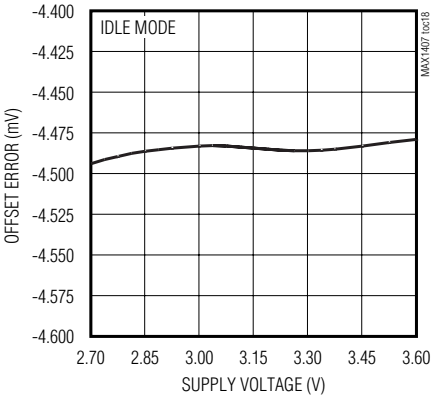
REFERENCE VOLTAGE vs. SUPPLY VOLTAGE



DAC OFFSET ERROR vs. TEMPERATURE



DAC OFFSET ERROR vs. SUPPLY VOLTAGE

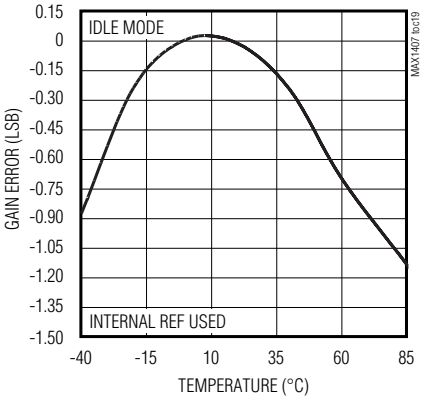


Low-Power, 16-Bit Multichannel DAS with Internal Reference,10-Bit DACs, and RTC

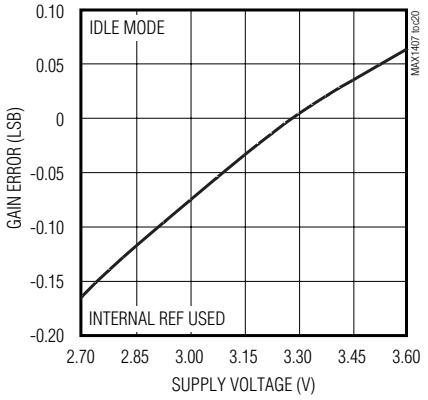
Typical Operating Characteristics (continued)

(AV_{DD} = DV_{DD} = 3V, MAX1407 used, T_A = +25°C, unless otherwise noted.)

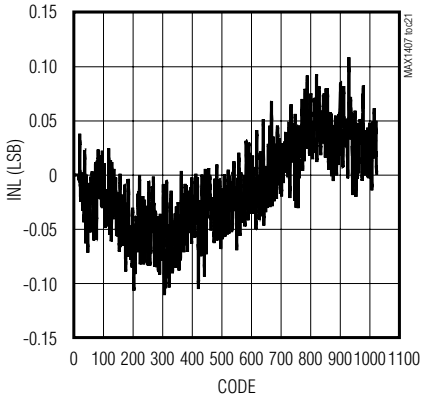
DAC GAIN ERROR vs. TEMPERATURE



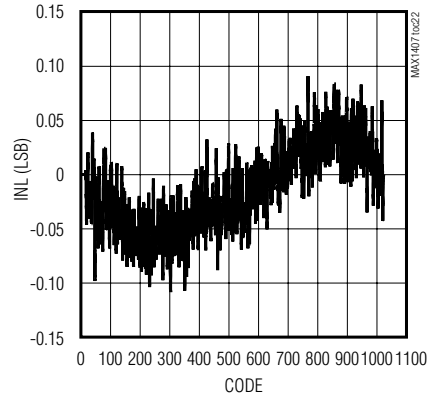
DAC GAIN ERROR vs. SUPPLY VOLTAGE



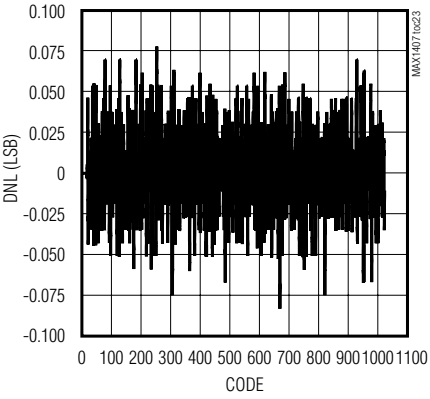
DAC INTEGRAL NONLINEARITY vs. DIGITAL CODE (AV_{DD} = 2.7V)



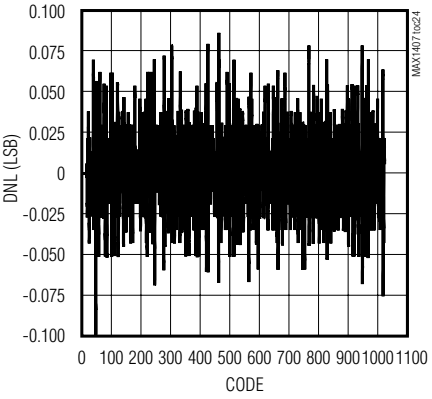
DAC INTEGRAL NONLINEARITY vs. DIGITAL CODE (AV_{DD} = 3.6V)



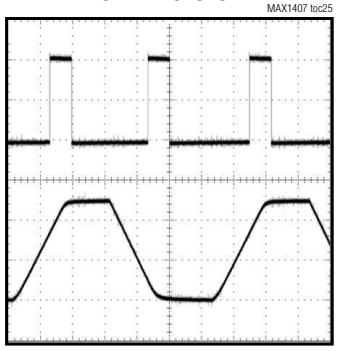
DAC DIFFERENTIAL NONLINEARITY vs. DIGITAL CODE (AV_{DD} = 2.7V)



DAC DIFFERENTIAL NONLINEARITY vs. DIGITAL CODE (AV_{DD} = 3.6V)



DAC LARGE-SIGNAL OUTPUT STEP RESPONSE

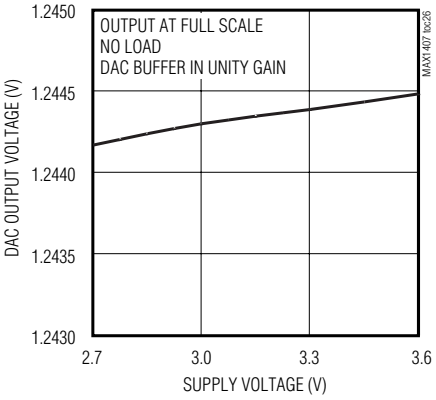


V_{REF} = 1.25V, AV_{DD} = 3.0V, R_L = 0

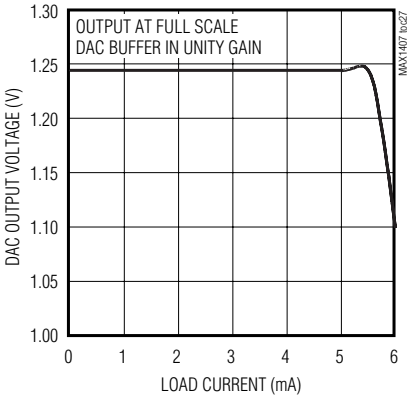
Typical Operating Characteristics (continued)

(A_{VDD} = D_{VDD} = 3V, MAX1407 used, T_A = +25°C, unless otherwise noted.)

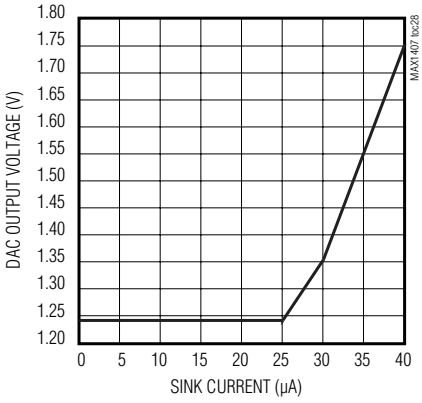
DAC OUTPUT VOLTAGE vs. SUPPLY VOLTAGE



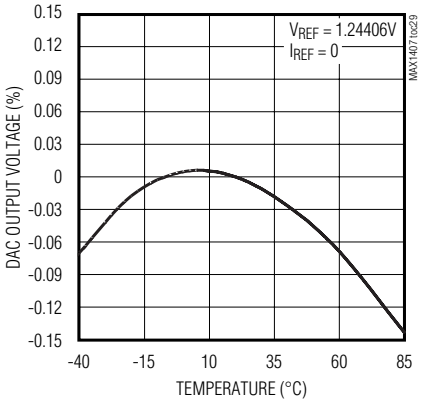
DAC OUTPUT VOLTAGE vs. SOURCE CURRENT



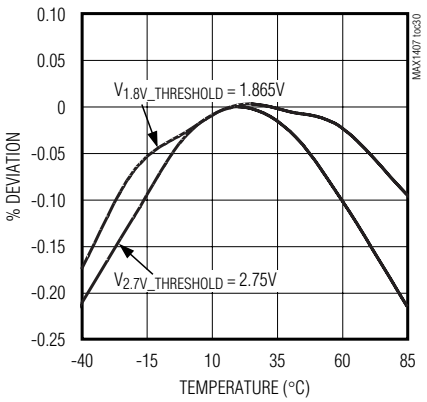
DAC OUTPUT VOLTAGE vs. SINK CURRENT



DAC OUTPUT VOLTAGE vs. TEMPERATURE



VOLTAGE MONITOR THRESHOLD vs. TEMPERATURE



Low-Power, 16-Bit Multichannel DAS with Internal Reference,10-Bit DACs, and RTC

Pin Description

MAX1407 MAX1414	MAX1408	MAX1409	PIN	FUNCTION
1	—	—	FB2	Force/Sense DAC2 Feedback Input
—	1	—	IN7	Analog Input. Analog input to the negative mux only.
—	—	1	FB1	Force/Sense DAC1 Feedback Input
2	2	—	D0	Digital Output. Three-state general-purpose digital output.
3	—	—	FB1	Force/Sense DAC1 Feedback Input
—	3	—	IN6	Analog Input. Analog input to the negative mux only.
4	—	2	OUT1	Force/Sense DAC1 Output
—	4	—	IN4	Analog Input. Analog input to the positive mux only.
5	5	3	IN0	Analog Input. Analog input to both the positive and negative mux.
6	6	4	REF	1.25V Reference Buffer Output/External Reference Input. Reference voltage for the ADC and the DAC. Connect a 4.7µF capacitor to REF between REF and AGND.
7	7	5	AGND	Analog Ground. Reference point for the analog circuitry. AGND connects to the IC substrate.
8	8	6	AV_{DD}	Analog Supply Voltage
9	9	7	CPLL	PLL Capacitor Connection Pin. Connect an 18nF ceramic capacitor between CPLL and AV_{DD}.
10	10	8	$\overline{WU1}$	Active-Low Wake-Up Input. Internally pulled up. The device will wake-up from Sleep mode to Standby mode when $\overline{WU1}$ is asserted.
11	11	9	$\overline{WU2}$	Active-Low Wake-Up Input. Internally pulled up. The device will wake-up from Sleep mode to Standby mode when $\overline{WU2}$ is asserted.
12	12	10	$\overline{RESET}$	Active-Low RESET Output. It remains low while AV_{DD} is below the threshold and stays low for a timeout period after AV_{DD} rises above the threshold. $\overline{RESET}$ is an open-drain output.
13	13	—	IN1	Analog Input. Analog input to both the positive and negative mux.
14	14	—	IN2	Analog Input. Analog input to both the positive and negative mux.
15	15	—	$\overline{SHDN}$	Programmable Shutdown Output. Goes low in Sleep mode.
16	16	—	$\overline{DRDY}$	Active-Low Data Ready Output. A logic low indicates that a new conversion result is available in the Data register. $\overline{DRDY}$ returns high upon completion of a full output word read operation. $\overline{DRDY}$ also signals the end of an ADC offset-calibration.
17	17	11	FOUT	2.4576MHz Clock Output. FOUT can be used to drive the input clock of a µP.
18	18	12	CLKOUT	32kHz Crystal Output. Connect a 32kHz crystal between CLKIN and CLKOUT.
19	19	13	CLKIN	32kHz Crystal Input. Connect a 32kHz crystal between CLKIN and CLKOUT.

Pin Description (continued)

MAX1407 MAX1414	MAX1408	MAX1409	PIN	FUNCTION
20	20	14	$\overline{INT}$	Active-Low Interrupt Output. $\overline{INT}$ goes low when the PLL output is ready, when the signal-detect comparator is tripped, or when the alarm is triggered.
21	21	15	DOUT	Serial Data Output. DOUT outputs serial data from the internal shift register on SCLK's falling edge. When $\overline{CS}$ is high, DOUT is three-stated.
22	22	16	DIN	Serial Data Input. Data on DIN is written to the input shift register and is clocked in at SCLK's rising edge when $\overline{CS}$ is low.
23	23	17	SCLK	Serial Clock Input. Apply an external serial clock to transfer data to and from the device. This serial clock can be continuous, with data transmitted in a train of pulses, or intermittent while $\overline{CS}$ is low.
24	24	18	$\overline{CS}$	Active-Low Chip-Select Input. $\overline{CS}$ is used to select the active device in systems with more than one device on the serial bus. Data will not be clocked into DIN unless $\overline{CS}$ is low. When $\overline{CS}$ is high, DOUT is three-stated.
25	25	19	DGND	Digital Ground. Reference point for digital circuitry.
26	26	20	DV_{DD}	Digital Supply Voltage
27	27	—	IN3	Analog Input. Analog input to both the positive and negative mux.
28	—	—	OUT2	Force/Sense DAC2 Output
—	28	—	IN5	Analog Input. Analog input to the positive mux only.

Detailed Information

The MAX1407/MAX1408/MAX1409/MAX1414 are low-power, general-purpose, multichannel DAS featuring a multiplexed fully differential 16-bit ΣΔ analog-to-digital converter (ADC), 10-bit force/sense digital-to-analog converters (DAC), a real-time clock (RTC) with an alarm, a bandgap voltage reference, a signal detect comparator, two power-supply voltage monitors, wake-up control circuitry, and a high-frequency phase-locked loop (PLL) clock output all controlled by a 3-wire serial interface. (See Table 1 for the MAX1407/MAX1408/MAX1409/MAX1414 feature sets and Figures 1, 2, 3 for the *Functional Diagrams*). These DAS directly interface to various sensor outputs and once configured provide the stimulus, conditioning, and data conversion, as well as microprocessor support. Figure 4 is a *Typical Application Circuit* for the MAX1407/MAX1414.

The 16-bit ΣΔ ADC is capable of programmable continuous conversion rates of 30Hz or 60Hz and gains of 1/3, 1, and 2V/V to suit applications with different power and dynamic range constraints. The force/sense DACs provide 10-bit linearity for precise sensor applications.

Table 1. MAX1407/MAX1408/MAX1409/MAX1414 Feature Sets

PART	ADC AUXILIARY ANALOG INPUTS	FORCE/ SENSE DAC	THREE-STATE DIGITAL OUTPUT	COMPARATOR THRESHOLD (mV)	RTC	ADC DATA READY (DRDY)	EXTERNAL POWER-SUPPLY SHUTDOWN CONTROL	ADC DIFFERENTIAL INPUT MUX
MAX1407	4	2	Yes	0	Yes	Yes	Yes	8
MAX1414	4	2	Yes	50	Yes	Yes	Yes	8
MAX1408	8	0	Yes	0	Yes	Yes	Yes	8
MAX1409	1	1	No	0	Yes	No	No	4

Low-Power, 16-Bit Multichannel DAS with Internal Reference,10-Bit DACs, and RTC

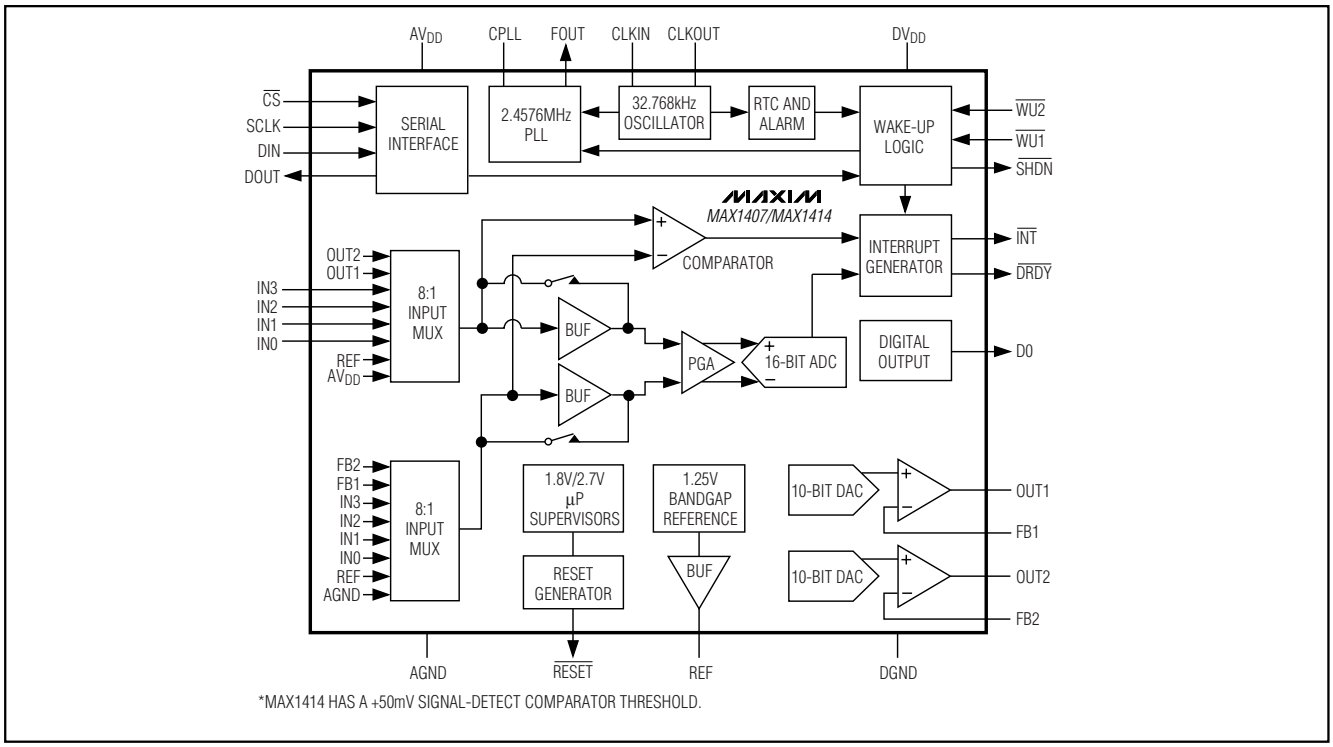


Figure 1. MAX1407/MAX1414 Functional Diagram

With the use of two external resistors, the DAC output can go from 0.05V to AV_{DD} - 0.2V. The ADCs and DACs both utilize a precise low-drift 1.25V internal bandgap reference for conversions and setting of the full-scale range. For applications that require increased accuracy, power-down the internal reference and connect an external reference at REF. The RTC is leap year compensated until 9999 and provides an alarm function that can be used to wake-up the system or cause an interrupt at a predefined time. The power-supply voltage monitors detect when AV_{DD} falls below a trip threshold voltage at either +1.8V or +2.7V causing the reset to be asserted. The 4-wire serial interface is used to communicate directly between SPI, QSPI, and MICROWIRE devices for system configuration and readback functions.

Analog Input Protection

Internal protection diodes clamp the analog input to AV_{DD} and AGND, which allow the channel input pins to swing from AGND - 0.3V to AV_{DD} + 0.3V without damage. However, for accurate conversions near full scale, the inputs must not exceed AV_{DD} by more than 50mV or be lower than AGND by 50mV.

Analog Mux

The MAX1407/MAX1408/MAX1414 include a dual 8 to 1 multiplexer for the positive and negative inputs of the ADC. The MAX1409 has a dual 4 to 1 multiplexer at the inputs of the ADC. Figures 1, 2, and 3 illustrate which signals are present at the inputs of each multiplexer for the MAX1407/MAX1408/MAX1409/MAX1414. The MUXP and MUXN bits of the MUX register choose which inputs will be seen at the input to the ADC (Tables 4 and 5) and the signal-detect comparator. See the MUX Register description under the *On-Chip Registers* section for multiplexer functionality.

Input Buffers

The MAX1407/MAX1408/MAX1409/MAX1414 provide input buffers to isolate the analog inputs from the capacitive load presented by the ADC modulator (Figure 5 and 6). The buffers are chopper stabilized to reduce the effect of their DC offsets and low-frequency noise. Since the buffers can represent more than 25% of the total analog power dissipation (typically 220µA), they may be shut down in applications where minimum power dissipation is required and the capacitive input load is not a concern (see *ADC and Power1 Registers*). Disable the buffers in applications where the inputs must operate close to AGND or above +1.4V. The buffers are individually enabled or disabled.

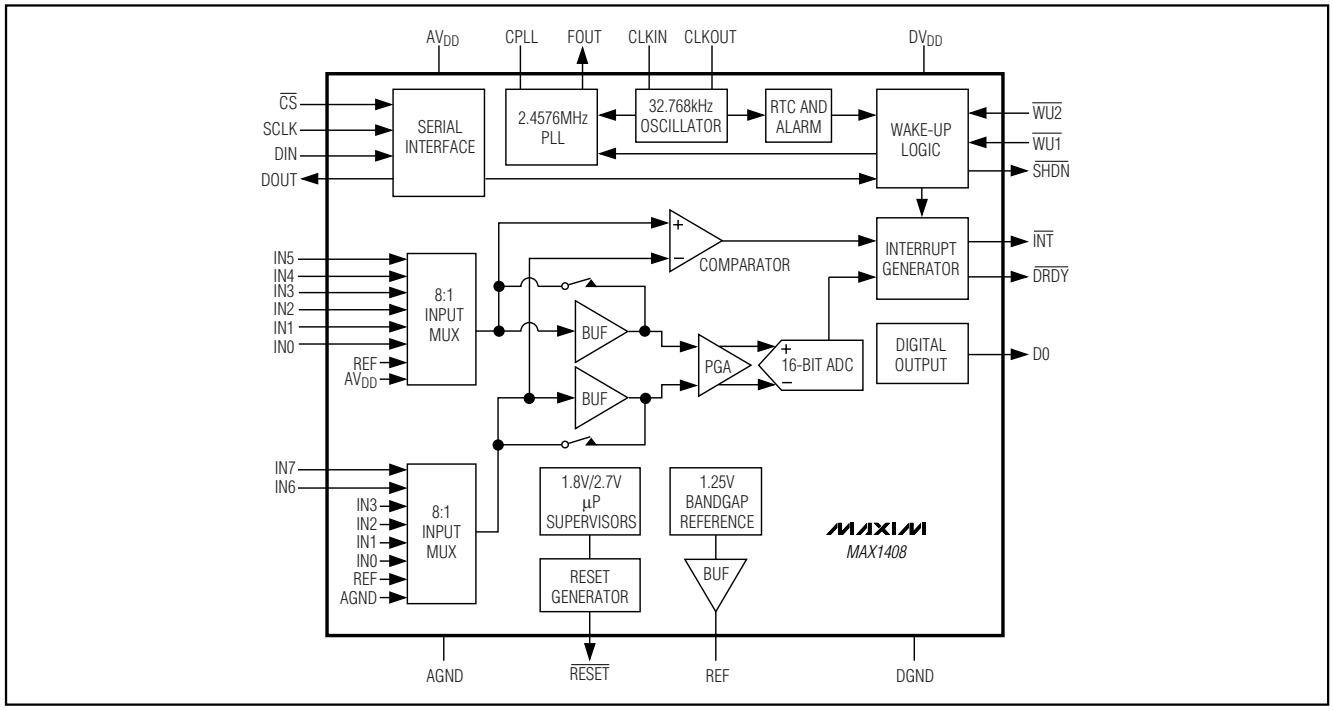


Figure 2. MAX1408 Functional Diagram

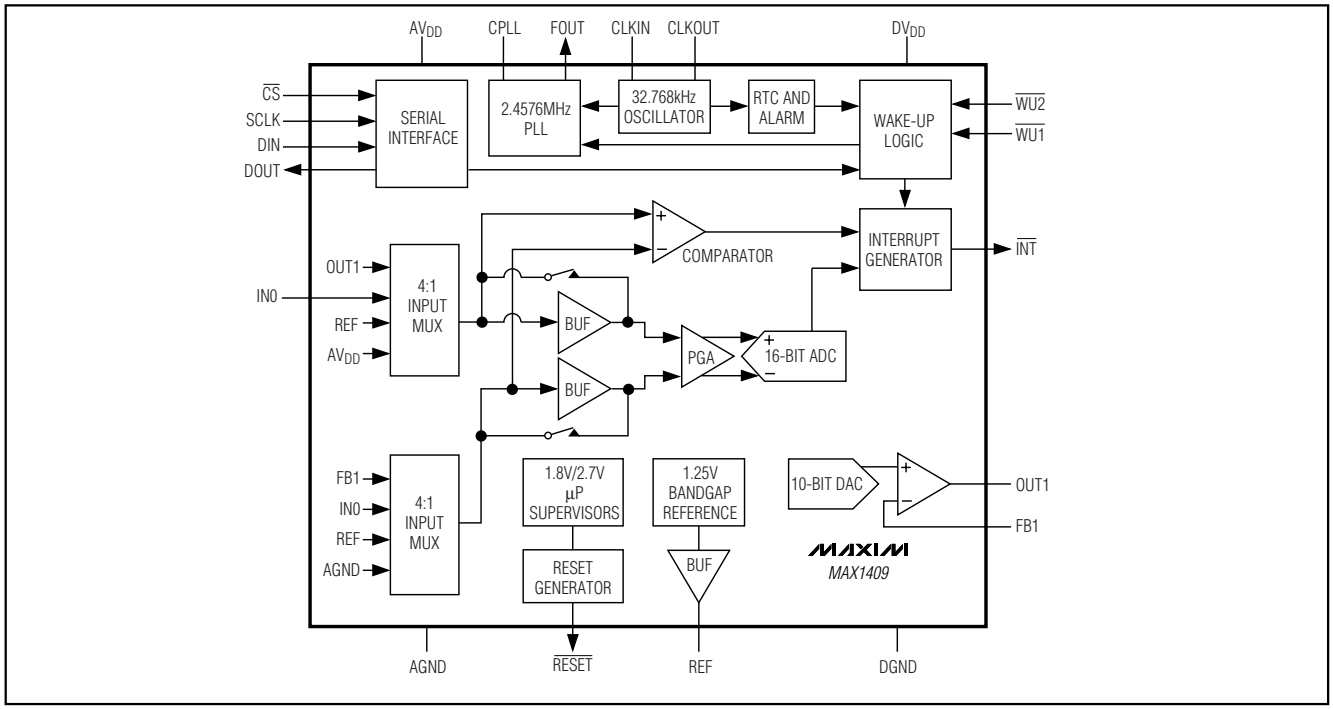


Figure 3. MAX1409 Functional Diagram

Low-Power, 16-Bit Multichannel DAS with Internal Reference,10-Bit DACs, and RTC

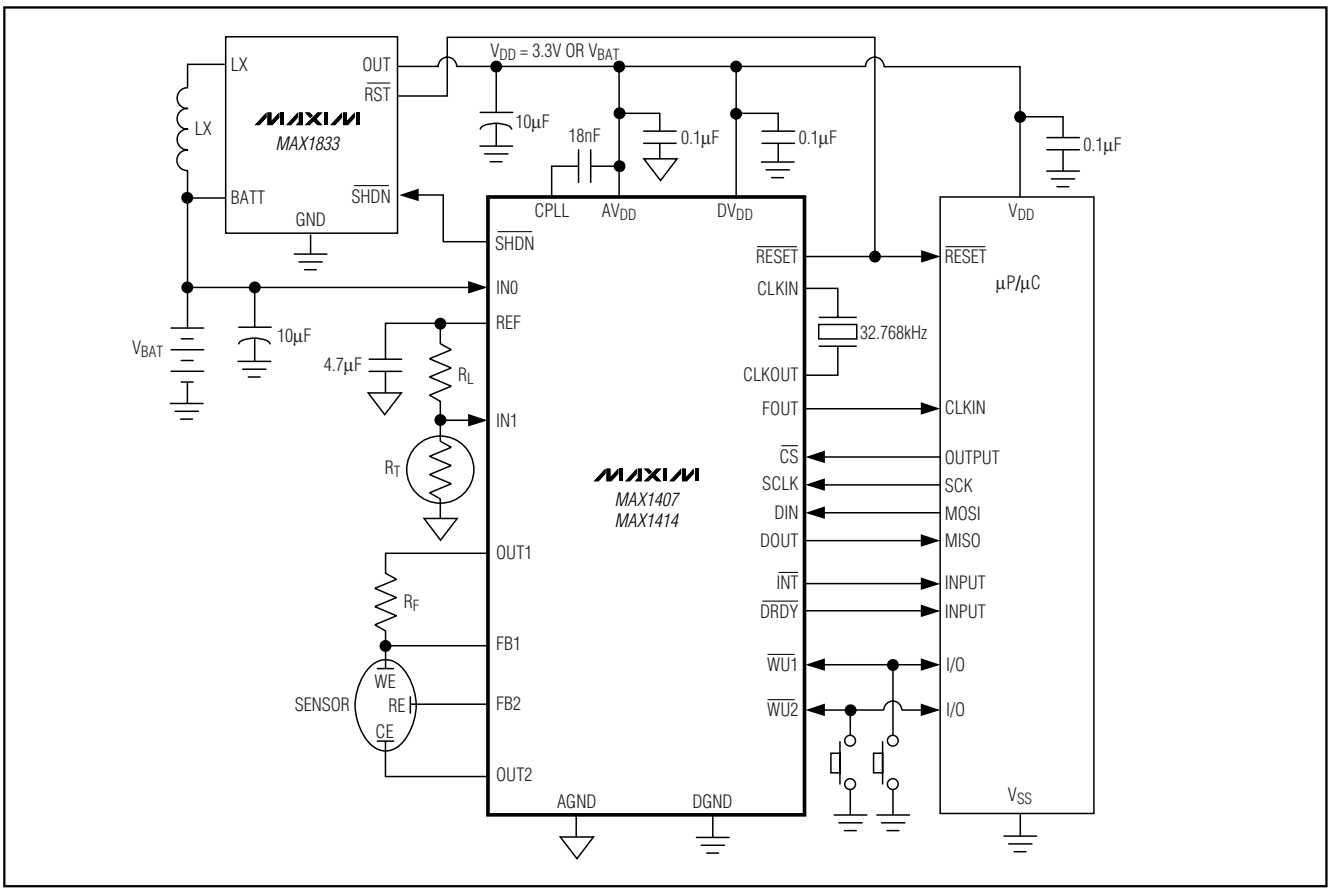


Figure 4. MAX1407/MAX1414 Typical Application Circuit

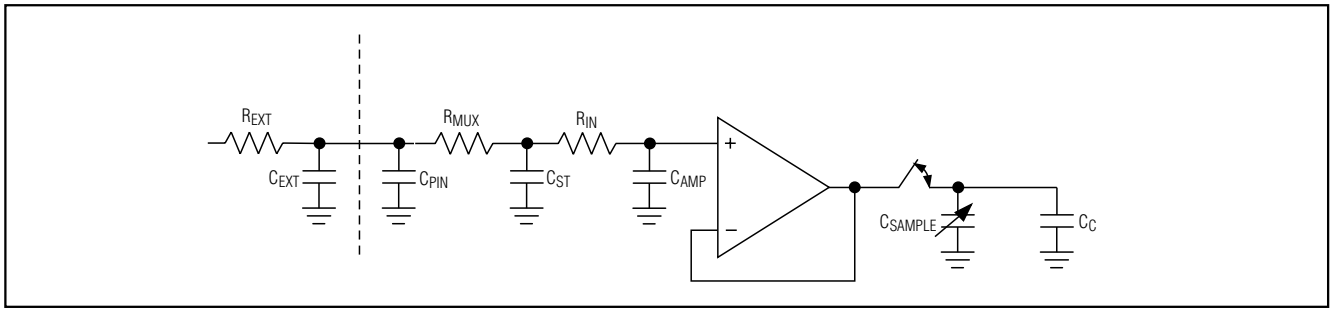


Figure 5. Analog Input—Buffered Mode

Buffered Mode

When used in buffered mode, the buffers isolate the inputs from the sampling capacitors. The sampling-related gain error is dramatically reduced since only a small dynamic load is present from the chopper. The multiplexer exhibits an input leakage current of 0.5nA (typ). With high-source resistances, this leakage current may result in a large DC offset error.

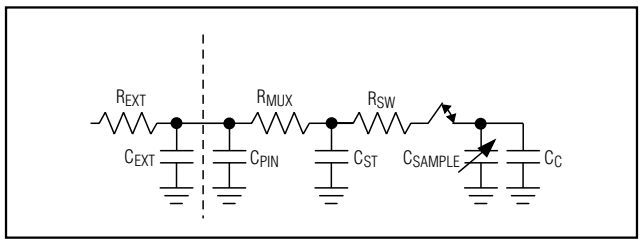


Figure 6. Analog Input—Unbuffered Mode

Unbuffered Mode

When used in unbuffered mode, the switched capacitor sampling front end of the modulator presents a dynamic load to the driving circuitry. The size of the internal sampling capacitor and the input sampling frequency (Figure 6) determines the dynamic load (see *Dynamic Input Impedance* section). As the gain increases, the input sampling capacitance also increases. Since the MAX1407/MAX1408/MAX1409/MAX1414 sample at a constant rate for all gain settings, the dynamic load presented by the inputs varies with the gain setting.

PGA Gain

An integrated programmable-gain amplifier (PGA) provides three user-selectable gains: +1/3V/V, +1V/V, and +2V/V to maximize the dynamic range of the ADC. Bits GAIN1 and GAIN0 set the desired gain (see *ADC Register*). The gain of +1/3V/V allows the direct measurement of the supply voltage through an internal multiplexer input or through an auxillary input.

ADC Modulator

The MAX1407/MAX1408/MAX1409/MAX1414 perform analog-to-digital conversions using a single-bit, second-order, switched-capacitor delta-sigma modulator. The delta-sigma modulation converts the input signal into a digital pulse train whose average duty cycle represents the digitized signal information. The pulse train is then processed by a digital decimation filter.

The modulator provides 2nd-order frequency shaping of the quantization noise resulting from the single bit quantizer. The modulator is fully differential for maximum signal-to-noise ratio and minimum susceptibility to power-supply noise. The modulator operates at one of two different sampling rates resulting in an output data rate of either 30Hz or 60Hz (see *ADC Register*).

ADC Offset Calibration

The MAX1407/MAX1408/MAX1409/MAX1414 are capable of performing digital offset correction to eliminate changes due to power-supply voltage or system temperature. At the end of a calibration cycle, a 16-bit calibration value is stored in the Offset register in two's compliment format. After completing a conversion, the MAX1407/MAX1408/MAX1409/MAX1414 subtract the calibration value from the ADC conversion result and write the offset compensated data to the Data register (see *Offset Register* section). Either a positive or negative offset can be calibrated. During offset calibration, $\overline{DRDY}$ will go high. $\overline{DRDY}$ goes low after calibration is complete. The offset register can be programmed to skew the ADC offset with a maximum range from -2^{15} to $(+2^{15} - 1)$LSBs, e.g., if the programmed 2's complement value is +2LSB (-2LSB), this translates to a -2LSB (+2LSB) shift in bipolar mode or a -4LSB (+4LSB) shift in unipolar mode.To maintain optimum performance, recalibrate the ADC if the temperature changes by more than 20°C. Offset calibration should also be performed after any changes in PGA gain, bipolar/unipolar input range, buffered/unbuffered mode, or conversion speed. During calibration, the two mulitplexers will be disabled and the inputs to the ADC will internally be shorted to a common-mode voltage.

ADC Digital Filter

The on-chip digital filter processes the 1-bit data stream from the modulator using a $SINC^3$ filter function. The $SINC^3$ filters settle in three data word periods. The settling time is 3/60Hz or 50ms (for RATE bit in ADC register set to 1) and 3/30Hz or 100ms (for RATE bit set to "0").

ADC Digital Filter Characteristics

The transfer function for a $SINC^3$ filter function is that of three cascaded $SINC^1$ filters. This can be described in the Z-domain by:

$$H(z) = \left[\frac{1}{N}\frac{\left(1 - z^{-N}\right)}{\left(1 - z^{-1}\right)}\right]^3$$

and in the frequency domain by:

$$H(f) = \left[\frac{1}{N}\frac{\sin\left(N\pi\frac{f}{f_M}\right)}{\sin\left(\pi\frac{f}{f_M}\right)}\right]^3$$

where N, the decimation factor, is the ratio of the modulator frequency f_M to the output frequency f_N.

Low-Power, 16-Bit Multichannel DAS with Internal Reference,10-Bit DACs, and RTC

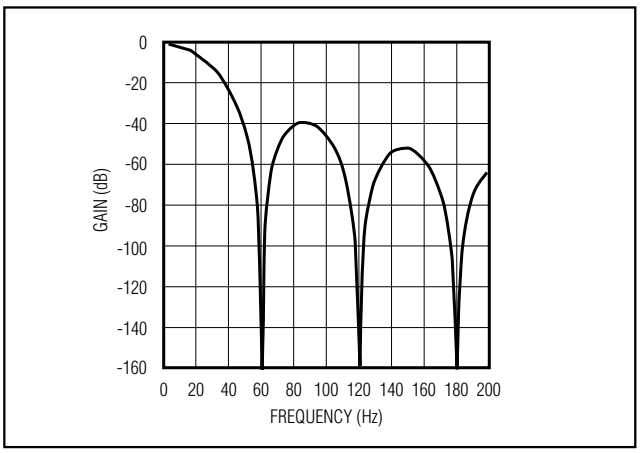


Figure 7. Frequency Response of the SINC^3 Filter (Notch at 60Hz)

Figure 7 shows the filter frequency response. The SINC^3 characteristic cutoff frequency is 0.262 times the first notch frequency. This results in a cutoff frequency of 15.72Hz for a first filter notch frequency of 60Hz (output data rate of 60Hz). The response shown in Figure 7 is repeated at either side of the digital filter's sample frequency (f_M) (f_M = 15.36kHz for 30Hz and f_M = 30.72kHz for 60Hz) and at either side of the related harmonics ($2f_M$, $3f_M$,....).

The output data rate for the digital filter corresponds with the positioning of the first notch of the filter's frequency response. Therefore, for the plot of Figure 7 where the first notch of the filter is at 60Hz, the output data rate is 60Hz. The notches of this $(\sin x/x)^3$ filter are repeated at multiples of the first notch frequency. The SINC^3 filter provides an attenuation of better than 100dB at these notches.

For step changes at the input, enough settling time must be allowed before valid data can be read. The settling time depends upon the output data rate chosen for the filter. The settling time of the SINC^3 filter to a full-scale step input can be up to four times the output data period, or three times if the step change is synchrozied with FSYNC.

Force/Sense DAC (MAX1407/MAX1409/MAX1414)

The MAX1407/MAX1414 incorporate two 10-bit force/sense DACs while the MAX1409 has one. The DACs use a precise 1.25V internal bandgap reference for setting the full-scale range. Program the DAC1 and DAC2 registers through the serial interface to set the output voltages of the DACs seen at OUT1 and OUT2. Shorting FB1(2) and OUT1(2) configures the DAC in a unity-gain setting. Connecting resistors in a voltage-divider configuration between OUT1(2), FB1(2), and GND sets a different closed-loop gain for the output amplifier (see the *Applications Information* section).

The DAC output amplifier typically settles to $\pm 1/2$LSB from a full-scale transition within 65µs, when it is connected in unity gain and loaded with 12kΩ in parallel with 200pF. Loads less than 2kΩ may degrade performance. See the *Typical Operating Characteristics* section for the source-and-sink capabilty of the DAC output.

The MAX1407/MAX1409/MAX1414 feature a software-programmable shutdown mode for the DACs that reduce the total power consumption when they are not used. The two DACs can be powered-down independently or simultaneously by clearing the DA1E and DA2E bits (see *Power1 Register*). DAC outputs OUT1 and OUT2 go high impedance when powered down. The DACs are automatically powered up and ready for a conversion when Idle or Run mode is entered.

Voltage Monitors

The MAX1407/MAX1408/MAX1409/MAX1414 include two on-board voltage monitors. When AV_{DD} is below the $\overline{RESET}$ trip threshold, $\overline{RESET}$ goes low and the RST bit of the Status register is set to "1". When AV_{DD} is below the Low V_{DD} trip threshold, the LVD bit of the Status register is set to 1.

$\overline{RESET}$ Voltage Monitor

The $\overline{RESET}$ voltage monitor is powered up at all times (provided that VM = 0 and LVDE = 1 or VM = 1 and LSDE = 1). A threshold voltage of either +1.8V or +2.7V may be selected for the $\overline{RESET}$ voltage monitor (see *Power2 Register*). At initial power-up, the $\overline{RESET}$ trip threshold is set to 2.7V. If the $\overline{RESET}$ voltage monitor is tripped, the RST bit of the status register is set to "1" and $\overline{RESET}$ goes low. $\overline{RESET}$ is held low for 1.54 seconds (typ) after AV_{DD} rises above the $\overline{RESET}$ voltage monitor threshold. If AV_{DD} is no longer below the $\overline{RESET}$ threshold, reading the Status register will clear RST.

Low V_{DD} Voltage Monitor

When the device is operating in Run, Idle, or Standby mode (see *Power Modes*) and AV_{DD} goes below +2.7V, the low V_{DD} monitor trips, indicating that the supply voltage is below the safe minimum for proper operation. When tripped, the Low V_{DD} Voltage Monitor sets the LVD bit of the Status register to 1. If AV_{DD} is no longer below +2.7V, reading the Status register will clear LVD. The low V_{DD} monitor is powered down in Sleep mode. When it is powered down, the LVD bit stays unchanged. The LVD is cleared if it is read in Sleep mode.

Internal/External Reference

The MAX1407/MAX1408/MAX1409/MAX1414 have an internal low-drift +1.25V reference used for both ADC and DAC conversion. The buffered reference output can be used as a reference source for other devices in the system. The internal reference requires a 4.7µF low-ESR ceramic capacitor or tantalum capacitor connected between REF and AGND. For applications that require increased accuracy, power-down the internal reference by writing a 0 to the REFE bit of the Power1 register and connect an external reference source to REF. The valid external reference voltage range is 1.25V ±100mV.

Crystal Oscillator

The on-chip oscillator requires an external crystal (or resonator) connected between CLKIN and CLKOUT with an operating frequency of 32.768kHz. This oscillator is used for the RTC, alarm, signal-detect comparator, and PLL. The oscillator is operational down to 1.8V. In any crystal-based oscillator circuit, the oscillator frequency is based on the characteristics of the crystal. It is important to select a crystal that meets the design requirements, especially the capacitive load (C_L) that must be placed across the crystal pins in order for the crystal to oscillate at its specified frequency. C_L is the capacitance that the crystal needs to "see" from the oscillator circuit; it is not the capacitance of the crystal itself. The MAX1407/MAX1408/MAX1409/MAX1414 have 6pF of capacitance across the CLKIN and CLKOUT pins. Choose a crystal with a 32.768kHz oscillation frequency and a 6pF capacitive load such as the C-002RX32-E from Epson Crystal. Using a crystal with a C_L that is larger than the load capacitance of the oscillator circuit will cause the oscillator to run faster than the specified nominal frequency of the crystal. Conversely, using a crystal with a C_L that is smaller than the load capacitance of the oscillator circuit will cause the oscillator to run slower than the specified nominal frequency of the crystal.

Phase-Locked Loop (PLL) and FOUT

An on-board phase-locked loop generates a 2.4576MHz clock at FOUT from the 32.768kHz crystal oscillator. FOUT can be used to clock a µP or other digital circuitry. Connect an 18nF ceramic capacitor from CPLL to AV_{DD} to create the 2.4576MHz clock signal at FOUT. To power down the PLL, clear PLLE in the Power2 register (see *Power2 Register*) or write to the Sleep register. FOUT will be active for 1.95ms (t_{DFOF}) after receiving either power-down command and then go low. This provides extra clock signals to the µP to complete a shutdown sequence. The PLL is active in all modes except the sleep mode (see *Power Modes*). To reactivate the PLL, the following conditions must be met: AV_{DD} is greater than the low V_{DD} voltage monitor threshold, $\overline{RESET}$ is deasserted, and the PLLE bit is equal to "1". FOUT is enabled 31.25ms (t_{DFON}) after the PLL is activated. At initial power-up, the PLL is enabled. If $\overline{RESET}$ is asserted while the PLL is running, the PLL does not shut down.

Real-Time Clock (RTC)

The integrated RTC provides the current second, minute, hour, date, month, day, year, century, and millenium information. An internally generated reference clock of 1.024kHz (derived from the 32.768kHz crystal) drives the RTC. The RTC operates in either 24-hour or 12-hour format with an AM/PM indicator (see *RTC_Hour Register*). An internal calendar compensates for months with less than 31 days and includes leap year correction through the year 9999. The RTC operates from a supply voltage of +1.8V to +3.6V and consumes less than 1µA current.

Time of Day Alarm

The MAX1407/MAX1408/MAX1409/MAX1414 offer a time of day alarm which generates an interrupt when the RTC reaches a preset combination of seconds, minutes, hours, and day (see *Alarm Registers*). In addition to setting a "single-shot" alarm, the Time of Day Alarm can also be programmed to generate an alarm every second, minute, hour, day, or week. "Don't care" states can be inserted into one or more fields if it is desired for them to be ignored for the alarm condition. The Time of Day Alarm wakes up the device into Standby mode if it is in Sleep mode. The Time of Day Alarm operates from a supply voltage of +1.8V to +3.6V.

Interrupt ($\overline{INT}$)

$\overline{INT}$ indicates one of three conditions. After receiving a valid interrupt ($\overline{INT}$ goes low), read the Status register and the AI_Status register (if the alarm is enabled) to identify the source of the interrupt. The three sources of interrupts are from the CLK, SDC, and ALIRQ bits.

PLL Ready

On power-up, $\overline{INT}$ is high. 7.82ms (t_{DFI}) after the PLL output appears on FOUT, $\overline{INT}$ goes low (see Figure 15). The CLK bit of the Status register is set to "1" after FOUT is enabled. Reading the Status register clears the CLK bit. $\overline{INT}$ remains low until the device detects a start bit through the serial interface from the µP. The purpose of this interrupt is to inform the µP that the FOUT clock signal is present.

Low-Power, 16-Bit Multichannel DAS with Internal Reference,10-Bit DACs, and RTC

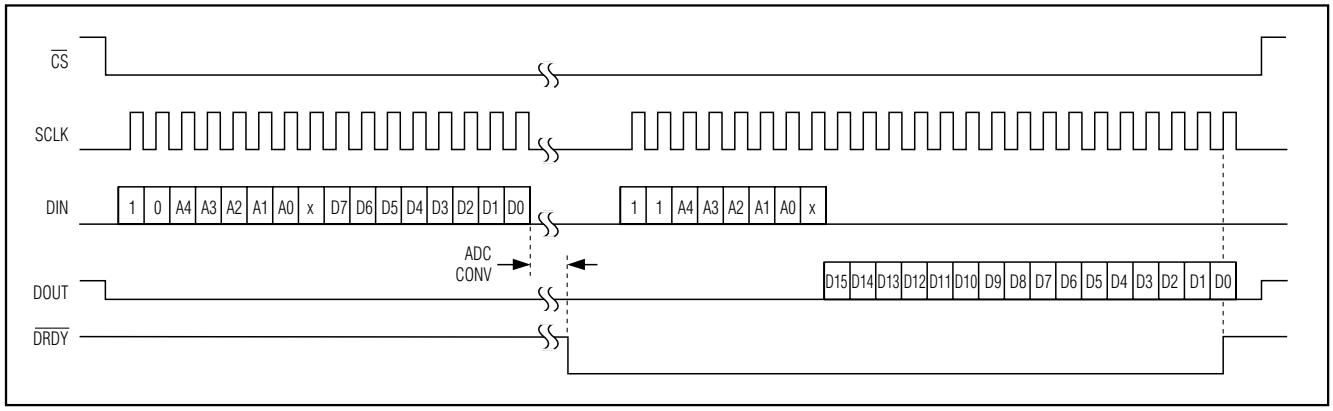


Figure 8. ADC Conversion Timing Diagram

Signal Detect

The INT pin will also go low and stay low when the differential voltage on the selected analog inputs exceeds the signal-detect comparator trip threshold (0mV for the MAX1407/MAX1408/MAX1409 and 50mV for the MAX1414). This will latch the SDC bit of the Status register to one. Additional signal detect interrupts cannot be generated unless the SDC bit is cleared. To clear the SDC bit, the Status register must be read and the input must be below the signal-detect threshold. Powering down the signal detect-comparator without reading the Status register will also clear the SDC bit. Similar to the power-up case, INT goes high when the device detects a start bit through the serial interface from the µP.

Time of Day Alarm

If the device is in Sleep mode, the alarm will wake up the device and set the ALIRQ bit. INT is asserted when the PLL is turned on. If an alarm occurs while the device is awake (BIASE = 1), the ALIRQ bit will be set and INT will go low. INT remains low until the device detects a start bit through the serial interface from the µP. ALIRQ is reset to 0 when any alarm register is read or written to.

Shutdown (SHDN)

SHDN is an active-low output that can be used to control an external power supply. Powering up the PLL (PLLE = 1) or writing a "1" to the SHDE bit of the Power2 register causes SHDN to go high. SHDN goes low when the SHDE bit is set to 0 only if the PLL is powered down (PLLE = 0). The SHDN output stays high for 2.93ms (t_{DPD}) after receiving a power-down command, allowing the external power supply to stay alive so that the µP can properly complete a shutdown sequence. SHDN is not available on the MAX1409. **Note:** Entering Sleep mode automatically sets PLLE and SHDE to 0. Any wake-up event will cause SHDN to go high. (See *Wake-Up* section.)

Data Ready (DRDY)

This pin will go low and stay low upon completion of an ADC conversion or end of an ADC calibration. This signals the µP that a valid conversion or calibration result has been written to the DATA or the OFFSET register. The DRDY pin goes high either when the µP has finished reading the conversion/calibration result on the last rising edge of SCLK (see Figure 8), or when the next conversion result is about to be written to the DATA register. When no read operation is performed, DRDY pulses at 60Hz with a pulse high time of 162.76µs (or 30Hz with a pulse high time of 325.52µs) DRDY is not available on the MAX1409. To see when the ADC has completed a normal conversion or a calibration conversion for the MAX1409, check the status of the ADD bit in the Status register.

Serial Digital Interface

The SPI/QSPI/MICROWIRE-serial interface consists of chip select (CS), serial clock (SCLK), data in (DIN), and data out (DOUT) (See Figure 9). The serial interface provides access to 29 on-chip registers, allowing control to all the power modes and functional blocks, including the ADCs, DACs, and RTC. Table 2 lists the address and read/write accessibility of all the registers.

A logic high on CS three-states DOUT and causes the MAX1407/MAX1408/MAX1409/MAX1414 to ignore any signals on SCLK and DIN. To clock data into or out of the internal shift register, drive CS low. SCLK synchronizes the data transfer. The rising edge of SCLK clocks DIN into the shift register, and the falling edge of SCLK

clocks DOUT out of the shift register. DIN and DOUT are transferred as MSB first (data is left justified). Figure 10 shows detailed serial interface timing.

All communication with the MAX1407/MAX1408/MAX1409/MAX1414 begins with a command byte on DIN, where the first logic 1 on DIN will be recognized as the START bit (MSB) for the command byte (Table 3). The following seven clock cycles load the command into a shift register. These seven bits specify which of the registers will be accessed, whether a read or write operation will take place, and the length of the subsequent data (0-bit, 8-bit, 16-bit, or burst mode). Idle DIN low between writes to the MAX1407/MAX1408/MAX1409/MAX1414. Figures 11–14 show the read and write timing for 8- and 16-bit data. Data is updated on the last rising edge of the SCLK in the command word. $\overline{CS}$ should not go high between data transfers. If $\overline{CS}$ is toggled before the end of a write or read operation, the device can enter an incorrect mode. Clock in 72 zeros to clear this state and re-arm the serial interface.

After loading the command byte into the shift register, additional clocks shift out data on DOUT for a read and shift in data on DIN for a write operation.

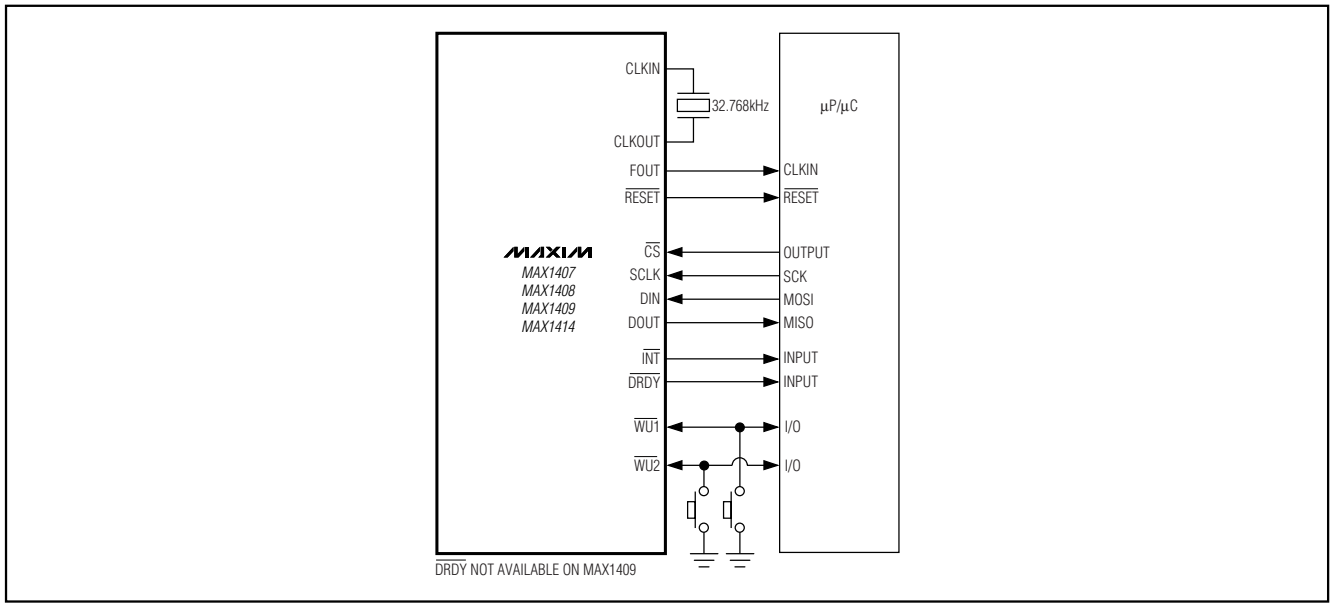


Figure 9. SPI/QSPI Interface Connections

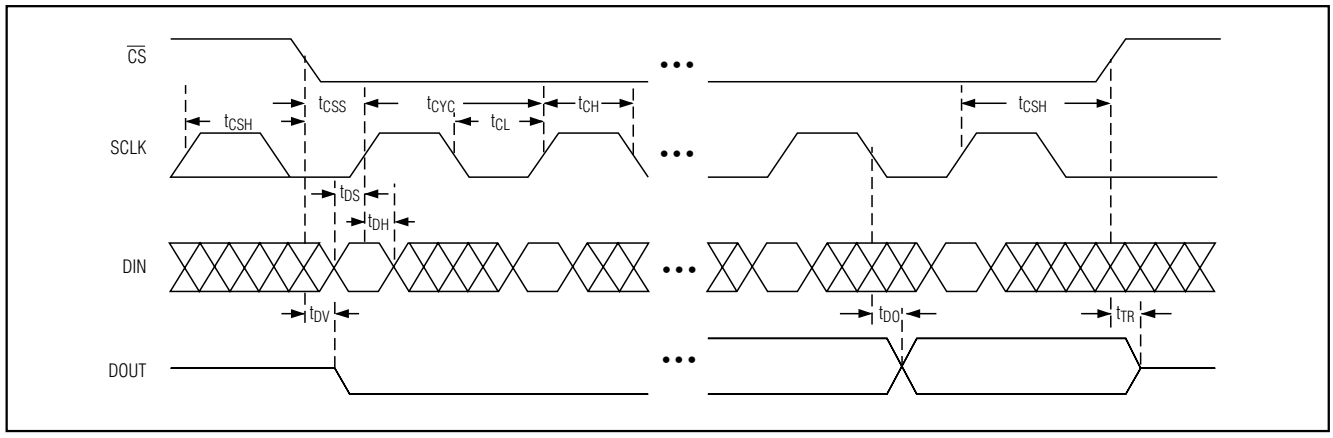


Figure 10. Detailed Serial Interface Timing

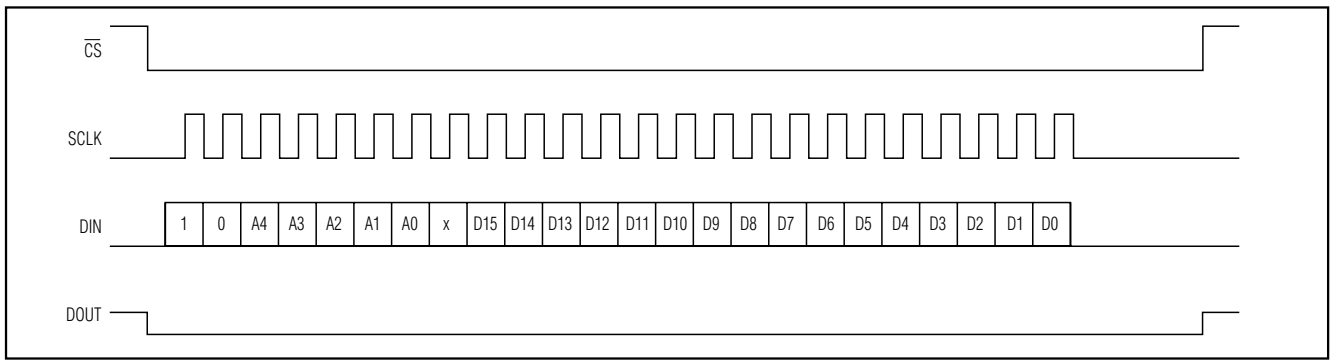


Figure 11. Serial Interface 16-Bit Write Timing Diagram

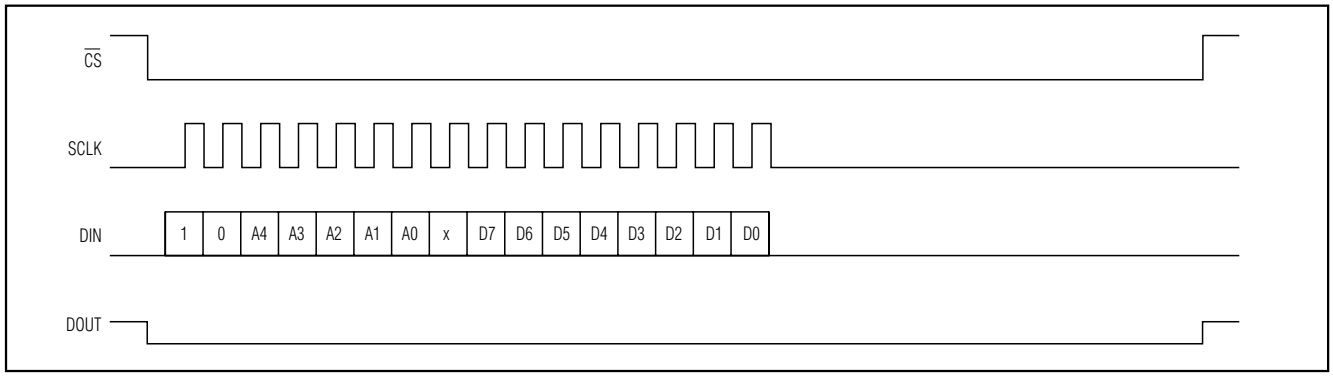


Figure 12. Serial Interface 8-Bit Write Timing Diagram

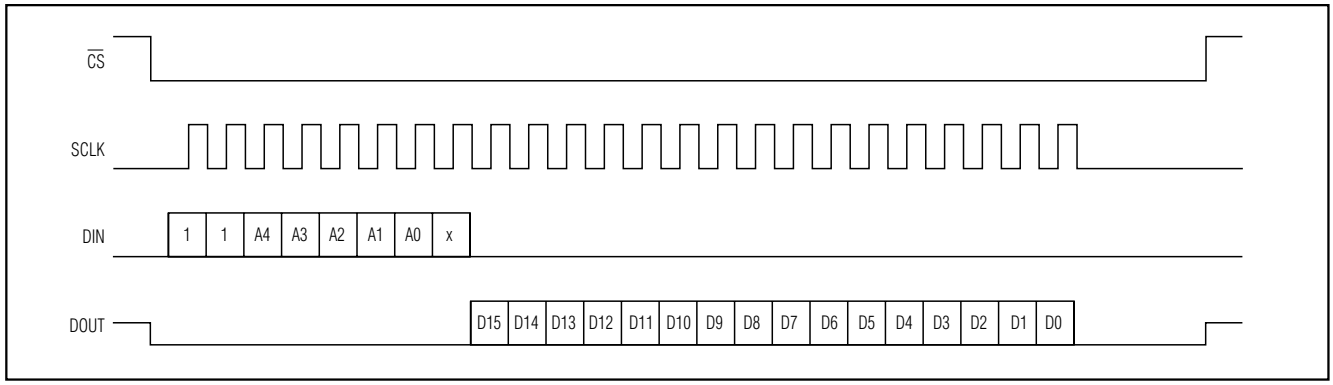


Figure 13. Serial Interface 16-Bit Read Timing Diagram

$\overline{CS}$ allows the SCLK, DIN, and DOUT signals to be shared among several devices. When short on processor I/O pins, connect $\overline{CS}$ to DGND, and operate the serial digital interface in CPOL = 1, CPHA = 1 or CPOL = 0, CPHA = 0 modes using SCLK, DIN, and DOUT.

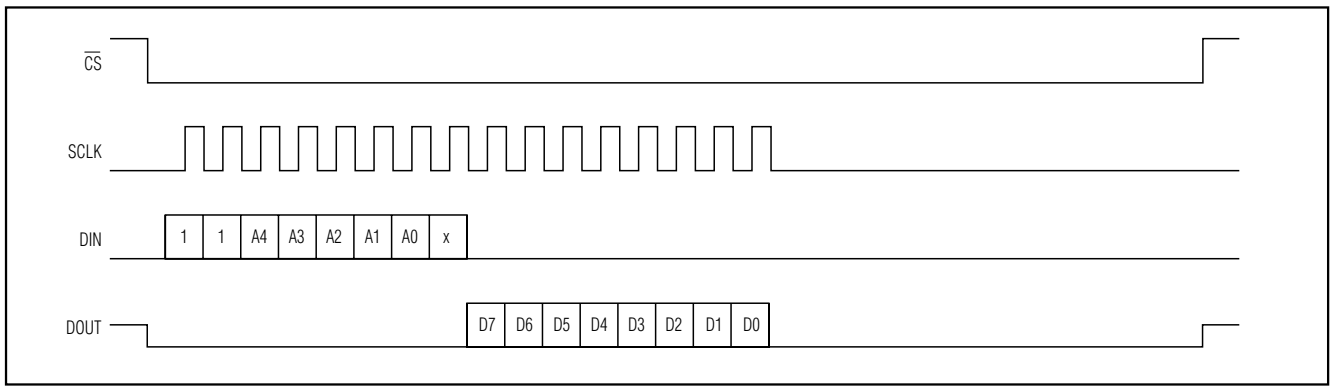


Figure 14. Serial Interface 8-Bit Read Timing Diagram

Table 2. Register Summary and Addressing

TARGET REGISTER	R/W ACCESS	ADD4:ADD0
ADC Register	R/W	00000
MUX Register	R/W	00001
Data Register	R	00010
Offset Register	R/W	00011
DAC1 Register	R/W	00100
DAC2 Register	R/W	00101
Status Register	R	00110
AI_Burst Register	R/W	01000
AI_Sec Register	R/W	01001
AI_Min Register	R/W	01010
AI_Hour Register	R/W	01011
AI_Day Register	R/W	01100
AI_Status Register	R	01101
Alarm/Clock_Ctrl Register	R/W	01110
RTC_Burst Register	R/W	01111

TARGET REGISTER	R/W ACCESS	ADD4:ADD0
RTC_Sec Register	R/W	10000
RTC_Min Register	R/W	10001
RTC_Hour Register	R/W	10010
RTC_Date Register	R/W	10011
RTC_Month Register	R/W	10100
RTC_Day Register	R/W	10101
RTC_Year Register	R/W	10110
RTC_Century Register	R/W	10111
Power1 Register	R/W	11000
Power2 Register	R/W	11001
Sleep Register	W	11010
Standby Register	W	11011
Idle Register	W	11100
Run Register	W	11101

Table 3. Command Byte Format

COMMAND	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
Write	1	0	ADD4:ADD0 (see Table 2)					X
Read	1	1	ADD4:ADD0 (see Table 2)					X